(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 October 2020 (29.10.2020)

WIPO | PCT

(10) International Publication Number
WO 2020/217060 A1

(51) International Patent Classification:
H01L 21/02 (2006.01) *H01L 29/786* (2006.01)

(21) International Application Number:
PCT/GB2020/051009

(22) International Filing Date:
24 April 2020 (24.04.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1905743.9 24 April 2019 (24.04.2019) GB

(71) Applicant: **THE UNIVERSITY OF MANCHESTER** [GB/GB]; Oxford Road, Manchester M13 9PL (GB).

(72) Inventors: **SONG, Aimin**; The University of Manchester, Oxford Road, Manchester Greater Manchester M13 9PL (GB). **CAI, Wensi**; The University of Manchester, Oxford Road, Manchester Greater Manchester M13 9PL (GB).

(74) Agent: **APPLEYARD LEES IP LLP**; 15 Clare Road, Halifax Yorkshire HX1 2HY (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

WO 2020/217060 A1

(54) Title: DEVICE AND METHOD

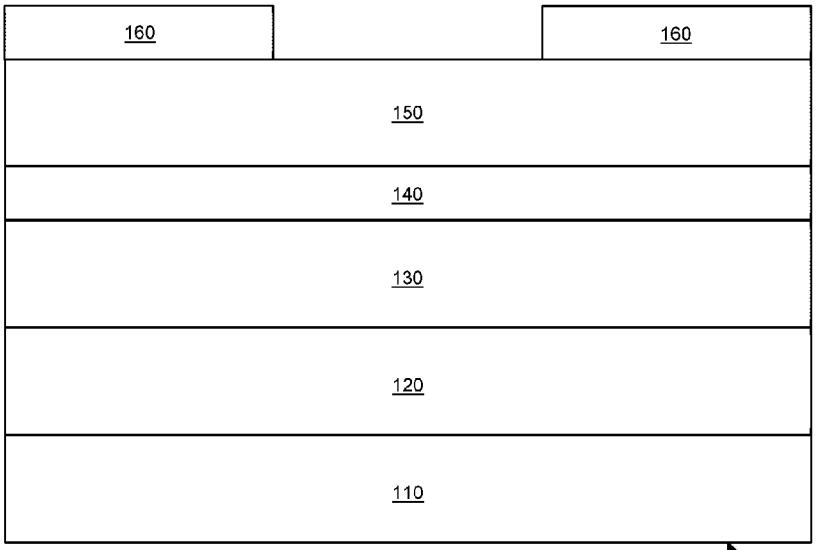

Fig. 1A

(57) Abstract: A method of fabricating at least a part of a device is described. The method comprises: providing a self-assembled monolayer, SAM, on an insulator layer; and depositing a first thickness of an oxide semiconductor layer on the SAM, comprising plasma sputtering the first thickness of the oxide semiconductor layer onto the SAM at a first power density PD1, wherein the first power density PD1 is selected to balance a first rate of damage of the SAM due, at least in part, to the plasma sputtering of the oxide semiconductor layer thereupon and a second rate of damage of the SAM due, at least in part, to the plasma.

[Continued on next page]

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

Device and method

Field

The present invention relates to a method of fabricating a device comprising a self-assembled monolayer, SAM, and an oxide semiconductor layer thereupon, and to such a device.

Background to the invention

Thin-film transistors (TFTs) have been investigated for many years and have shown great potential in diverse applications, from large-area sensor arrays to biochemical sensors and from active-matrix flat panel displays to radio-frequency identification tags. It is generally accepted that the properties of the dielectric/channel interface play an important role in the electrical performance of TFTs. These interface properties and electrical performance of organic TFTs (OTFTs) may be improved by treatment to provide a self-assembled monolayer (SAM), for example octadecyltrichlorosilane (OTS) or hexamethyldisilazane (HMDS), onto the dielectric surface, enabling tuning of the surface energy and a reduction of the interface trap density. Typically, the carrier mobility and current on/off ratio of SAM-treated OTFTs may be increased by an order of magnitude or more. Therefore, SAM treatment has become a standard process in OTFT fabrication.

Oxide semiconductors may be deposited on SAMs using solution-processing, as for organic semiconductors. However, to obtain satisfactory electrical properties, such solution-processing requires also high annealing temperatures, which may damage the SAMs, particularly ultra-thin SAMs, in turn attenuating the achievable electrical properties.

Hence, there is a need to improve methods of fabricating devices comprising self-assembled monolayers, SAMs, and oxide semiconductor layers thereupon.

Summary of the Invention

It is one aim of the present invention, amongst others, to provide a method of fabricating a device comprising a self-assembled monolayer, SAM, and an oxide semiconductor layer thereupon which at least partially obviates or mitigates at least some of the disadvantages of the prior art, whether identified herein or elsewhere. For instance, it is an aim of embodiments of the invention to provide a method of fabricating such a device that reduces damage to the SAM, while improving electrical properties of the device, compared with conventional methods. For instance, it is an aim of embodiments of the invention to provide such a method that simplifies and/or accelerates fabrication, while improving electrical properties of the device, compared with

conventional methods. For instance, it is an aim of embodiments of the invention to provide such a device, having improved electrical properties, compared with devices obtained via conventional methods.

A first aspect provides a method of fabricating at least a part of a device, the method comprising:
providing a self-assembled monolayer, SAM, on an insulator layer; and
depositing a first thickness of an oxide semiconductor layer on the SAM, comprising plasma sputtering the first thickness of the oxide semiconductor layer onto the SAM at a first power density PD1, wherein the first power density PD1 is selected to balance a first rate of damage of the SAM due, at least in part, to the plasma sputtering of the oxide semiconductor layer thereupon and a second rate of damage of the SAM due, at least in part, to the plasma;
preferably wherein the first power density PD1 is equivalent to less than 50 W, preferably in a range from 15 W to less than 50 W, more preferably in a range from 25 W to 47.5 W, most preferably in a range from 30 W to 45 W, for example 35 W or 40 W for a sputtering target having a diameter of 3 inches (76.2 mm).

A second aspect provides a device fabricated, at least in part, according to the method of the first aspect, the device comprising an insulator layer, having a self-assembled monolayer, SAM, provided on the insulator layer and an oxide semiconductor layer deposited on the SAM,
wherein a breakdown electric field of the insulator layer and the SAM is at least 3 MV cm^{-1}, preferably at least 5 MV cm^{-1}, more preferably at least 7 MV cm^{-1}.

Detailed Description of the Invention

According to the present invention there is provided, as set forth in the appended claims. Also provided is. Other features of the invention will be apparent from the dependent claims, and the description that follows.

Method

The first aspect provides a method of fabricating at least a part of a device, the method comprising:
providing a self-assembled monolayer, SAM, on an insulator layer; and
depositing a first thickness of an oxide semiconductor layer on the SAM, comprising plasma sputtering the first thickness of the oxide semiconductor layer onto the SAM at a first power density PD1, wherein the first power density PD1 is selected to balance a first rate of damage of the SAM due, at least in part, to the plasma sputtering of the oxide semiconductor layer thereupon and a second rate of damage of the SAM due, at least in part, to the plasma;

preferably wherein the first power density PD1 is equivalent to less than 50 W, preferably in a range from 15 W to less than 50 W, more preferably in a range from 25 W to 47.5 W, most preferably in a range from 30 W to 45 W, for example 35 W or 40 W for a sputtering target having a diameter of 3 inches (76.2 mm).

In this way, the method of fabricating the device reduces damage to the SAM, while improving electrical properties of the device, compared with conventional methods. By plasma sputter deposition of the oxide semiconductor, high temperature annealing, as required for conventional solution processing deposition and which may damage the SAM, is avoided. Particularly, the inventors have determined a regimen for plasma sputtering that provides deposition of the oxide semiconductor on the SAM without adversely damaging the SAM. Without wishing to be bound by any theory, it is thought that this regimen for plasma sputtering directly onto the SAM balances two causes of damage to the SAM:

1. damage to the SAM due to the deposition of the oxide semiconductor, which increases as the power density increases and is thus the dominant cause of damage to the SAM at relatively higher power densities; and
2. damage to the SAM due to the plasma, for example due to the ions accelerated towards the target, which increases with exposure thereto and thus plasma sputtering time and appears to be the dominant cause of damage to the SAM at relatively lower power densities.

Hence, the regimen for plasma sputtering is at intermediate power densities therebetween, that are still significantly lower, though, than power densities conventionally used for plasma sputtering of oxide semiconductors.

This method simplifies and/or accelerates fabrication, while improving electrical properties of the device, compared with conventional methods, such as solution processing.

In contrast to conventional solution process deposition, the method according to the first aspect uses plasma sputtering. Typically, plasma sputtering is rarely used with SAMs owing to the potential damage to SAMs caused by the plasma. A previous attempt to deposit an oxide semiconductor on a SAM by plasma sputtering has been relatively unsuccessful since while the SAM appeared to survive the plasma sputtering of InGaZnO (IGZO), the resulting TFT displayed a mobility less than 2 cm^2 Vs^{-2}, which is much lower than the typical and required carrier mobility for IGZO TFTs.

In parallel work, the inventors have developed an ultra-thin, anodized Al_xO_y for a gate insulator, which provides IGZO TFTs having an ultra-low operating voltage of just 1 V. In embodiments described herein, the inventors have improved IGZO TFTs having sputtered channel layers by using SAM treatment on the gate dielectrics prior to the sputtering of the oxide semiconductor.

In order to study possible plasma damage to the SAM during the sputtering, several sputtering powers have been tested. Under optimized sputtering conditions, OTS treatment in IGZO TFTs significantly improves the electrical performance, including a decrease of interface trap density by 50% as well as an increase of current on/off ratio and carrier mobility by a factor of 76 and 2.3, respectively. Such an inexpensive and yet effective method is applicable to other sputtered oxide semiconductors.

Despite being a standard process in fabrication of organic thin-film transistors (TFTs) to reduce interface traps and decrease surface energy, self-assembled monolayer (SAM) treatment of gate dielectrics is rarely used in oxide-semiconductor-based TFTs due to possible damage to SAMs during semiconductor deposition. As described herein, the inventors demonstrate significant improvements in the characteristics of InGaZnO TFTs using an octadecyltrichlorosilane (OTS)-treated, ultra-thin Al_xO_y gate dielectric. The interface trap density is reduced by 50%, while carrier mobility and current on/off ratio increase by a factor of 2.3 and 76, respectively. The effects on gate leakage, breakdown characteristics and bias stress stability have also been studied.

Device

The method is of fabricating at least a part of the device. In one example, the device comprises and/or is a TFT, an inverter, a logic gate, an integrated circuit, an analogue circuit or a display.

SAM

The method comprises providing the self-assembled monolayer, SAM, on the insulator layer.

Generally, SAMs of organic molecules are molecular assemblies formed spontaneously on surfaces by adsorption and are organized into more or less large ordered domains. In some cases molecules that form the monolayer do not interact strongly with the substrate. This is the case for instance of the two-dimensional supramolecular networks of e.g. perylenetetracarboxylic dianhydride (PTCDA) on gold or of e.g. porphyrins on highly oriented pyrolitic graphite (HOPG). In other cases the molecules possess a head group that has a strong affinity to the substrate and anchors the molecule to it. Common head groups include thiols, silanes and phosphonates.

In one example, the SAM comprises and/or is a silane, for example a long chain alkyl organosilane, such as octadecyltrichlorosilane (OTS), hexamethyldisilazane (HMDS), aminopropyltriethoxysilane (APS), mercaptopropyltriethoxysilane (MPS), and perfluorooctyltriethoxysilane (PFOTES).

Long chain alkyl organosilane molecules are widely used to modify the properties of inorganic material surfaces. These organosilanes, which have several functional groups of different electronegativity, are characterized by an electric dipole determined by the charge distribution within the molecule. When these molecules closely pack to form a SAM, each molecule's electric dipole produces an overall net polarization inside the SAM and introduces a surface dipole at the interface between the semiconductor and the dielectric. A surface dipole of the SAM modulates the energy level of the semiconductor at the interface. These organosilanes can form very stable films, thus are commonly used in semiconductor technology. Silane-based precursor molecules can contain one (R_3SiX), two (R_2SiX_2) or three ($RSiX_3$) good leaving groups. Although all three silanes are used in the modification of hydroxylated surfaces, only trifunctional ones are able to form closely packed monolayers, because of their ability to form cross-linking bonds between two adjacent head groups. SAMs formed from mono- and di-functional self-assembling molecules are less dense due to steric repulsion between the 'R' groups of adjacent silane head groups. Precursor molecules with three reactive sites are usually functionalised with either halogen or alkoxy groups ($Si\text{-}X_3$ where X = Cl, $(OCH_3)_3$ or $(OCH_2CH_3)_3$), and chlorosilanes are preferred over alkoxysilanes as they are more reactive. However, the high reactivity and the water sensitivity of the chlorosilane head group limits the range of terminal functional groups that can be introduced onto the silane precursors. If the terminal functional group reacts with the trichlorosilane group, this leads to the formation of polymeric aggregates in solution, which subsequently react with the surface, resulting in an inhomogeneous film.

In one example, the providing the SAM comprises and/or is by solution deposition and/or vapour phase deposition. Other processes for providing the SAM are known.

Insulator layer

In one example, the insulator layer (also known as a dielectric layer) comprises and/or is Al_xO_y and/or SiO_2. Other insulator layers are known.

Oxide semiconductor layer

The method comprises depositing the first thickness of the oxide semiconductor layer on the SAM, comprising plasma sputtering the first thickness of the oxide semiconductor layer onto the SAM at a first power density PD1, wherein the first power density PD1 is selected to balance a first rate of damage of the SAM due, at least in part, to the plasma sputtering of the oxide semiconductor layer thereupon and a second rate of damage of the SAM due, at least in part, to the plasma, as described previously. It should be understood that the first thickness of the oxide semiconductor layer is deposited directly on the SAM, without any further layer therebetween.

In one preferred example, the first power density PD1 is equivalent to less than 50 W, preferably in a range from 15 W to less than 50 W, more preferably in a range from 25 W to 47.5 W, most preferably in a range from 30 W to 45 W, for example 35 W or 40 W for a sputtering target having a diameter of 3 inches (76.2 mm).

As understood by the skilled person, an efficiency and/or an effective power density of the plasma sputtering may dependent inter alia on a configuration of the particular plasma sputtering apparatus used, including a shape and/or size of the sputtering target, and/or the associated sputter gun. Hence, the first power density PD1 is defined as equivalent (i.e. corresponding) to a particular power, within the defined ranges, for the sputtering target having the diameter of 3 inches (76.2 mm).

Oxide semiconductor

It should be understood that the oxide semiconductor layer comprises and/or is formed from an oxide semiconductor having a sufficiently high conductivity for the device.

In one example, the oxide semiconductor comprises and/or is an amorphous oxide semiconductor. In one example, the oxide semiconductor comprises and/or is a crystalline oxide semiconductor. In one example, the oxide semiconductor comprises and/or is an n-type oxide semiconductor. In one example, the oxide semiconductor comprises and/or is a p-type oxide semiconductor.

In one example, the oxide semiconductor comprises and/or is a ZnO-based oxide semiconductor, preferably an amorphous ZnO-based oxide semiconductor. In one example, the ZnO-based oxide semiconductor includes at least one selected from the group consisting of hafnium (Hf), yttrium (Y), tantalum (Ta), zirconium (Zr), titanium (Ti), copper (Cu), nickel (Ni), chromium (Cr), indium (In), gallium (Ga), aluminum (Al), tin (Sn), and magnesium (Mg).

In one example, the oxide semiconductor comprises and/or is ZnO, ZnGaO, ZnSnO, In_2O_3, InSnO, InZnO, InGaO, InGaZnO, InHfZnO, InSiZnO, InZrZnO, InSnZnO, InGaSnO, SnO_2, AlZnO, AlZnSnO and/or ZrZnSnO. In one example, the oxide semiconductor comprises and/or is crystalline, for example polycrystalline, ZnO, crystalline, for example polycrystalline, ZnGaO, crystalline, for example polycrystalline, ZnSnO, crystalline, for example polycrystalline, In_2O_3, crystalline, for example polycrystalline, InSnO, crystalline, for example polycrystalline, InZnO, crystalline, for example polycrystalline, InGaO, crystalline, for example polycrystalline, InGaZnO, crystalline, for example polycrystalline, InHfZnO, crystalline, for example polycrystalline, InSiZnO, crystalline, for example polycrystalline, InZrZnO, crystalline, for

example polycrystalline, InSnZnO, crystalline, for example polycrystalline, InGaSnO, crystalline, for example polycrystalline, SnO_2, crystalline, for example polycrystalline, AlZnO, crystalline, for example polycrystalline, AlZnSnO, and/or crystalline, for example polycrystalline, ZrZnSnO. In one example, the oxide semiconductor comprises and/or is amorphous ZnO, amorphous ZnGaO, amorphous ZnSnO, amorphous In_2O_3, amorphous InSnO, amorphous InZnO, amorphous InGaO, amorphous InGaZnO, amorphous InHfZnO, amorphous InSiZnO, amorphous InZrZnO, amorphous InSnZnO, amorphous InGaSnO, amorphous SnO_2, amorphous AlZnO, amorphous AlZnSnO, and/or amorphous ZrZnSnO.

In one preferred example, the oxide semiconductor is InGaZnO (IGZO). The oxide semiconductor may be $a(In_2O_3).b(Ga_2O_3).c(ZnO)$. More preferably, the oxide semiconductor is amorphous InGaZnO (IGZO). The oxide semiconductor may be amorphous $a(In_2O_3).b(Ga_2O_3).c(ZnO)$. In one example, a, b, and c are real numbers where $a \geq 0$, $b \geq 0$, and/or $c > 0$. In one example, a, b, and c are real numbers where $a \geq 1$, $b \geq 1$, and/or $0 < c \leq 1$. In one example, $a = 1$, $b = 1$ and $c = 2$.

In one example, the first thickness is in a range from 1 nm to 50 nm, preferably in a range from 2 nm to 10 nm, more preferably in a range from 3 nm to 8 nm, for example 5 nm. It should be understood that the first thickness is measured orthogonal to a surface, for example the upper (i.e. exposed during plasma sputtering) surface of the oxide semiconductor layer. Such a relatively thinner first thickness is suitable for subsequent deposition of a second thickness thereupon, as described below. In one example, the first thickness is a total thickness of the oxide semiconductor layer and is in a range from 1 nm to 50 nm, preferably in a range from 5 nm to 40 nm, more preferably in a range from 10 nm to 30 nm, for example 15, 20 or 25 nm. Such a relatively thinner first thickness is suitable as a complete oxide semiconductor layer, before deposition of other layers thereupon.

In one example, the method comprises depositing a second thickness of the oxide semiconductor layer on the deposited first thickness thereof, comprising plasma sputtering the second thickness of the oxide semiconductor layer onto the first thickness of the oxide semiconductor layer at a second power density PD2, wherein the second power density PD2 is greater than the first power density PD1. In this way, the first thickness of the oxide semiconductor protects the SAM from plasma sputtering at the subsequent higher second power density PD2.

In one example, the second power density PD2 is equivalent to less than 250 W, preferably in a range from 25 W to less than 150 W, more preferably in a range from 50 W to 100 W for the sputtering target having the diameter of 3 inches (76.2 mm).

In one example, the second thickness is in a range from 1 nm to 50 nm, preferably in a range from 5 nm to 40 nm, more preferably in a range from 10 nm to 30 nm, for example 20 nm.

In one example, the plasma sputtering comprises radio frequency, RF, plasma sputtering.

In one example, the plasma sputtering comprises non-reactive plasma sputtering, for example wherein the plasma sputtering is in an atmosphere consisting essentially and/or consisting of an inert gas, for example Ar, Xe and/or Kr, having only impurities therein. Conversely, in one example, the plasma sputtering comprises reactive plasma sputtering, for example wherein the plasma sputtering is in an atmosphere comprising H_2, O_2 and/or N_2.

In one example, the plasma sputtering is performed at an insulator layer temperature less than 180 °C, preferably up to 100 °C, more preferably up to 50 °C, most preferably up to 30 °C, for example room temperature, RT. In this way, the fabricated part of the device is at a relatively low temperature, thereby reducing temperature-induced damage to the SAM.

In one example, the plasma sputtering is in an atmosphere at a pressure in a range from 1E-5 mbar to 1E-1 mbar, preferably in a range from 1E-4 mbar to 1E-2 mbar, for example 5E-3 mbar.

In one example, a distance between the SAM and the sputtering target is in a range from 5 cm to 25 cm, preferably in a range from 10 cm to 15 cm, for example 12 cm.

The second aspect provides a device fabricated, at least in part, according to the method of the first aspect, the device comprising an insulator layer, having a self-assembled monolayer, SAM, provided on the insulator layer and an oxide semiconductor layer deposited on the SAM,
wherein a breakdown electric field of the insulator layer and the SAM is at least 3 MV cm^{-1}, preferably at least 5 MV cm^{-1}, more preferably at least 7 MV cm^{-1}.

In one example, the breakdown electric field of the SAM-treated insulator layer is increased by at least 1 MV cm^{-1}, preferably at least 2 MV cm^{-1}, more preferably at least 3 MV cm^{-1} compared an untreated insulator layer (i.e. wherein the insulator layer is not SAM-treated).

In one example, the device comprises and/or is a thin film transistor, TFT, wherein the device has a leakage current density of < 15 nA cm^{-2}.

In one example, the device comprises and/or is a TFT, wherein the leakage current density is decreased by at least 10%, preferably at least 20%, more preferably at least 30% compared with a device wherein the insulator layer is untreated (i.e. wherein the insulator layer is not SAM-treated).

In one example, the device comprises and/or is a TFT, wherein the device has an interface trap density < 1E12 cm^{-2} eV^{-1}, preferably < 5E11 cm^{-2} eV^{-1}.

In one example, the device comprises and/or is a TFT, wherein the interface trap density is decreased by at least 20%, preferably at least 30%, more preferably at least 40% compared with a device wherein the insulator layer is untreated (i.e. wherein the insulator layer is not SAM-treated).

In one example, the device comprises and/or is a TFT, wherein the device has a mobility in a saturation regime of > 9 $cm^2V^{-1}s^{-1}$, preferably >10 $cm^2V^{-1}s^{-1}$, more preferably > 11 $cm^2V^{-1}s^{-1}$, most preferably > 12 $cm^2V^{-1}s^{-1}$.

In one example, the device comprises and/or is a TFT, wherein the mobility of the SAM-treated device is increased by a factor of at least 1.2, preferably at least 1.5, more preferably at least 2, compared with a device wherein the insulator layer is untreated (i.e. wherein the insulator layer is not SAM-treated).

Definitions

Throughout this specification, the term “comprising” or “comprises” means including the component(s) specified but not to the exclusion of the presence of other components. The term “consisting essentially of” or “consists essentially of” means including the components specified but excluding other components except for materials present as impurities, unavoidable materials present as a result of processes used to provide the components, and components added for a purpose other than achieving the technical effect of the invention, such as colourants, and the like.

The term “consisting of” or “consists of” means including the components specified but excluding other components.

Whenever appropriate, depending upon the context, the use of the term “comprises” or “comprising” may also be taken to include the meaning “consists essentially of” or “consisting essentially of”, and also may also be taken to include the meaning “consists of” or “consisting of”.

The optional features set out herein may be used either individually or in combination with each other where appropriate and particularly in the combinations as set out in the accompanying claims. The optional features for each aspect or exemplary embodiment of the invention, as set

out herein are also applicable to all other aspects or exemplary embodiments of the invention, where appropriate. In other words, the skilled person reading this specification should consider the optional features for each aspect or exemplary embodiment of the invention as interchangeable and combinable between different aspects and exemplary embodiments.

Brief description of the drawings

For a better understanding of the invention, and to show how exemplary embodiments of the same may be brought into effect, reference will be made, by way of example only, to the accompanying diagrammatic Figures, in which:

Figure 1A schematically depicts an IGZO transistor according to an exemplary embodiment; Figure 1B shows a chemical structure of OTS (octadecyltrichlorosilane); Figure 1C shows a photograph of a drop of deionized (DI) water on OTS-treated Al_xO_y films showing the contact angle; Figure 1D schematically depicts capacitors with and without OTS treatment; Figure 1E shows a graph of low voltage *J-V* characteristics of the capacitors of Figure 1D; and Figure 1F shows a graph of high voltage *J-V* characteristics of the capacitors of Figure 1D;

Figure 2A shows a graph of transfer characteristics of TFTs fabricated using a power of 25 W to sputter IGZO as the channel layer (devices A and D); Figure 2B shows a graph of transfer characteristics of TFTs fabricated using a power of 40 W to sputter IGZO as the channel layer (devices B and E); Figure 2C shows a graph of transfer characteristics of TFTs fabricated using a power of 50 W to sputter IGZO as the channel layer (devices C and F); Figure 2D shows a graph of interface trap density for the TFTs of Figures 2A to 2C gated with bare Al_xO_y (solid squares) and OTS-modified Al_xO_y (open circles) at different IGZO sputtering powers; Figure 2E shows a graph of threshold voltage for the TFTs of Figures 2A to 2C gated with bare Al_xO_y (solid squares) and OTS-modified Al_xO_y (open circles) at different IGZO sputtering powers; and Figure 2F shows a graph of mobility for the TFTs of Figures 2A to 2C gated with bare Al_xO_y (solid squares) and OTS-modified Al_xO_y (open circles) at different IGZO sputtering powers;

Figure 3A1 shows a graph of output characteristics of IGZO transistors of Figure 2B gated with OTS-modified Al_xO_y; Figure 3A2 shows a graph of output characteristics of IGZO transistors of Figure 2B gated with bare Al_xO_y; Figure 3B shows a graph of mobility as a function of V_G for IGZO transistors gated with bare Al_xO_y (solid squares) or OTS-modified Al_xO_y (open circles); Figure 3C shows a graph of current on/off ratio; Figure 3D shows a graph of maximum leakage current; Figure 3E shows a graph of threshold voltage as a function of time; and Figure 3F shows a graph of mobility change as a function of time of IGZO TFTs gated with bare Al_xO_y (solid squares) or OTS-modified Al_xO_y (open circles) under a bias stress of $V_G = 1$ V and $V_D = 1$ V up to 3000 s. The IGZO layer was 25-nm-thick and the sputtering power was 40 W;

Figure 4A shows a graph of *C-V* characteristics of devices using Al/Al_xO_y/Al (solid squares) and Al/Al_xO_y/OTS/Al (open circles) structures measured at 100 kHz; Figure 4B shows a graph of *C-f* characteristics of devices using Al/Al_xO_y/Al (solid squares) and Al/Al_xO_y/OTS/Al (open circles) structures that were measured at a bias voltage of 1 V;

Figures 5A, 5B and 5C schematically depict diagrams devices for testing sputtering damage to the OTS layer; Figure 5D shows a graph of leakage current density for devices using the devices of Figures 5A, 5B and 5C; and Figure 5E shows a graph of leakage current density for 8 devices, according to Figure 5A, using 40 W sputtered IGZO;

Figure 6A1 shows a graph of output characteristics of IGZO transistors gated with OTS-modified Al_xO_y for sputtering IGZO at 25 W; Figure 6A2 shows a graph of output characteristics of IGZO transistors gated with bare Al_xO_y for sputtering IGZO at 25 W; Figure 6B1 shows a graph of output characteristics of IGZO transistors gated with OTS-modified Al_xO_y for sputtering IGZO at 50 W; Figure 6B2 shows a graph of output characteristics of IGZO transistors gated with bare Al_xO_y for sputtering IGZO at 50 W; Figures 6A1 and 6A2 are the corresponding output characteristics of Figure 2A; Figures 6B1 and 6B2 are the corresponding output characteristics of Figure 2C;

Figure 7 shows graphs of statistical information for the devices. Reproducibility and uniformity test of current on/off ratio, mobility, subthreshold swing and threshold voltage of ten IGZO TFTs gated with OTS-modified Al_xO_y. The IGZO sputtering power is 40 W. The devices show similar behaviours including a current on/off ratio of $(2.7 \pm 1.5) \times 10^7$, a mobility of 11.7 ± 1.3 cm^2/Vs, a subthreshold swing of 68 ± 3 mV/dec and a threshold voltage of 0.3 ± 0.09 V; and

Figure 8 schematically depicts a method according to an exemplary embodiment.

Detailed Description of the Drawings

Experimental

IGZO TFTs 100 were fabricated using a bottom-gate, top-contact structure as shown in Figure 1A, comprising a substrate 110, a gate electrode 120, an Al_xO_y insulator layer 130, a SAM 140, an oxide semiconductor layer 150 and source and drain electrodes 160. Generally, like features are referenced using like reference numbers.

First, 200-nm-thick Al gate was thermally evaporated on the glass substrate 110 to provide the

gate electrode 120. Next, approximately 3-nm-thick Al_xO_y insulator layer 130 was grown by anodization of this Al in 1 mM citric acid. A constant anodization current (0.1 mA/cm^2) was applied to the Al until the targeted anodization voltage (2.3 V) was achieved. The sample was held at this voltage until the current fell below 0.015 mA/cm^2. Such a thin Al_xO_y dielectric recently enabled IGZO TFTs capable of operating voltage at 1 V (Cai, Wensi, et al. "One-Volt IGZO Thin-Film Transistors With Ultra-Thin, Solution-Processed Al_xO_y Gate Dielectric."IEEE Electron Device Letters 39.3 (2018): 375-378, the subject matter of which is incorporated herein). The anodized Al_xO_y film was then treated by spin coating of 0.1 wt% *n*-octadecyltrichlorosilane (OTS) in trichloroethylene (TCE) to provide the SAM 140. The chemical structure of OTS is shown in Figure 1B. As shown in Figure 1C, the contact angle after deposition of the OTS SAM was found to be 92°. A 25-nm-thick IGZO (In:Ga:Zn = 1:1:1) channel layer (i.e. the oxide semiconductor layer 150) was then deposited by radio-frequency magnetron sputtering in an Ar atmosphere (5E-3 mbar BOC PURESHIELD ARGON 99.998%) at room temperature using a 3 inch diameter InGaZnO (In:Ga:Zn = 1:1:1) target (PI-KEM), having a purity of 99.99% and a 12 cm target to TFT distance, using a MOORFIELD minilab 025 deposition system. Finally, 150-nm-thick Al was thermally evaporated through a shadow mask to form the source and drain electrodes 160. The channel length and width were 60 µm and 2 mm, respectively. The electrical characteristics of the devices were measured using an Agilent E5270B semiconductor analyzer and an Agilent E4980A LCR meter at room temperature.

Results and discussion

First, the properties of the ultra-thin Al_xO_y gate insulator with and without OTS treatment were studied. Capacitance measurements were carried out using the structure 200 shown in Figure 1D. A capacitance density of about 1000 nF/cm^2 at 100 kHz was found in the Al/3-nm-thick Al_xO_y/Al structure (see Figure 4A and 4B). After the application of OTS, the capacitance density was reduced to about 490 nF/cm^2 (see Figure 4A and 4B). The leakage current density of the capacitors using bare Al_xO_y film or OTS-modified Al_xO_y film as the insulator is shown in Figure 1E. After the addition of the OTS layer, the leakage current density decreased by roughly 3 times and was less than 3 nA/cm^2 throughout the whole test, confirming the formation of a high quality monolayer and improved insulating properties. As shown in Figure 1F, while the breakdown voltage for bare Al_xO_y was about 3.5 V, no breakdown was observed for Al_xO_y/OTS, even at 10 V. The corresponding electric field was larger than 17 MV/cm, which is better than typical ultra-thin insulator layers reported previously and further confirms the high quality of the Al_xO_y/OTS dielectric film.

During the sputtering of IGZO on top of organic materials, plasma-induced damage may occur. A higher sputtering power will not only mean more energetic ion bombardments, but also gives a higher deposition rate and thereby a quicker coverage of the OTS SAM. In order to study the

dependence of possible damage to OTS on the sputtering power, transistors gated with bare Al_xO_y (devices A, B and C) and OTS-modified Al_xO_y (devices D, E and F) have been fabricated using 25 W (devices A and D), 40 W (devices B and E) and 50 W (devices C and F) sputtered IGZO as the channel layer. Figures 2A to 2C show the transfer characteristics of IGZO TFTs gated with bare Al_xO_y (no markers) and OTS-modified Al_xO_y (circle markers). The obtained electrical characteristics of these devices are summarized in Table 1. The comparisons between devices A and D, devices B and E, and devices C and F clearly show an increase of current on/off ratio by more than one order of magnitude after the OTS modification at all sputtering powers. Also, the gate leakage current, I_G, of the TFTs gated with OTS-modified Al_xO_y is found to be much smaller than that of the TFTs gated with bare Al_xO_y, indicating superior insulating properties of the OTS-modified Al_xO_y dielectric. In addition, a significant decrease in hysteresis is clearly seen after the OTS modification, which is critical to many circuit applications. A possible reason to this is the application of OTS forms a less polar surface and thus reduces water and hydroxyl group adsorption. The subthreshold swing, *SS*, is found to be about 70 mV/dec in all six devices, which is very close to the theoretical limit at 300 K. This demonstrates a large insulator capacitance and a low interface trap density.

The interface trap density, D_{it}, can be calculated as

$$D_{it} = [\frac{SS\ log(e)}{kT/q} - 1]\frac{C}{q^2}, \quad (1)$$

where k is the Boltzmann constant, T is the temperature, q is the electron charge and C is the capacitance per unit area. To calculate D_{it}, the capacitance of every device was measured by positively biasing the gate at +1 V so that the semiconductor was not depleted and hence did not contribute to the capacitance. The obtained capacitances in devices A, B, C, D, E and F at 100 Hz were 1090, 1130, 1080, 730, 560 and 580 nF/cm^2, respectively. By taking into account the measured capacitances, D_{it} was found to be 1.2 × 10^{12}, 1.2× 10^{12}, 1.1 × 10^{12}, 7.7 × 10^{11}, 4.8 × 10^{11} and 8.6 × 10^{11} cm^{-2} eV^{-1} in devices A, B, C, D, E and F, respectively. As indicated in Figure 2D, a lower D_{it} is found for devices D, E and F, suggesting a suppressed level of trap states at the dielectric/channel interface owing to the OTS treatment.

As shown in Figure 2E, the threshold voltage, V_{TH}, is found to be left-shifted after the OTS modification of the dielectric layer. With the decrease of interface trap density caused by the application of the OTS SAM at the dielectric/channel interface, a lower gate voltage is required to switch on the TFTs.

The mobility, μ, in the saturation regime can be derived from

$$I_D = \frac{W}{2L}\mu C(V_G - V_{TH})^2, \quad (2)$$

where $\frac{W}{L}$ is the width to length ratio and V_G is the gate voltage. As a result, the calculated μ for devices A, B, C, D, E and F are 4.9, 5, 8.2, 7.8, 13 and 9.6 cm^2/Vs, respectively. A clear increase of mobility after the OTS modification is shown in Figure 2F. This also confirms an improvement of the gate dielectric/channel interface quality and a decreased number of trap states by the SAM treatment.

However, unlike devices A, B and C, the interface trap density of devices D, E and F changes with the IGZO sputtering power, as shown in Figure 2D. A slightly higher D_{it} is obtained in device F than in device E, which might be due to a slightly more damaged OTS layer in device F. Because a higher sputtering power results in Ar ions with higher energy, there is likely more damage to the OTS layer. However, the comparison of D_{it} in devices D and E indicates that a worse interface quality was obtained in the lower power case. As the plasma damage should mainly occur before the OTS layer is covered by IGZO, the more severe damage to the OTS layer at lower power may be attributed to the longer time required for IGZO to effectively cover the OTS layer. A combination of the lowest subthreshold swing, the lowest interface trap density and the highest mobility is clearly seen in device E, demonstrating that the use of 40 W for the sputtering of IGZO results in the lowest damage to the OTS layer.

To further study the damage to OTS layer due to sputtering, parallel plate structures using Al/Al_xO_y/OTS/IGZO/Al (300 Figure 5A), Al/Al_xO_y/OTS/Al (400 Figure 5B) and Al/Al_xO_y/IGZO/Al (500 Figure 5C) have been fabricated. Regardless of the IGZO deposition power, devices with OTS-modified Al_xO_y show a significantly lower leakage current density than the devices without OTS modification. This indicates that the OTS layer is at least not completely damaged during the sputtering process (see Figure 5D). Compared to the devices without IGZO, a two times higher leakage current density of devices using 25 W and 50 W sputtered IGZO is found at an applied voltage of 1 V, which may be caused by greater damage to OTS layer at these two sputtering powers. Similar leakage current density is observed in the device without IGZO and device using 40 W sputtered IGZO, also indicating a much lower damage to the OTS layer when using 40 W to sputter IGZO. For the 40 W sputtering power, 8 devices that were fabricated in different batches have been randomly chosen from 40 devices to test the leakage current density. Similar leakage current density is found for all devices, demonstrating good uniformity and reproducibility (see Figure 5E).

The corresponding output characteristics (I_D-V_D) of the IGZO TFTs sputtered at 40 W and gated with OTS-modified Al_xO_y or bare Al_xO_y are shown in Figures 3A1 and 3A2. Figures 6A1, 6A2, 6B1, 6B2 shows the output characteristics of devices with 25 W and 50 W sputtered IGZO. All TFTs show clear linear, pinch-off and on-state regimes. Clearly, the application of the OTS layer helped increasing the saturation current due to the improved interface properties.

As shown in Figure 3B, a mobility of 13.5 cm^2/Vs is obtained at 1 V for the device gated with OTS-modified Al_xO_y, which is about 2.3 times of the value for the device without OTS modification. This large increase of mobility is in agreement with the significantly decreased D_{it} from 1.2×10^{12} to 4.8×10^{11} cm^{-2} eV^{-1}. Such a low D_{it} value is comparable with or lower than those in most IGZO TFTs that use optimized bilayer or trilayer dielectrics. More importantly, the comparison in terms of mobility, current on/off ratio, subthreshold swing and operating voltage is found to be better than previously reported oxide-semiconductor-based TFTs gated with solution-processed, ultra-thin dielectric layers (see Table 2).

The study of the uniformity and reproducibility of these devices was performed on ten OTS-modified Al_xO_y/IGZO TFTs that were fabricated in different batches (see Figure 7). The devices show similar behaviours including a current on/off ratio of $(2.7 \pm 1.5) \times 10^7$, a mobility of 11.7 ± 1.3 cm^2/Vs, a subthreshold swing of 68 ± 3 mV/dec and a threshold voltage of 0.3 ± 0.09 V.

To further study the role of the OTS interlayer on device operational stability, both types of devices (i.e. without and with OTS treatment) were continuously biased at V_G = 1 V and V_D = 1 V up to 3000 s and the obtained results are shown in Figures 3C to 3F. All devices using OTS-modified Al_xO_y achieved a current on/off ratio of about 10^7 and a maximum leakage current less than 0.1 nA. This is much better than those using bare Al_xO_y as the gate dielectric and suggests that a stable OTS layer has been formed at the interface. After a bias stress of 3000 s, the threshold voltage for the device gated with bare Al_xO_y shifted by approximately 0.17 V from 0.46 to 0.63 V, which is 0.06 V more than the threshold voltage shift of the device using an OTS-modified Al_xO_y. Both types of devices show a little change of mobility after bias stress, but the mobility degradation in the device gated with OTS-modified Al_xO_y is 20 times smaller than that of the device using a bare Al_xO_y insulator.

C-V and *C-f* characteristics (Figures 4A and 4B), electrical properties obtained for IGZO TFTs gated with bare Al_xO_y or OTS-modified Al_xO_y (Table 1), leakage current density (Figures 5A to 5E), output characteristics of IGZO TFTs (Figures 6A1, 6A2, 6B1, 6B2), comparison of oxide-semiconductor-based TFTs gated with solution-processed, ultra-thin dielectric layer (Table 2), and statistical information (Figure 7).

	Sputtering power (W)	Current on/off ratio	*SS* (mV/dec)	*C/A* (nF/cm^2)	D_{it} (cm^{-2} eV^{-1})	V_{TH} (V)	μ (cm^2/Vs)
With OTS	25	2.9×10^7	69	730	7.7×10^{11}	0.45	7.8
	40	4.1×10^7	68	560	4.8×10^{11}	0.27	13
	50	1.7×10^7	74	580	8.6×10^{11}	0.19	9.6
Without OTS	25	4.1×10^5	70	1090	1.2×10^{12}	0.5	4.9
	40	5.4×10^5	70	1130	1.2×10^{12}	0.46	5
	50	6.8×10^5	70	1080	1.1×10^{12}	0.3	8.2

Table 1: Electrical characteristics obtained for the devices shown in Figure 2.

TFT (dielectric/ semiconductor)	Dielectric thickness (nm)	Operating voltage (V)	I_{ON}/I_{OFF}	*SS* (mV/dec)	D_{it} (cm^{-2} eV^{-1})	μ (cm^2/Vs)	Ref
(Al_xO_y|OTS)/IGZO	**~ 6**	**1**	**4.1×10^7**	**68**	**4.8×10^{11}**	**13**	**This work**
Al_xO_y/IGZO	3	1	1.6×10^6	68	8.5×10^{11}	5.4	1
Al_xO_y/IGZO	12	2	5.9×10^4	110	/	6.3	2
YO_x/In_2O_3	17	1.5	6×10^6	75	7×10^{11}	15.98	3
ZrO_x/ZnO	5	3	10^5	250	/	0.45	4

Table 2: Comparison of oxide-semiconductor-based TFTs gated with solution-processed, ultra-thin dielectric layers.

Figure 8 schematically depicts a method according to an exemplary embodiment. Particularly, the method is of fabricating at least a part of a device.

At S801, a self-assembled monolayer, SAM, is provided on an insulator layer.

At S802, a first thickness of an oxide semiconductor layer is deposited on the SAM, comprising plasma sputtering the first thickness of the oxide semiconductor layer onto the SAM at a first power density PD1, wherein the first power density PD1 is selected to balance a first rate of damage of the SAM due, at least in part, to the plasma sputtering of the oxide semiconductor layer thereupon and a second rate of damage of the SAM due, at least in part, to the plasma; preferably wherein the first power density PD1 is equivalent to less than 50 W, preferably in a range from 15 W to less than 50 W, more preferably in a range from 25 W to 47.5 W, most preferably in a range from 30 W to 45 W, for example 35 W or 40 W for a sputtering target having a diameter of 3 inches (76.2 mm).

Summary

Although a preferred embodiment has been shown and described, it will be appreciated by those skilled in the art that various changes and modifications might be made without departing from the scope of the invention, as defined in the appended claims and as described above.

In summary, the invention provides a method of fabricating at least a part of a device, the method comprising providing a self-assembled monolayer, SAM, on an insulator layer; and depositing a first thickness of an oxide semiconductor layer on the SAM, comprising plasma sputtering the first thickness of the oxide semiconductor layer onto the SAM at a first power density PD1, wherein the first power density PD1 is selected to balance a first rate of damage of the SAM due, at least in part, to the plasma sputtering of the oxide semiconductor layer thereupon and a second rate of damage of the SAM due, at least in part, to the plasma.

Thin-film transistors (TFTs) have been investigated for many years and have shown great potentials in applications such as sensors and displays. It is generally accepted that the properties of the dielectric/channel interface play an important role in the electrical performance of TFTs. For organic TFTs, it is now been a standard process to apply a self-assembled monolayer (SAM) onto the gate dielectric to reduce the interface trap density and decrease surface energy, so that the carrier mobility and current on/off can be increased by orders of magnitude. However, such treatment is rarely used in oxide-semiconductor-based TFTs due to possible damage to SAMs during the semiconductor deposition.

In this work, different sputtering powers for InGaZnO (IGZO) deposition have been tested for TFTs gated with octadecyltrichlorosilane (OTS)-modified, ultra-thin Al_xO_y. The experiments show that depending on the sputtering power the damage to the OTS layer can be minimized. The damage to OTS SAM shows a clear dependence on the IGZO sputtering power, which means by carefully controlling the IGZO sputtering power, it is able to minimize the plasma damage to OTS SAM and thus significantly increase the electrical properties of the obtained devices. Under the optimal sputtering conditions, the obtained devices show a reduction of interface trap density by 50%, an increase of carrier mobility by 2.3 times and an increase of current on/off ratio by 76 times, compared with the devices without OTS treatment. Such an inexpensive and yet effectively way might also be applicable to other SAMs and sputtered oxide semiconductors to significantly improve the performance, and might have potential applications in future fabrication of low-power, low-cost electronic devices.

Attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with

this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at most some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, and drawings) may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A method of fabricating at least a part of a device, the method comprising:
providing a self-assembled monolayer, SAM, on an insulator layer; and
depositing a first thickness of an oxide semiconductor layer on the SAM, comprising plasma sputtering the first thickness of the oxide semiconductor layer onto the SAM at a first power density PD1, wherein the first power density PD1 is selected to balance a first rate of damage of the SAM due, at least in part, to the plasma sputtering of the oxide semiconductor layer thereupon and a second rate of damage of the SAM due, at least in part, to the plasma;
preferably wherein the first power density PD1 is equivalent to less than 50 W, preferably in a range from 15 W to less than 50 W, more preferably in a range from 25 W to 47.5 W, most preferably in a range from 30 W to 45 W, for example 35 W or 40 W for a sputtering target having a diameter of 3 inches (76.2 mm).

2. The method according to claim 1, wherein the first thickness is in a range from 1 nm to 50 nm, preferably in a range from 2 nm to 10 nm, more preferably in a range from 3 nm to 8 nm, for example 5 nm.

3. The method according to any previous claim, comprising depositing a second thickness of the oxide semiconductor layer on the deposited first thickness thereof, comprising plasma sputtering the second thickness of the oxide semiconductor layer onto the first thickness of the oxide semiconductor layer at a second power density PD2, wherein the second power density PD2 is greater than the first power density PD1.

4. The method according to claim 3, wherein the second power density PD2 is equivalent to less than 250 W, preferably in a range from 25 W to less than 150 W, more preferably in a range from 50 W to 100 W for the sputtering target having the diameter of 3 inches (76.2 mm).

5. The method according to any of claims 3 to 4, wherein the second thickness is in a range from 1 nm to 50 nm, preferably in a range from 5 nm to 40 nm, more preferably in a range from 10 nm to 30 nm, for example 20 nm.

6. The method according to any previous claim, wherein the plasma sputtering comprises radio frequency, RF, plasma sputtering.

7. The method according to any previous claim, wherein the plasma sputtering comprises non-reactive plasma sputtering.

8. The method according to any previous claim, wherein the plasma sputtering is performed at an insulator layer temperature less than 180 °C, preferably up to 100 °C, more preferably up to 50 °C, most preferably up to 30 °C, for example room temperature, RT.

9. The method according to any previous claim, wherein the plasma sputtering is in an atmosphere at a pressure in a range from 1E-5 mbar to 1E-1 mbar, preferably in a range from 1E-4 mbar to 1E-2 mbar, for example 5E-3 mbar.

10. The method according to any previous claim, wherein a distance between the SAM and the sputtering target is in a range from 5 cm to 25 cm, preferably in a range from 10 cm to 15 cm, for example 12 cm.

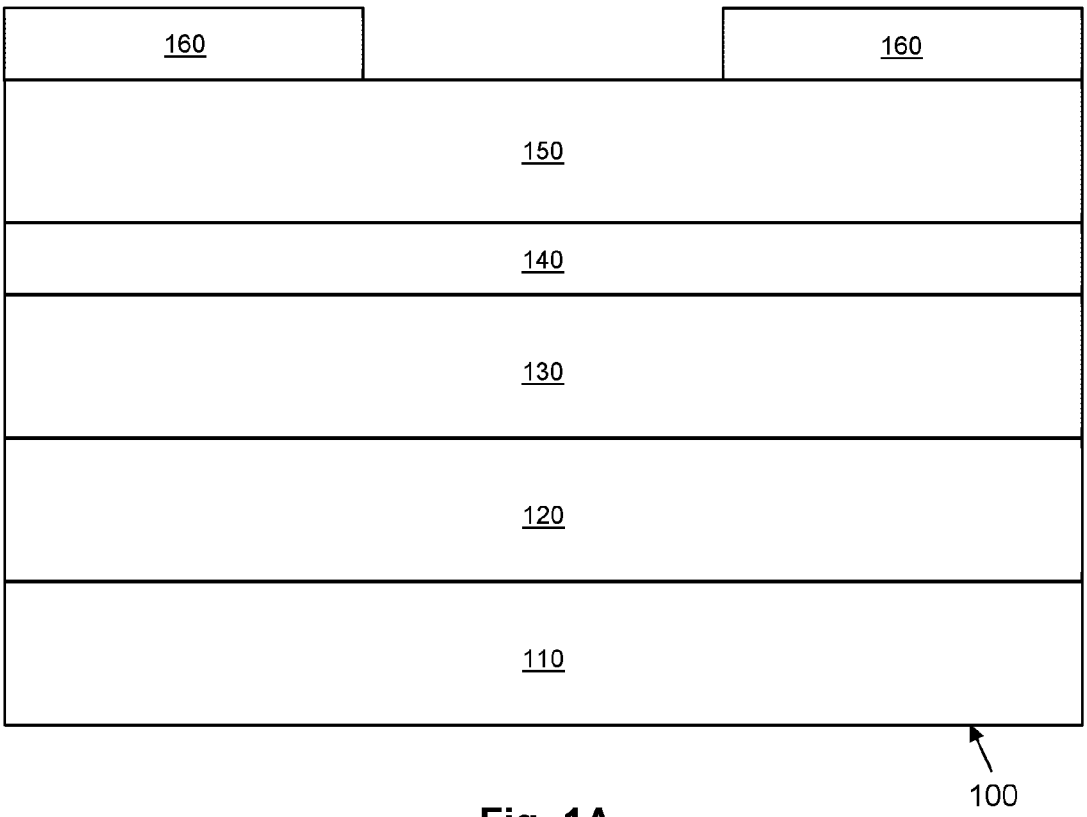

Fig. 1A

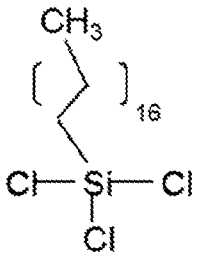

Fig. 1B

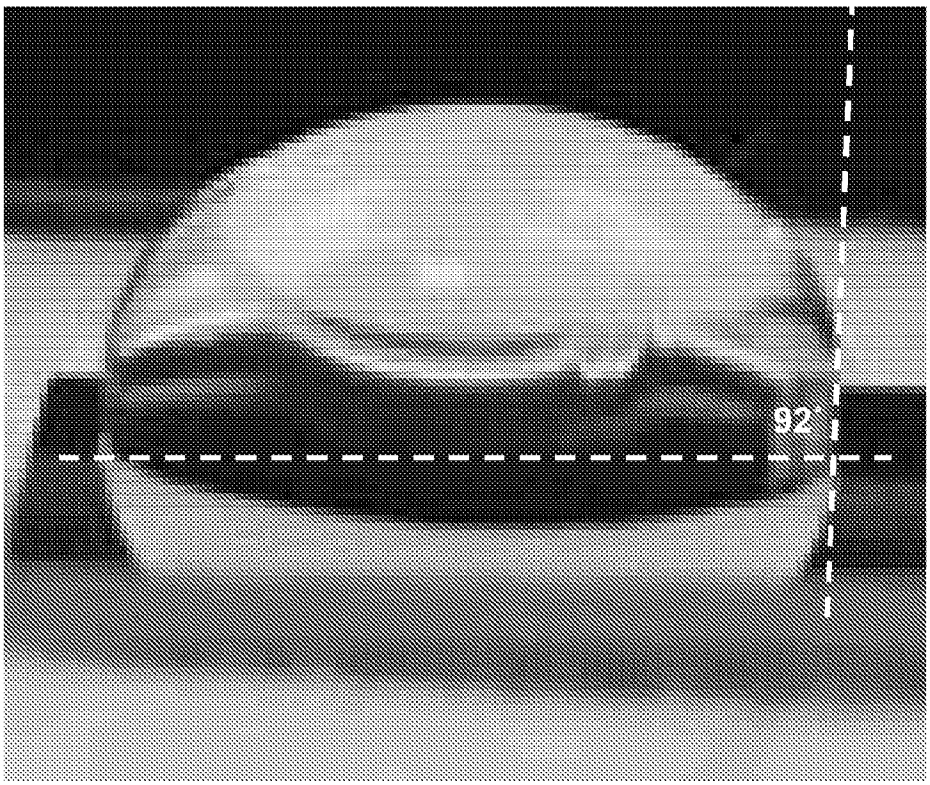

Fig. 1C

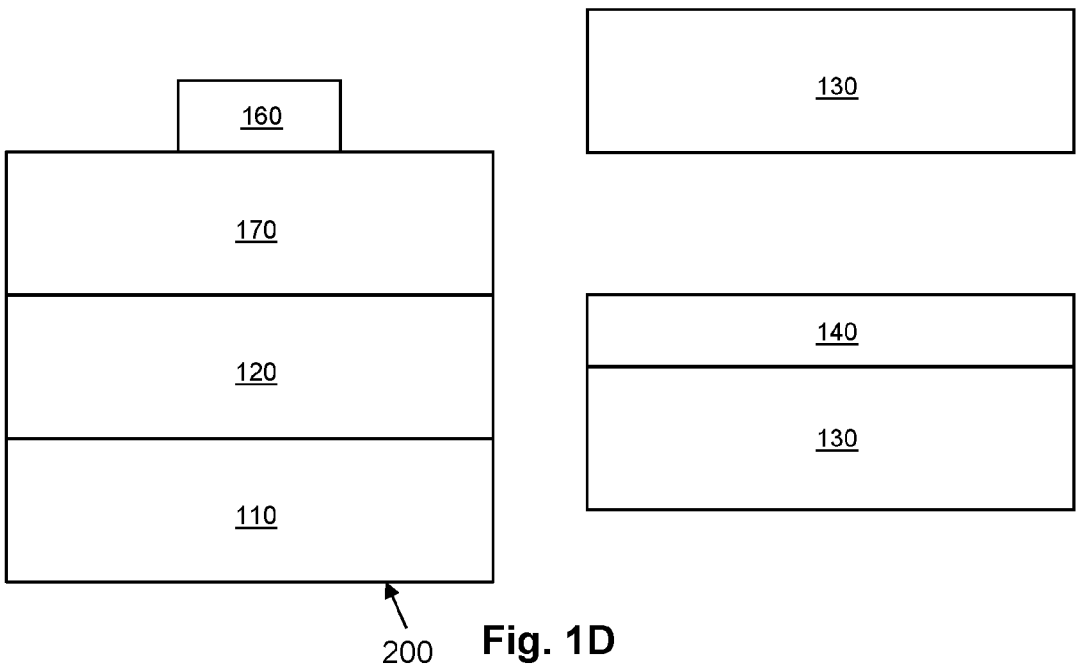

Fig. 1D

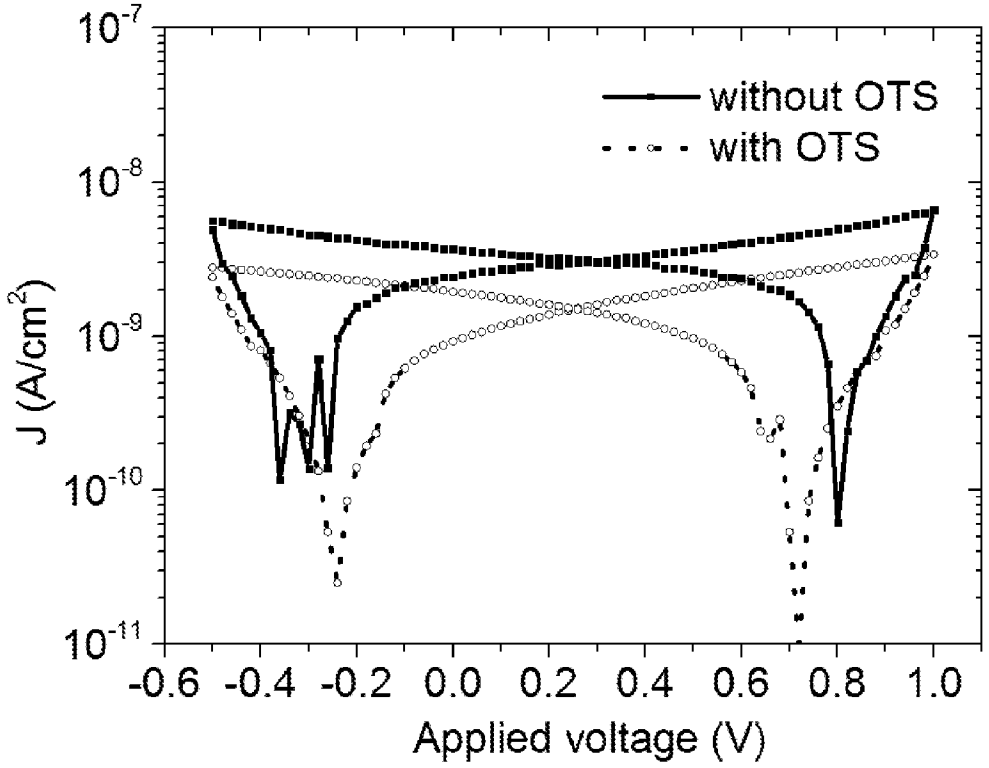
without OTS
with OTS
J (A/cm^2)
Applied voltage (V)

Fig. 1E

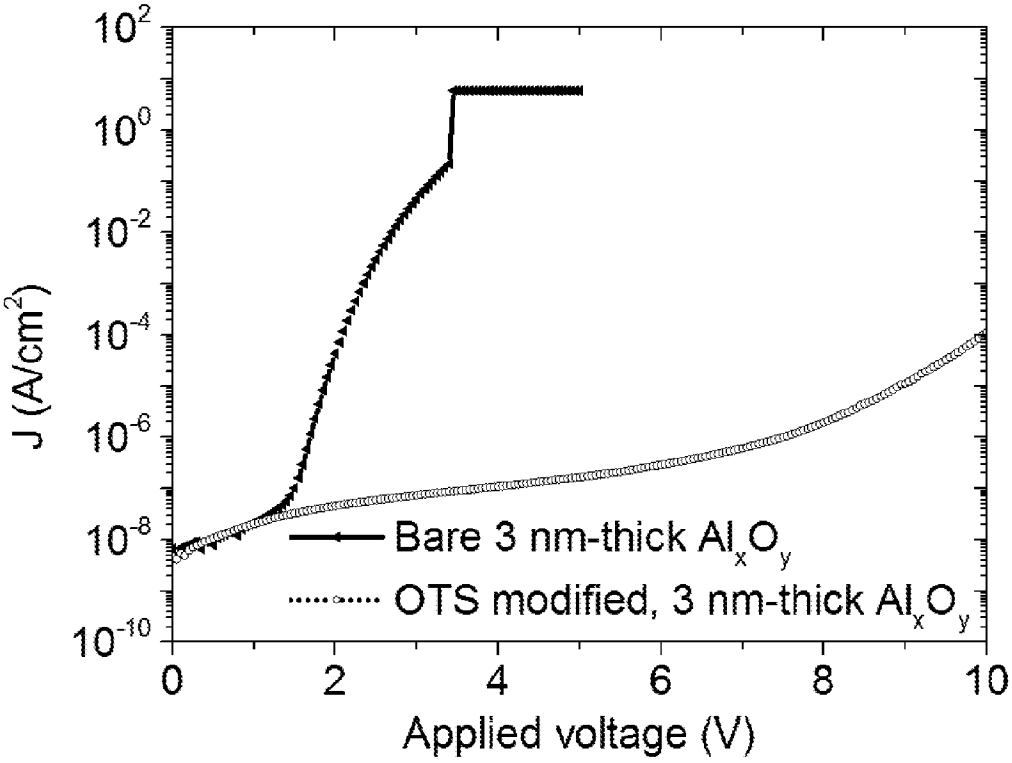
Bare 3 nm-thick Al_xO_y
OTS modified, 3 nm-thick Al_xO_y
J (A/cm^2)
Applied voltage (V)

Fig. 1F

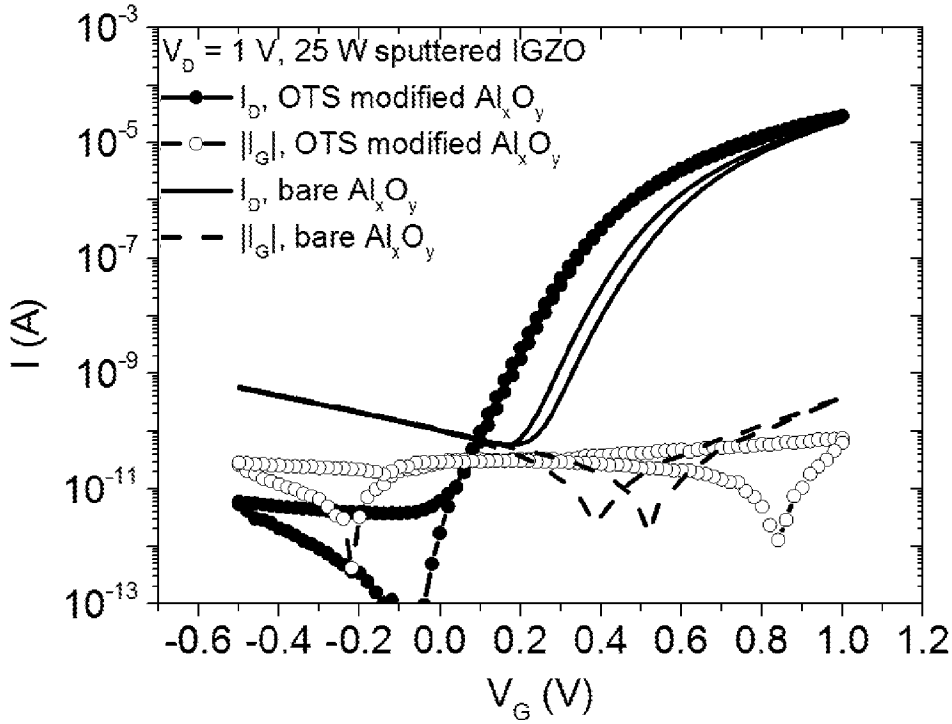
V_D = 1 V, 25 W sputtered IGZO
I_D, OTS modified Al_xO_y
$|I_G|$, OTS modified Al_xO_y
I_D, bare Al_xO_y
$|I_G|$, bare Al_xO_y
I (A)
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
-0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0 1.2
V_G (V)

Fig. 2A

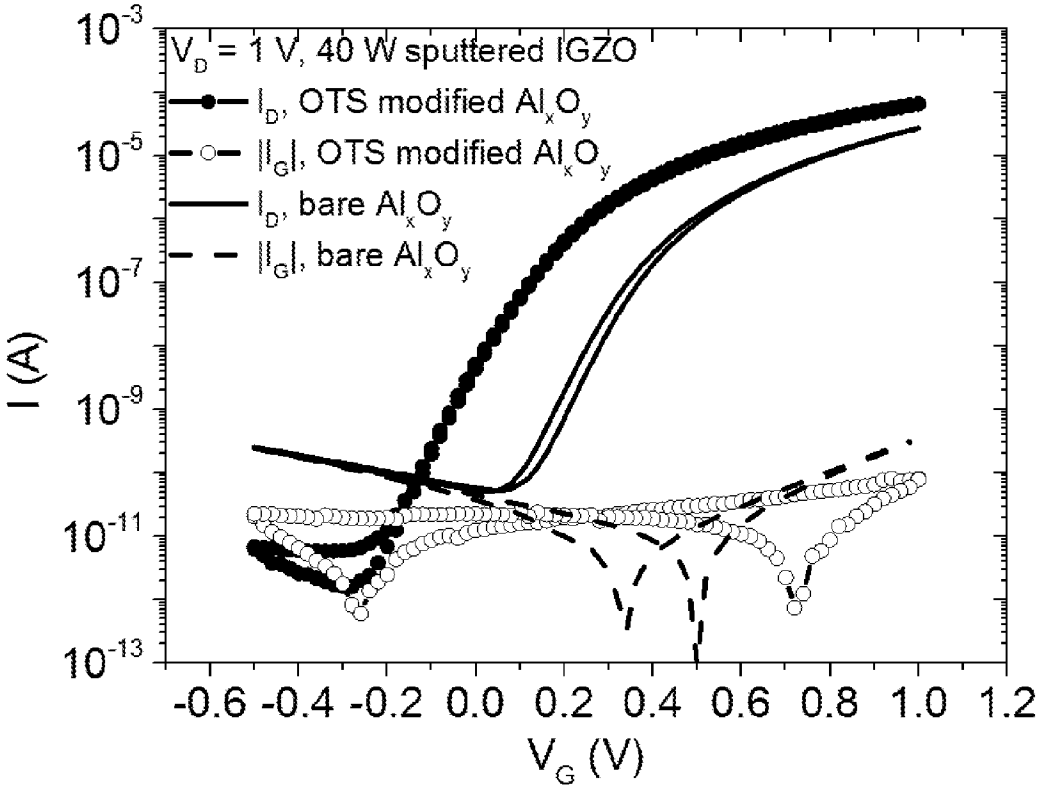
V_D = 1 V, 40 W sputtered IGZO
I_D, OTS modified Al_xO_y
$|I_G|$, OTS modified Al_xO_y
I_D, bare Al_xO_y
$|I_G|$, bare Al_xO_y
I (A)
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
-0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0 1.2
V_G (V)

Fig. 2B

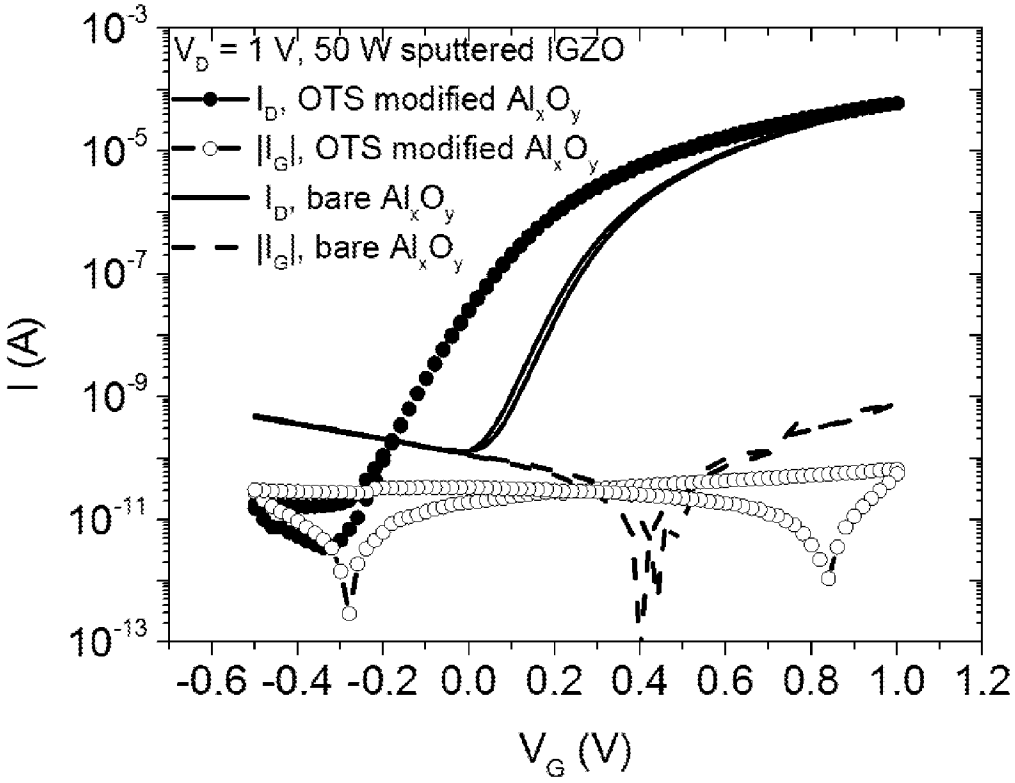
V_D = 1 V, 50 W sputtered IGZO
I_D, OTS modified Al_xO_y
$|I_G|$, OTS modified Al_xO_y
I_D, bare Al_xO_y
$|I_G|$, bare Al_xO_y
I (A)
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
-0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0 1.2
V_G (V)

Fig. 2C

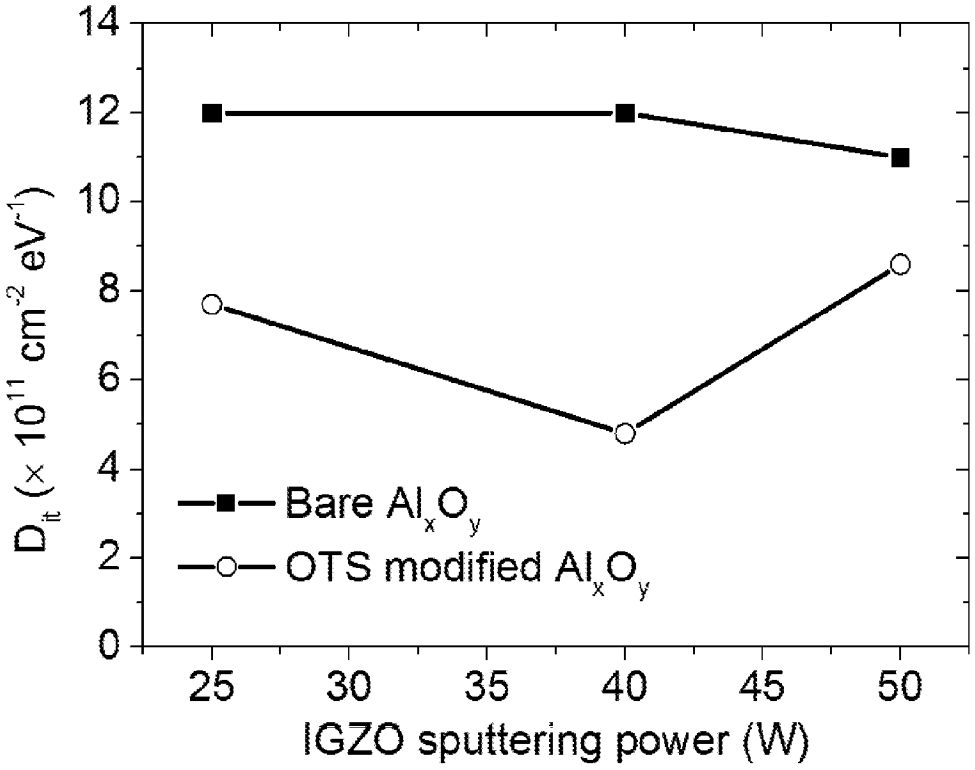
D_{it} ($\times 10^{11}$ cm^{-2} eV^{-1})
0 2 4 6 8 10 12 14
Bare Al_xO_y
OTS modified Al_xO_y
25 30 35 40 45 50
IGZO sputtering power (W)

Fig. 2D

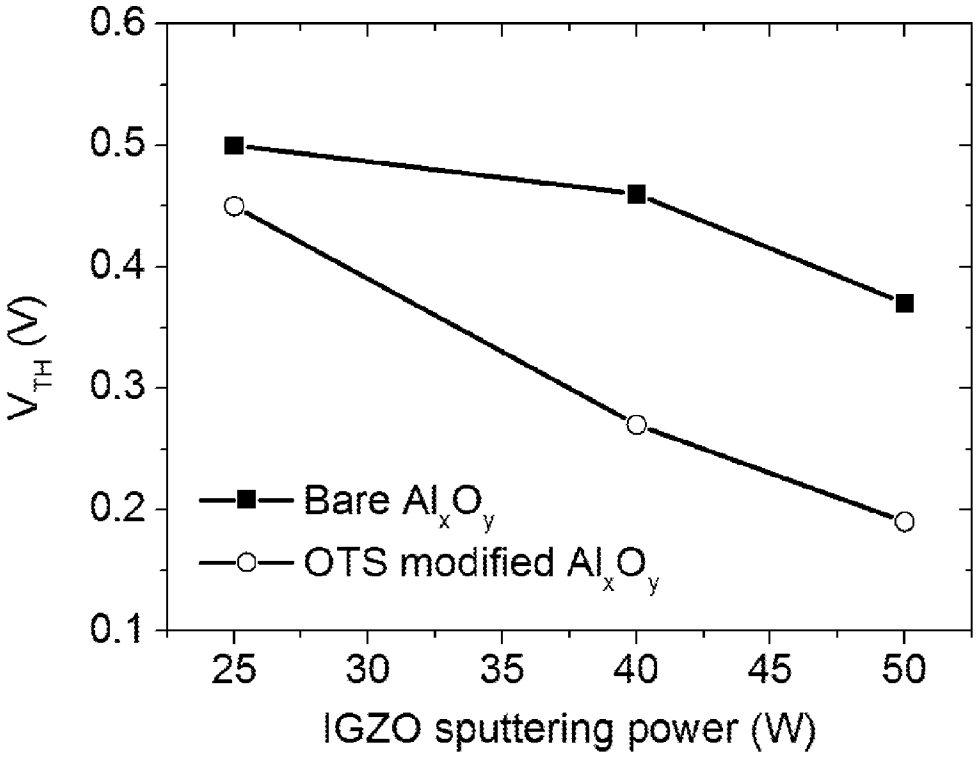
0.6
0.5
0.4
0.3
0.2
0.1
V_{TH} (V)
Bare Al_xO_y
OTS modified Al_xO_y
25
30
35
40
45
50
IGZO sputtering power (W)

Fig. 2E

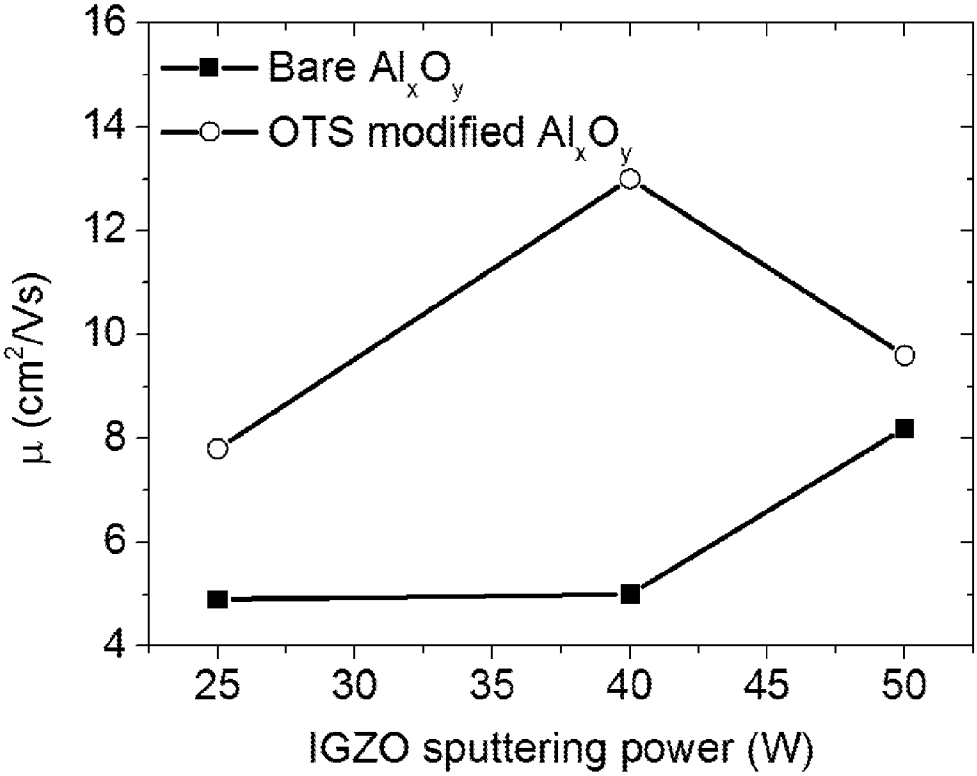
16
14
12
10
8
6
4
μ (cm^2/Vs)
Bare Al_xO_y
OTS modified Al_xO_y
25
30
35
40
45
50
IGZO sputtering power (W)

Fig. 2F

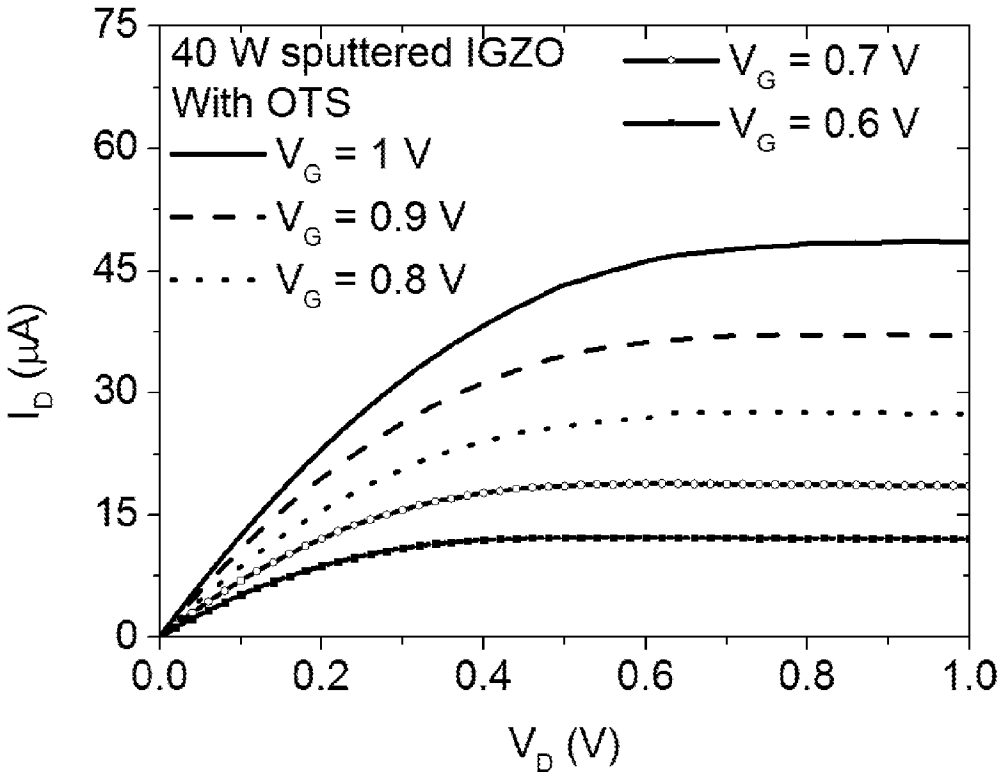

Fig. 3A1

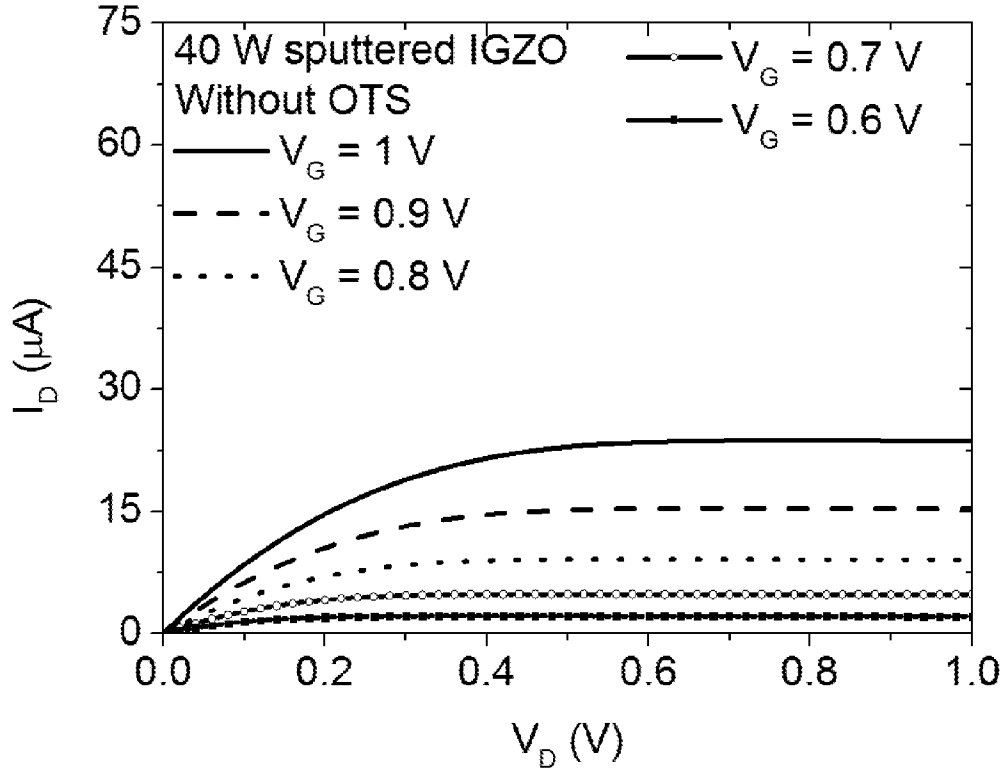

Fig. 3A2

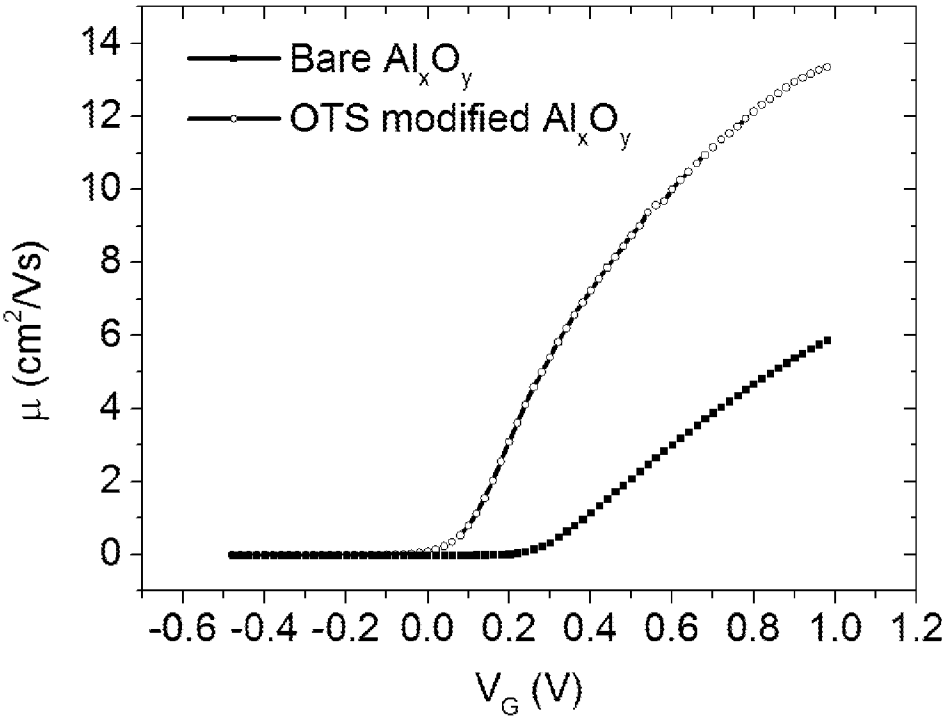
Bare Al_xO_y
OTS modified Al_xO_y
μ (cm^2/Vs)
V_G (V)
14
12
10
8
6
4
2
0
-0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0 1.2

Fig. 3B

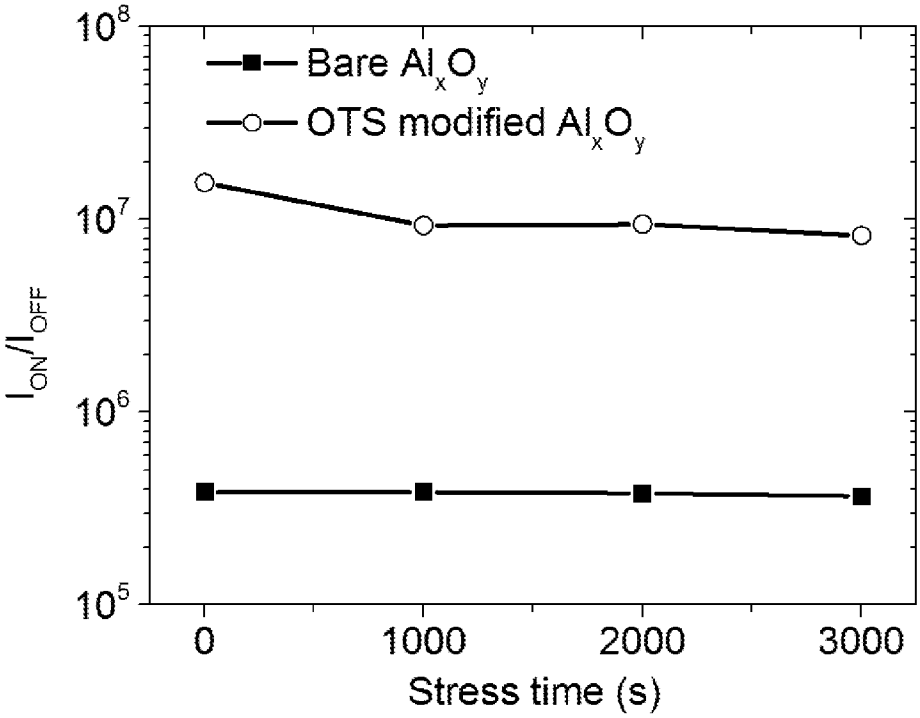
Bare Al_xO_y
OTS modified Al_xO_y
I_{ON}/I_{OFF}
Stress time (s)
10^8
10^7
10^6
10^5
0
1000
2000
3000

Fig. 3C

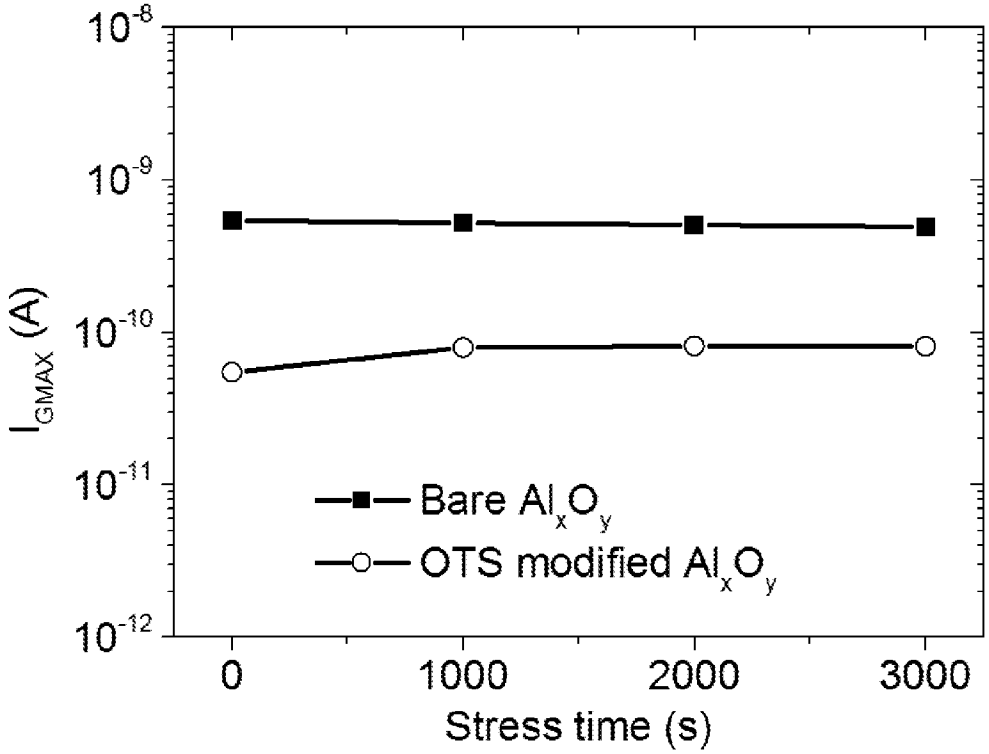
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I_{GMAX} (A)
Bare Al_xO_y
OTS modified Al_xO_y
0
1000
2000
3000
Stress time (s)

Fig. 3D

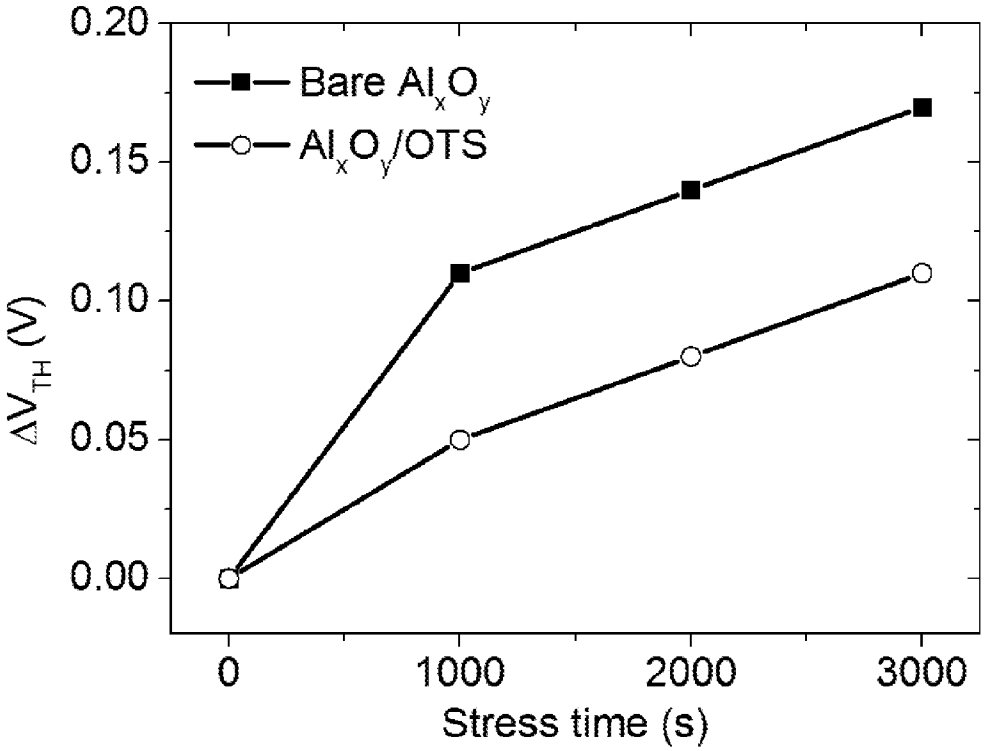
0.20
0.15
0.10
0.05
0.00
ΔV_{TH} (V)
Bare Al_xO_y
Al_xO_y/OTS
0
1000
2000
3000
Stress time (s)

Fig. 3E

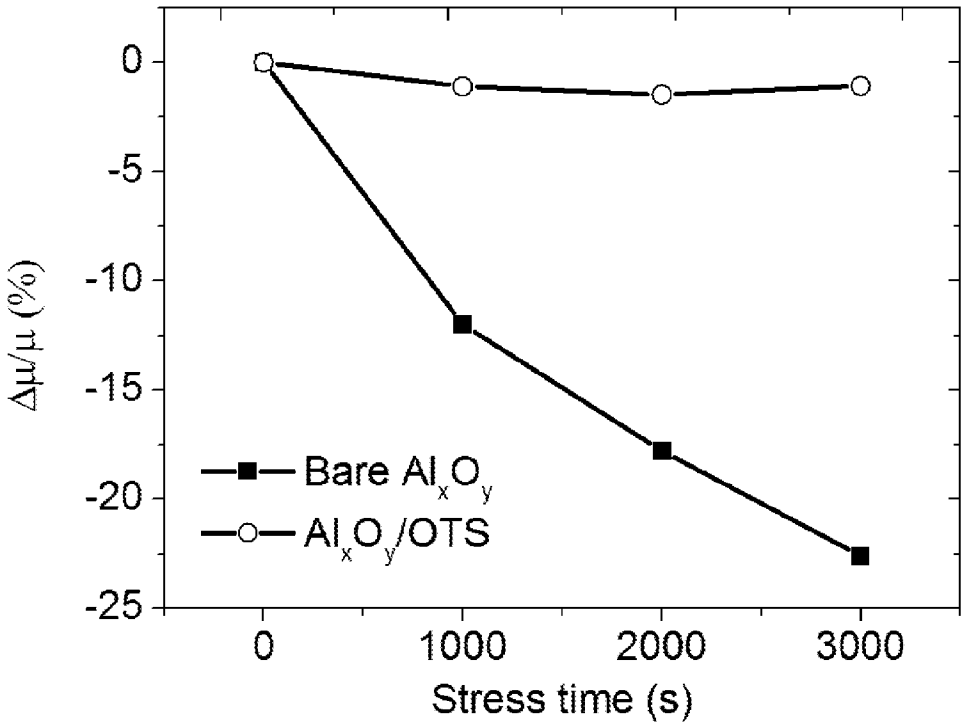
0
-5
-10
-15
-20
-25
Δμ/μ (%)
0
1000
2000
3000
Stress time (s)
Bare AlxOy
AlxOy/OTS

Fig. 3F

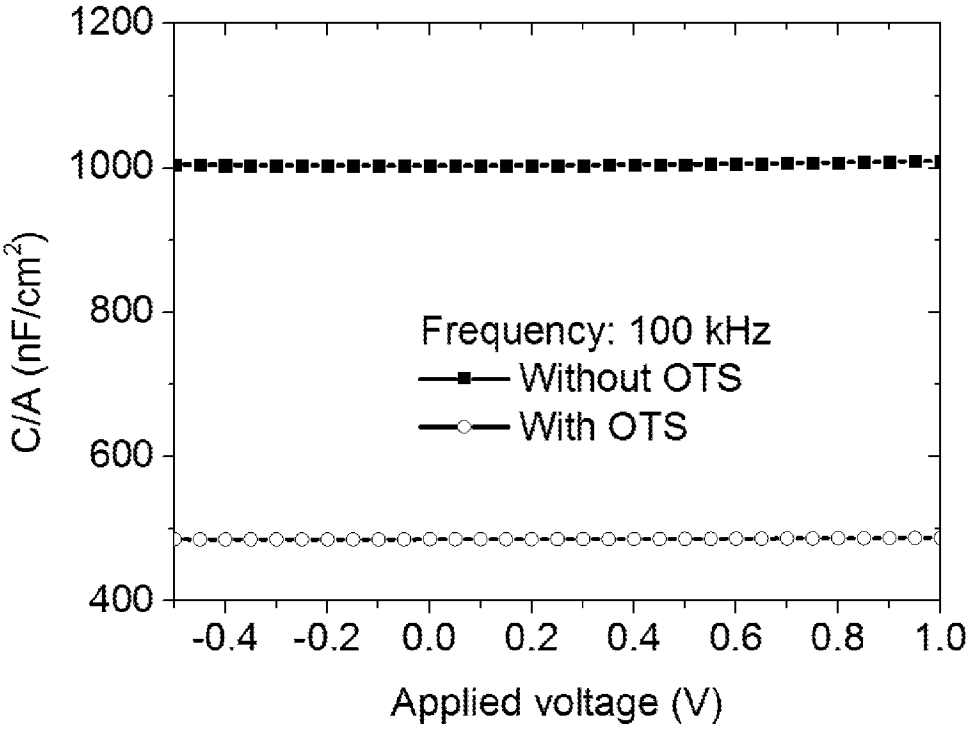
1200
1000
800
600
400
C/A (nF/cm^2)
Frequency: 100 kHz
Without OTS
With OTS
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0
Applied voltage (V)

Fig. 4A

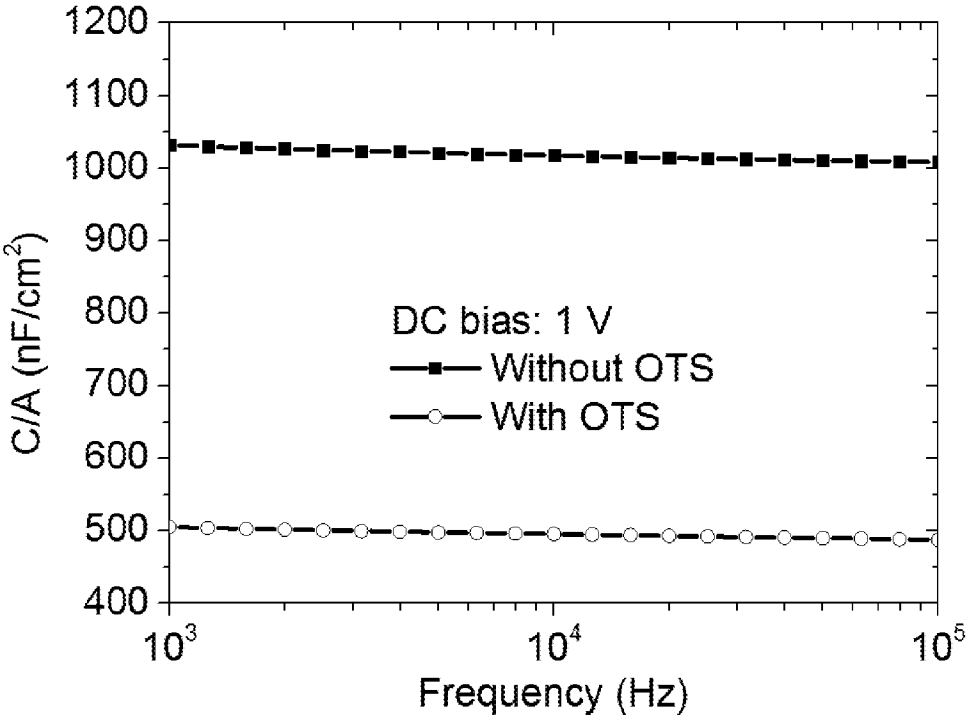
1200
1100
1000
900
800
700
600
500
400
C/A (nF/cm^2)
DC bias: 1 V
Without OTS
With OTS
10^3
10^4
10^5
Frequency (Hz)

Fig. 4B

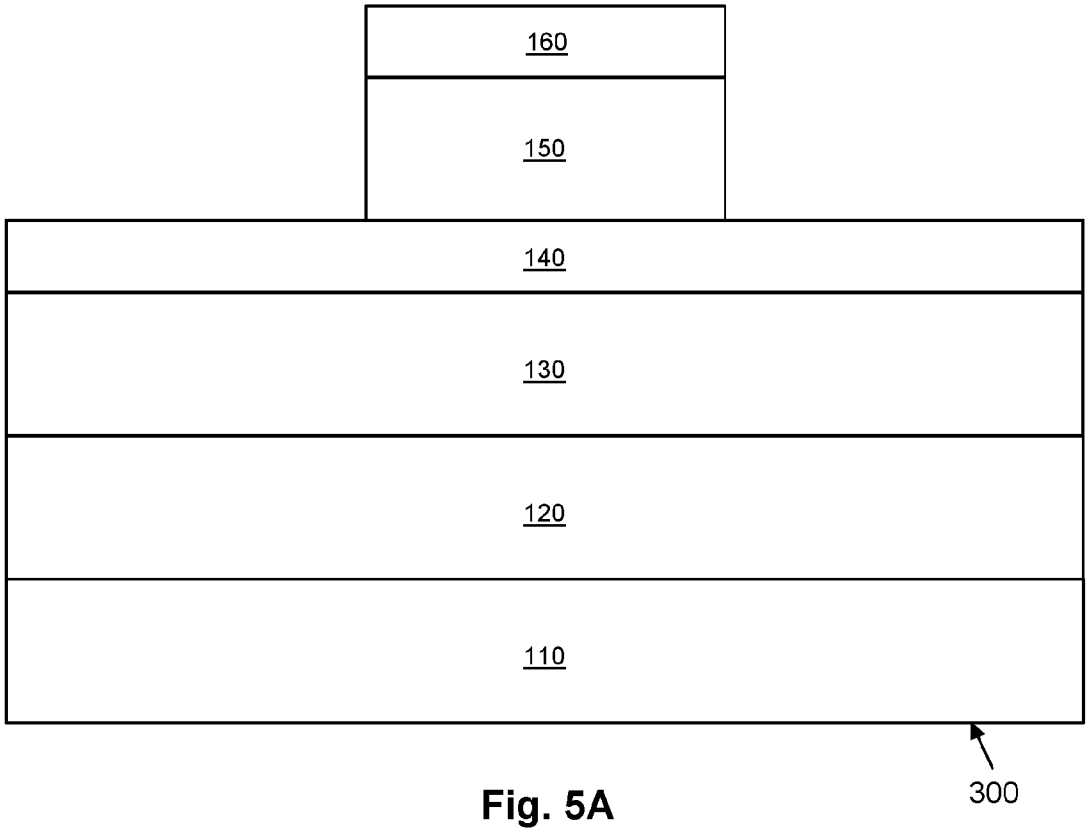

Fig. 5A

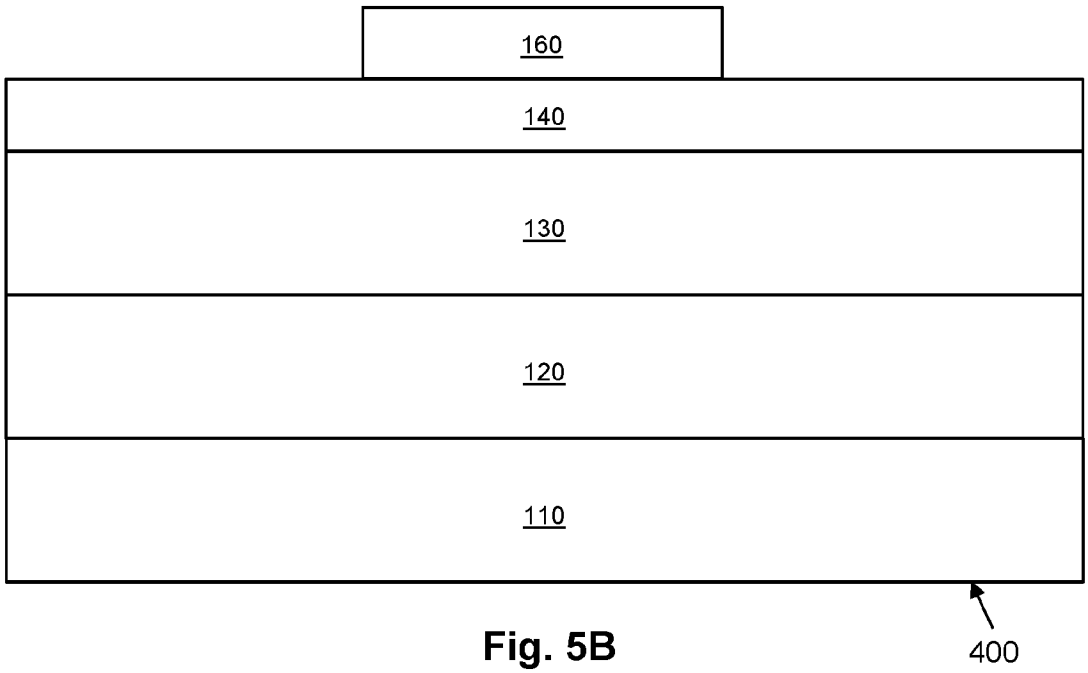

Fig. 5B

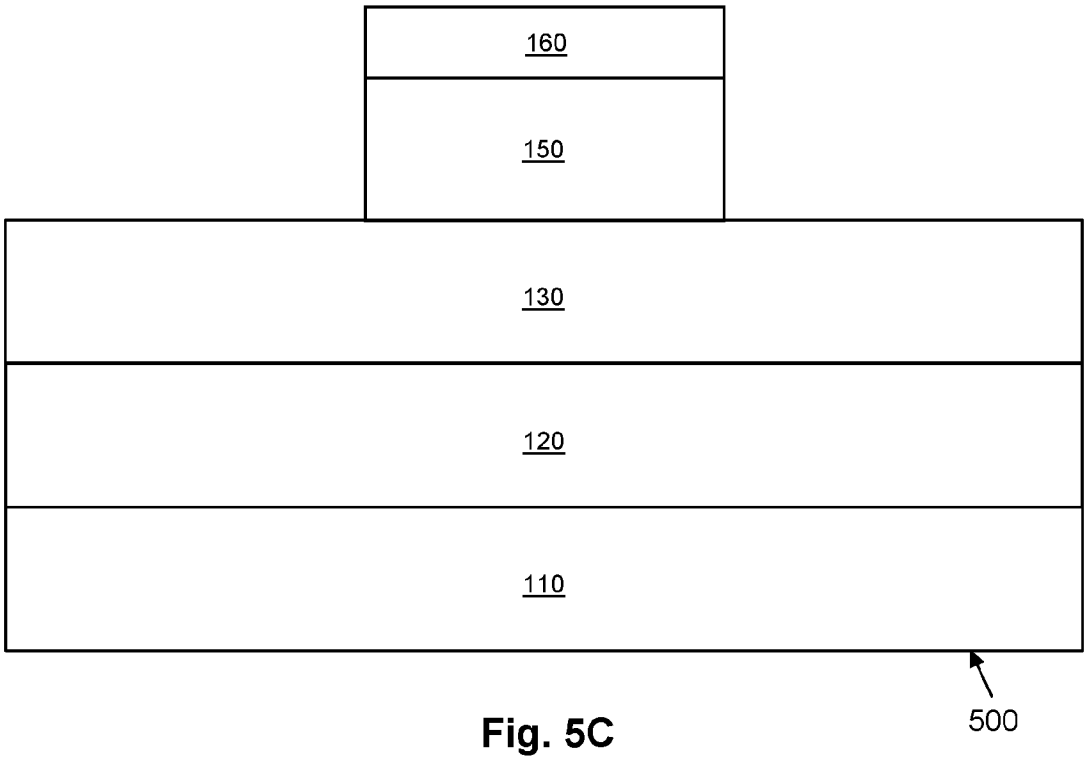
160
150
130
120
110
500

Fig. 5C

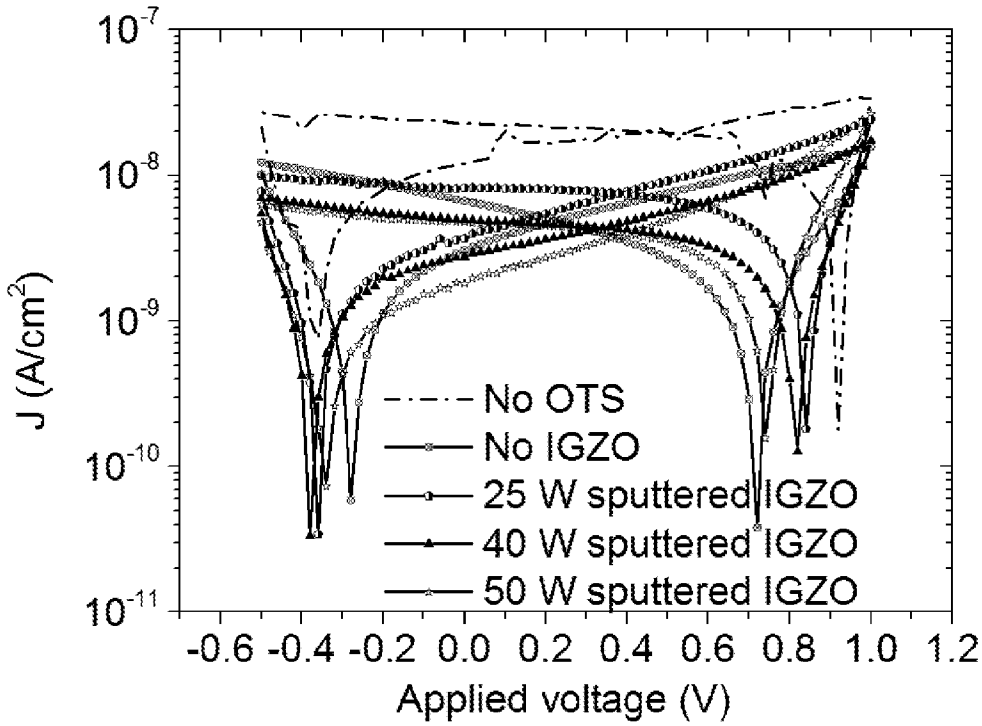
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
J (A/cm^2)
No OTS
No IGZO
25 W sputtered IGZO
40 W sputtered IGZO
50 W sputtered IGZO
-0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0 1.2
Applied voltage (V)

Fig. 5D

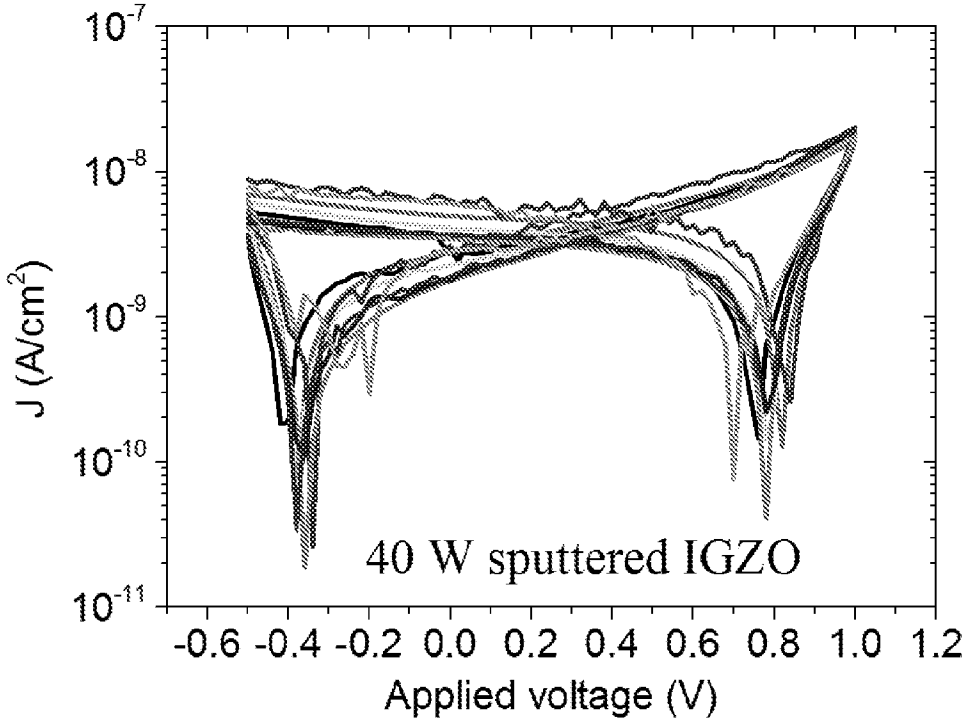
10-7
10-8
10-9
10-10
10-11
J (A/cm2)
40 W sputtered IGZO
-0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0 1.2
Applied voltage (V)

Fig. 5E

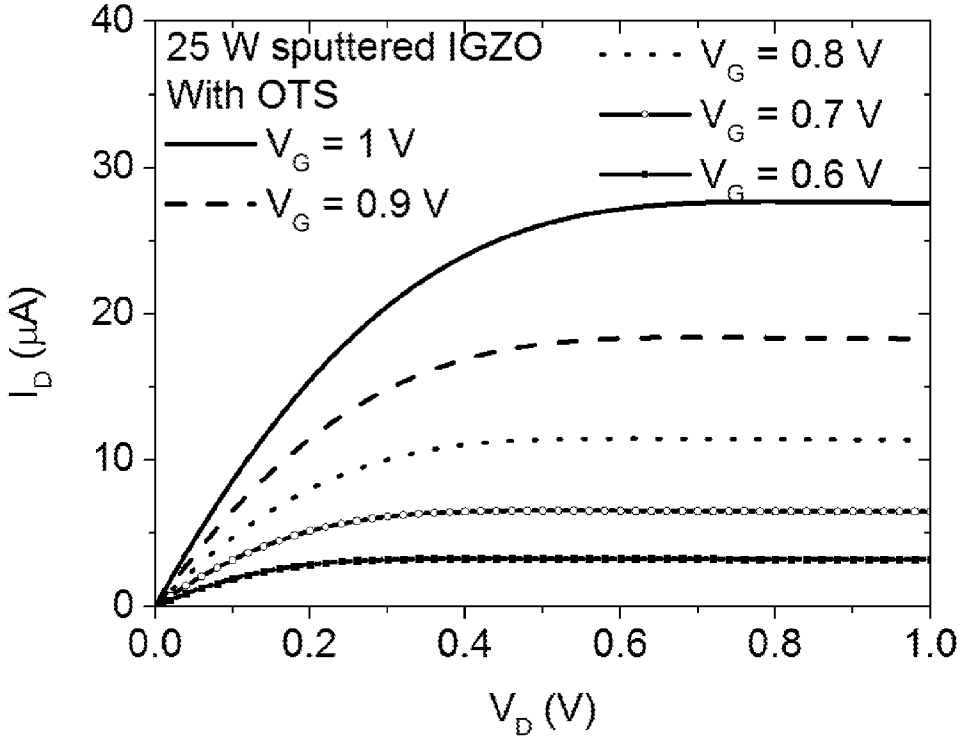

Fig. 6A1

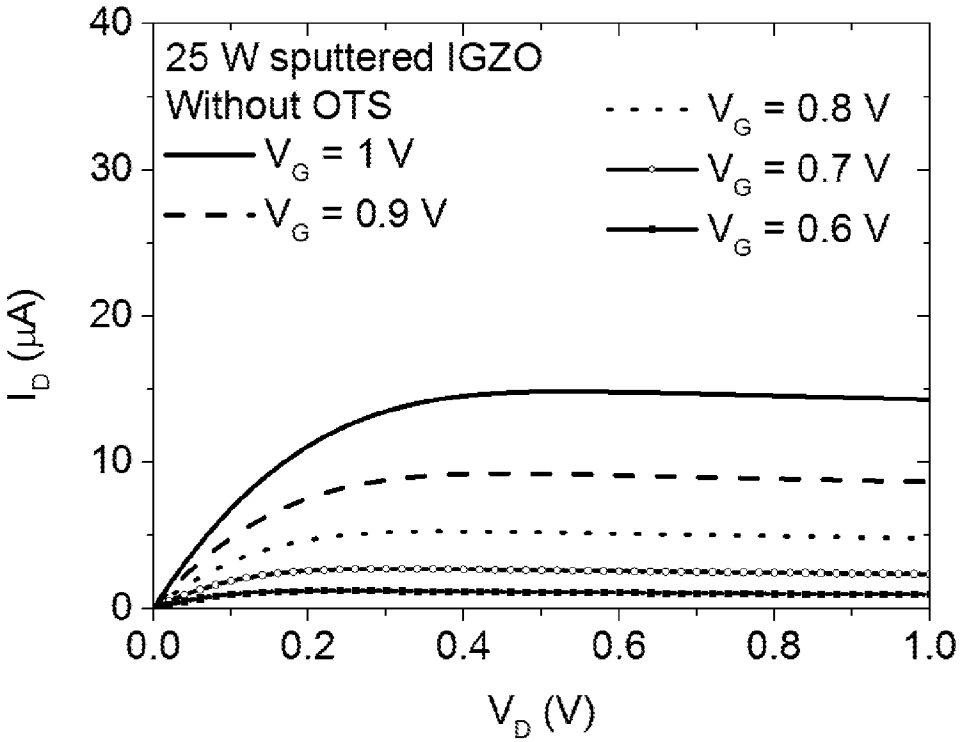

Fig. 6A2

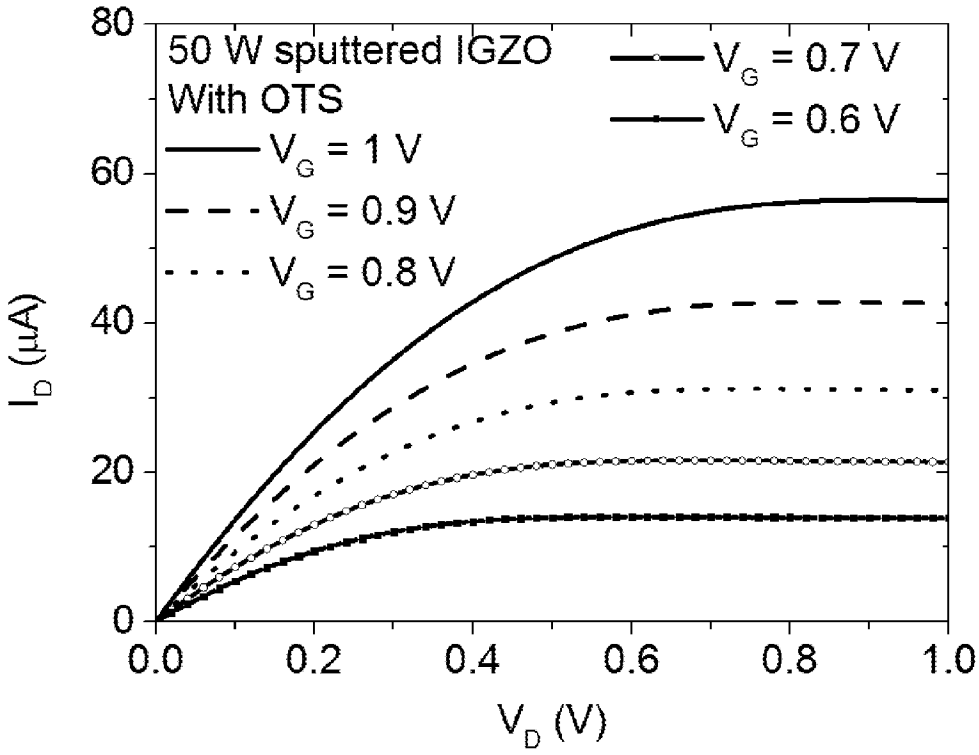

Fig. 6B1

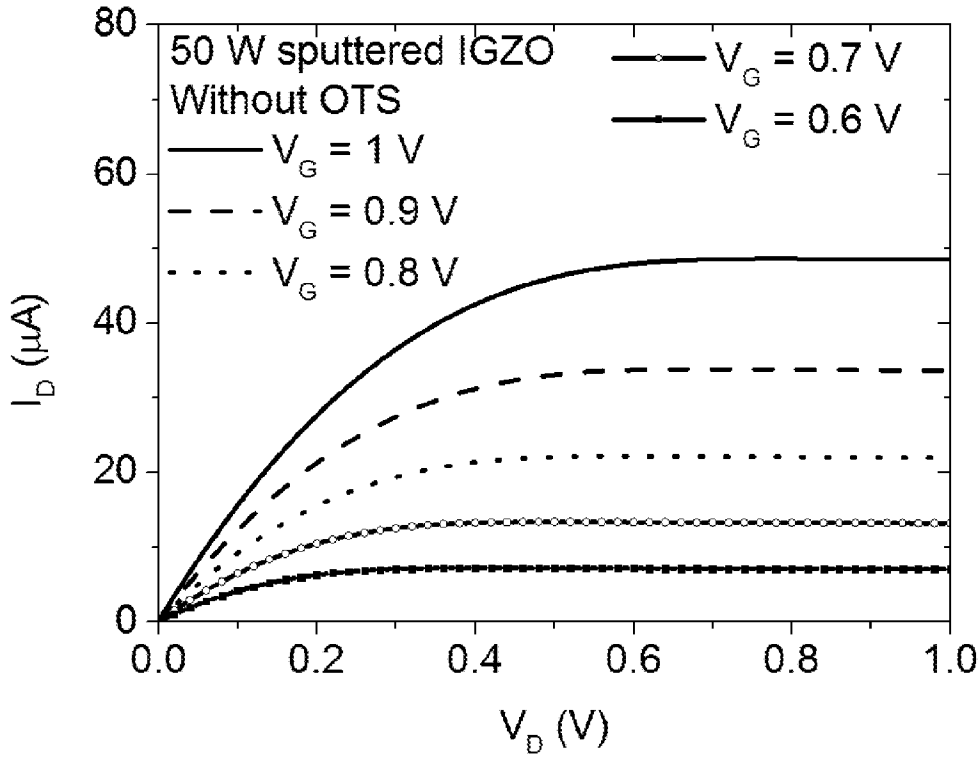

Fig. 6B2

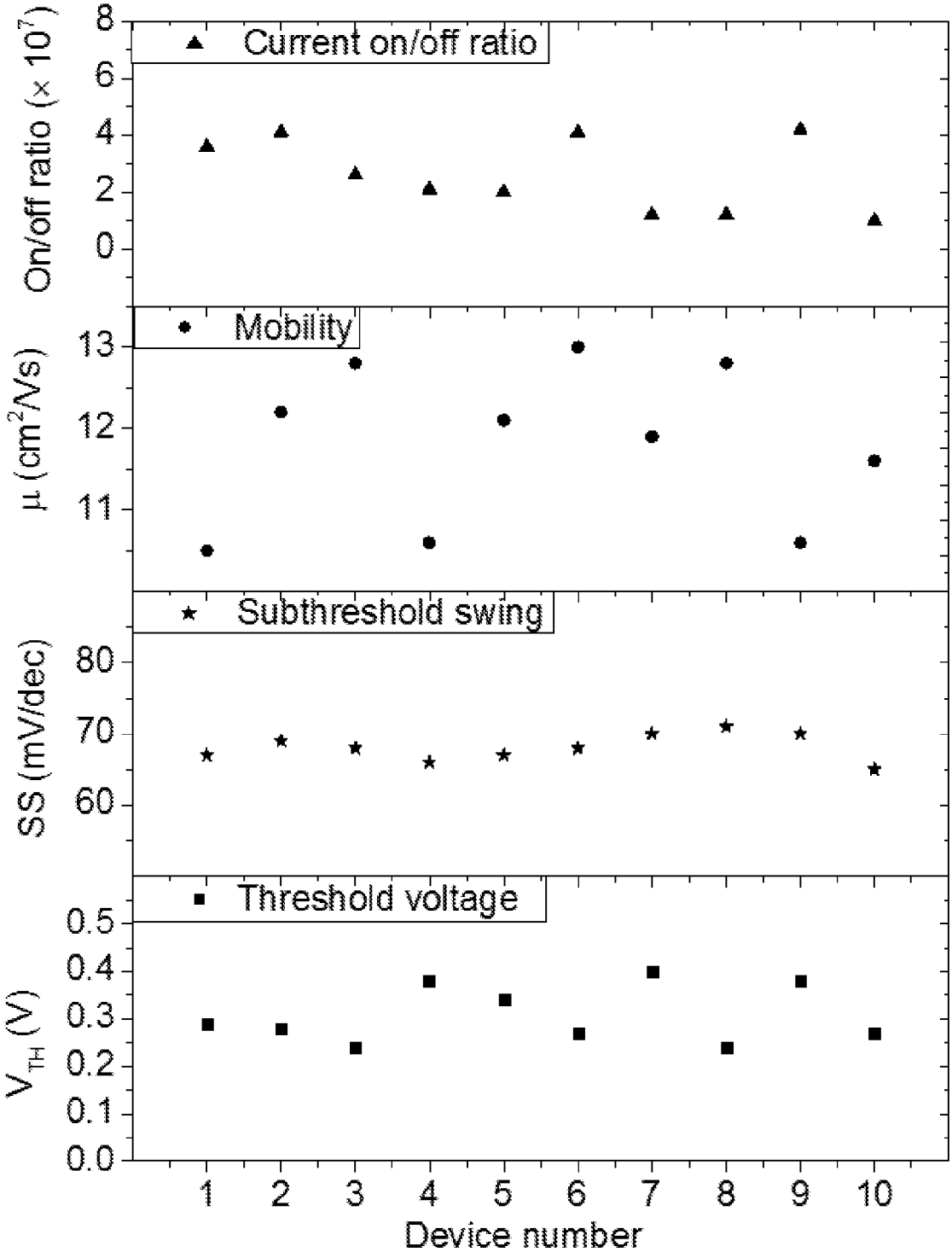
Current on/off ratio
On/off ratio (× 10^7)
8
6
4
2
0
Mobility
μ (cm²/Vs)
13
12
11
Subthreshold swing
SS (mV/dec)
80
70
60
Threshold voltage
V_TH (V)
0.5
0.4
0.3
0.2
0.1
0.0
1
2
3
4
5
6
7
8
9
10
Device number

Fig. 7

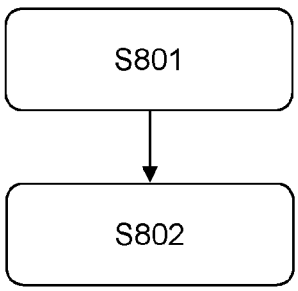

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2020/051009

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/02 H01L29/786
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PARK MIJEONG ET AL: "The effects of organic material-treated SiOdielectric surfaces on the electrical characteristics of inorganic amorphous In-Ga-Zn-O thin film transistors", APPLIED PHYSICS LETTERS, A I P PUBLISHING LLC, US, vol. 100, no. 10, 5 March 2012 (2012-03-05), pages 102110-102110, XP012155103, ISSN: 0003-6951, DOI: 10.1063/1.3691920 [retrieved on 2012-03-08] the whole document ----- -/--	1-10

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 2020	11/08/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Bruckmayer, Manfred

3

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2020/051009

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/133650 A1 (SUGAWARA YUTA [JP]) 12 May 2016 (2016-05-12) paragraph [0056] - paragraph [0068] paragraph [0125] - paragraph [0128] figure 8	1-10
X	US 2010/289024 A1 (ITO YUTAKA [JP]) 18 November 2010 (2010-11-18) paragraph [0125] - paragraph [0135] paragraph [0180] - paragraph [0188] figure 3	1-10
A	JUNFEI SHI ET AL: "The influence of RF power on the electrical properties of sputtered amorphous In-Ga-Zn-O thin films and devices", JOURNAL OF SEMICONDUCTORS, vol. 34, no. 8, August 2013 (2013-08), page 084003, XP055719671, GB; CN ISSN: 1674-4926, DOI: 10.1088/1674-4926/34/8/084003 the whole document	1-10
A	US 2011/006300 A1 (MOCHIZUKI FUMIHIKO [JP] ET AL) 13 January 2011 (2011-01-13) paragraph [0064] - paragraph [0093]	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2020/051009

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016133650 A1	12-05-2016	JP 6057106 B2	11-01-2017
		JP WO2014192221 A1	23-02-2017
		US 2016133650 A1	12-05-2016
		WO 2014192221 A1	04-12-2014
US 2010289024 A1	18-11-2010	NONE	
US 2011006300 A1	13-01-2011	JP 5528734 B2	25-06-2014
		JP 2011018777 A	27-01-2011
		KR 20110005217 A	17-01-2011
		US 2011006300 A1	13-01-2011