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Petty et al.

[11] **3,797,011**

[45] **Mar. 12, 1974**

[54] **OPERATION OF GASEOUS DISCHARGE DISPLAY/MEMORY PANELS**

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[73] Assignee: **Owens-Illinois, Inc.**, Toledo, Ohio

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[21] Appl. No.: **251,608**

[52] **U.S. Cl.** ..... **340/324 M**, 315/169 R, 340/343

[51] **Int. Cl.** **G08b 5/36**

[58] **Field of Search** ..... 340/324 M; 315/169 R

[56] **References Cited**

UNITED STATES PATENTS

3,609,747	9/1971	Ngo	340/324 M
3,614,769	10/1971	Coleman et al.	340/324 M
3,618,071	11/1971	Johnson et al.	340/324 M
3,651,509	3/1972	Ngo	340/324 M
3,654,388	4/1972	Slottow et al.	315/169 TV
3,671,938	6/1972	Ngo	340/166 EL

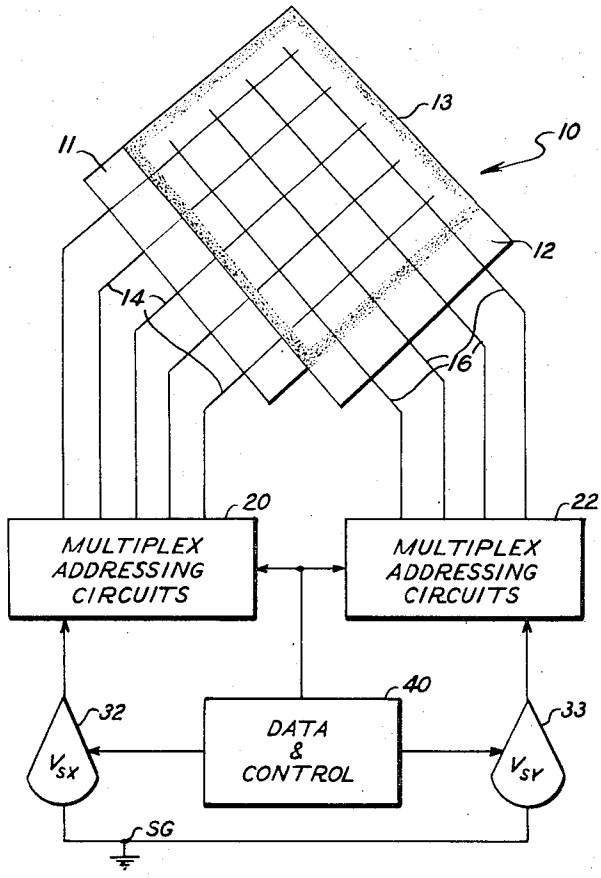
Primary Examiner—David L. Trafton

Attorney, Agent, or Firm—Donald Keith Wedding

[57] **ABSTRACT**

A gas discharge display/memory panel uses operating control pulses in the saturation mode. The operating control pulses include discharge initiating and/or discharge terminating pulses, each selected pulse being of a magnitude such that every discharge associated with each selected pulse occurs in the saturation mode and the effects of panel non-uniformity are minimized.

5 Claims, 11 Drawing Figures



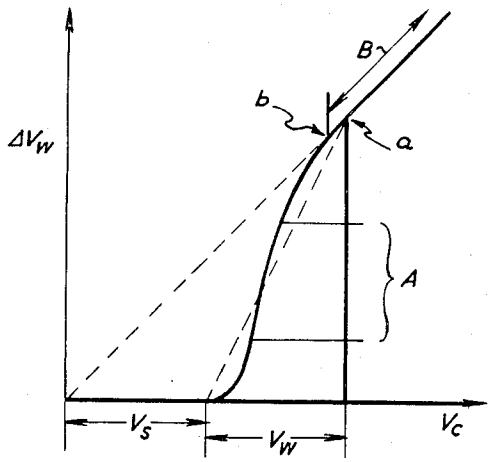


FIG. 1

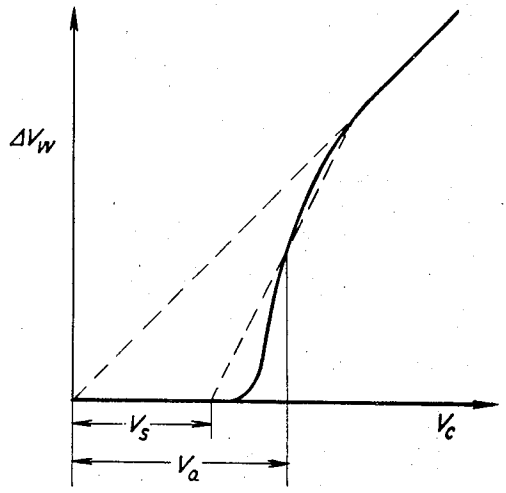


FIG. 2

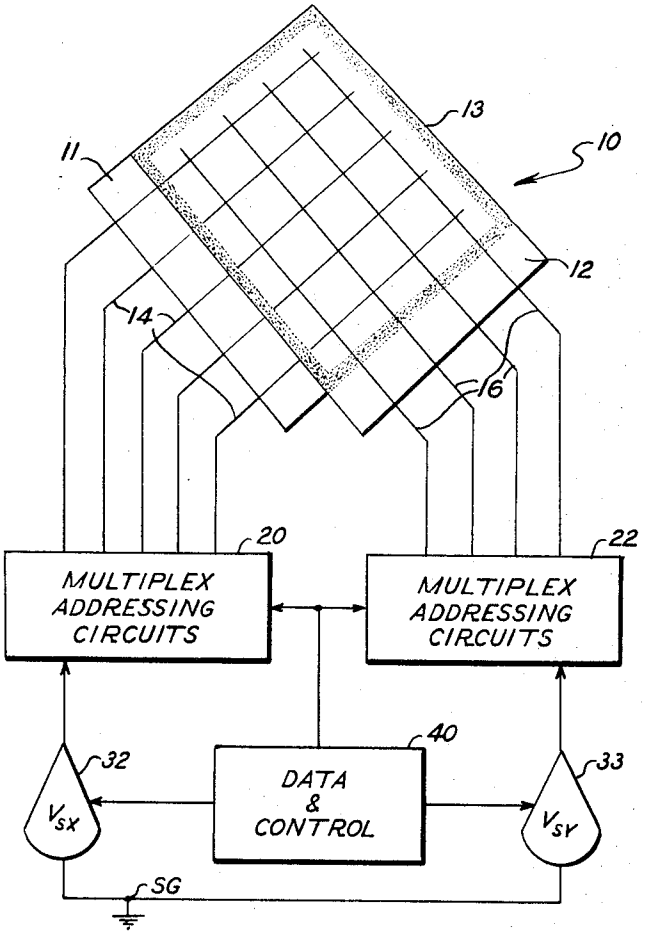


FIG. 3

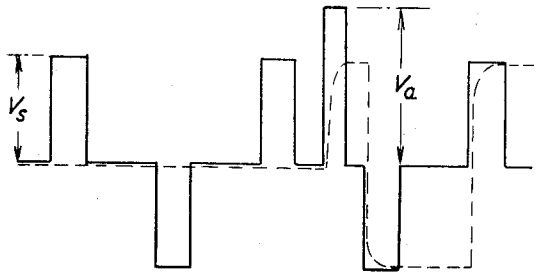


FIG. 4

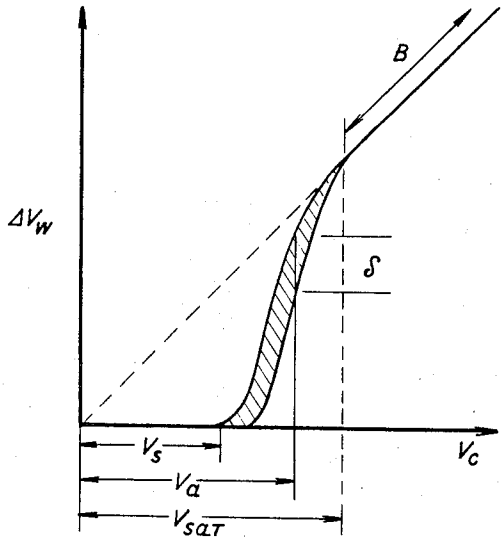


FIG. 5

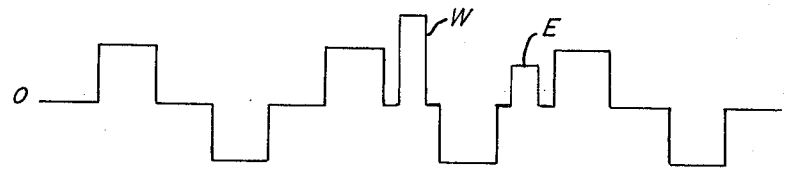


FIG. 6 (PRIOR ART)

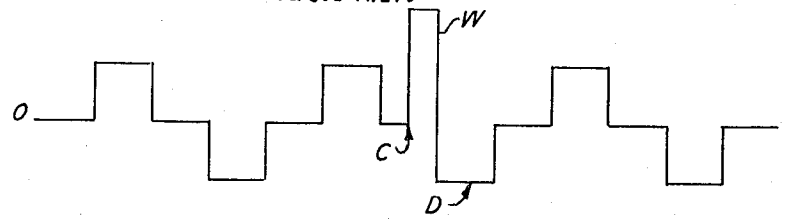


FIG. 7

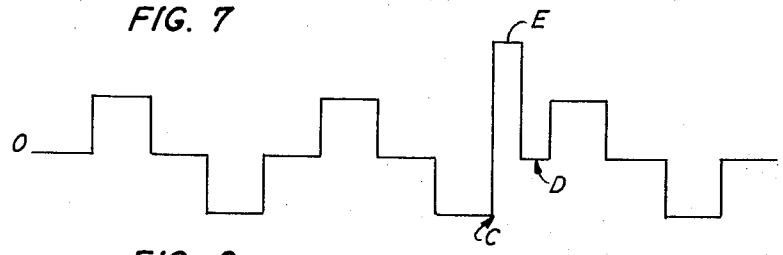


FIG. 8

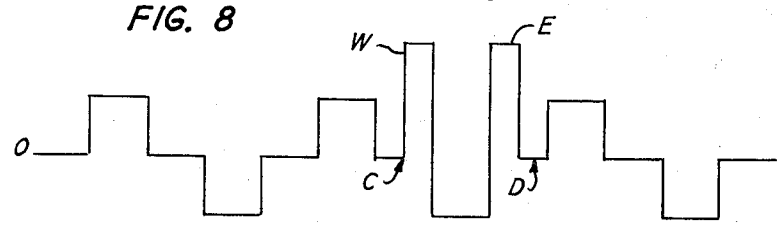


FIG. 9

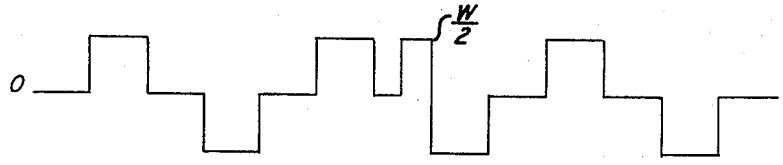


FIG. 10

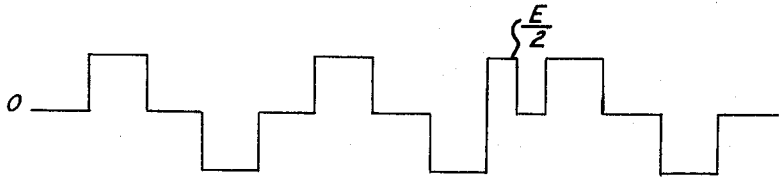


FIG. 11

OPERATION OF GASEOUS DISCHARGE DISPLAY/MEMORY PANELS

BACKGROUND OF THE INVENTION

Gaseous discharge display/memory panels and devices of the type to which the present invention pertain are disclosed in U. S. Pat. No. 3,499,167 issued to Baker, et al. and U. S. Pat. No. 3,559,190 issued to Bitzer, et al. Panels as disclosed in these patents have inherent memory constituted by the storage of charges produced by discharge on one or more dielectric surfaces in contact with the gas and dielectrically or insulatively isolating the electrodes for supplying operating potential from the gaseous medium. Typically, the electrodes are non-conductively coupled to the gas and in the case of Baker, et al. patent the dielectric is a thin glass coating on each conductor array. The conductors are arrayed in columns and rows to form a cross-conductor matrix between which a gas medium, typically a mixture of two gases, is placed at a selected pressure. For example, a neon-argon gas mixture (99.9 percent neon and 0.1 percent argon at a pressure slightly less than atmospheric) is suitable. The dielectric coatings in such panels may have a dielectric or insulating overcoating as disclosed in U. S. Pat. No. 3,634,719, issued to Ernsthausen.

Evidence to date indicates that in normal operation of panels as described above, such panel sustains in a saturation mode, that is, the applied sustaining signal is essentially neutralized by the wall voltage formed on discharge. However, the selected addressing (both write and erase) pulse has been accomplished by attempting to set the wall voltage level at some more or less precise value by firing the cell sites in the panel at an intermediate point on the curve or plot of the change in wall voltage versus the V_c characteristic of the panel. Due to the stable nature of discharge sequences once initiated, deviations from this are permissible. In fact, deviations are inevitable due to panel non-uniformities so that the average write voltage actually produces a variety of wall voltages, V_w, depending upon the particular site in the panel which has been selected.

In accordance with the present invention, cell sites are operated in the saturation mode so that panel non-uniformities are minimized or become irrelevant and have no significant effect on panel behavior by the application of at least one member selected from a discharge initiating (write) pulse or discharge terminating (erase) pulse. The selected pulse voltage must be at least as great as the saturation voltage for all discharges. Thus for purposes of writing and entering information to the panel, a relatively larger firing voltage pulse is used so as to achieve saturation mode in the first firing.

The above and other objects and advantages and features of the invention will become more apparent from the following specification, when considered with the accompanying drawings wherein:

FIG. **1** is a graph illustrating a prior art mode of sustaining of gaseous discharge panels,

FIG. **2** is a graph illustrating an ideal mode of addressing a gaseous discharge display/memory panel according to the prior art,

FIG. **3** illustrates the firing, sustaining and wall voltage waveform generators for the ideal operation illustrated in FIG. **2**,

FIG. **4** illustrates the sustaining and write waveforms and the wall voltage waveform according to the ideal operation as described in the prior art,

FIG. **5** is a graph illustrating the prior art mode of panel operation as depicted in FIG. **2** and the saturation voltage as incorporated in the present invention,

FIGS. **6, 7, 8, 9, 10,** and **11** illustrate various addressing signal waveforms for addressing the panel.

In FIG. **3,** gaseous discharge display panel **10,** for example, of the type disclosed in Baker, et. al. U. S. Pat. No. 3,499,167, provided with thin overcoating on the dielectric (not shown) with the discharge gap (distance between dielectric surfaces bounded the gas) set at between 4 and 6 mils. The panel **10** is constituted by a row conductor plate **11** and a column conductor plate **12** joined in spaced apart relation by a spacer sealant **13** to provide the aforementioned discharge gap distance and the thin gas chamber in which the gaseous medium is placed under a suitable pressure, e.g., slightly under atmospheric and in the flat portion of the paschen curve for a neon-argon gas mixture.

The row conductor plate **11** carries row conductor array **14** and border conditioning conductor (not shown) at the conductor plate **11,** and has column conductor array **16** in the writing or viewing area of the data display of the panel and border conditioning or side conductors (not shown). In a typical panel, the conductors may be spaced very closely together as, for example, on 20 mil centers and the conductors may be served with operating potentials from the same end or edge of the plates or from opposite ends in alternate fashion as disclosed in Hoehn U.S. Pat. No. 3,631,287.

Addressing circuits **20** for the row conductors and addressing circuits **22** for the column conductors may be of any suitable type such as multiplex resistor-diode selection matrices or individual addressing or pulsing circuits for each row or column conductor. An example of such matrix circuits is disclosed in copending U. S. patent application Ser. No. 135,621, filed Apr. 19, 1971, by Donald Leuck and assigned to the same assignee as the instant patent application now U. S. Pat. No. 3,665,400. Such matrix circuits float upon their respective sustainer sources **32** and **33,** respectively. It will be noted that the sustainer generators **32** and **33** have a common point of reference potential SG. The row addressing circuits and the column addressing circuits are controlled by signals from data source and control circuit **40** which also controls the sustainer generators **32** and **33.**

In accordance with this invention, it has been discovered that the effects of panel non-uniformity are minimized by applying all panel operating potentials at a magnitude such that every panel cell discharge occurs in the saturation mode.

For the purposes of this invention, the saturation mode of operation is defined in FIG. **1** by the section of the V_c versus ΔV_w characteristic to the right of point *b;* that is, the section B of the curve in which the cell voltage is essentially neutralized by the produced discharge or where V_c is approximately equal to ΔV_w.

As mentioned above, studies show that in normal operation any discharge site of panel **10,** when supplied with a normal sustaining potential, will, in the ON state, operate in a saturation mode; that is, the applied sus-

tainer voltage signal pulse is essentially neutralized by the discharge as shown by point a in FIG. 1. FIG. 1 is a plot of the change in wall voltage ΔV_w against the voltage appearing at the site, V_c. It will be noted that in the normal conditions the sustaining voltage V_s when added to the wall voltage V_w results in the voltage V_c which is the normal saturation mode operating point for the site in this sustained operation. That is, the applied signal V_s (in the saturation mode) is in essence completely neutralized by the wall voltage, e.g., the discharge. However, in the past, on addressing both the write and erase functions have been accomplished by attempting to set the wall voltage level at some more or less precise value by firing the sites in the portion of region of the curve marked A in FIG. 1.

The ideal is shown in FIG. 2 and the waveforms therefor shown in FIG. 4. As stated, deviations are allowed due to the stable nature of the discharge sequence, and, in fact, these deviations are inevitable due to panel non-uniformity. Thus, the characteristic curve of a panel operation shown in FIG. 5 hereof gives a more accurate representation of the panel characteristics. Note that the average write voltage (V_a) actually produces a variety of wall voltages with deviation δ depending upon the particular sites selected. In accordance with the present invention, all sites are operated by applying selected write and/or erase voltages in the saturation mode (that is in the region B of FIG. 4) so that the panel non-uniformities become substantially irrelevant and have no effect on panel behavior. This is because all sites will reach the same potential when fired. Thus, the V_c must be at least equal to or greater than the saturation voltage V_{sat} for the sustaining signal discharges plus the discharges associated with at least one member selected from a discharge initiating pulse (write) and/or discharge terminating pulse (erase).

FIG. 6 shows one typical prior art sustaining waveform signal with a write pulse W and an erase pulse E.

FIG. 7 shows the same prior art sustaining waveform, but with a write pulse W in accordance with the practice of this invention. The write pulse of FIG. 6 turns a cell on by attempting to precisely set the wall voltage at the appropriate level in a single discharge, whereas the write pulse of FIG. 7 as practiced in this invention uses two discharges to accomplish the same result. However, because both of the discharges of FIG. 7 are in the saturation mode, cell to cell non-uniformities become insignificant and panel operation is improved. The amplitude of the write pulse is sufficient to cause an OFF cell to fire in the saturated mode thereby bringing the wall voltage to substantially the same voltage as the applied pulse voltage. On the negative transition the cell voltage is, thus, again sufficient to cause a discharge in the saturation mode, bringing the wall voltage effectively to the sustaining pulse level. The cell is then ON.

FIG. 8 shows a prior art sustaining waveform with an erase pulse E in accordance with the practice of this invention. As with the write pulse, the erase pulse turns the cell OFF with a two discharge sequence, both of which are in the saturated region of the V_c versus ΔV_w characteristic of FIG. 5. The pulse is sufficient to cause a cell in the ON state to discharge in the saturation mode placing a wall voltage essentially equal to the pulse amplitude across the cell. On the return to zero, this voltage again is sufficient to cause a discharge which will essentially neutralize the applied signal resulting in zero wall charge and the cell in the OFF state.

FIG. 9 illustrates a prior art sustaining signal with the write pulse of FIG. 7 and the erase pulse of FIG. 8.

FIG. 10 shows a half select signal (that is the signal which appears on the other cells along the row and column of the selected cell) which could be derived from FIG. 7. The half-write pulse amplitude is no greater than the sustaining signal so that no undesired charges will occur. FIG. 11 illustrates a half select signal for FIG. 8. The half-erase amplitude is no greater than the sustaining signal so that no undesired discharge occurs. However, in this case all ON cells will have a discharge due to the half-erase pulse rather than the subsequent sustaining pulse.

We claim:

1. In a process for operating a multiple gaseous discharge display/memory panel wherein an addressing signal is applied to the panel,

the improvement wherein a portion of the addressing signal is of a magnitude to cause addressed sites in said panel to be in the saturation mode such that panel non-uniformities become substantially irrelevant and have no effect on panel behavior and such portion has a square waveform.

2. In a gas discharge panel apparatus comprising the combination of

a gaseous discharge panel, said panel having a pair of transverse conductor arrays at least one of which is non-conductively coupled to a gas discharge medium and having an internal memory constituted by stored charges, said transverse conductor arrays defining multiple discharge sites in said panel, and

circuit means supplying operating potentials to said panel, including sustaining potentials and discharge initiating pulse potentials which are of a magnitude such that all said discharge sites in said panel reach the same potential when fired and every discharge occurs in the saturation mode.

3. Apparatus as defined in claim 2 wherein said saturation mode is defined the section of the V_C versus V_W characteristic curve wherein the applied V_C voltage is at least equal to or greater than the saturation voltage (V_{SAT}) for the sustaining signal discharge plus the discharges associated with a discharge condition manipulating pulse voltage.

4. The invention defined in claim 3 wherein the discharge condition manipulating pulse voltage is the discharge initiating (write) pulse voltage.

5. The invention defined in claim 3 wherein the discharge condition manipulating pulse voltage is the discharge terminating (erase) pulse voltage.

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