Title: IMPEDANCE AND SWING CONTROL FOR VOLTAGE-MODE DRIVER

Abstract: A driver circuit includes a plurality of output circuits (208) coupled in parallel between a differential input (DrvIn, Inp) and a differential output (Txn, Txp) and having a first common node (V_s) and a second common node (V_db). Each of the plurality of output circuits includes a series combination of a pair of inverters (M_{p1}, M_{p2}) and a pair of resistors (R, R_0), coupled between the differential input and the differential output; first source terminals of the pair of inverters coupled to the first common node; and second source terminals of the pair of inverters coupled to the second common node. The driver circuit further includes a first voltage regulator (210) having an output coupled to the first common node of the plurality of output circuits; a second voltage regulator (210d) having an output coupled to the second common node of the plurality of circuits; and a current compensation circuit (206) coupled between the outputs of the first voltage regulator and the second voltage regulator.

FIG. 2
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IMPEDEANCE AND SWING CONTROL FOR VOLTAGE-MODE DRIVER

TECHNICAL FIELD

Examples of the present disclosure generally relate to electronic circuits and, in particular, to impedance and swing control for a voltage-mode driver.

BACKGROUND

In serial communication systems, a large percentage of the total power is consumed in the transmitter, which must provide for adequate signal swing on a low-impedance channel while maintaining an appropriate source termination. In addition, the transmitter often includes equalization to compensate for frequency-dependent loss in the channel. The driver circuit in the transmitter often consumes the majority of the power of the transmitter. Driver circuits can be implemented as current-mode drivers or voltage-mode drivers. Voltage-mode drivers are known to consume far less power in comparison to current-mode drivers. For example, a voltage-mode driver can consume four times less DC power than a current-mode driver to provide the same output swing.

A voltage-mode driver for a transmitter requires swing and impedance control such that the swing and common-mode/differential-mode return loss are within specifications. One technique for output signal swing control in a driver circuit is to use a single voltage regulator to generate a reference voltage that sets the voltage swing. However, with a single regulator, the common-mode will shift as the output swing of the driver circuit changes. Such a shift in the common-mode can cause the return loss to exceed specifications.

SUMMARY

Techniques for impedance and swing control for a voltage-mode driver are described. In an example, a driver circuit includes a plurality of output circuits coupled in parallel between a differential input and a differential output and having a first common node and a second common node. Each of the plurality of output circuits includes a series combination of a pair of inverters and a pair of resistors, coupled between the differential input and the differential output; first source terminals of the pair of inverters coupled to the first common node; and second source terminals of the pair of inverters coupled to the second
common node. The driver circuit further includes a first voltage regulator having an output coupled to the first common node of the plurality of output circuits; a second voltage regulator having an output coupled to the second common node of the plurality of circuits; and a current compensation circuit coupled between the outputs of the first voltage regulator and the second voltage regulator.

In another example, a driver circuit includes a plurality of output circuits coupled in parallel between a differential input and a differential output and having a first common node and a second common node. Each of the plurality of output circuits includes a series combination of a pair of enable circuits, a pair of inverters, and a pair of resistors, coupled between the differential input and the differential output; a first transistor coupled between the first common node and first source terminals of the pair of inverters; and a second transistor coupled between the second common node and second source terminals of the pair of inverters. The driver circuit further includes first and second replica output circuits coupled in series between the first and second common nodes; and a control circuit coupled to each of: respective gates of the first and second transistors in each of the plurality of output circuits; and the first and second replica output circuits.

In another example, a method of controlling a driver circuit in a transmitter includes receiving a plurality of outputs of an equalizer in the transmitter; coupling each of the plurality of outputs of the equalizer to at least one of a plurality of output circuits of the driver circuit; enabling first and second voltage regulators coupled to the plurality of output circuits; and enabling at least one of a plurality of current compensation circuits coupled between the first and second voltage regulators.

These and other aspects may be understood with reference to the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

So that the manner in which the above recited features can be understood in detail, a more particular description, briefly summarized above, may be had by reference to example implementations, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings
illustrate only typical example implementations and are therefore not to be considered limiting of its scope.

Fig. 1 is a block diagram depicting an example of a serial communication system.

Fig. 2 is a schematic diagram depicting an output driver according to an example.

Figs. 3A-3B depict a schematic diagram of an output driver according to another example.

Fig. 4 is a flow diagram depicting a method of controlling a driver circuit in a transmitter according to an example.

Fig. 5 is a block diagram depicting an example of a serial communication system.

Fig. 6 is a schematic diagram depicting an output driver according to an example.

Fig. 7 is a schematic diagram depicting a voltage regulator according to an example.

Fig. 8 is a schematic diagram depicting an error amplifier for the voltage regulator of Fig. 7 according to an example.

Fig. 9 is a block diagram depicting an example of a serial communication system.

Fig. 10 is a block diagram depicting a portion of a transmitter according to an example.

Fig. 11 is a schematic diagram depicting an output driver according to an example.

Fig. 12 is a schematic diagram depicting a current compensation circuit of the output driver of Fig. 11.

Fig. 13A is a table illustrating an example portion of a 1T main-cursor signal and its associated 2T odd signals.

Fig. 13B is a table illustrating an example portion of a 1T main-cursor signal and its associated 2T even signals.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements of one example may be beneficially incorporated in other examples.
DETAILED DESCRIPTION

Various features are described hereinafter with reference to the figures. It should be noted that the figures may or may not be drawn to scale and that the elements of similar structures or functions are represented by like reference numerals throughout the figures. It should be noted that the figures are only intended to facilitate the description of the features. They are not intended as an exhaustive description of the claimed invention or as a limitation on the scope of the claimed invention. In addition, an illustrated example need not have all the aspects or advantages shown. An aspect or an advantage described in conjunction with a particular example is not necessarily limited to that example and can be practiced in any other examples even if not so illustrated or if not so explicitly described.

Techniques for impedance and swing control for a voltage-mode driver are described. In an example, a driver circuit includes output circuits between a differential input and a differential output. The output circuits are coupled between first and second common nodes. Each output circuit includes a pair of inverters and a pair of resistors coupled between the differential input and output. First source terminals of the pair of inverters are coupled to the first common node and second source terminals of the pair of inverters are coupled to the second common node. First and second voltage regulators are coupled to the first and second common nodes. A current compensation circuit is coupled between outputs of the first and second voltage regulators. Zero or more of the current compensation circuits can be selectively enabled to draw dummy current from the voltage regulators to improve return loss, as discussed further below. Further, use of dual regulators allows for a fixed common mode in both low- and high-swing modes. These and further aspects are discussed below with respect to the drawings.

Fig. 1 is a block diagram depicting an example of a serial communication system 100. The serial communication system 100 comprises a transmitter 112 coupled to a receiver 126 over transmission medium 160. The transmitter 112 can be part of a serializer-deserializer (SERDES) 116. The receiver 126 can be part of a SERDES 122. The transmission medium 160 comprises an electrical path between the transmitter 112 and the receiver 126 and can include printed
circuit board (PCB) traces, vias, cables, connectors, decoupling capacitors, and the like. In examples, the transmission medium 160 includes a matched pair of transmission lines each having a characteristic impedance (Z0). The receiver of the SERDES 116, and the transmitter of the SERDES 122, are omitted for clarity. In some examples, the SERDES 116 can be disposed in an integrated circuit (IC) 110, and the SERDES 122 can be disposed in an IC 120.

In general, the transmitter 112 generates a serial data signal from a parallel data path (serialization). The serial data signal has a particular data rate (symbol rate). In some examples, data bytes from the parallel data path can be encoded prior to serialization using, for example, and 8B/10B encoder or the like. The transmitter 112 drives the serial data signal onto the transmission medium 160 using a digital modulation technique, such as binary non-return-to-zero (NRZ) pulse amplitude modulation (PAM). The transmission medium 160 propagates electrical signal(s) representing symbols of the serial data signal (e.g., logic “1” and logic “0”) towards the receiver 126.

In the example shown, the transmission medium 160 is a differential channel. Data on the differential channel is represented using two electrical signals (“true” and “complement” signals). A logic “0” is represented by driving the true signal to its lower voltage limit and driving the complement signal to its upper voltage limit. A logic “1” is represented by driving the true signal to its upper voltage limit and driving the complement signal to its lower voltage limit. Thus, the logic value of each transmitted symbol is based on the difference between the true and complement signals, and not based on the level of either signal individually. The peak-to-peak difference between the true signal and the complement signal is the voltage swing (also referred to as signal swing or swing).

The transmitter 112 includes a finite impulse response (FIR) filter 114, a pre-driver 115, an output driver 118, and control logic 150. The transmitter 112 is configured to equalize the serial data signal prior to transmission over the transmission medium 160. The FIR 114 can be used to mitigate inter-symbol interference (ISI) caused by the transmission medium 160. The transmission medium 160 degrades the signal quality of the transmitted signal. Channel insertion loss is the frequency-dependent degradation in signal power of the transmitted signal. When signals travel through a transmission line, the high
frequency components of the transmitted signal are attenuated more than the low frequency components. In general, channel insertion loss increases as frequency increases. Signal pulse energy in the transmitted signal can be spread from one symbol period to another during propagation on the transmission medium 160. The resulting distortion is known as ISI. In general, ISI becomes worse as the speed of the communication system increases.

The output of the FIR filter 114 is coupled to an input of the pre-driver 115. The output of the FIR filter 114 can include a plurality of signals, including a main-cursor signal, and one or more pre-cursor signals, one or more post-cursor signals, or a plurality of post-cursor and pre-cursor signals. For purposes of clarity by example, the present description assumes the FIR filter 114 outputs one main-cursor signal, one pre-cursor signal, and one post-cursor signal. The pre-driver 115 is configured to couple the output of the FIR filter 114 to the output driver 118. As discussed below, the output driver 118 is segmented and includes a plurality of output circuits coupled in parallel to the transmission medium 160. The pre-driver 115 couples each of the main-cursor, the pre-cursor, and the post-cursor signals to a selected percentage of the output circuits of the output driver 118. The percentages of output circuits driven by the main-cursor, pre-cursor, and post-cursor signals as selected by the pre-driver 115 is controlled by the control logic 150. The control logic 150 also controls aspects of the output driver 118, as discussed further below.

While the SERDES 116 and the SERDES 122 are shown, in other examples, each of the transmitter 112 and/or the receiver 126 can be a stand-alone circuit not being part of a larger transceiver circuit. In some examples, the transmitter 112 and the receiver 126 can be part of one or more integrated circuits (ICs), such as application specific integrated circuits (ASICs) or programmable ICs, such as field programmable gate arrays (FPGAs).

Fig. 2 is a schematic diagram depicting the output driver 118 according to an example. The output driver 118 includes output circuits 208, through 208, (where N is an integer greater than one), voltage regulators 210, and 210, and current compensation circuits 206, through 206, (where M is an integer greater than one). The output circuits 208, through 208, are collectively referred to as output circuits 208; the voltage regulators 210, and 210, are collectively referred

to as voltage regulators 210; and the current compensation circuits 206, through 206_1 are collectively referred to as current compensation circuits 206.

The output circuits 208 are coupled in parallel between a differential input 202 and a differential output (Txp, Txn). The differential input 202 includes N differential signals output by the pre-driver 115. Each differential signal includes a true signal, Inp, and a complement signal, Inn. Thus, the differential input 202 includes signals Inp_1 through Inp_4 and signals Inn_1 through Inn_4.

The output circuits 208 are coupled to common nodes Vrefp and Vrefn. Each of the output circuits 208 includes transistors M_{p1}, M_{p2}, M_{n1}, and M_{n2}. Each of the output circuits 208 also includes resistors R_p and R_n. The transistors M_{p1} and M_{n1} comprise p-channel field effect transistors (FETs), such as P-type metal-oxide semiconductor FETs (MOSFETs) (also referred to as PMOS transistors). The transistors M_{p2} and M_{n2} comprise n-channel FETs, such as N-type MOSFETs (also referred to as NMOS transistors). For purposes of clarity, only the output circuit 208_1 is shown in detail. However, each of the output circuits 208_2 through 208_n are configured identically with the output circuit 208_1.

Sources of the transistors M_{p1} and M_{n1} are coupled to the common node V_{nep}. Drains of the transistors M_{p1} and M_{n1} are coupled to drains of the transistors M_{p2} and M_{n2}, respectively. Sources of the transistors M_{p2} and M_{n2} are coupled to the common node V_{nen}. Gates of the transistors M_{p1} and M_{p2} are coupled together and are coupled to receive a signal Inp of one of the input differential signals. Gates of the transistors M_{n1} and M_{n2} are coupled together and are coupled to receive a signal Inn of one of the input differential signals. A first terminal of the resistor R_p is coupled to the drains of the transistors M_{p1} and M_{p2}, and a second terminal of the resistor R_p is coupled to the node Txp of the differential output. A first terminal of the resistor R_n is coupled to the drains of the transistors M_{n1} and M_{n2}, and a second terminal of the resistor R_n is coupled to the node Txn of the differential output. The transistors M_{p1} and M_{p2} form a first inverter (Mp), and the transistors M_{n1} and M_{n2} form a second inverter (Mn). A series combination of the pair of inverters (Mp, Mn) and the pair of resistors R_p and R_n is coupled between the differential input 202 and the differential output (Txp, Txn). The source terminals of the inverters are coupled between the nodes V_{nep} and V_{nen}. 
The voltage regulator 210 includes an operational amplifier \( A_{\text{vrefp}} \) and a transistor \( M_{\text{vrefp}} \). The transistor \( M_{\text{vrefp}} \) is an n-channel FET, such as an N-type MOSFET. A non-inverting input terminal of the operational amplifier \( A_{\text{vrefp}} \) is coupled to a first reference voltage source \( (V_{\text{ref1}}) \). An inverting input of the operational amplifier \( A_{\text{vrefp}} \) is coupled to the node \( V_{\text{vref}} \). A drain of the transistor \( M_{\text{vrefp}} \) is coupled to a supply voltage source \( (V_{\text{sup}}) \). A source of the transistor \( M_{\text{vrefp}} \) is coupled to the node \( V_{\text{vref}} \). A gate of the transistor \( M_{\text{vrefp}} \) is coupled to an output of the operational amplifier \( A_{\text{vrefp}} \).

The voltage regulator 210 includes an operational amplifier \( A_{\text{vrefn}} \) and a transistor \( M_{\text{vrefn}} \). The transistor \( M_{\text{vrefn}} \) is an n-channel FET, such as an N-type MOSFET. A non-inverting input terminal of the operational amplifier \( A_{\text{vrefn}} \) is coupled to a second reference voltage source \( (V_{\text{ref2}}) \). An inverting input of the operational amplifier \( A_{\text{vrefn}} \) is coupled to the node \( V_{\text{vref}} \). A source of the transistor \( M_{\text{vrefn}} \) is coupled to a ground voltage source. A drain of the transistor \( M_{\text{vrefn}} \) is coupled to the node \( V_{\text{vref}} \). A gate of the transistor \( M_{\text{vrefn}} \) is coupled to an output of the operational amplifier \( A_{\text{vrefn}} \).

The current compensation circuits 206 are coupled in parallel between the nodes \( V_{\text{vref}} \) and \( V_{\text{vref}} \). Each of the current compensation circuits 206 includes transistors \( M_1, M_2, \) and \( M_3 \). The transistor \( M_1 \) is a p-channel FET, such as a P-type MOSFET. The transistors \( M_2 \) and \( M_3 \) are n-channel FETs, such as an N-type MOSFET. For purposes of clarity, only the current compensation circuit 206 is shown in detail. However, each of the current compensation circuits 206 through 206 are configured identically with the current compensation circuit 206.

A source of the transistor \( M_1 \) is coupled to the node \( V_{\text{vref}} \). A drain of the transistor \( M_1 \) is coupled to a drain of the transistor \( M_2 \). A source of the transistor \( M_2 \) is coupled to a drain of the transistor \( M_3 \). A source of the transistor \( M_3 \) is coupled to the node \( V_{\text{vref}} \). A gate of the transistor \( M_2 \) in each of the current compensation circuits 206 is coupled to a bias voltage source \( V_{\text{bias}} \). A gate of the transistor \( M_3 \) is coupled to receive an enable signal of an enable input 204. The enable input 204 includes M enable signals \( EN_1 \) through \( EN_n \) coupled to the M current compensation circuits 206, respectively.
The output driver 118 further includes capacitors \( C_{vrefp} \) and \( C_{vrefn} \). The capacitor \( C_{vrefp} \) is coupled between the node \( V_{vrefp} \) and electrical ground. The capacitor \( C_{vrefn} \) is coupled between the node \( V_{vrefn} \) and electrical ground.

The differential output (Txp, Txn) is coupled to a pair of transmission lines 212, and 212, (collectively transmission lines 212). The transmission lines 212 drive a load resistance \( R_L \). The transmission lines 212 and the load resistance \( R_L \) are not part of the output driver 118. Rather, the transmission lines 212 are part of the transmission medium 160 and the load resistance \( R_L \) is part of the receiver 126.

In operation, each output circuit 208 includes a pair of inverters driven by complementary input (a differential signal of the differential input 202). Each differential signal of the differential input 202 can be one of a main-cursor signal, a post-cursor signal, or a pre-cursor signal. As discussed above, the pre-driver 115 controls the number of output circuits 208 receiving each of the main-cursor, post-cursor, and pre-cursor signals. For example, the output circuits can receive all main-cursor signals, some main-cursor signals and some pre-cursor signals, some main-cursor signals and some post-cursor signals, or some main-cursor signals, some post-cursor signals, and some pre-cursor signals. Mixing post/pre-cursor signals with the main-cursor signals is used to implement emphasis and de-emphasis equalization in the transmitter 112.

The voltage regulators 210 set the swing of the output driver 118. The differential peak-to-peak swing is \( V_{vrefp} - V_{vrefn} \). In an example, the voltage regulator 210, can include a switch 214 configured to short the drain of the transistor \( M_{vrefn} \) to electrical ground. This allows the voltage regulator 210, to be disabled in one mode (high-swing mode) and enabled in another mode (low swing mode). Zero or more of the current compensation circuits 206 are selectively enabled using the enable input 204 to draw dummy current from the voltage regulator 210 to improve return loss, as discussed further below. A control signal for the switch 214, and the enable input to the current compensation circuits 206, can be generated by the control logic 150.

With the dual regulators 210, and 210, in the output driver 118, the swing and common-mode can be set independently. For example, the common-mode can be fixed at 0.45 V. Table 1 below illustrates characteristics of the high-swing mode and the low-swing mode for both dual regulators and a single regulator.
As shown in Table 1, when both regulators 210₁ and 210₂ are enabled, the common-mode is the target 0.45 V for the low-swing mode (e.g., 0.6 V). If only the regulator 210₁ is enabled, the common mode is lower than the target: 0.45 V (e.g., 0.3 V) for the low-swing mode. Use of dual regulators allows for a fixed common mode in both low- and high-swing modes. The values in Table 1 are exemplary and the output driver 118 can be configured with other common-mode voltages, other high-swing voltages, and other low-swing voltages.

In the output driver 118, equalization can be implemented by driving a different number of the output circuits 208 with different main/pre/post cursor signals. With the dual-regulator approach, the swing is changed by adjusting the regulator voltage. Thus, equalization control is independent of the swing control. This allows for high FIR resolution even in low-swing mode.

For a voltage-mode driver, the current drawn by the output circuits 208 can be calculated using the following relationship: \( I_d = \frac{(\text{differential swing})}{(\text{external differential resistance} + \text{internal differential resistance})} \). In an example, each transmission line 212ᵣ and 212ᵦ has a characteristic impedance \( Z_0 \) of 50 ohms (external differential resistance = 100 ohms). Ideally, the output driver 118 provides a matching impedance of 50 ohms for each transmission line 212 (e.g., internal differential resistance = 100 ohms). If the desired swing is 0.9 V, then the current drawn by the output circuits 208 is approximately 4.5 mA. The actual current consumption may be higher to account for transient switching crowbar current.

For the above equation, it is noted that the current drawn by the output circuits 208 changes with the output swing. For lower swing, less current is drawn by the output circuits 208 from the voltage regulator 210₁. The output impedance of the voltage regulator 210₁ increases as less current is drawn from

<table>
<thead>
<tr>
<th>Regulator Mode</th>
<th>Swing</th>
<th>( V_{\text{refp}} )</th>
<th>( V_{\text{refn}} )</th>
<th>Common-mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual</td>
<td>0.6 V</td>
<td>0.75 V</td>
<td>0.15 V</td>
<td>0.45 V</td>
</tr>
<tr>
<td>Dual</td>
<td>0.9 V</td>
<td>0.9 V</td>
<td>0 V</td>
<td>0.45 V</td>
</tr>
<tr>
<td>Single</td>
<td>0.6 V</td>
<td>0.6 V</td>
<td>0 V</td>
<td>0.3 V</td>
</tr>
<tr>
<td>Single</td>
<td>0.9 V</td>
<td>0.9 V</td>
<td>0 V</td>
<td>0.45 V</td>
</tr>
</tbody>
</table>
the voltage regulator 210. Notably, the output impedance of the voltage regulator 210, is the output resistance of the transistor $M_{\text{rep}}$ (gm) divided by (1 + loop gain). When the voltage regulator 210, supplies low current, the operational amplifier $A_{\text{rep}}$ provides less loop gain, thereby increasing the output impedance of the voltage regulator 210. The output circuits 208 see an effective impedance of the capacitor $C_{\text{rep}}$ in parallel with the output impedance of the voltage regulator 210. For mid- to low-frequencies (e.g., 100 MHz), the impedance of the capacitor $C_{\text{rep}}$ is high and thus the output impedance of the voltage regulator 210, is not negligible. Thus, the decreased output impedance of the voltage regulator 210, due to low current draw by the output circuits 208 degrades the return loss of the output driver 118.

The current compensation circuits 206 are selectively enabled to mitigate the increase in return loss by drawing a constant dummy current in parallel with the output circuits 208. Thus, at higher swing settings, less or none of the current compensation circuits 206 can be enabled, as sufficient current is drawn from the voltage regulator 210. At lower swing settings, more of the current compensation circuits 206 can be enabled, which ensures that sufficient current is drawn from the voltage regulator 210, to maintain loop gain and low output impedance.

Figs. 3A-3B depict a schematic diagram of the output driver 118 according to another example. Fig. 3A shows a portion 118A of the output driver 118, and Fig. 3B shows a portion 118B of the output driver 118. Elements in Figs. 3A and 3B that are the same or similar to those of Fig. 2 are designated with identical reference numerals and are described above. The output driver 118 includes output circuits 308, through 308N (where N is an integer greater than one), the voltage regulators 210, 210Z, replica circuits 320, and 320Z, and a control circuit 350 comprising operational amplifiers Arepl1, Arepl2, and resistors $R_{\text{ref1}}$ through $R_{\text{ref11}}$. The output circuits 308, through 308N are collectively referred to as output circuits 308, and the replica circuits 320, and 320Z are collectively referred to as replica circuits 320. In some examples, the output driver shown in Figs. 3A and 3B can also include the current compensation circuits 206 described above. For purposes of clarity, the current compensation circuits 206 are omitted from Figs. 3A and 3B.
As shown in the portion 118A of the output driver 118 in Fig. 3A, the output circuits 308 are coupled in parallel between the differential input 202 and the differential output (Txp, Txn). The output circuits 308 are coupled to the common nodes V_{refp} and V_{refn}. Each of the output circuits 308 includes transistors M_{pdrv1}, M_{pdrv2}, M_{ndrv1}, M_{ndrv2}, M_{res1}, and M_{res2}. Each of the output circuits 208 also includes resistors R_{pdrv} and R_{ndrv}, and enable circuit U_e formed by NAND gate U_{p1} and U_{p2}, and an enable circuit U_n formed by U_{n1} and U_{n2}. The transistors M_{pdrv1} and M_{ndrv1} comprise p-channel FETs, such as P-type MOSFETs. The transistors M_{pdrv2} and M_{ndrv2} comprise n-channel FETs, such as N-type MOSFETs. Sources of the transistors M_{pdrv1} and M_{ndrv1} are coupled to a drain of the transistor M_{res1}. Drains of the transistors M_{pdrv1} and M_{pdrv2} are coupled to drains of the transistors M_{pdrv2} and M_{ndrv2}, respectively. Sources of the transistors M_{pdrv2} and M_{ndrv2} are coupled to a drain of the transistor M_{res2}.

Gates of the transistors M_{pdrv1} and M_{pdrv2} are coupled to outputs of the NAND gate U_{p1} and the NOR gate U_{p2}, respectively. In another example, the NAND gate U_{p1} and the NOR gate U_{p2} are replaced by a single inverter having an output coupled to the gates of the transistors M_{pdrv1} and M_{pdrv2}. First input terminals of the NAND gate U_{p1} and the NOR gate U_{p2} are coupled together, and are coupled to receive one end of a differential input signal (Inp). Second inputs of the NAND gate U_{p1} and the NOR gate U_{p2} are coupled to a true enable signal en and a complement enable signal enb. Gates of the transistors M_{ndrv1} and M_{ndrv2} are coupled to outputs of the NAND gate U_{n1} and the NOR gate U_{n2}, respectively. First input terminals of the NAND gate U_{n1} and the NOR gate U_{n2} are coupled together, and are coupled to receive the other end of the differential input signal (Inn). Second inputs of the NAND gate U_{n1} and the NOR gate U_{n2} are coupled to the true enable signal en and the complement enable signal enb. The true enable signal en and the complement enable signal enb are signals of a true enable input and a complement enable input, respectively. The true enable input includes N true enable signals en, through en_{n}, respectively coupled to the N output circuits 308, and the complement enable input includes N complement enable signals enb, through enb_{n}, respectively coupled to the N output circuits 308.

A source of the transistor M_{res1} is coupled to the common node V_{refp}. A source of the transistor M_{res2} is coupled to the common node V_{refn}. A gate of the
transistor $M_{res1}$ is coupled to an output of the operational amplifier $A_{rep1}$ (designated node $V_{g1}$). A gate of the transistor $M_{res2}$ is coupled to an output of the operational amplifier $A_{rep2}$ (designated node $V_{g2}$).

One terminal of the resistor $R_{pdrv}$ is coupled to the drains of the transistors $M_{pdrv1}$ and $M_{pdrv2}$, and another terminal of the resistor $R_{pdrv}$ is coupled to the node $T_{xp}$ of the differential output. One terminal of the resistor $R_{ndrv}$ is coupled to the drains of the transistors $M_{ndrv1}$ and $M_{ndrv2}$, and another terminal of the resistor $R_{ndrv}$ is coupled to the node $T_{xn}$ of the differential output. The transistors $M_{pdrv1}$ and $M_{pdrv2}$ form a first inverter ($M_{pdrv}$), and the transistors $M_{ndrv1}$ and $M_{ndrv2}$ form a second inverter ($M_{ndrv}$). A series combination of the enable circuits ($U_p, U_n$), the pair of inverters ($M_{pdrv}, M_{ndrv}$) and the pair of resistors $R_{pdrv}$ and $R_{ndrv}$ is coupled between the differential input 202 and the differential output ($T_{xp}, T_{xn}$). The source terminals of the inverters ($M_{pdrv}, M_{ndrv}$) are coupled between the nodes $V_{rep}$ and $V_{neh}$.

As shown in the portion 118B of the output driver 118, the replica output circuit 3201 includes transistors $M_{resrepl1}$ and $M_{repl1}$ and a resistor $R_{repl1}$. The transistors $M_{resrepl1}$ and $M_{repl1}$ are each a p-channel FET, such as a P-type MOSFET. A source of the transistor $M_{resrepl1}$ is coupled to the common node $V_{rep}$. A drain of the transistor $M_{repl1}$ is coupled to a source of the transistor $M_{repl1}$. A drain of the transistor $M_{repl1}$ is coupled to one terminal of the resistor $R_{repl1}$. Another terminal of the resistor $R_{repl1}$ is coupled to one terminal of a resistor $R_{repl_load}$ at a node $V_p$. A gate of the transistor $M_{resrepl1}$ is coupled to the output of the operational amplifier $A_{repl1}$. A gate of the transistor $M_{repl1}$ is coupled to a ground source.

The replica output circuit 3202 includes transistors $M_{resrepl2}$ and $M_{repl2}$ and a resistor $R_{repl2}$. The transistors $M_{resrepl2}$ and $M_{repl2}$ are each an n-channel FET, such as a N-type MOSFET. A source of the transistor $M_{resrepl2}$ is coupled to the common node $V_{neh}$. A drain of the transistor $M_{repl2}$ is coupled to a source of the transistor $M_{repl2}$. A drain of the transistor $M_{repl2}$ is coupled to one terminal of the resistor $R_{repl2}$. Another terminal of the resistor $R_{repl2}$ is coupled to a second terminal of a resistor $R_{repl_load}$ at a node $V_n$. A gate of the resistor $M_{resrepl2}$ is coupled to the output of the operational amplifier $A_{repl2}$. A gate of the transistor $M_{repl2}$ is coupled to a supply source ($V_{sup}$). The replica output circuit 3202 also...
includes a startup circuit S1. The startup circuit S1 comprises a switch coupled between the output of the operational amplifier A_{repl1} and the supply source \( V_{ref} \).

An inverting input of the operational amplifier A_{repl1} is coupled between the resistor R_{ref1} and the resistor R_{repl_load}. A non-inverting input of the operational amplifier A_{repl1} is coupled to a switched resistor network 322\_1. The switched resistor network 322\_1 comprises the resistors R_{ref1} through R_{ref5} and a switch Sw1. The resistors R_{ref1} through R_{ref5} are coupled in series between the node V_{refp} and the resistor R_{ref6}. The switched resistor network 322\_1 includes a plurality of taps (e.g., 5 taps in the example). The switch Sw1 is controllable to couple the non-inverting input of the operational amplifier A_{repl1} to one of the taps.

An inverting input of the operational amplifier A_{repl2} is coupled between the resistor R_{ref2} and the resistor R_{repl_load}. A non-inverting input of the operational amplifier A_{repl2} is coupled to a switched resistor network 322\_2. The switched resistor network 322\_2 comprises the resistors R_{ref2} through R_{ref11} and a switch Sw2. The resistors R_{ref7} through R_{ref11} are coupled in series between the node V_{refn} and the resistor R_{ref6}. The switched resistor network 322\_2 includes a plurality of taps (e.g., 5 taps in the example). The switch Sw2 is controllable to couple the non-inverting input of the operational amplifier A_{repl2} to one of the taps.

One example technique for impedance control is to provide a pair of programmable resistors stacked in series with all output slices of the driver array. The intent is to adjust the programmable resistors to compensate for variations in the output slices. However, as the programmable resistors are shared by all of the output slices, the differential impedance will deviate from the desired 100 ohms when some output slices are driven in the opposite direction. Another example technique for impedance control is to configure the output slices of the driver array to be selectively enabled/disabled. However, such a technique alone does not compensate for the difference in process variations of PMOS and NMOS transistors, e.g., when PMOS is at fast corner while NMOS is at slow corner and vice versa.

In an example, the output driver 118 provides for impedance control that addresses these problems. Turning on/off output circuits 308 is used to only compensate for on-chip resistor variations. To compensate for NMOS/PMOS...
variations, each output circuit 308 includes a pair of stacked programmable resistors (described below). The impedance of the stacked programmable resistors is controlled by two impedance control loops.

In operation, the output circuits 308 can be selectively enabled on or off through the enable input. The enable input can be provided by the control logic 150. If enabled, an output circuit 308 contributes to the differential output (Txp, Txn). If disabled, the output circuit 308 does not contribute to the differential output (Txp, Txn) (high impedance state). Turning output circuits 308 on/off provides for coarse impedance control to compensate for variation in the on-chip resistors $R_{pdrv}$ and $R_{ndrv}$. The transistors $M_{res1}$ and $M_{res2}$ are driven to operate in the triode region to provide programmable resistors controllable through $V_{gs1}$ and $V_{gs2}$, respectively. The transistors $M_{res1}$ and $M_{res2}$ are controlled to compensate for variation in the transistors $M_{pdrv1}$, $M_{pdrv2}$, $M_{ndrv1}$, and $M_{ndrv2}$. The resistance provided by the transistors $M_{res1}$ and $M_{res2}$ is controlled by adjusting their respective gate-to-source voltages using feedback control loops. A feedback control loop that controls the transistor $M_{res1}$ comprises the replica 320, and the operational amplifier $A_{repl1}$. A feedback control loop that controls the transistor $M_{res2}$ comprises the replica 320, and the operational amplifier $A_{repl2}$.

The operational amplifier $A_{repl1}$ adjusts the gate-to-source voltage of the transistor $M_{repl1}$ such that its impedance is set to a desired value. Notably, the transistor $M_{repl1}$ is fabricated to be a replica of the transistor $M_{res1}$. The transistor $M_{repl1}$ is fabricated to be a replica of a p-channel FET in the output circuits 308 (e.g., the characteristics for each of $M_{pdrv1}$, $M_{pdrv2}$, and $M_{repl1}$ are the same or substantially similar). The resistor $R_{repl\_load}$ is fabricated to be a replica of an on-chip resistor in the output circuits 308 (e.g., the characteristics for each of $R_{pdrv}$, $R_{ndrv}$, and $R_{repl\_load}$ are the same or substantially similar). Each output circuit 308 (if enabled) includes an internal impedance in series with one of the transmission lines 212 formed by a series combination of $M_{res1}$, one p-channel FET (i.e., $M_{pdrv1}$ or $M_{ndrv1}$), and one resistor ($R_{pdrv}$ or $R_{ndrv}$). The replica 3201 replicates this internal impedance. The desired voltage at node $V_p$ is selected at the non-inverting input of the operational amplifier $A_{repl1}$ and the operational amplifier $A_{repl1}$ drives the node $V_p$ to that voltage by controlling the impedance of the transistor $M_{repl1}$. The operational amplifier $A_{repl1}$ provides the same control voltage to the gate of the transistor $M_{res1}$ in each output circuit 308.
The operational amplifier \( A_{\text{rep2}} \) adjusts the gate-to-source voltage of the transistor \( M_{\text{res2}} \) such that its impedance is set to a desired value. The transistor \( M_{\text{res2}} \) is fabricated to be a replica of the transistor \( M_{\text{res}} \) and \( M_{\text{rep}} \) is fabricated to be a replica of an \( n \)-channel FET in the output circuits 308 (e.g., the characteristics for each of \( M_{\text{rev1}}, M_{\text{rev2}}, \) and \( M_{\text{rep}} \) are the same or substantially similar). The resistor \( R_{\text{rep2}} \) is fabricated to be a replica of an on-chip resistor in the output circuits 308 (e.g., the characteristics for each of \( R_{\text{drv}}, R_{\text{ndrv}}, \) and \( R_{\text{rep2}} \) are the same or substantially similar). Each output circuit 308 (if enabled) includes an internal impedance in series with one of the transmission lines 212 formed by a series combination of \( M_{\text{res}} \), one \( n \)-channel FET (i.e., \( M_{\text{rev1}} \) or \( M_{\text{rev2}} \)), and one resistor \( (R_{\text{drv}} \) or \( R_{\text{ndrv}} \)). The replica 320 replicates this internal impedance. The desired voltage at node \( V_n \) is selected at the non-inverting input of the operational amplifier \( A_{\text{rep2}} \) and the operational amplifier \( A_{\text{rep2}} \) drives the node \( V_n \) to that voltage by controlling the impedance of the transistor \( M_{\text{rep2}} \). The operational amplifier \( A_{\text{rep2}} \) provides the same control voltage to the gate of the transistor \( M_{\text{res}} \) in each output circuit 308.

By including transistors \( M_{\text{res1}} \) and \( M_{\text{res2}} \) in each output circuit 308, the differential output impedance of the output driver 118 can be maintained to match the transmission medium 160 even when the main and pre/post cursor signals switch in the opposite direction. Further, by provide two feedback control loops for separately controlling the resistance provided by the transistors \( M_{\text{res1}} \) and \( M_{\text{res2}} \), the output driver 118 can compensate for different NMOS and PMOS process variations.

As shown in Fig. 3B, the two feedback control loops are coupled together through the resistor \( R_{\text{rep2 load}} \) so that the current through the two loops can be reused. To ensure both loops start up properly, the startup circuit S1 can be incorporated into the replica circuit 3202. The startup circuit S1 can disable one loop initially so that the other loop starts up properly. Alternatively, rather than the startup circuit S1, a common-mode buffer can be used to decouple the two feedback control loops by driving the midpoint of the replica load to a common-mode voltage.

To illustrate the impedance control in more detail, consider an example where the output driver 118 includes \( N=75 \) to 85 output circuits 308. Typically, an on-chip resistor can change by \( \pm 10\% \) due to process variations. As
discussed above, variation in the on-chip resistors $R_{pdrv}$ and $R_{ndrv}$ is compensated for by adjusting the number of enabled output circuits 308 (e.g., between 75 and 85 as shown in the example of Table 2).

<table>
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<th>Table 2</th>
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<td>Transistor resistance</td>
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<td>On-chip resistance</td>
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As shown in Table 2, the total output impedance can be maintained at approximately 50 ohms for a given differential output (assuming a 50-ohm characteristic impedance of the transmission line) despite a ±10% variation in on-chip resistance by enabling more or less of the output circuits 308. To calibrate the number of output circuits 308 to be turned on/off, the resistance of the on-chip resistors $R_{pdrv}$ and $R_{ndrv}$ can be sensed with a constant current source (not shown). The control logic 150 can read the output of the sensing operation and then enable/disable the output circuits 308 based on values in a lookup table.

One difference between the replica output circuits 320 and the output circuits 308 is that the load of the replica circuits 320, $R_{repl\_load}$, is implemented with an on-chip resistor, while the actual load for the transmitter, $R_{load}$, is a constant termination at the receiver. To avoid using an external resistor or trimming the on-chip resistor $R_{repl\_load}$, the reference voltages used in the feedback control loops can be adjusted to compensate for variation in the on-chip replica resistor $R_{repl\_load}$. This is achieved by selecting a desired voltage at the non-inverting inputs to the operational amplifiers $Arepl1$ and $Arepl2$. Note that although each switched resistor network 322 is shown has having five taps for
providing five reference voltages, the switched resistor networks 322 can have more or less than five taps.

Fig. 4 is a flow diagram depicting a method 400 of controlling a driver circuit in a transmitter according to an example. The method 400 can be performed to control the output driver 118 of the transmitter 112. The method 400 begins at step 402, where the pre-driver 115 receives the outputs of an equalizer in the transmitter 112 (e.g., FIR filter 114). At step 404, the pre-driver 115 couples each equalizer output to at least one of a plurality of output circuits in the output driver 118 (e.g., output circuits 208 or 308). Step 404 implements equalizer control independently from swing control and impedance control. The main-, pre-, and post-cursor signals can be coupled to any number of output circuits in the output driver 118 to achieve the desired emphasis or de-emphasis.

At step 406, the control logic 150 enables first and second voltage regulators 210 coupled to the output circuits in the output driver 118 to establish a desired swing. The voltage output from the dual voltage regulators 210 can be set to generate a desired peak-to-peak voltage swing at the output of the output driver 118. In some cases, at step 410, the control logic 150 can optionally enable one or more current compensation circuits 206 to equalize current drawn from the current-supplying voltage regulator (e.g., the voltage regulator 210,). Step 406 implements output swing control independent of equalizer control and impedance control.

At step 408, the impedance of the output driver is controlled. For example, at step 412, the control logic 150 disables one or more of the output circuits in the output driver 118 to compensate for on-chip resistor variation. This provides for a coarse impedance control. At step 414, feedback control loops in the output driver adjust the gate-to-source voltage of stacked transistors M\textsubscript{res1} and M\textsubscript{res2} in each output circuit based on feedback from replica circuits 320 to adjust for NMOS/PMOS transistor variation and provide for fine impedance control. As discussed above, the feedback control loops can independently adjust the impedance of the stacked transistors M\textsubscript{res1} and M\textsubscript{res2}, to independently compensate for NMOS and PMOS variations.
FAST TRANSIENT LOW DROP-OUT VOLTAGE REGULATOR FOR A VOLTAGE-MODE DRIVER

In serial communication systems, a large percentage of the total power is consumed in the transmitter, which must provide for adequate signal swing on a low-impedance channel while maintaining an appropriate source termination. In addition, the transmitter often includes equalization to compensate for frequency-dependent loss in the channel. The driver circuit in the transmitter often consumes the majority of the power of the transmitter. Driver circuits can be implemented as current-mode drivers or voltage-mode drivers. Voltage-mode drivers are known to consume far less power in comparison to current-mode drivers. For example, a voltage-mode driver can consume four times less DC power than a current-mode driver to provide the same output swing.

A voltage-mode driver for a transmitter requires swing and impedance control such that the swing and common-mode/differential-mode return loss are within specifications. One technique for output signal swing control in a driver circuit is to use a single voltage regulator to generate a reference voltage that sets the voltage swing. However, with a single regulator, the common-mode will shift as the output swing of the driver circuit changes. Such a shift in the common-mode can cause the return loss to exceed specifications. Further, conventional low drop-out (LDO) voltage regulators suffer from large ripple, which results in large jitter. Deterministic jitter is an important specification of transmitter driver. A voltage regulator in the transmitter driver should suppress supply ripple as much as possible to have low jitter.

Techniques for providing a fast transient low drop-out (LDO) voltage regulator for a voltage-mode driver are described. In an example, a voltage regulator includes an output transistor that includes a source coupled to a first voltage supply node and a drain coupled to an output node. The voltage regulator further includes a first transistor that includes a source coupled to the output node, and a second transistor that includes a source coupled to a gate of the output transistor and a drain coupled to a second voltage supply node. The voltage regulator further includes a resistor coupled between the second voltage supply node and a first node that includes the drain of the first transistor and a gate of the second transistor. The voltage regulator further includes an error amplifier that includes a first input coupled to a reference voltage node, a second
input coupled to the output node, and another output coupled to a gate of the first transistor.

In another example, a driver circuit includes a voltage-mode output driver and a voltage regulator coupled to the voltage-mode output driver. The voltage regulator provides an output voltage to the voltage-mode output driver. The voltage regulator includes an output transistor that includes a source coupled to a first voltage supply node and a drain coupled to an output node, which supplies the output voltage. The voltage regulator further includes a first transistor that includes a source coupled to the output node, and a second transistor that includes a source coupled to a gate of the output transistor and a drain coupled to a second voltage supply node. The voltage regulator further includes a resistor coupled between the second voltage supply node and a first node that includes the drain of the first transistor and a gate of the second transistor. The voltage regulator further includes an error amplifier that includes a first input coupled to a reference voltage node, a second input coupled to the output node, and an output coupled to a gate of the first transistor.

In another example, a voltage regulator includes an output transistor that includes a source coupled to a first voltage supply node and a drain coupled to an output node that supplies a regulated output voltage. A DC regulation loop includes a first source follower configured to control the regulated output voltage and an error amplifier configured to control the first source follower. A fast transient loop that includes a second source follower, a resistor, and the first source follower, the second source follower configured to control the output transistor. A voltage between the resistor and the first source follower controls the second source follower.

Techniques for providing a fast transient low drop-out (LDO) voltage regulator for a voltage-mode driver are described. In an example, a voltage regulator includes an output transistor having a source coupled to a first voltage supply node and a drain coupled to an output node. A first transistor includes a source coupled to the output node. A second transistor includes a source coupled to a gate of the output transistor and a drain coupled to a second voltage supply node. A resistor is coupled between the second voltage supply node and a first node that includes the drain of the first transistor and a gate of the second transistor. An error amplifier includes a first input coupled to a
reference voltage node, a second input coupled to the output node, and an output coupled to a gate of the first transistor.

The voltage regulator regulates output voltage by controlling the voltage at the output node using a DC regulation loop and a fast transient loop. The DC regulation loop includes a source follower, formed by the first transistor and the output transistor, and the error amplifier. The fast transient loop includes another source follower, formed by the second transistor and a current source, which controls the gate voltage of the output transistor. The second transistor acts as a level-shifter and creates a low impedance pole at the gate of the output transistor. The dominant pole is at the output node and two non-dominant poles are in the gigahertz (GHz) range. This allows the voltage regulator to achieve high bandwidth. This significantly mitigates output ripple at the output node. Rather than using two separate loops, the DC regulation loop and the fast transient loop are coupled in the voltage regulator (through the first source follower). These and further aspects are described below with respect to the drawings.

Fig. 5 is a block diagram depicting an example of a serial communication system 500. The serial communication system 500 comprises the transmitter 112 coupled to the receiver 126 over the transmission medium 160, as shown in Fig. 1 and described above. The output driver 118 couples a differential signal to the transmission medium 160. In the present example, the output driver 118 includes a pair of voltage regulators 162 that supply upper and lower voltages to circuits of the output driver 118. An example voltage regulator is shown in Fig. 7 and described below.

Fig. 6 is a schematic diagram depicting the output driver 118 according to an example. Elements of Fig. 6 that are the same or similar to those of Fig. 2 are designated with identical reference numerals. The output driver 118 includes the output circuits 208, through 208n, (where N is an integer greater than one) and voltage regulators 1621 and 1622. The output circuits 208, through 208n, are collectively referred to as output circuits 208. The voltage regulators 1621 and 1622, are collectively referred to as voltage regulators 162. The voltage regulator 1621, is coupled to the common node Vrefp. The voltage regulator 1622 controls the voltage at the node Vrefp and supplies current to the output circuits 208. The voltage regulator 1622 is coupled to the common node Vrefp. The voltage
regulator 162\textsubscript{2} controls the voltage at the node V\textsubscript{refn} and sinks current from the output circuits 208.

In operation, each output circuit 208 includes a pair of inverters driven by complementary input (a differential signal of the differential input 202). Each differential signal of the differential input 202 can be one of a main-cursor signal, a post-cursor signal, or a pre-cursor signal. As discussed above, the pre-driver 115 controls the number of output circuits 208 receiving each of the main-cursor, post-cursor, and pre-cursor signals. For example, the output circuits can receive all main-cursor signals, some main-cursor signals and some pre-cursor signals, some main-cursor signals and some post-cursor signals, or some main-cursor signals, some post-cursor signals, and some pre-cursor signals. Mixing post/pre-cursor signals with the main-cursor signals is used to implement emphasis and de-emphasis equalization in the transmitter 112. In the output driver 118, equalization can be implemented by driving a different number of the output circuits 208 with different main/pre/post cursor signals.

For a voltage-mode driver, the current drawn by the output circuits 208 can be calculated using the following relationship: \( I_d = \frac{V_{\text{swing}}}{(\text{external differential resistance} + \text{internal differential resistance})} \) (e.g., each transmission line 212\textsubscript{p} and 212\textsubscript{n} has a characteristic impedance \( Z_0 \) of 50 ohms (external differential resistance = 100 ohms). Ideally, the output driver 118 provides a matching impedance of 50 ohms for each transmission line 212 (e.g., internal differential resistance = 100 ohms). If the desired swing is 0.75 V, then the current drawn by the output circuits 208 is approximately 3.75 mA. The actual current consumption may be higher to account for transient switching current. For the above equation, it is noted that the current drawn by the output circuits 208 changes with the output swing. For lower swing, less current is drawn by the output circuits 208 from the voltage regulator 1621.

The voltage regulators 162 set the swing of the output driver 118. The differential peak-to-peak swing is \( V_{\text{swing}} = V_{\text{refn}} \). For example, the voltage regulator 162\textsubscript{1} can control the voltage at the common node \( V_{\text{refp}} \) to be 0.75 V, and the voltage regulator 162\textsubscript{2} can control the voltage at the common node \( V_{\text{refn}} \) to be 0.15 V. In such an example, the output swing is 0.6 V. Each of the voltage regulators 162 can be a linear voltage regulator, such as a low drop-out (LDO) voltage regulator.
Jitter is a critical specification for the output driver 118. As both supply voltages provided to the output driver 118 (e.g., voltages at common nodes \( V_{\text{ref}} \) and \( V_{\text{in}} \), it is important to have the ripple be as small as possible on each supply voltage to reduce jitter. In order to achieve small ripple, the voltage regulators 162 should be fast transient regulators.

One example LDO voltage regulator applies input voltage to a pass element, which is an n-channel or p-channel FET. The pass element operates in the linear region and drops the input voltage to the desired output voltage. A voltage divider divides the output voltage and an error amplifier senses the divided output voltage. The error amplifier compares the sensed voltage to a reference voltage and drives the gate of the pass element to the appropriate operating point to control the output voltage. Such an LDO regulator has a small bandwidth. The gate node of the pass element is a high-impedance node and is designed as the dominant pole. In order to have sufficient direct current (DC) gain, the impedance at the gate node is high. The dominant pole can be in the range of kilohertz. The non-dominant pole is formed at the output node. For small output ripple, a large decoupling capacitor can be used. Thus, a considerable current is required in order to move the non-dominant pole to higher frequencies and improve the circuit bandwidth. The voltage ripple is proportional to the load current divided by a product of the output capacitance and the bandwidth. The output ripple is significantly high for large changes in the load current. Increasing the output capacitance can reduce ripple, but it also reduces bandwidth. As discussed further below, the voltage regulator shown in Fig. 3 is based on a flipped voltage follower (FVF), which solves this problem with comparatively less current.

Another example LDO voltage regulator uses an FVF architecture. An FVF LDO regulator includes replica biasing. A transistor is biased using a replica circuit including a current mirror and an error amplifier to generate the reference voltage. Such an LDO regulator includes two decoupled loops, one to control the DC output and another to reduce transients. One issue with such an LDO regulator is the DC accuracy. Such an LDO regulator is less immune to process and temperature (PVT) variations. Furthermore, the DC gain of the fast transient loop is low, which results in poor load regulation. Further, the dominant pole in the fast transient loop is formed at the output. Under large load
conditions, stability of the system is a concern as the dominant pole moves to higher frequencies (e.g., a few tens of MHz, especially in technology nodes less than 28 nm).

Fig. 7 is a schematic diagram of a voltage regulator 700 according to an example. The voltage regulator 700 is an LDO voltage regulator that can be used as the voltage regulator 162 described above. Those skilled in the art will appreciate that the voltage regulator 700 can be used in a myriad of other applications that make use of a low drop-out, linear voltage regulator.

The voltage regulator 700 includes transistors \( M_{\text{Power}} \), \( M_{\text{SF1}} \), and \( M_{\text{SF2}} \).

The voltage regulator 700 further includes a resistor \( R_1 \), a current source \( I_{\text{bias}} \), and an error amplifier 702. The transistors \( M_{\text{Power}} \), \( M_{\text{SF1}} \), and \( M_{\text{SF2}} \) are n-channel FETs, such as NMOS transistors. The transistor \( M_{\text{Power}} \) includes a source coupled to a first voltage node (designated as electrical ground in the example), a base coupled to a node \( V_s \), and a drain coupled to a node \( V_{\text{out}} \). The transistor \( M_{\text{SF1}} \) includes a source coupled to the node \( V_{\text{out}} \), a base coupled to an output of the error amplifier 702, and a drain coupled to a node \( V_s \). The resistor \( R_1 \) is coupled between a second supply node (designated \( V_{\text{sup}} \) in the example) and the node \( V_s \). The transistor \( M_{\text{SF2}} \) includes a source coupled to the node \( V_s \), a drain coupled to the supply node \( V_{\text{sup}} \), and a base coupled to the node \( V_s \). The current source \( I_{\text{bias}} \) is coupled between the node \( V_s \) and the ground node. In the example, the current source \( I_{\text{bias}} \) sources current away from the node \( V_s \). The error amplifier 702 includes supply inputs coupled to the node \( V_{\text{sup}} \), and the ground node, respectively. The error amplifier 702 further includes a non-inverting input coupled to a node \( V_{\text{ref}} \) and an inverting input coupled to the node \( V_{\text{out}} \). An example of the error amplifier 702 is shown in Fig. 8 and described below. A capacitor \( C_{\text{out}} \) is coupled between the node \( V_{\text{out}} \) and the ground node.

In operation, the voltage regulator 700 generates a regulated output voltage at the node \( V_{\text{out}} \) from a supply voltage between the node \( V_{\text{sup}} \) and the ground node. The regulated output voltage appears across the drain and source of the transistor \( M_{\text{Power}} \) (e.g., the regulated output voltage is \( V_{\text{DS}} \) of the transistor \( M_{\text{Power}} \)). The transistor \( M_{\text{Power}} \) is also referred to herein as an output transistor. A load \( R_{\text{Load}} \) can be coupled between a supply voltage (e.g., \( V_{\text{sup}} \) in Fig. 6) and the node \( V_{\text{out}} \) of the voltage regulator 700. Thus, in an example, the voltage at \( V_{\text{out}} \) is the voltage \( V_{\text{ref}} \) shown in Fig. 6. The load \( R_{\text{Load}} \) supplies a DC current, \( I_{\text{Load}} \),
which is sinked by the transistor $M_{\text{Power}}$. The transistor $M_{\text{Power}}$ conducts a current $I_{DS}$ that includes the load current $I_{\text{Load}}$ and a drain-to-source current of the transistor $M_{SF1}$. The transistor $M_{\text{Power}}$ is a power MOSFET or the like sized to accommodate a desired range of load current supplied by the load $R_{\text{Load}}$.

The voltage regulator 700 regulates the output voltage by controlling the voltage at the node $V_{\text{out}}$ using a DC regulation loop and a fast transient loop. The DC regulation loop includes a first source follower (SF1) that controls the output voltage at the node $V_{\text{out}}$ and the error amplifier 702, which controls the first source follower. The first source follower is formed by the transistor $M_{SF1}$ and the transistor $M_{\text{Power}}$. The input of the first source follower is a voltage $Vg$ and the output by the error amplifier 702. An output of the first source follower is the node $V_{\text{out}}$. A common input to the first source follower is the node $V_i$. The DC regulation loop includes the voltage $V_s$ applied to the gate of the transistor $M_{SF1}$, which controls the voltage at the node $V_{\text{out}}$, which is fed back to the non-inverting input of the error amplifier 702, which generates the voltage $Vg$. The error amplifier 702 sets the operating point of the transistor $M_{SF1}$ so that the difference between the voltage $V_{\text{ref}}$ and $V_{\text{out}}$ is substantially zero.

The fast transient loop includes a second source follower (SF2), the resistor $R_1$, and the first source follower (SF1). The second source follower (SF2) includes the transistor $M_{SF2}$ and the current source $I_{b\text{ext}}$. The input of the second source follower is the voltage at the node $V_i$. An output of the first source follower is the node $V_s$. A common input to the first source follower is the supply node $V_{\text{esp}}$. The drain-to-source current of the transistor $M_{SF2}$ is set to the current $I_{b\text{ext}}$. The second source follower controls the transistor $M_{\text{Power}}$ by controlling the voltage at the node $V_s$. The voltage between the resistor $R_1$ and the first source follower (SF1) (the node $V_i$) controls the second source follower (e.g., the gate voltage of the transistor MSF2). The transistor MSF2 acts as a level shifter and creates a low impedance node at the gate of the transistor $M_{\text{Power}}$. The dominant pole is at the output node $V_{\text{out}}$ and two non-dominant poles are in the gigahertz (GHz) range. This allows the voltage regulator 700 to achieve high bandwidth. This significantly mitigates output ripple at the node $V_{\text{out}}$. Rather than using two separate loops, the DC regulation loop and the fast transient loop are coupled in the voltage regulator 700 (through the first source follower SF1).
Compared to the example LDO regulators described above, the DC accuracy of the voltage regulator 700 is higher. When the load current ILoad increases, the gate voltage of the transistor $M_{\text{Power}}$ increases through action of the fast transient loop to sink the additional load current. Conversely, when the load current ILoad decreases, the gate voltage of the transistor $M_{\text{Power}}$ decreases through active of the fast transient loop to respond to the change in IDS of the transistor $M_{\text{Power}}$. The voltage $V_g$ at the gate of the transistor $M_{\text{g}}$ is almost constant, which results in less variations for the DC gain for different load currents and improves load regulation.

In an embodiment, the error amplifier 700 includes a folded cascoded amplifier. An example of the error amplifier 700 is shown in Fig. 8. The output voltage at the node $V_{\text{out}}$ is directly fed back to the error amplifier 700, rather than a divided output voltage. When the error amplifier 700 is based on a folded cascaded amplifier, the DC gain is high, which provides immunity to PVT variations. Although the DC gain of the fast transient loop is low, the high DC gain of the error amplifier 700 compensates, resulting in small variations of the voltage $V_g$ at the gate of the transistor $M_{\text{g}}$. Thus, the output voltage at the node $V_{\text{out}}$ is substantially constant and results in good load regulation.

The resistor $R_1$ is used in the fast transient loop to generate the voltage $V_i$ rather than use of a current mirror. Since the voltage regulator 700 is not based on replica biasing, using the resistor $R_1$ instead of a current mirror in the fast transient loop has minimal impact on the DC accuracy. The resistor $R_1$ also allows the non-dominant pole to be pushed to higher frequencies without a significant increase in the quiescent current.

Fig. 8 is a schematic diagram depicting the error amplifier 702 according to an example. The error amplifier 702 includes a source-coupled transistor pair (M1, M2), a current source $I_{\text{bias2}}$ and a cascode branch circuit 802. The cascode branch circuit 802 (also referred to as an output circuit) includes a base-coupled transistor pair (M3, M4), a base-coupled transistor pair (M_{\text{cascode1}}, M_{\text{cascode2}}), a base-coupled transistor pair (M_{\text{cascode3}}, M_{\text{cascode4}}), and a base-coupled transistor pair (M5, M6). The transistor M1 includes a source coupled to the source of the transistor M2. The transistor M3 includes a base coupled to a node $V_{\text{ref}}$ and a drain coupled to a drain of the transistor M4. The transistor M2 includes a base coupled to the node $V_{\text{out}}$ and a drain coupled to a drain of the transistor M3. The
current \( i_{\text{bias2}} \) is coupled between the supply node \( V_{\text{sup}} \) and the source node of the source-coupled transistor pair \((M_1, M_2)\). The transistors \( M_1 \) and \( M_2 \) are p-channel FETs, such as PMOS transistors.

The transistor \( M_3 \) includes a source coupled to the ground node, a base coupled to a node \( V_{\text{bias3}} \), and a drain coupled to a source of the transistor \( M_{\text{cascode1}} \). The transistor \( M_4 \) includes a source coupled to the ground node, a base coupled to a node \( V_{\text{bias4}} \), and a drain coupled to a source of the transistor \( M_{\text{cascode2}} \). The transistor \( M_{\text{cascode1}} \) includes a base coupled to a node \( V_{\text{bias2}} \) and a drain coupled to the drain of the transistor \( M_{\text{cascode3}} \). The transistor \( M_{\text{cascode2}} \) includes a base coupled to a node \( V_{\text{bias2}} \) and a drain coupled to the drain of the transistor \( M_{\text{cascode4}} \). The transistor \( M_{\text{cascode3}} \) includes a base coupled to the node \( V_{\text{bias1}} \) and a source coupled to a drain of the transistor \( M_5 \). The transistor \( M_{\text{cascode4}} \) includes a base coupled to the node \( V_{\text{bias1}} \) and a source coupled to a drain of the transistor \( M_5 \). The transistor \( M_5 \) includes a source coupled to a node including the base of the transistor \( M_6 \) and another node that includes the drains of the transistors \( M_{\text{cascode1}} \) and \( M_{\text{cascode3}} \). The transistor \( M_6 \) includes a source coupled to the supply node \( V_{\text{sup}} \). The transistor \( M_7 \) includes a source coupled to the supply node \( V_{\text{sup}} \). The transistors \( M_{\text{cascode1}} \), \( M_{\text{cascode2}} \), \( M_5 \), and \( M_6 \) are n-channel FETs, such as NMOS transistors. The transistors \( M_{\text{cascode3}} \), \( M_{\text{cascode4}} \), \( M_5 \), and \( M_6 \) are p-channel FETs, such as PMOS transistors. A node including the drains of the transistors \( M_{\text{cascode1}} \) and \( M_{\text{cascode2}} \) provides the voltage \( V_i \) coupled to the input of the source follower \( \text{SF1} \) shown in Fig. 7 (e.g., the base of the transistor \( M_{\text{SF1}} \)).

In operation, the transistor pair \((M_3, M_4)\) are load transistors for the source-coupled pair \((M_1, M_2)\). The transistors \( M_5 \) and \( M_6 \) are gate-biased into saturation by a bias source (not shown) coupled to the node \( V_{\text{bias3}} \). Likewise, the cascode pair \((M_{\text{cascode1}}, M_{\text{cascode2}})\) and the cascode pair \((M_{\text{cascode3}}, M_{\text{cascode4}})\) are gate-biased into saturation by bias sources (not shown) coupled to the nodes \( V_{\text{bias2}} \) and \( V_{\text{bias1}} \), respectively. The transistors \( M_5 \) and \( M_{\text{cascode3}} \) form a cascode current mirror whose current is reflected to the transistor \( M_6 \). The transistors \((M_1, M_2)\) together with the current source \( i_{\text{bias2}} \) steer a tail current between the two sides of the source-coupled pair to the load transistors \((M_3, M_4)\) in response to a differential input voltage \( (V_{\text{ref}} - V_{\text{out}}) \). When the voltage \( V_{\text{ref}} \) is equal to the...
voltage \( V_{out} \), an equal current \( I_{bias2/2} \) flows to each of the load transistors \( M_3 \) and \( M_4 \).

The load transistors \( M_3 \) and \( M_4 \) also receive a fixed current produced by the current mirror \( (M_5, M_{\text{cascode3}}) \) and associated transistors \( M_6, M_{\text{cascode1}} \).

When the input voltages are equal, the drain-to-source current through load transistors \( M_3 \) and \( M_4 \) is equal to one half of \( I_{bias2} \) plus the current of the current mirror and cascoded transistors. An imbalance in the input voltage \( (V_{ref} - V_{out}) \) causes an imbalance in current between the branches of the cascode branch circuit 802, which in turn shifts the voltage \( V_g \) in same direction as the change in the input voltage. Thus, if \( V_{out} > V_{ref} \), then \( V_g \) is driven lower, which in turn causes the source follower SF1 to drive the output node \( V_{out} \) lower. If \( V_{out} < V_{ref} \), then \( V_g \) is driven higher, which in turn cases the source follower SF1 to drive the output node \( V_{out} \) higher. The high gain of the error amplifier 702 ensures that, in steady state, \( V_g \) includes only small variations from a constant value.

DATA DEPENDENT CURRENT COMPENSATION IN A VOLTAGE-MODE DRIVER

In serial communication systems, a large percentage of the total power is consumed in the transmitter, which must provide for adequate signal swing on a low-impedance channel while maintaining an appropriate source termination. In addition, the transmitter often includes equalization to compensate for frequency-dependent loss in the channel. The driver circuit in the transmitter often consumes the majority of the power of the transmitter. Driver circuits can be implemented as current-mode drivers or voltage-mode drivers. Voltage-mode drivers are known to consume far less power in comparison to current-mode drivers. For example, a voltage-mode driver can consume four times less DC power than a current-mode driver to provide the same output swing.

A transmitter can include a plurality of voltage-mode drivers coupled to a common output node. A voltage regulator provides a regulated supply voltage to the voltage-mode drivers. The voltage-mode drivers are driven by different input signals to implement equalization. Thus, the voltage-mode drivers draw a data-dependent current from the voltage regulator. Large swings in the average supply current can degrade the deterministic jitter of the transmitter.
Techniques for data-dependent current compensation in a voltage-mode driver are described. In an example, an output driver includes a plurality of output circuits coupled in parallel between a first voltage supply node and a second voltage supply node. Each of the plurality of output circuits includes a differential input that is coupled to receive a logic signal of a plurality of logic signals and a differential output that is coupled to a common output node. The output driver further includes at least one voltage regulator coupled to a respective at least one of the first voltage supply node and the second voltage supply node. The output driver further includes a current compensation circuit.

The current compensation circuit includes a switch coupled in series with a current source, where the series combination of the switch and the current source is coupled between the first voltage supply node and the second voltage supply node. The current compensation circuit further includes an event detector coupled to the switch to supply an enable signal, where the event detector is configured to control state of the enable signal based on presence of a pattern in the plurality of logic signals.

In another example, a transmitter includes a finite impulse response (FIR) filter configured to supply a plurality of logic signals in response to input data. The transmitter further includes a pre-driver configured to couple the plurality of logic signals to an output driver. The output driver includes a plurality of output circuits coupled in parallel between a first voltage supply node and a second voltage supply node, where each of the plurality of output circuits including a differential input that is coupled to receive a logic signal of the plurality of logic signals and a differential output that is coupled to a common output node. The output driver further includes at least one voltage regulator coupled to a respective at least one of the first voltage supply node and the second voltage supply node. The output driver further includes a current compensation circuit. The current compensation circuit includes a switch coupled in series with a current source, where the series combination of the switch and the current source is coupled between the first voltage supply node and the second voltage supply node. The current compensation circuit further includes an event detector coupled to the switch to supply an enable signal, where the event detector configured to control state of the enable signal based on presence of a pattern in the plurality of logic signals.
In another example, a method of controlling an output driver in a transmitter includes receiving a plurality of logic signals from an equalizer in the transmitter, coupling each of the plurality of logic signals to at least one of a plurality of output circuits of the output driver, the plurality of output circuits coupled between a first voltage supply node and a second voltage supply node, at least one of the first voltage supply node and the second voltage supply node coupled to a voltage regulator, detecting a pattern in the plurality of logic signals, and enabling at least one of a plurality of current sources coupled between the first voltage supply node and the second voltage supply node.

Fig. 9 is a block diagram depicting an example of a serial communication system 900. The serial communication system 900 comprises the transmitter 912 coupled to the receiver 926 over the transmission medium 960. The transmitter 912 can be part of a serializer-deserializer (SERDES) 916. The receiver 926 can be part of a SERDES 922. The transmission medium 960 comprises an electrical path between the transmitter 912 and the receiver 926 and can include printed circuit board (PCB) traces, vias, cables, connectors, decoupling capacitors, and the like. In examples, the transmission medium 960 includes a matched pair of transmission lines each having a characteristic impedance (Z0). The receiver of the SERDES 916, and the transmitter of the SERDES 922, are omitted for clarity. In some examples, the SERDES 916 can be disposed in an integrated circuit (IC) 910, and the SERDES 922 can be disposed in an IC 920.

In operation, the SERDES 916 serializes an input digital signal. As used herein, a digital signal is a sequence of k-bit codes, where k is a positive integer. A k-bit code may be referred to as a word (or data word). In specific examples, an 8-bit code may be referred to as a byte (or data byte). The number of codes per second is the data rate (also referred to as sample rate). A digital signal can also be conceptually viewed as a discrete-time, discrete-amplitude signal, where the amplitude of the signal at each discrete time is selected from 2k discrete values. As used herein a logic signal is a sequence of 1-bit codes. A logic signal can be viewed as a discrete-time, discrete amplitude signal, where the amplitude of the signal at each discrete time is selected from two states referred to as logic high (or logic “1”) and logic low (or logic “0”). The input signal is serialized by decomposing each k-bit code at a discrete time into a sequence of j
bits over \( j \) discrete times (referred to as serial data), where \( j \) is a positive integer greater than or equal to \( k \). In some examples, data words provided by the input digital signal can be encoded prior to serialization using, for example, an 8B/10B encoder or any other line-coding scheme (e.g., \( j > k \)).

The SERDES 916 generates one or more logic signals to provide the serial data to the transmitter 912. The transmitter 912 drives the serial data onto the transmission medium 960 using a digital baseband modulation technique. In general, the serial data is divided into symbols. The transmitter 912 converts each symbol into an analog voltage mapped to the symbol. The transmitter 912 couples the analog voltage generated from each symbol to the transmission medium 960. In the examples described herein, the transmitter 912 uses a binary non-return-to-zero (NRZ) modulation scheme. In binary NRZ, a symbol is one bit of the serial data and two analog voltages are used to represent each bit. Those skilled in the art will appreciate that the techniques described herein can also be used with other digital baseband modulation techniques, such as pulse-amplitude modulation (PAM), where a symbol includes a plurality of bits of the serial data.

In the example shown, the transmission medium 960 is a differential channel. Analog voltage is coupled to the transmission medium 960 using two complementary analog signals (referred to as positive and negative analog signals). For binary NRZ, a logic “0” of the serial data is represented by driving the transmission medium 960 with the positive analog signal at its lower voltage limit and the negative analog signal at its upper voltage limit. A logic “1” of the serial data is represented by driving the transmission medium 960 with the positive analog signal at its upper voltage limit and the negative analog signal to its lower voltage limit. Thus, the logic value of each bit of the serial data is based on the difference between the positive and negative analog signals, and not based on the level of either analog signal individually. The peak-to-peak difference between the positive analog signal and the negative analog signal is the voltage swing (also referred to as output swing or swing). The two complementary analog signals form a differential signal (also referred to as the transmitted signal).

The transmitter 912 includes a finite impulse response (FIR) filter 914, a pre-driver 915, an output driver 918, and control logic 950. The transmitter 912
is configured to process the serial data to pre-emphasize the transmitted signal and equalize the transmission medium 960. The FIR 914 can be used to mitigate inter-symbol interference (ISI) caused by the transmission medium 960. The transmission medium 960 degrades the signal quality of the transmitted signal. Channel insertion loss is the frequency-dependent degradation in signal power of the transmitted signal. When signals travel through a transmission line, the high frequency components of the transmitted signal are attenuated more than the low frequency components. In general, channel insertion loss increases as frequency increases. Signal pulse energy in the transmitted signal can be spread from one symbol period to another during propagation on the transmission medium 960. The resulting distortion is known as ISI. In general, ISI becomes worse as the speed of the communication system increases. The transmitter 912 uses pre-emphasis to equalize the transmission medium 960.

The output of the FIR filter 914 is coupled to an input of the pre-driver 915. An output of the pre-driver 915 is coupled to an input of the output driver 918. An output of the output driver 918 is coupled to the transmission medium 960. In operation, the FIR filter 914 receives the serial data. The FIR filter 914 includes a plurality of taps each providing a state of the serial data at different discrete times. In an example, the FIR filter 914 includes three taps, where one tap provides a current symbol of the serial data, another tap provides a delayed symbol of the serial data, and another tap provides an advanced symbol of the serial digital signal. The current, delayed, and advanced symbols are referred to as the main-cursor, the pre-cursor, and the post-cursor, respectively. The FIR filter 914 outputs a plurality of logic signals generated from the main-, pre-, and post-cursors, as described further below. While the FIR filter 914 is described as having three taps, in general, the FIR filter 914 can include a plurality of taps that provide a main-cursor, as well as one or more pre-cursors and/or one or more post-cursors.

The pre-driver 915 couples the logic signals output by the FIR filter 914 to the output driver 918. As discussed below, the output driver 918 is segmented and includes a plurality of output circuits coupled to the transmission medium 960. Each of the output circuits includes a series-source terminated (SST) output driver (e.g., a voltage-mode driver). The pre-driver 915 multiplexes the logic signals output by the FIR filter 914 among the output circuits to provide
each of the main-, pré-, and post-cursors to a respective percentage of the output circuits. The numbers of the output circuits driven by the main-cursor, pre-cursor, and post-cursor are selected by the control logic 950 to provide a selected pre-emphasis to the transmitted signal for equalizing the transmission medium 960.

In the example, the output driver 918 couples a differential signal to the transmission medium 960. The output circuits in the output driver 918 draw a data-dependent current from voltage regulator(s). A change in the average supply current can degrade deterministic jitter (DJ) of the transmitter. Accordingly, the output driver 918 includes a current compensation circuit 1150 that ensures a constant average current is drawn from the voltage regulator(s). The current compensation circuit 1150 is described below.

While the SERDES 916 and the SERDES 922 are shown, in other examples, each of the transmitter 912 and/or the receiver 926 can be a stand-alone circuit not being part of a larger transceiver circuit. In some examples, the transmitter 912 and the receiver 926 can be part of one or more ICs, such as application specific integrated circuits (ASICs) or programmable ICs, such as field programmable gate arrays (FPGAs).

Fig. 10 is a block diagram depicting the transmitter 912 according to an example. An input of the transmitter 912 is coupled to a parallel-in-serial-out (PISO) circuit 1002 of the SERDES 916. The PISO circuit 1002 includes a parallel input to receive a digital signal to be transmitted. The PISO circuit 1002 serializes the digital signal to generate serial data. In the example, the PISO circuit 1002 outputs two logic signals referred to as the even signal and the odd signal. The even signal includes every even symbol of the serial data, and the odd signal includes every odd symbol of the serial data. In the examples described herein, each symbol is 1-bit of the serial data hence the terms symbol and bit are used interchangeably for these examples. If the transmitter 912 is configured to use a multi-bit symbol modulation scheme, such as PAM, each symbol would include a plurality of bits. The serial data includes a period T between symbols (a symbol rate 1/T). Each of the even signal and the odd signal has a period 2T (a data rate 1/(2T)).

The FIR filter 914 receives the even and odd signals output by the PISO 1002. In the example, the FIR filter 914 includes three taps that provide main-,
pré-, and post-cursors for each of the événí and odd signals (referred to as événí and odd main-, pré-, and post-cursors). The FIR filter 914 outputs a plurality of logic signals that provide the even and odd main-, pré-, and post-cursors. In particular, the FIR filter 914 outputs logic signals for each of the odd pré-cursor ("pré-cursor odd"), the even pre-cursor ("pré-cursor even"), the odd main-cursor ("main-cursor odd"), the even main-cursor ("main-cursor even"), the odd post-cursor ("post-cursor odd"), and the even post-cursor ("post-cursor even"). Each of the logic signals output by the FIR filter 914 has a period 2T.

The pre-driver 915 includes multiplexers 10041 through 1004N (collectively multiplexers 1004) and multiplexing logic (MUX) 1006. Each of the multiplexers 1004 is a 2:1 multiplexer. The multiplexing logic 1006 includes inputs receiving the odd pré-cursor signal, the even pré-cursor signal, the odd main-cursor signal, the even main-cursor signal, the odd post-cursor signal, and the even post-cursor signal. The multiplexing logic 1006 includes 2T odd outputs coupled a first input of each of the multiplexers 1004 and a 2T even output coupled to a second input of each of the multiplexers 1004. Each 2T odd output of the multiplexing logic 1006 provides complementary logic signals for one of the pré-cursor, main-cursor, or post-cursor odd signals. Each 2T even output of the multiplexing logic 1006 provides complementary logic signals for one of the pré-cursor, main-cursor, or post-cursor even signals. The inputs of each multiplexer 1004 are alternately coupled to its output at a rate of 1/T. Thus, the output of each multiplexer 1004 provides complementary logic signals having a period T. For clarity, control inputs of the multiplexers 1004 are omitted from the drawing. Control inputs of the multiplexers 1004 are coupled to a clock signal to selects between the even and odd inputs at a rate of 1/T.

The output driver 918 includes a plurality of output circuits 1008 (e.g., N output circuits). As discussed above, each of the pré-cursor, main-cursor, and post-cursor signals is coupled to a certain percentage of the output circuits 1008 of the output driver 918. The MUX logic 1006 is configured to distribute the pré-, main-, and post-cursor signals among the multiplexers 1004, which feed the output circuits 1008. The MUX logic 1006 can couple logic signals for any of the pré-cursor, the main-cursor, or the post-cursor to any of the multiplexers 1004. The MUX logic 1006 includes a control input coupled to the control logic 950. The control logic 950 configures the MUX logic 1006 to couple logic signals for...
the pré-curşor to a selected number of the multiplexers 1004, logic signals for
the post-curşor to a selected number of the multiplexers 1004, and logic signals
for the main-curşor to a selected number of the multiplexers 1004. The
multiplexers 1004 convert the 2T outputs of the multiplexing logic 1006 to 1T
inputs of the output circuits 1008.

Fig. 11 is a schematic diagram depicting the output driver 918 according
to an example. The output driver 918 is configured similarly to the output driver
118. The output driver 918 includes output circuits 2081 through 208N (where N
is an integer greater than one), voltage regulators 2101 and 2102, and a current:
compensation circuit 1150. The voltage regulator 2101 is coupled to the
common node \( V_{\text{wlp}} \). The voltage regulator 2101 controls the voltage at the node
\( V_{\text{wlp}} \) and supplies current to the output circuits 208. The voltage regulator \( 210_2 \):
is coupled to the common node \( V_{\text{refh}} \). The voltage regulator \( 210_2 \) controls the
voltage at the node \( V_{\text{refh}} \) and sinks current from the output circuits 208 (e.g.,
supplies a negative current to the output circuits 208). The voltage regulator
\( 210_1 \) is coupled to a first supply voltage \( V_{\text{wlp}} \), and the voltage regulator \( 210_2 \) is
coupled to a second supply voltage (e.g., electrical ground).

The voltage regulators 210 set the swing of the output driver 918. The
differential peak-to-peak swing is based on \( V_{\text{wlp}} - V_{\text{refh}} \). With the dual regulators
\( 210_1 \) and \( 210_2 \) in the output driver 918, the swing and common-mode can be set
independently. For example, for a common-mode of 0.45 V and an output swing
of 0.6 V, \( V_{\text{wlp}} \) is set to 0.75 V and \( V_{\text{refh}} \) is set to 0.15 V. In the output driver 918,
equalization can be implemented by driving a different number of the output
circuits 208 with different main/pre/post cursor signals. With the dual-regulator
approach, the swing is changed by adjusting the regulator voltage. Thus,
equalization control is independent of the swing control. This allows for high FIR
resolution even in low-swing mode.

The output circuits 208 draw a data-dependent current from the voltage
regulators 210. The current drawn from the voltage regulators 210 is inversely
proportional to the magnitude of the differential output voltage. The magnitude
of the differential output voltage itself depends on the state of the main-, pre-, and
post-curşors. When the main-curşor has a different state than the pre-
cursor and/or post-curşor, the magnitude of the differential output voltage is large,
and the supplied current is small. That is, the magnitude of the differential output.
The voltage is large and the supplied current is small whenever a bit of the main-cursor \(1T\) signal is different from its previous and/or subsequent bit. Conversely, when the main-cursor has the same state as the pre-cursor and/or post-cursor, the magnitude of the differential output voltage is small and the supplied current is large. That is, the magnitude of the differential output voltage is small and the supplied current is large whenever a bit of the main-cursor \(1T\) signal is the same as its previous and/or subsequent bit. The difference between the “large” current and the “small” current (i.e., the current swing) can be large enough to degrade the deterministic jitter of the transmitter 912.

The current compensation circuit 1150 is coupled between the common nodes \(V_{\text{vlp}}\) and \(V_{\text{vln}}\). The current compensation circuit 1150 is controllable (e.g., using the control logic 950) to draw a selected current from the voltage regulator 210, (and sinked by the voltage regulator 210\(_s\)). The control logic 950 can control the current compensation circuit 1150 to equalize the average current supplied by the voltage regulator 210, and sinked by the voltage regulator 2502. The current compensation circuit 1150 is controlled to minimize the current swing and maintain the deterministic jitter performance of the transmitter 912. An example of the current compensation circuit 1150 is described below with respect to Fig. 12.

Fig. 12 is a schematic diagram depicting the current compensation circuit 1150 according to an example. In general, the current compensation circuit 1150 includes an event detector 1220 and a branch circuit 1202 that is coupled between the common nodes \(V_{\text{vlp}}\) and \(V_{\text{vln}}\). The branch circuit 1202 includes a switch 1210 coupled to a current source 1212. The series combination of the switch 1210 and the current source 1212 is coupled between the common nodes \(V_{\text{vlp}}\) and \(V_{\text{vln}}\). The event detector 1220 is coupled to the switch 1210 to supply a logic signal referred to as an enable signal \((\text{Sel1})\). The event detector 1220 controls the state of the enable signal \((\text{Sel1})\) based on presence of a pattern in logic signals output by the FIR filter 914.

In particular, the event detector 1220 detects a pattern in a plurality of \(2^T\) logic signals output by the FIR filter 914 that occurs when the state of a current symbol of the serial data is different from that of a delayed symbol and/or advanced symbol. Upon detecting the pattern, the event detector 1220 controls the enable signal \((\text{Sel1})\) to close the switch 1210, which couples the current.
sourcě 1212 between the common nodes \( V_{refp} \) and \( V_{refn} \). The current sourcě 1212 is controlled to draw a known amount of current from the voltage regulators 210. Upon absence of the pattern, the event detector 1220 controls the enable signal (Sel1) to open the switch 1210, which decouples the current source 1212 between the common nodes \( V_{refp} \) and \( V_{refn} \). In this manner, the average current drawn from the voltage regulators 210 is controlled based on the state of the serial data to minimize its effect on deterministic jitter of the transmitter 912.

In an example, the current compensation circuit 1150 generally includes M branch circuits 1202 coupled in parallel, e.g., branch circuits 1202, through 1202_m, where M is a positive integer. The switch 1210 generally includes switch circuits 1210, through 1210_i. Likewise, the current source 1212 includes current source circuits 1212, through 1212_m. The branch circuits 1202, through 1202_m respectively include the switch circuits 1210, through 1210_i and the current source circuits 1212, through 1212_m. When M is greater than one, the switch circuits 1210, through 1210_i are responsive to the enable signal (Sel1) and individual enable signals \( W_i \) through \( W_m \), which are logic signals that can be generated by the control logic 950. In operation, when the event detector 1220 detects the pattern, the event detector 1220 enables a selected number of the current source circuits 1212, through 1212_m as controlled by the control logic 950. The individual enable signals \( W_i \) through \( W_m \) thus control the weight of the current drawn by the branch circuits 1202, through 1202_m. The branch circuits 1202, through 1202_m implement a current-output digital-to-analog converter (DAC) that generates an analog current in response to the enable signal (Sel1) and a digital signal formed by the logic signals \( W_i \) through \( W_m \) (e.g., an M-bit digital code selecting from 2M current levels). The strength of the DAC can be programmed to match the strength of the equalization.

The event detector 1220 includes a logic gate 1222 configured to generate the enable signal (Sel1). In the example shown, the logic gate 1222 is an exclusive NOR (XNOR) gate. One input of the logic gate 1222 is coupled to receive the \( 2T \) odd main-cursor (designated main_odd (2T)). Another input of the logic gate 1222 is coupled to receive the \( 2T \) odd pre-cursor (designated pre_odd (2T)). The logic signal output by the logic gate 1222 is logic “0” when state of the odd main-cursor signal is different than the state of the odd pre-cursor signal. The logic signal output by the logic gate 1222 is logic “1” when the.
state of the odd main-cursor signal is the same as the state of the odd pre-cursor signal. As such, the logic gate 1222 detects a pattern where state of the odd main-cursor signal is different than the state of the odd pre-cursor signal, which indicates that a bit of the 1T main-cursor signal is different from its previous bit. Upon detecting the pattern, the logic gate 1222 asserts the enable signal, which enables activation one or more branch circuits 1202. Since the current compensation circuit 1150 equalizes the average current drawn from the supplies, the current compensation circuit 1150 can use 2T signals to detect the pattern, rather than the 1T signals, which is more energy efficient.

Fig. 13A is a table illustrating an example portion of a 1T main-cursor signal and its associated 2T odd signals. In the example, the 1T main-cursor signal has a bit sequence 0011100010 for discrete times 2n+1 through 2n+10, where n is an integer. The 2T odd main-cursor signal includes the bits from the odd discrete times 2n+1, 2n+3, ..., 2n+9, which is the bit pattern 01101. The 2T odd post-cursor signal is the bit pattern 01000 for odd discrete times 2n+1, 2n+3, ..., 2n+9. The 2T odd pre-cursor signal is the bit pattern 0100 for the odd discrete times 2n+3, 2n+5, ..., 2n+9. The shaded boxes show where the 2T odd main-cursor is different from the 2T odd pre-cursor and/or the 2T odd post-cursor. This occurs at discrete times 2n+3, 2n+5, and 2n+9. The logic gate 1222 in the example of Fig. 12 asserts the enable signal (Sel1) at discrete times 2n+3 and 2n+9 when detecting a state difference between the 2T odd main-cursor and the 2T odd pre-cursor.

Returning to Fig. 12, the logic gate 1222 looks for a pattern indicative of a bit of the 1T main-cursor signal being different from its previous bit. The event detector 1220 can also include a logic gate 1224 that looks for a pattern indicative of a bit of the 1T main-cursor signal being different from its subsequent bit. In the example shown, the logic gate 1224 is an XNOR gate. The logic gate 1224 outputs a logic signal referred to as an enable signal (Sel2). One input of the logic gate 1224 is coupled to receive main_odd (2T). Another input of the logic gate 1224 is coupled to receive the 2T odd post-cursor (designated post_odd (2T)). The logic signal output by the logic gate 1224 is logic “0” when state of the odd main-cursor signal is different than the state of the odd post-cursor signal. The logic signal output by the logic gate 1224 is logic “1” when the state of the odd main-cursor signal is the same as the state of the odd post-
čuřšor signal. As such, the logic gate 1224 detects a pattern where state of the odd main-cursor signal is different than the state of the odd post-cursor signal, which indicates that a bit of the 1T main-cursor signal is different from its subsequent bit. Upon detecting the pattern, the logic gate 1224 asserts the enable signal (Sel2). In the example of Fig. 13A, the logic gate 1224 asserts the enable signal (Sel2) at discrete times 2n+5 and 2n+9.

The enable signal (Sel2) is used to control another resistance coupled in parallel with the current source 1212. In particular, the current compensation circuit 1150 includes at least one branch circuit 1204 that is coupled between the common nodes V_{ref} and V_{ref}. The branch circuit(s) 1204 provide a switch 1214 coupled in series with a current source 1216. The series combination of the switch 1214 and the current source 1216 is coupled between the common nodes V_{ref} and V_{ref}. The event detector 1220 is coupled to the switch 1214 to supply the enable signal (Sel2).

In an example, the current compensation circuit 1150 generally includes M branch circuits 1204 coupled in parallel, e.g., branch circuits 1204, through 1204. The switch 1214 generally includes switch circuits 1214, through 1214. Likewise, the current source 1216 includes current source circuits 1216, through 1216. The branch circuits 1204, through 1204, respectively include the switch circuits 1214, through 1214, and the current source circuits 1216, through 1216. When M is greater than one, the switch circuits 1214, through 1214, are responsive to the enable signal (Sel2) and individual enable signals X, through X, which are logic signals that can be generated by the control logic.950. The branch circuits 1204, through 1204, implement another current-output DAC that generates an analog current in response to the enable signal (Sel2) and a digital signal formed by the logic signals X, through X (e.g., an M-bit digital code selecting from 2M current levels).

In an example, each switch circuit 1210, through 1210, includes a logic gate 1206 and a transistor M. In the example shown, the logic gate 1206 is a NAND gate and the transistor M is a p-channel FET, such as a PMOS transistor. An output of the logic gate 1206 is coupled to a gate of the transistor M. A source of the transistor M is coupled to the common node V_{ref}. A drain of the transistor M is coupled to a respective current source circuit 1212 through 1212. One input of the logic gate 1206 receives the enable signal
Another input of the logic gate 1206 receives one of the individual enable signals W<\text{M}:1>. Likewise, each switch circuit 1214, through 1214<\text{i}>, includes a logic gate 1208 and a transistor M<\text{i}>. In the example shown, the logic gate 1208 is a NAND gate and the transistor M<\text{i}> is a p-channel FET, such as a PMOS transistor. An output of the logic gate 1208 is coupled to a gate of the transistor M<\text{i}>. A source of the transistor M<\text{i}> is coupled to the common node V_{\text{ref}}. A drain of the transistor M<\text{i}> is coupled to a respective current source circuit 1216 through 1216<\text{i}>. One input of the logic gate 1208 receives the enable signal (Sel2).

Another input of the logic gate 1208 receives one of the individual enable signals X<\text{M}:1>.

In an example, each current source circuit 1212, through 1212<\text{i}>, includes a transistor M<\text{i}> and a transistor M<\text{s}>. A drain of the transistor M<\text{s}> is coupled to a drain of the transistor M<\text{i}>. A source of the transistor M<\text{s}> is coupled to a drain of the transistor M<\text{i}>. A source of the transistor M<\text{s}> is coupled to the common node V_{\text{ref}}. A gate of the transistor M<\text{s}> is coupled to a bias node (Bias2). A gate of the transistor M<\text{s}> is coupled to a bias node (Bias1). Likewise, each current source circuit 1216, through 1216<\text{i}>, includes a transistor M<\text{s}> and a transistor M<\text{s}>. A drain of the transistor M<\text{s}> is coupled to a drain of the transistor M<\text{i}>. A source of the transistor M<\text{s}> is coupled to a drain of the transistor M<\text{i}>. A source of the transistor M<\text{s}> is coupled to the common node V_{\text{ref}}. A gate of the transistor M<\text{s}> is coupled to a bias node (Bias2). A gate of the transistor M<\text{s}> is coupled to a bias node (Bias1). The transistors M<\text{i}>, M<\text{s}>, M<\text{s}>, and M<\text{s}> are n-channel FETs, such as NMOS transistors. The transistors M<\text{s}>, M<\text{s}>, M<\text{s}>, and M<\text{s}> are biased into saturation by the bias voltages Bias1 and Bias2.

In the example of Fig. 12, the event detector 1220 compares the 2T odd main-cursor signal with the respective 2T odd pre- and post-cursor signals. In other examples, the event detector 1220 can compare the 2T even main-cursor signal with the respective 2T even pre- and post-cursor signals. Fig. 13B is a table illustrating an example portion of a 1T main-cursor signal and its associated 2T even signals. In the example, the 1T main-cursor signal has the same bit sequence 0011100010 for discrete times 2n+1 through 2n+10 as shown in Fig. 13A. The 2T even main-cursor signal includes the bits from the even discrete times 2n+2, 2n+4,...,2n+10, which is the bit pattern 01000. The
2T even post-cursor signal is the bit pattern 1101 for even discrete times 2n+2, 2n+4,….2n+8. The 2T even pre-cursor signal is the bit pattern 01101 for the even discrete times 2n+2, 2n+4,….2n+10. The shaded boxes show where the 2T even main-cursor is different from the 2T even pre-cursor and/or the 2T even post-cursor. This occurs at discrete times 2n+2, 2n+4, 2n+6, 2n+8, and 2n+10. The event detector 1220 can be configured to assert the enable signal (Sel1) at discrete times 2n+6 and 2n+10, and assert the enable signal (Sel2) at discrete times 2n+2 and 2n+8.

While the foregoing is directed to specific examples, other and further examples may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.
CLAIMS
What is claimed is:

1. A driver circuit, comprising:
   a plurality of output circuits coupled in parallel between a differential input and a differential output and having a first common node and a second common node, each of the plurality of output circuits comprising:
   a series combination of a pair of inverters and a pair of resistors, coupled between the differential input and the differential output;
   first source terminals of the pair of inverters coupled to the first common node; and
   second source terminals of the pair of inverters coupled to the second common node;
   a first voltage regulator having an output coupled to the first common node of the plurality of output circuits;
   a second voltage regulator having an output coupled to the second common node of circuits; and
   a current compensation circuit coupled between the outputs of the first and second voltage regulators.

2. The driver circuit of claim 1, wherein the current compensation circuit comprises:
   a plurality of circuits having an enable input, a first bias input, and a second bias input, each of the plurality of circuits having a first transistor, a second transistor, and a third transistor serially connected to provide a current path between the outputs of the first and second voltage regulators.

3. The driver circuit of claim 2, wherein, for each of the plurality of circuits of the current compensation circuit, a gate of the first transistor is coupled to receive a signal of the enable input, a gate of the second transistor is coupled to receive a signal of the first bias input, and a gate of the third transistor is coupled to receive a signal of the second bias input.
4. The driver circuit of claim 1, wherein the first voltage regulator comprises:
a first transistor coupled between a supply voltage source and the first common node of the plurality of outputs circuits; and
a first operational amplifier having a first input coupled to a first reference voltage source, a second input coupled to the first common node of the plurality of output circuits, and an output coupled to a gate of the first transistor.

5. The driver circuit of claim 4, wherein the second voltage regulator comprises:
a second transistor coupled between a ground source and the second common node of the plurality of outputs circuits; and
a second operational amplifier having a first input coupled to a second reference voltage source, a second input coupled to the second common node of the plurality of output circuits, and an output coupled to a gate of the second transistor.

6. The driver circuit of claim 1, wherein the second voltage regulator comprises:
an output transistor that includes a source coupled to a first voltage supply node and a drain coupled to an output node;
a first transistor that includes a source coupled to the output node;
a second transistor that includes a source coupled to a gate of the output transistor and a drain coupled to a second voltage supply node;
a resistor coupled between the second voltage supply node and a first node that includes the drain of the first transistor and a gate of the second transistor; and
an error amplifier that includes a first input coupled to a reference voltage node, a second input coupled to the output node, and an output coupled to a gate of the first transistor.
7. The driver circuit of claim 6, wherein the error amplifier includes a folded cascode amplifier that includes: a source-coupled transistor pair, which includes a source node coupled to a current source and drains coupled to an output circuit, wherein the output circuit is disposed between the first voltage supply node and the second voltage supply node, and wherein gates of the source-coupled transistor pair are coupled to the reference voltage node and the output node, respectively.

8. The driver circuit of claim 1, wherein the current compensation circuit includes:
   a switch coupled in series with a current source, the series combination of the switch and the current source coupled between a first voltage supply node and a second voltage supply node; and
   an event detector coupled to the switch to supply an enable signal, the event detector configured to control state of the enable signal based on presence of a pattern in the plurality of logic signals.

9. The driver circuit of claim 8, wherein:
   the current source includes a plurality of current source circuits and the switch includes a plurality switch circuits respectively coupled in series with the plurality of current source circuits;
   the enable signal is a common enable signal; and
   each of the plurality of switch circuits is responsive to the common enable signal and a respective one of a plurality of individual enable signals.

10. The driver circuit of claim 9, wherein each of the plurality of switch circuits includes:
    a transistor coupled in series with a respective one of the plurality of current source circuits and a logic gate coupled to a gate of the transistor, the logic gate having a first input coupled to receive the common enable signal and a second input coupled to receive a respective one of the plurality of individual enable signals.
11. The driver circuit of claim 10, wherein each of the plurality of current source circuits of the current source includes:
   a first transistor in series with a second transistor, the first transistor including a gate coupled to a first bias node and the second transistor including a gate coupled to a second bias node.

12. The driver circuit of claim 1, further comprising:
   a first capacitor coupled between the first common node of the plurality of output circuits and a ground source; and
   a second capacitor coupled between the second common node of the plurality of output circuits and the ground source.

13. The driver circuit of claim 1, wherein the differential output of the plurality of output circuits is coupled to a pair of transmission lines.

14. A method of controlling a driver circuit in a transmitter, comprising:
   receiving a plurality of outputs of an equalizer in the transmitter;
   coupling each of the plurality of outputs of the equalizer to at least one of a plurality of output circuits of the driver circuit;
   enabling first and second voltage regulators coupled to the plurality of output circuits; and
   enabling at least one of a plurality of current compensation circuits coupled between the first and second voltage regulators.

15. The method of claim 19, wherein the plurality of output circuits is coupled in parallel between a differential input and a differential output and includes a first common node and a second common node, wherein each of the plurality of output circuits comprises a series combination of a pair of enable circuits, a pair of inverters, and a pair of resistors, coupled between the differential input and the differential output; a first transistor coupled between the first common node and first source terminals of the pair of inverters; and a second transistor coupled between the second common node and second source terminals of the pair of inverters, and wherein the method further comprises:
   disabling at least one of the plurality of output circuits; and
adjusting a gate-to-source voltage of each of the first transistor and the second transistor in each of the plurality of circuits based on feedback from first and second replica output circuits.
Receive outputs of equalizer in the transmitter

Couple each of the equalizer outputs to at least one of a plurality of output circuits of the driver circuit

Enable first and second voltage regulators coupled to the output circuits to establish a desired swing

Enable one or more current compensation circuits to equalize current drawn from the voltage regulator

Control impedance of output driver

Disable one or more of the output circuits to compensate for on-chip resistor variation

Adjust Vgs of stacked transistors in each output circuit based on feedback from replica circuits to adjust for NMOS/PMOS transistor variation

FIG. 4
FIG. 6
FIG. 7
FIG. 8
FIG. 9
### FIG. 13A

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### FIG. 13B

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A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K19/0185 H04L25/02
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H03K H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of Box C.  [X] See patent family annex.

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Date of the actual completion of the international search
30 October 2017

Date of mailing of the international search report
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Authorized officer
Mesic, Mate
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