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PHOTO-DETECTOR AND RELATED METHODS

FIELD OF THE INVENTION

[0001] The present invention relates generally to photodetectors, particularly photodetectors used in accelerometers, and methods for forming such photodetectors.

BACKGROUND OF THE INVENTION

[0002] In some accelerometers, a light source such as a light emitting diode (LED) is used in conjunction with a moveable shadow arm to project light onto a pair of photodiodes. Movement of the shadow arm caused by changes in acceleration experienced by the accelerometer results in changes in how light from the LED projects onto the photodiodes, and correspondingly affects current flow through the photodiodes. In such accelerometers, the photodiodes are often subject to and/or are the source of a number of problems. Such problems include, but are not necessarily limited to, excessive amounts of dark current (current arising from thermal energy rather than light), bias shifts resulting from minor shifts in light distribution, conductors blocking light, conductors increasing the distance between the shadow arm and photodiodes, and increased sensitivity of the accelerometer to temperature changes. As such, there is a need for improved photodiodes and methods of forming such diodes, particularly as they incorporated into accelerometers.

SUMMARY OF THE INVENTION

[0003] The present invention is directed to an apparatus comprising at least one multilayer wafer including a device layer adjacent to a barrier layer wherein the device layer comprises at least two photoconductive regions separated by an etched channel extending through the device layer. In some instances the apparatus may be an accelerometer comprising at least two photodiodes formed on a silicon-on-insulator (SOI) wafer wherein each diode comprises at least one photosensitive region of a device layer of the SOI wafer, each of the photosensitive regions of the at least two photodiodes being defined by one or more etched channels extending through the device layer of the SOI wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The exact nature of this invention, as well as the objects and advantages thereof, will become readily apparent from consideration of the following specification in conjunction with the accompanying drawings in which like reference numerals designate like parts throughout the figures thereof and wherein:

[0005] Figure 1 is preferred accelerometer according to the present invention.

[0006] Figure 2 is a multi-layer wafer.

[0007] Figure 3 is the wafer of figure 2 after formation and separation of photosensitive areas.

[0008] Figure 4 is the wafer of figure 3 after metallization and wirebonding.

[0009] Figure 5 is a top view of a wafer after the device layer has been removed from non-diode areas.

[0010] Figure 6 is a top view of the wafer of figure 4 illustrating doping regions

[0011] Figure 7 is a top view of the wafer of figure 5 after metallization.

[0012] Figure 8 is a top view of the wafer of figure 6 after wirebonding.

[0013] Figure 9 illustrates a dicing pattern.

[0014] Figure 10 is a alternate embodiment of an accelerometer according to the present invention.

[0015] Figure 11 illustrates a prior art accelerometer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] Reference will now be made to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that these embodiments are not intended to limit the invention. On the contrary, the invention is

intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be understood by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure the important aspects of the present invention.

[0017] In Figure 1, a preferred accelerometer 1 comprises a light source 3 in the form of an LED, a shadow arm 5, a photodiode assembly 7, an electrical circuit assembly 9, and an accelerometer sub-plate 11. The shadow arm 5 is moveably coupled between the light source 3 and the photodiode assembly 7 such that it forms a shadow in the light from the source 3 projecting onto the assembly 7, and acceleration of the accelerometer 1 causes a corresponding movement of the arm 3 and a shift in the light from the source 3 projected onto the assembly 7.

[0018] The photodiode assembly 7 is formed from a multi-layer wafer comprising a device layer 13, a barrier layer 15, and a handle layer 17, and includes photodiodes 19 and 21, electrically conductive pads/traces 23, 25, and 27, wirebonds 29 and 31, and epoxy 33. The photodiodes 19 and 21 each comprise a photosensitive region of the device layer 13 where the device layer 13 has been etched to separate the photosensitive regions of the photodiodes 19 and 21. The pads/traces 23 are positioned so as to be in direct contact with the photosensitive regions of diodes 19 and 21. The pads/traces 25 are positioned to be electrically isolated from pads/traces 23 other than through the wirebonds 29, and the pads/traces 27 are electrically coupled to and/or extensions of the pads/traces 25. The wirebonds 31 are used to electrically couple pads/traces 25 to chip assembly 9, and are bonded to the handle portion 17 of photodiode assembly 7 by epoxy 33.

[0019] The photodiode assembly 7 is physically bonded to the body 37 of the circuit assembly 9 by the bonding layer 35, and electrically coupled via the wirebonds 31 to the electrically conductive pads/traces 39 of the circuit assembly 9. In some instances circuit assembly 9 will consist essentially of conductors on a substrate, while in other instances it

may comprise additional electrical components, such components possibly including but not being limited to resistors, capacitors, inductors, diodes, transistors, and operational amplifiers.

[0020] Figures 2-4 illustrate a method of forming a photo-detector. In figure 2, a SOI wafer comprises a silicon device layer 13 separated from a silicon handle layer 17 by a layer of silicon oxide 15. All or portions of the device layer 13 are doped or otherwise treated to make at least two desired regions photosensitive. The at least two photosensitive regions are then isolated from each other and from any other portions of the device layer 13 by etching through the device layer 13 (and possibly through the oxide layer 15). As shown in figure 3, the at least two regions correspond to two photodiodes 19 and 21 being formed. After etching, the SOI is metalized to form pads and/or traces 23 and 25, and possibly also to mask portions of the photosensitive regions. After the pads and/or traces are formed, gold wirebonds 29 are coupled to and extended between the pads/traces 23 positioned on/in the photosensitive regions with other pads/traces 25 that are on the SOI wafer, but not on/in the photosensitive regions. As illustrated by figure 1, the handle layer 17 can then be physically bonded to the body 37 of the circuit assembly 9 by the bonding layer 35, and electrically coupled via the wirebonds 31 extending between pads/traces 27 and the electrically conductive pads/traces 39 of the circuit assembly 9.

[0021] Although described as having gold wirebonds, other embodiments may utilize other types of wirebonds such as aluminum wirebonds. Similarly the pads and traces described may comprise any conductive material that can be coupled to the device layer, but in many instances will comprise aluminum, and in some instances function both as a pad and as a light shield.

[0022] Figures 5-8 also illustrate a method of forming a photo-detector. The method of figures 5-8 is substantially similar to that of figures 2-4. As such, additional understanding might be obtained if figures 5-8 are viewed as if they provide a top view of a method of forming a device shown in side views in figures 2-4.

[0023] In figure 5, a SOI wafer comprises a silicon device layer 13 separated from a silicon handle layer by a layer of silicon oxide 15. In figure 5, portions of the device layer that will not be used to form photo-diodes have been removed by etching to expose silicon oxide layer 15. Separating the device layer of a wafer into photodiode pairs by etching rather than mechanical methods eliminates the possibility of such cutting forming micro fissures that extend into the photodiodes, and as a result, decreases the amount of dark current resulting from such micro fissures.

[0024] In figure 6, the remaining portions of the device layer 13 are doped to form areas 13A of P+ diffusion, and areas 13B of N+ diffusion. In figure 7, metallization has been performed to form pads 25, 27, 23A and 23B where pads 23B are in the form of light shields covering the areas of N+ diffusion and portions of the areas of P+ diffusion. In figure 8, wirebonds 29 and 33 have been added as has epoxy 33.

[0025] It is important to note that providing pads 25 and 27, and the traces coupling the pads, shortens and simplifies the routing of wirebonds 29. As the wirebonds 29 need not be routed over any conductive surfaces other than those they are electrically bound to, there is no need to utilize epoxy or some other materials to isolate central portions of the wirebonds from the surfaces they are adjacent to. The elimination of epoxy on the surface eliminates the possibility of such epoxy interfering with the performance of the device through negative effects from thermal expansion and/or contraction. As can be seen, some of the traces form conductive paths extending from one side of the device to the other such that wirebonds coupling the device to an external circuit are all located on a single side of the device without having any wirebonds extending between the two photo-diodes.

[0026] It is contemplated that pads/traces 25 may advantageously be formed on the silicon oxide layer 15, or on a portion of device layer 13 that has been electrically isolated from the photodiode portions of layer 13.

[0027] It is contemplated that, prior to bonding the handle layer 17 to body 37, wirebonds 31 may be coupled to pads/traces 25 and bonded via epoxy to a side or back of the SOI wafer. In such a form, the assembly is readily handled and transported, and suited for later mounting to the body 37 and electrical connection to the pads/traces 39 of the circuit assembly 9.

[0028] In some embodiments, such as that shown in figure 10, the wirebonds may extend between pads/traces on the photodiodes to pads/traces positioned off of the SOI wafer. For such embodiments, after etching and metallization, the handle layer 17 may be physically bonded to a ceramic carrier 49 comprising pads/traces 43 using bonding layer 47. Gold wirebonds are then positioned between pads/traces 23 on the SOI wafer that are photodiode connectors and pads/traces 43 on the ceramic carrier. Afterwards, the ceramic carrier can be physically bonded to the body 37 of the circuit assembly 9 by the bonding layer 51, and electrically coupled via the wirebonds 45 to the electrically conductive pads/traces 39 of the circuit assembly 9.

[0029] It is contemplated that after the photosensitive regions are isolated via etching, and after light shields, pads, and/or traces having been added by metallization, individual regions, or groups of regions that were simultaneously formed on the SOI wafer may be separated, possibly by dicing or some other mechanism. Figure 9 illustrates one of many possible dicing patterns. The pattern of figure 9 forms pairs of photodiodes positioned relative to each other. Dicing, as used herein, refers to a mechanical process of separation rather than a chemical process, and includes at least slicing, sawing, and other cutting methods where an external force is applied to the wafer to separate the wafer into pieces.

[0030] The present invention provides many benefits over previous accelerometers such as accelerometer 52 of figure 11. In the device of figure 11, photodiodes 55 and 57 are formed on silicon substrates 67 and 69. Pads/traces 59 provide connections to photodiodes 55 and 57, and wirebonds 61 and 63 provide electrical connections between pads/traces 59 and pads/traces 9. Epoxy 65 insures that wirebonds 61 and 63 do not move inappropriately, and electrically isolates them from portions of the photodiodes they should not come in contact with. Substrates 67 and 69 are formed by mechanically separating a common substrate after it has been bonded to carrier 49 by layer 53. Carrier 49 is in turn bonded to body 37 via layer 51. As can be seen, photodiodes 55 and 57 must be positioned relative to each other with such relative positions being impacted by the process of bonding the photodiodes to carrier 49. Moreover, epoxy 65 can extend between the photodiodes and by expanding and contracting in response to temperature, humidity, etc., can cause undesired movement between the photodiodes. The substrates 67 and 69 will typically be formed by dicing with resultant damage extending into the photosensitive areas of diodes 55 and 57.

[0031] It is contemplated that any member described herein may unless specifically limited comprise a single piece or an assembly of pieces and each such piece may comprise any material or combination of materials that renders the piece suitable for its intended function. Similarly, the pieces, assemblies, and/or members may be sized and dimensioned in any manner that allows them to be used for their intended function. That being said, it is contemplated that some SOI wafer used as described herein may have a diameter of 4", 5", 6" or 8", may have a device layer that is 1 to 200 microns thick, may have a thermal oxide layer that is 0.1 to 2 microns thick, and may have a handle layer that is 300 to 800 microns thick.

[0032] It is contemplated that the methods and apparatus disclosed herein provide benefits over prior art methods and apparatus at least in part because: (a) photosensitive regions are separated by etching rather than by dicing to eliminate damage caused by dicing; and (b) there is no need for epoxy on the device layer or in any other location where thermal expansion and/or contraction of the epoxy can impact the relative positions of the photodiodes.

[0033] The embodiments of the present invention described herein comprise multiple novel features with each described embodiment including either a single such feature or a combination of such features. Other contemplated embodiments include all combinations of one or more such novel features not explicitly described herein as such combinations are readily discernable from the embodiments described. In light of the various contemplated embodiments, the present invention can be characterized in a number of ways with the following paragraphs providing examples of some such characterizations.

[0034] In some instances, an embodiment of the present invention may be characterized as an apparatus comprising at least one multilayer wafer, the at least one multi-layer wafer including a device layer adjacent to a barrier layer, wherein the device layer comprises at least two photoconductive regions separated by an etched channel extending through the device layer.

[0035] In some such instances, an embodiment of the present invention may also be characterized as an accelerometer comprising at least two photodiodes formed on a silicon-on-insulator (SOI) wafer wherein each diode comprises at least one photosensitive region of a

device layer of the SOI wafer, each of the photosensitive regions of the at least two photodiodes being defined by one or more etched channels extending through the device layer of the SOI wafer. Some such embodiments may also be characterized as satisfying or including one or more of the following: (a) the at least two photodiodes is electrically coupled to at least one electrically conductive pad or trace that is positioned on the SOI wafer but outside the photosensitive regions; (b) the at least one electrically conductive pad or trace is formed on an oxide layer of the SOI wafer underlying the device layer; (c) the at least one electrically conductive pad or trace is formed on a handle layer of the SOI wafer underlying an oxide layer of the SOI wafer underlying the device layer; (d) each photodiode is electrically coupled by a wirebond extending between an electrically conductive pad or trace formed on one of the photosensitive regions and an electrically conductive pad or trace formed outside of the photosensitive regions; (e) a plurality of electrically conductive pads or traces formed outside of the photosensitive regions that are electrically connected via a plurality of wirebonds to a plurality of electrically conductive pads or traces that are not formed on the SOI wafer wherein the plurality of wirebonds are bonded to a side of the SOI wafer; (f) an electrical circuit wherein the plurality of wirebonds bonded to a side of the SOI wafer are electrically coupled to the circuit; (g) a plurality of electrically conductive pads or traces formed outside of the photosensitive regions that are electrically connected via a plurality of wirebonds to a plurality of electrically conductive pads or traces that are formed on a carrier coupled to the SOI wafer opposite the device layer; (h) an electrical circuit and a plurality of wirebonds extending between a plurality of electrically conductive pads or traces that are formed on the carrier and the circuit.

[0036] In some instances, an embodiment of the present invention may also be characterized as having at least X photoconductive regions are positioned sufficiently far apart such that they can subsequently be separated by dicing without the dicing causing significant damage to the photoconductive regions where X is one of 2, 5, 10, 100, and 1000.

[0037] In some instances, an embodiment of the present invention may be characterized as an accelerometer comprising at least two photodiodes wherein the position of the photodiodes relative to each other is determined by the size and position of one or more removed regions of a device layer used to form the at least two photodiodes. In some such instances, the accelerometer may be characterized as satisfying or including one or more of

the following: (a) the accelerometer comprises at least one multilayer wafer including a device layer adjacent to a barrier layer and a handle layer coupled to the barrier layer opposite the device layer; (b) the device layer comprises at least two photoconductive regions separated by an etched channel extending through the device layer; (c) the barrier layer comprises at least one conductive trace extending from a first side of the barrier layer comprising a first of the at least two photodiodes to a second side of the device layer comprising a second of the at least two photodiodes; (d) the first side is opposite the second side; and (e) the accelerometer comprises a plurality of wirebonds but none of the wirebonds extend between the first and second sides.

[0038] In some instances, an embodiment of the present invention may be characterized as an apparatus including a plurality of photodiodes formed by: (a) obtaining a multilayer wafer comprising at least a device layer separated from a handle layer by a barrier layer; (b) modifying the device layer to form a plurality of photoconductive regions; (c) separating the photoconductive regions by etching away the device layer between the photoconductive regions; and (d) forming a first plurality of electrically conductive pads or traces on the photoconductive regions. In some instances, such an embodiment may further be characterizes as including or satisfying one or more of the following: (i) wirebonding at least one wire to at least some of the first plurality of electrically conductive pads or traces; (ii) separating the photoconductive regions by etching away the device layer between the photoconductive regions comprises using reactive ion etching; (iii) forming a second plurality of electrically conductive pads or traces on the device layer other than on the photoconductive regions; (iv) the second plurality of electrically conductive pads or traces is formed on the barrier layer; (v) electrically coupling at least some of the first plurality of electrically conductive pads or traces with at least some of the second plurality of electrically conductive pads or traces by wirebonding; and (vi) electrically coupling at least some of the first plurality of electrically conductive pads or traces with at least some of the second plurality of electrically conductive pads or traces by wirebonding.

CLAIMS

What Is Claimed Is:

1. An apparatus comprising at least one multilayer wafer, the at least one multi-layer wafer including a device layer adjacent to a barrier layer, wherein the device layer comprises at least two photoconductive regions separated by an etched channel extending through the device layer.
2. The apparatus of claim 1 wherein the apparatus is an accelerometer comprising at least two photodiodes formed on a silicon-on-insulator (SOI) wafer wherein each diode comprises at least one photosensitive region of a device layer of the SOI wafer, each of the photosensitive regions of the at least two photodiodes being defined by one or more etched channels extending through the device layer of the SOI wafer.
3. The apparatus of claim 2 wherein each of the at least two photodiodes is electrically coupled to at least one electrically conductive pad or trace that is positioned on the SOI wafer but outside the photosensitive regions.
4. The apparatus of claim 3 wherein the at least one electrically conductive pad or trace is formed on an oxide layer of the SOI wafer underlying the device layer.
5. The apparatus of claim 3 wherein each photodiode is electrically coupled by a wirebond extending between an electrically conductive pad or trace formed on one of the photosensitive regions and an electrically conductive pad or trace formed outside of the photosensitive regions.
6. The apparatus of claim 3 further comprising a plurality of electrically conductive pads or traces formed outside of the photosensitive regions that are electrically connected via a plurality of wirebonds to a plurality of electrically conductive pads or traces that are not formed on the SOI wafer wherein the plurality of wirebonds are bonded to a side of the SOI wafer.
7. The apparatus of claim 6 further comprising an electrical circuit wherein the plurality of wirebonds bonded to a side of the SOI wafer are electrically coupled to the circuit.

8. The apparatus of claim 3 further comprising a plurality of electrically conductive pads or traces formed outside of the photosensitive regions that are electrically connected via a plurality of wirebonds to a plurality of electrically conductive pads or traces that are formed on a carrier coupled to the SOI wafer opposite the device layer.
9. The apparatus of claim 8 further comprising an electrical circuit and a plurality of wirebonds extending between a plurality of electrically conductive pads or traces that are formed on the carrier and the electrical circuit.
10. The apparatus of claim 1 wherein the at least two photoconductive regions are positioned sufficiently far apart such that they can subsequently be separated by dicing without the dicing causing micro fissures to extend into the photoconductive regions.
11. The apparatus of claim 10 wherein the device layer comprises at least X photoconductive regions separated by a plurality of etched channels extending through the device layer, the photoconductive regions being positioned so that they can subsequently be separated by dicing without the dicing causing micro fissures to extend into the photoconductive regions wherein X is one of 5, 10, 100, and 1000.
12. An accelerometer comprising at least two photodiodes wherein the position of the photodiodes relative to each other is determined by the size and position of one or more etched regions of a device layer used to form the at least two photodiodes.
13. The accelerometer of claim 12 wherein:

the accelerometer comprises at least one multilayer wafer including a device layer adjacent to a barrier layer and a handle layer coupled to the barrier layer opposite the device layer;

the device layer comprises at least two photoconductive regions separated by an etched channel extending through the device layer;

the barrier layer comprises at least one conductive trace extending from a first side of the barrier layer comprising a first of the at least two photodiodes to a second side of the device layer comprising a second of the at least two photodiodes; and
the first side is opposite the second side.

14. The accelerometer of claim 13 wherein the accelerometer comprises a plurality of wirebonds but none of the wirebonds extend between the first and second sides.
15. A method of forming an apparatus including a plurality of photodiodes comprising:
obtaining a multilayer wafer comprising at least a device layer separated from a handle layer by a barrier layer;
modifying the device layer to form a plurality of photoconductive regions;
separating the photoconductive regions by etching away the device layer between the photoconductive regions; and
forming a first plurality of electrically conductive pads or traces on the photoconductive regions.
16. The method of claim 15 further comprising wirebonding at least one wire to at least some of the first plurality of electrically conductive pads or traces.
17. The method of claim 16 wherein separating the photoconductive regions by etching away the device layer between the photoconductive regions comprises using reactive ion etching.
18. The method of claim 17 further comprising forming a second plurality of electrically conductive pads or traces on the device layer other than on the photoconductive regions.
19. The method of claim 18 wherein the second plurality of electrically conductive pads or traces is formed on the barrier layer.

20. The method of claim 19 further comprising electrically coupling at least some of the first plurality of electrically conductive pads or traces with at least some of the second plurality of electrically conductive pads or traces by wirebonding.

FIG. 1

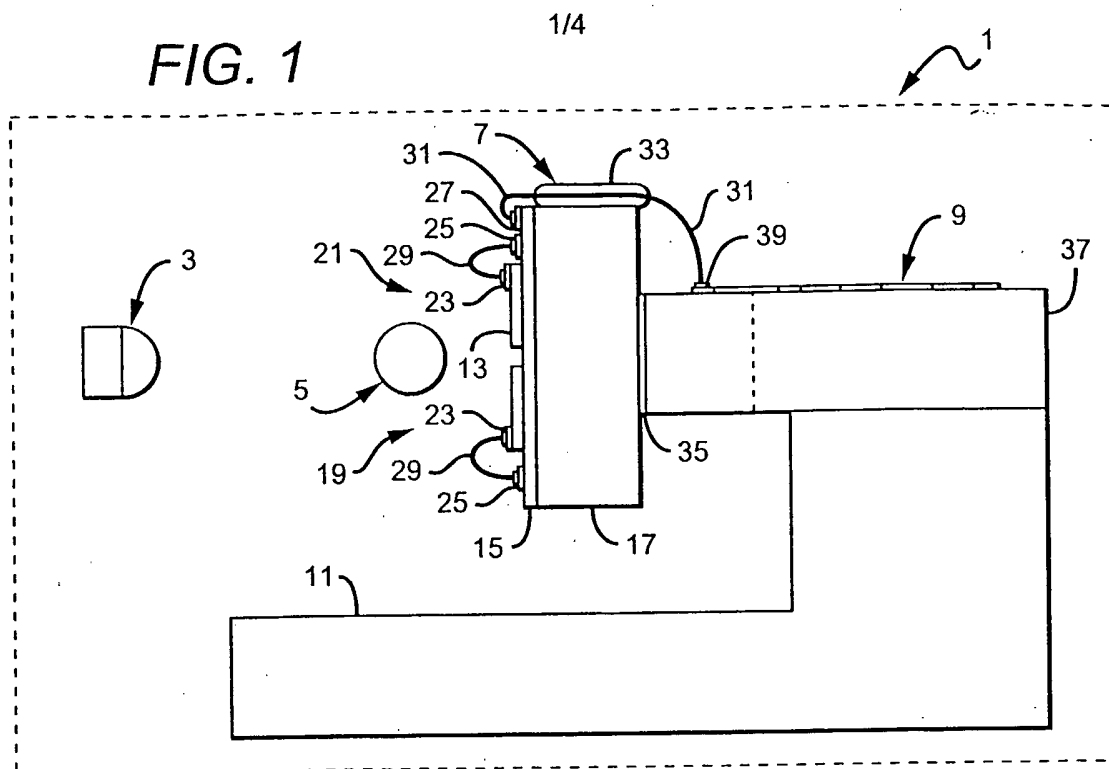


FIG. 2

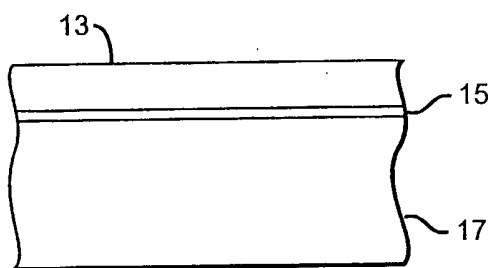


FIG. 3

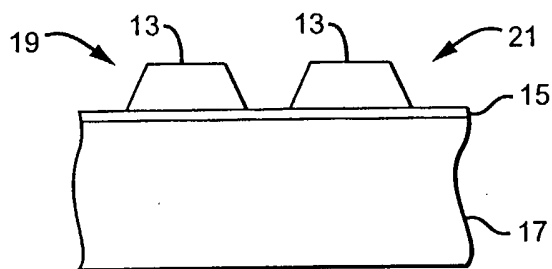
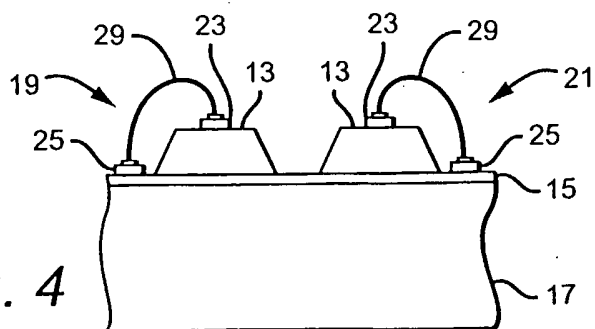


FIG. 4



2/4

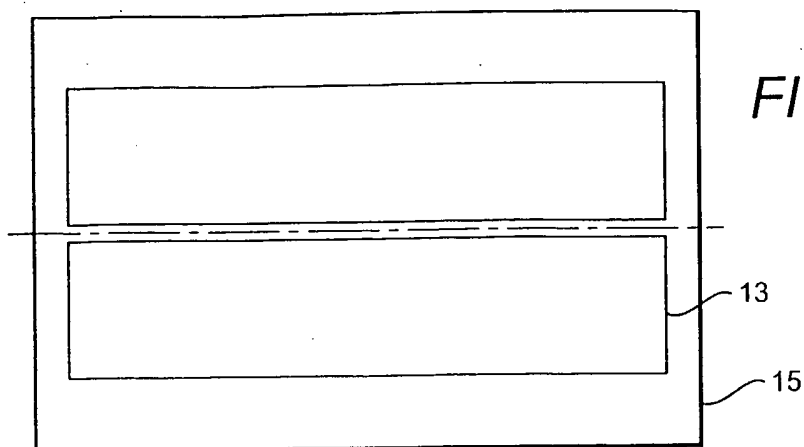


FIG. 5

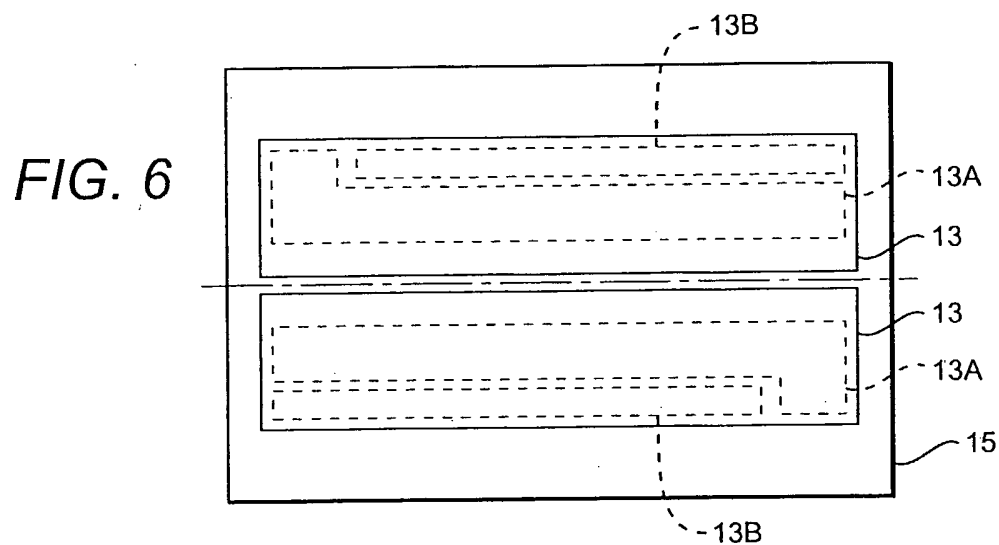


FIG. 6

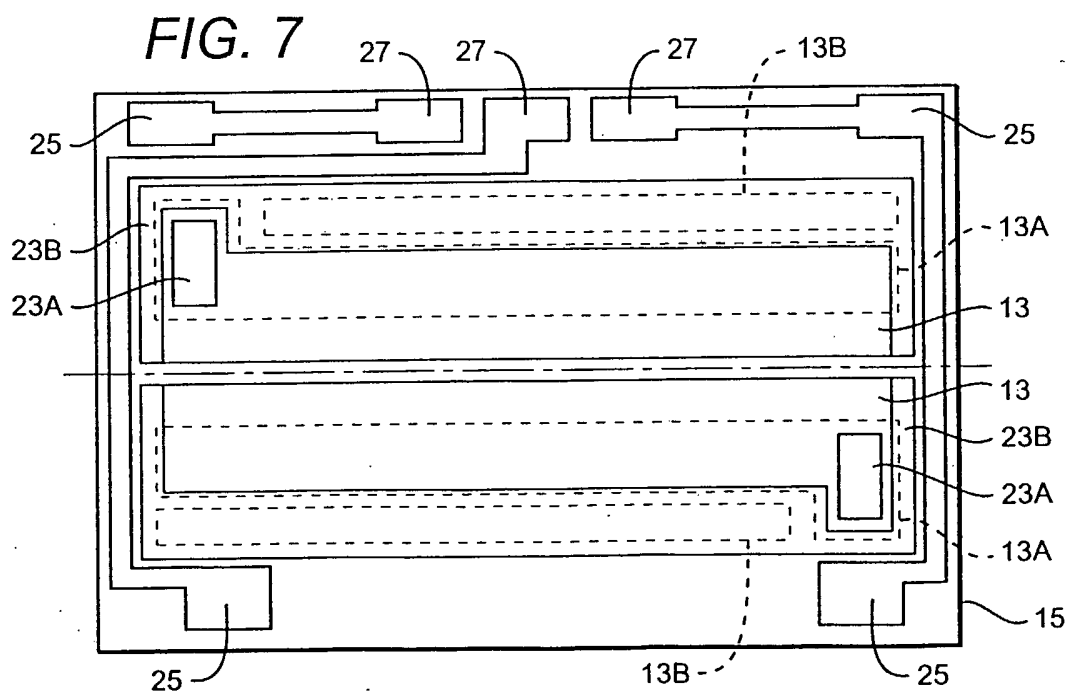


FIG. 7

FIG. 9

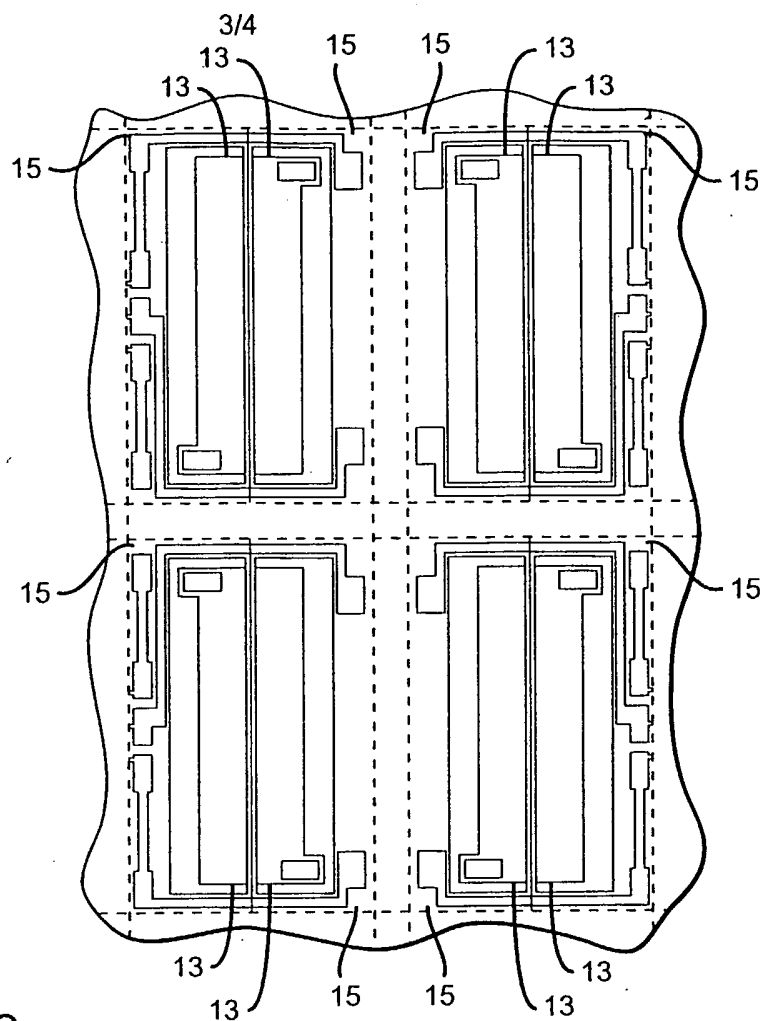


FIG. 8

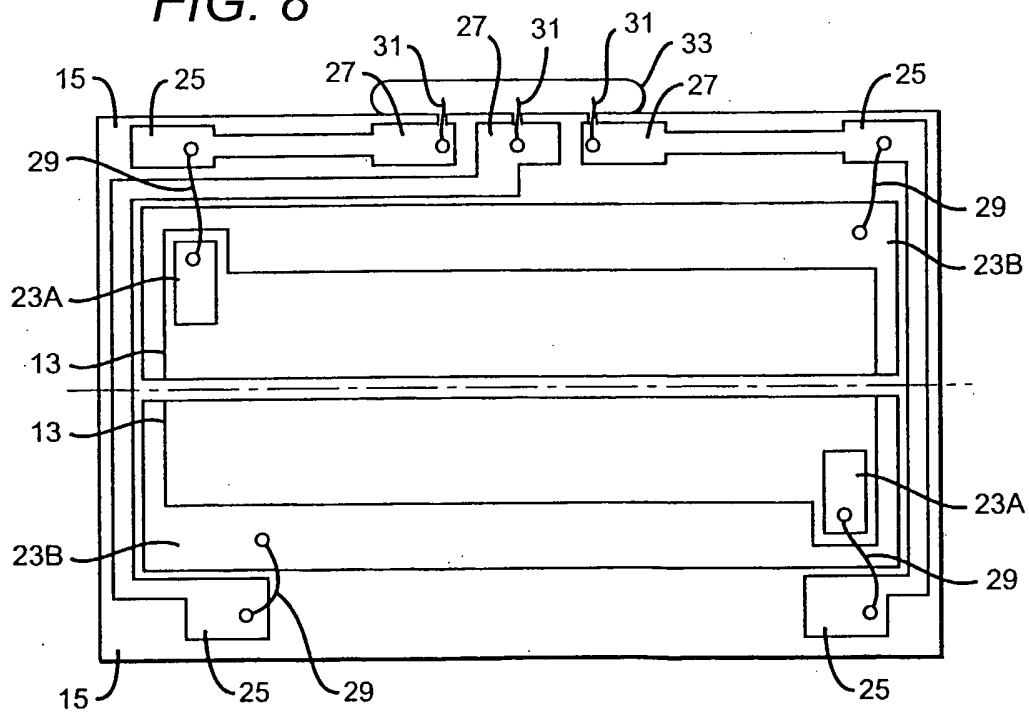
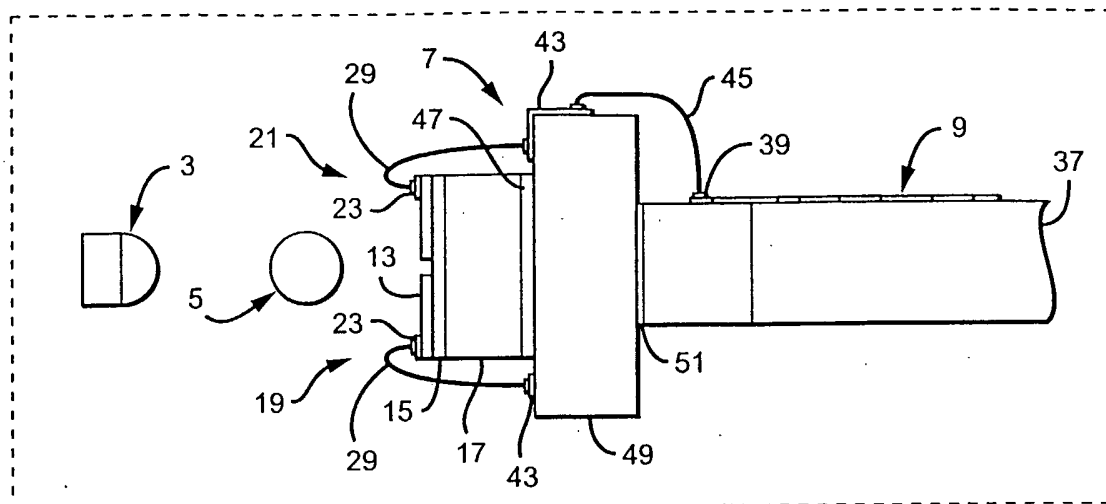
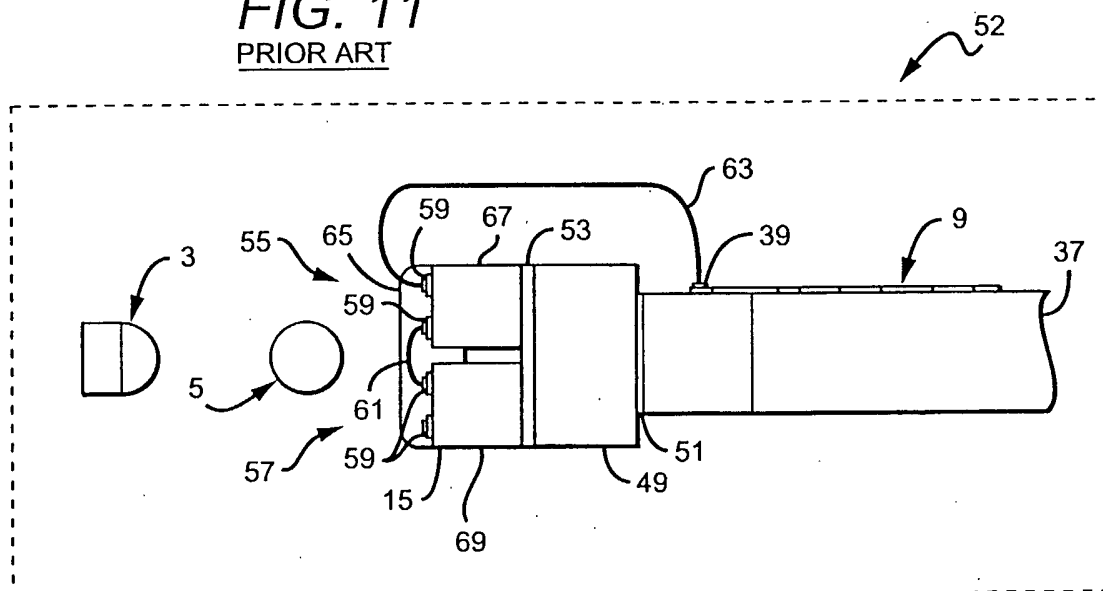


FIG. 10**FIG. 11**
PRIOR ART

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/035909

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L31/09 H01L27/144 G01P15/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X	US 2004/222358 A1 (BUI PETER STEVEN ET AL) 11 November 2004 (2004-11-11)	1,10,11, 15-17
Y	paragraphs [0018], [0066] - [0074]; figure 5	18-20
X	US 4 792 931 A (NISHIDA ET AL) 20 December 1988 (1988-12-20)	12
A	column 6, line 9 - line 31; figures 2,3	2,3,13, 16,18-20
X	DE 39 08 886 A1 (SIEMENS AG, 1000 BERLIN UND 8000 MUENCHEN, DE) 20 September 1990 (1990-09-20)	1,10,11, 15,16
	abstract; figures 1,2	
	----- -/--	

☒ Further documents are listed in the continuation of Box C

☒ See patent family annex

* Special categories of cited documents

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

Z document member of the same patent family

Date of the actual completion of the international search

11 May 2006

Date of mailing of the international search report

19/05/2006

Name and mailing address of the ISA/

European Patent Office, P.B 5818 Patentlaan 2
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Fax (+31-70) 340-3016

Authorized officer

Voignier, V

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2005/035909

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X	US 6 147 349 A (RAY ET AL) 14 November 2000 (2000-11-14) column 3, line 57 - column 4, line 51; figure 3 -----	15,16
Y	US 2002/000510 A1 (MATSUDA KENICHI) 3 January 2002 (2002-01-03) -----	18-20
A		3,5,15, 16
A	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 06, 30 April 1998 (1998-04-30) -& JP 10 048248 A (TOKIMEC INC), 20 February 1998 (1998-02-20) abstract; figures 1,5,6 -----	2,3,12, 13
A	US 2004/060355 A1 (NEMIROVSKY Yael ET AL) 1 April 2004 (2004-04-01) figures 2,3 -----	2,3,12, 13
A	US 2001/024460 A1 (YAMAMOTO MASAHIRO ET AL) 27 September 2001 (2001-09-27) paragraphs [0140] - [0143]; figure 28 -----	4-6, 18-20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2005/035909

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-11,13,14

An apparatus (for example an accelerometer) comprising at least two photodiodes formed in a device layer on a barrier layer formed on a substrate (for example a SOI substrate), and separated one from another by an etched channel.

2. claim: 12

An accelerometer with at least two photodiodes defined by etched regions

3. claims: 15-20

A method for forming several photodiodes in a photosensitive layer on a barrier layer formed on a substrate including the step of etching the photosensitive layer for separating the photodiodes, and forming pads on the formed photosensitive regions.

INTERNATIONAL SEARCH REPORT

mation on patent family members

International application No

PCT/US2005/035909

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