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(54) **LARGE BIT-PER-CELL THREE-DIMENSIONAL MASK-PROGRAMMABLE READ-ONLY MEMORY**

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Publication Classification

(57) **ABSTRACT**

A large bit-per-cell three-dimensional mask-programmable read-only memory (3D-MPROM$_B$) is disclosed. It can achieve large bit-per-cell (e.g. 4-bpc or more). 3D-MPROM$_B$ can be realized by adding resistive layer(s) or resistive element(s) to the memory cells.
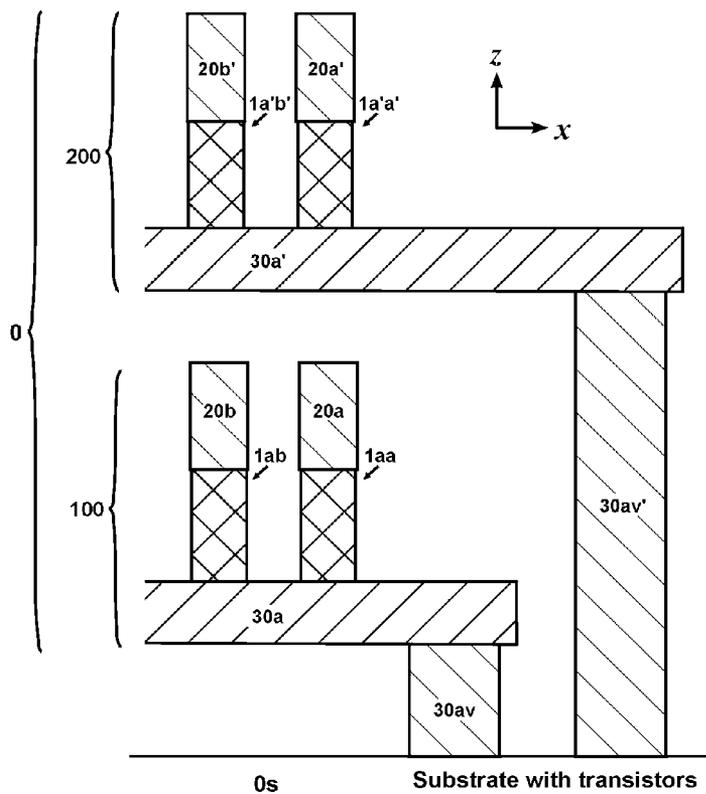
Fig. 1

Substrate with transistors
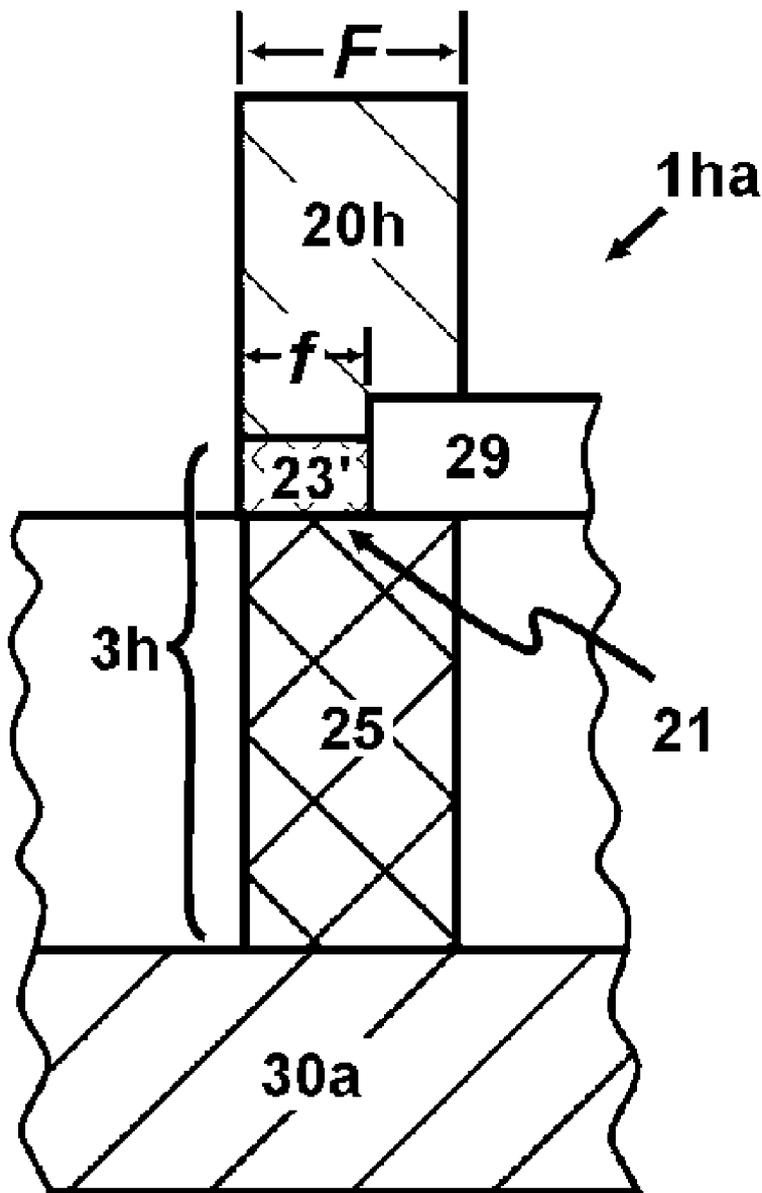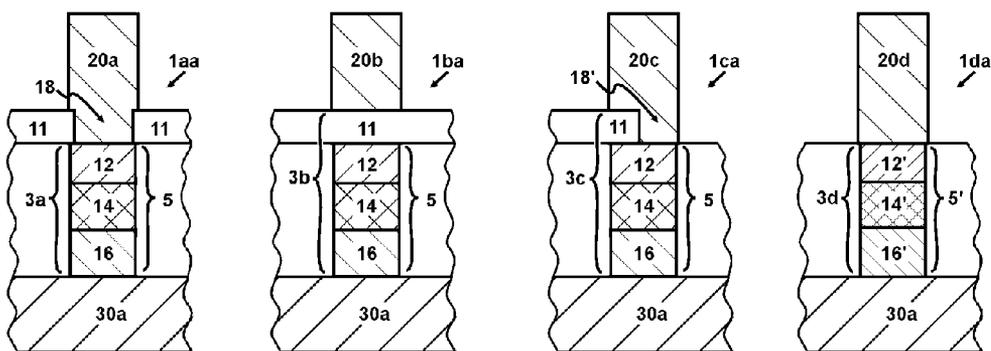
Fig. 2A
(Prior Art)

Fig. 2B
(Prior Art)

Fig. 2C
(Prior Art)

Fig. 2D
(Prior Art)

log (I)

410 411 412 423 414 425 416 427 418 419 420 421 422 423 424 425

I_T

'0' '1' '2' '3' '4' '5' '6' '7' '8' '9' 'a' 'b' 'c' 'd' 'e' 'f'

ΔV_T

V_{T0} V_{T1} V_{T2} V_{T3} V_{T4} V_{T5} V_{T6} V_{T7} V_{T8} V_{T9} V_{Ta} V_{Tb} V_{Tc} V_{Td} V_{Te} V_{Tf} V

TVW
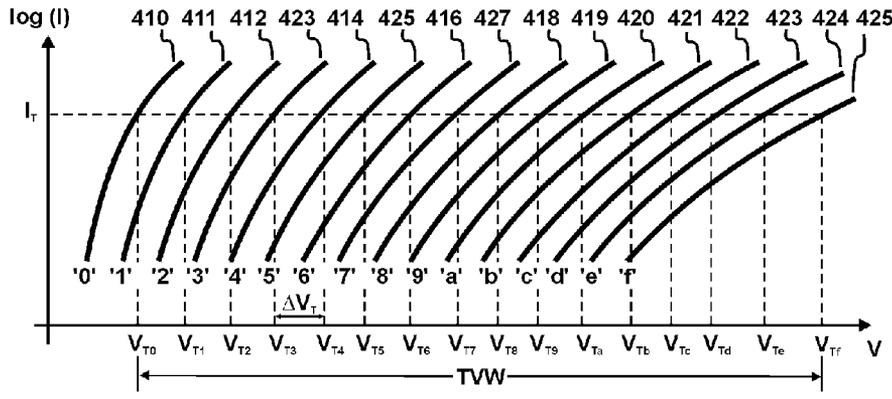
Fig. 3

Fig. 4A

Fig. 4B

Fig. 4C

Fig. 4D

log (I)

430   431   432

I_T

I-V(1za)   I-V(23)   I-V(1ea)

V_{T0} V_r V_T V

Fig. 5

502 ~ }23   Fig. 6A

501 ~
502 ~ }23   Fig. 6B

502 ~
503 ~ }23   Fig. 6C
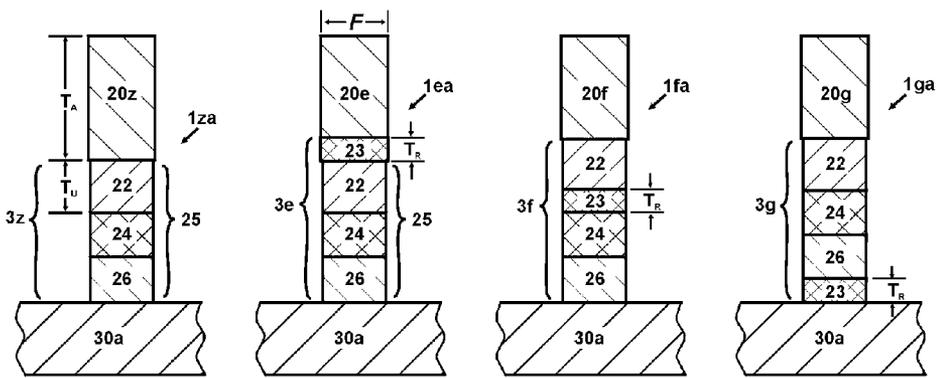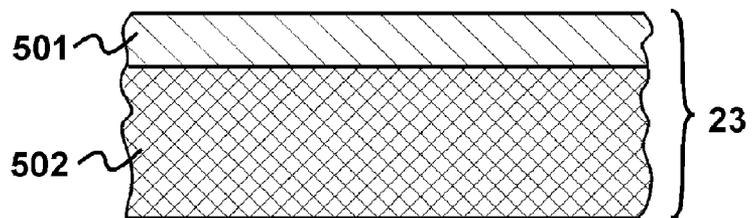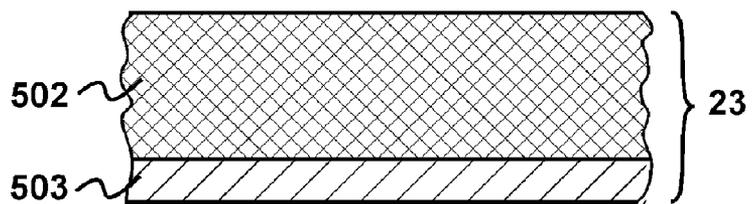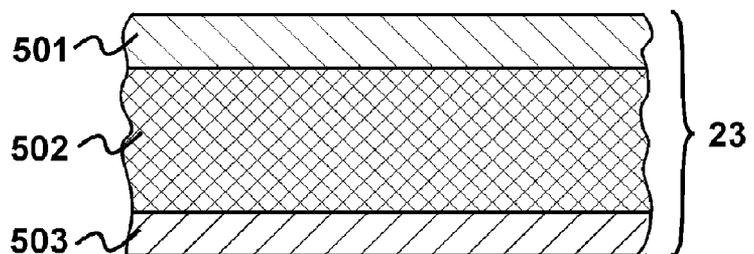
501 ~
502 ~
503 ~ }23   Fig. 6D
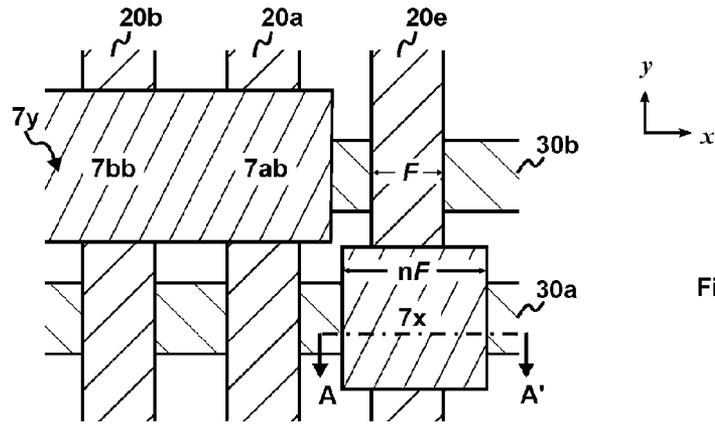
Fig. 7
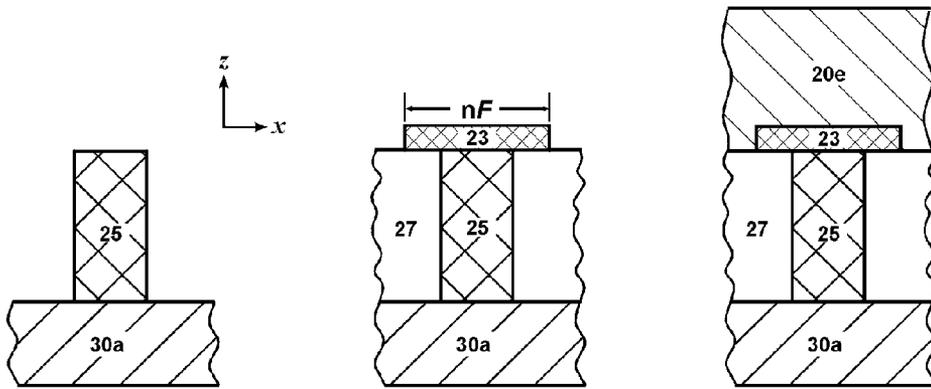
Fig. 8A

Fig. 8B

Fig. 8C

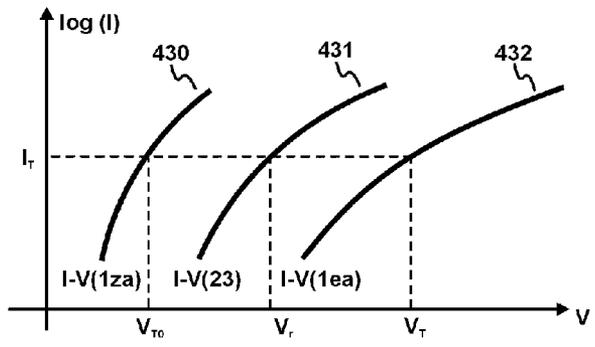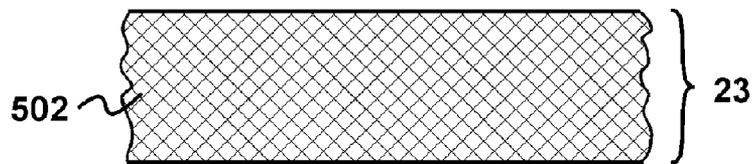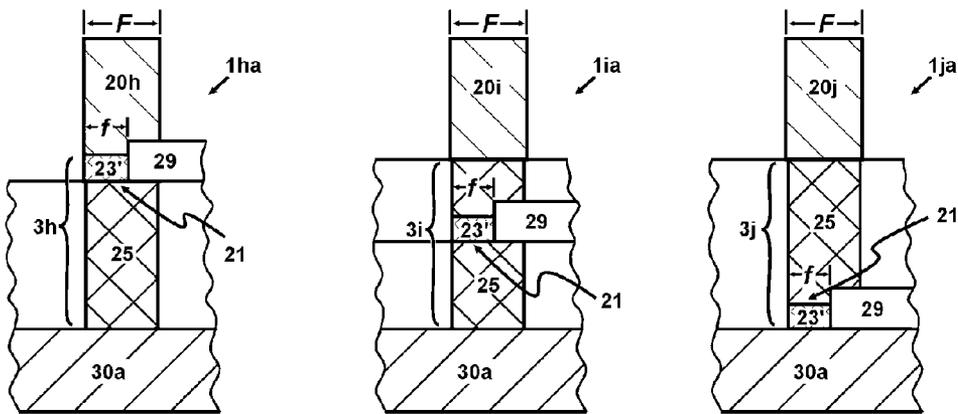Fig. 9A

Fig. 9B

Fig. 9C
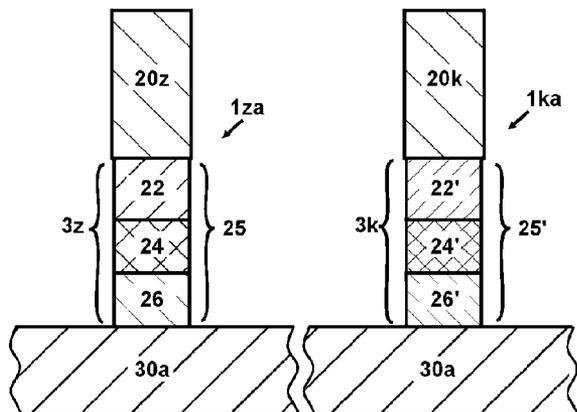
Fig. 10
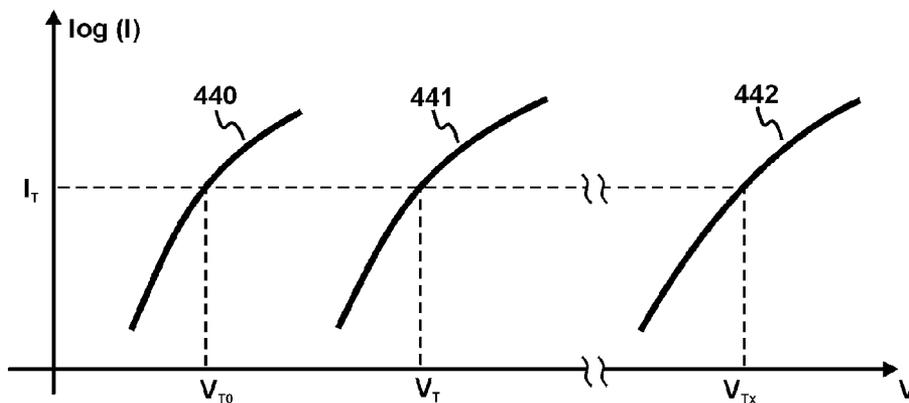
Fig. 11
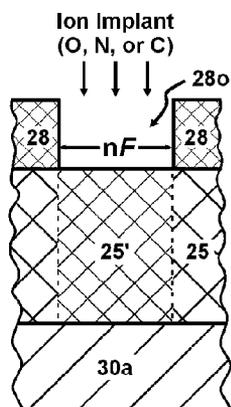
Fig. 12A
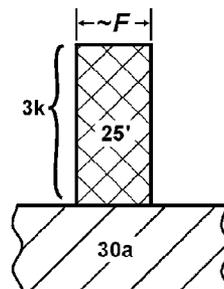
Fig. 12B
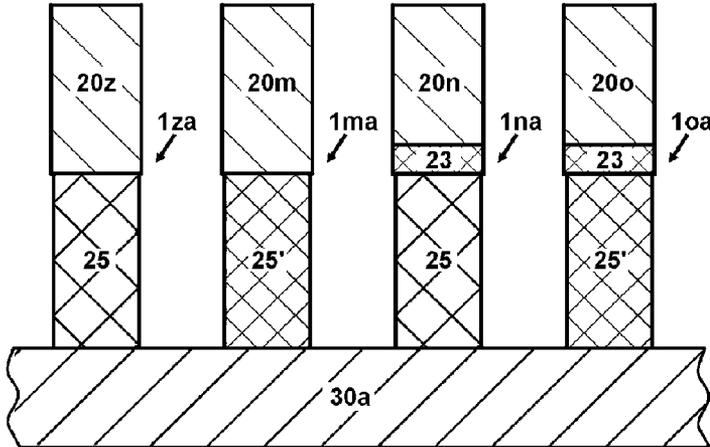
Fig. 13A
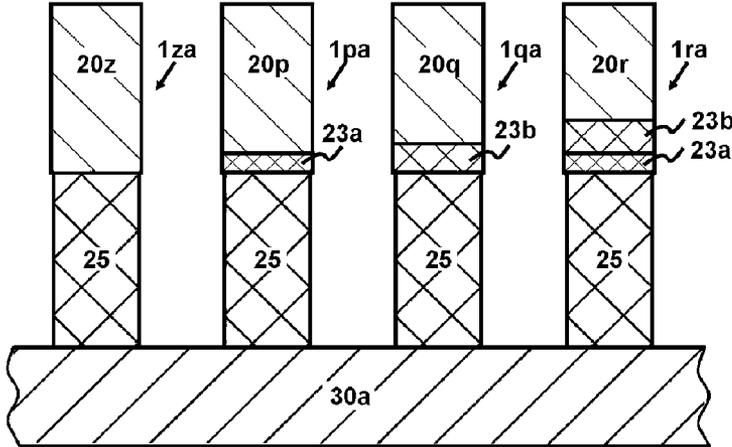
Fig. 13B
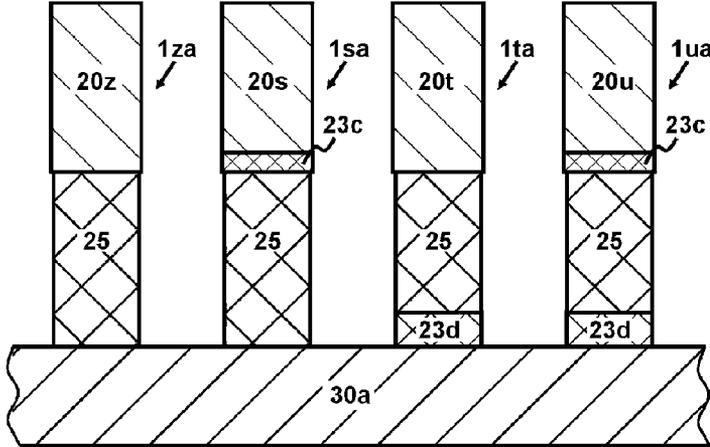
Fig. 13C
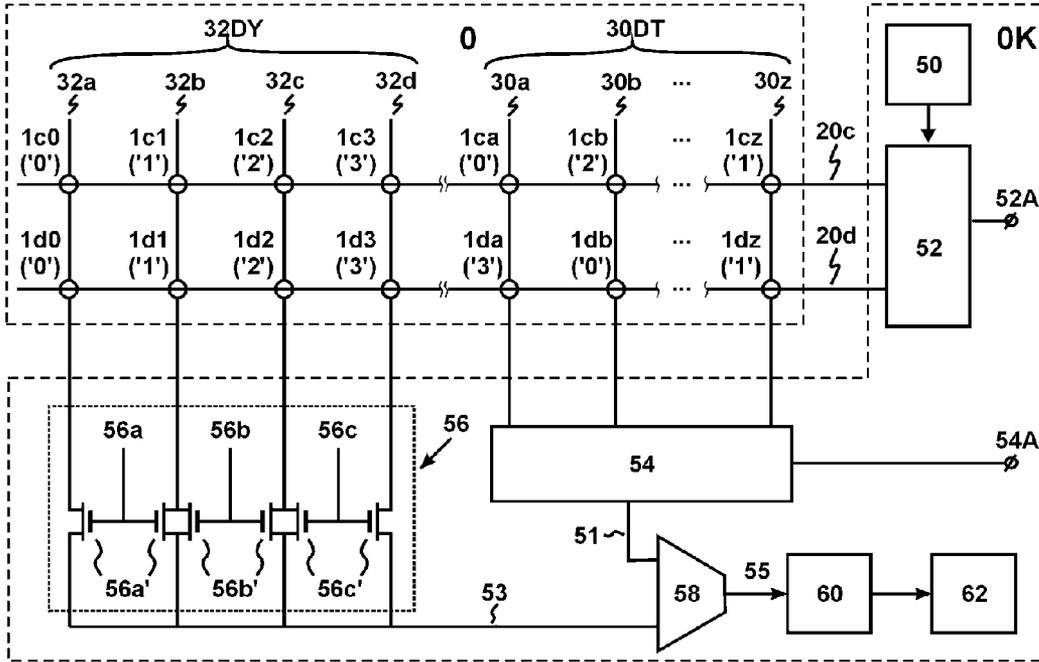
Fig. 14A
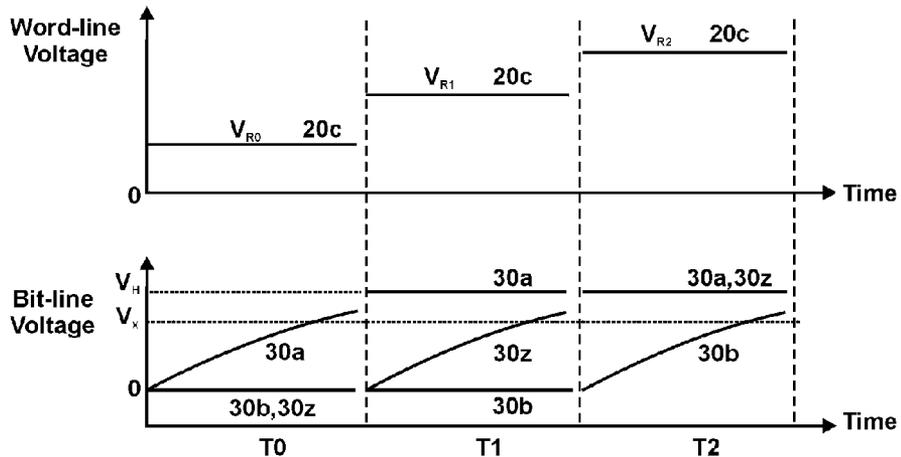
Fig. 14B

Cell State	Upper Resistive Layer 23x	Middle Resistive Layer 23y	Lower Resistive Layer 23z	Resistive Element
'0'	No	No	No	No
'1'	No	No	No	Yes
'2'	No	No	Yes	No
'3'	No	No	Yes	Yes
'4'	No	Yes	No	No
'5'	No	Yes	No	Yes
'6'	No	Yes	Yes	No
'7'	No	Yes	Yes	Yes
'8'	Yes	No	No	No
'9'	Yes	No	No	Yes
'a'	Yes	No	Yes	No
'b'	Yes	No	Yes	Yes
'c'	Yes	Yes	No	No
'd'	Yes	Yes	No	Yes
'e'	Yes	Yes	Yes	No
'f'	Yes	Yes	Yes	Yes

Fig. 15A
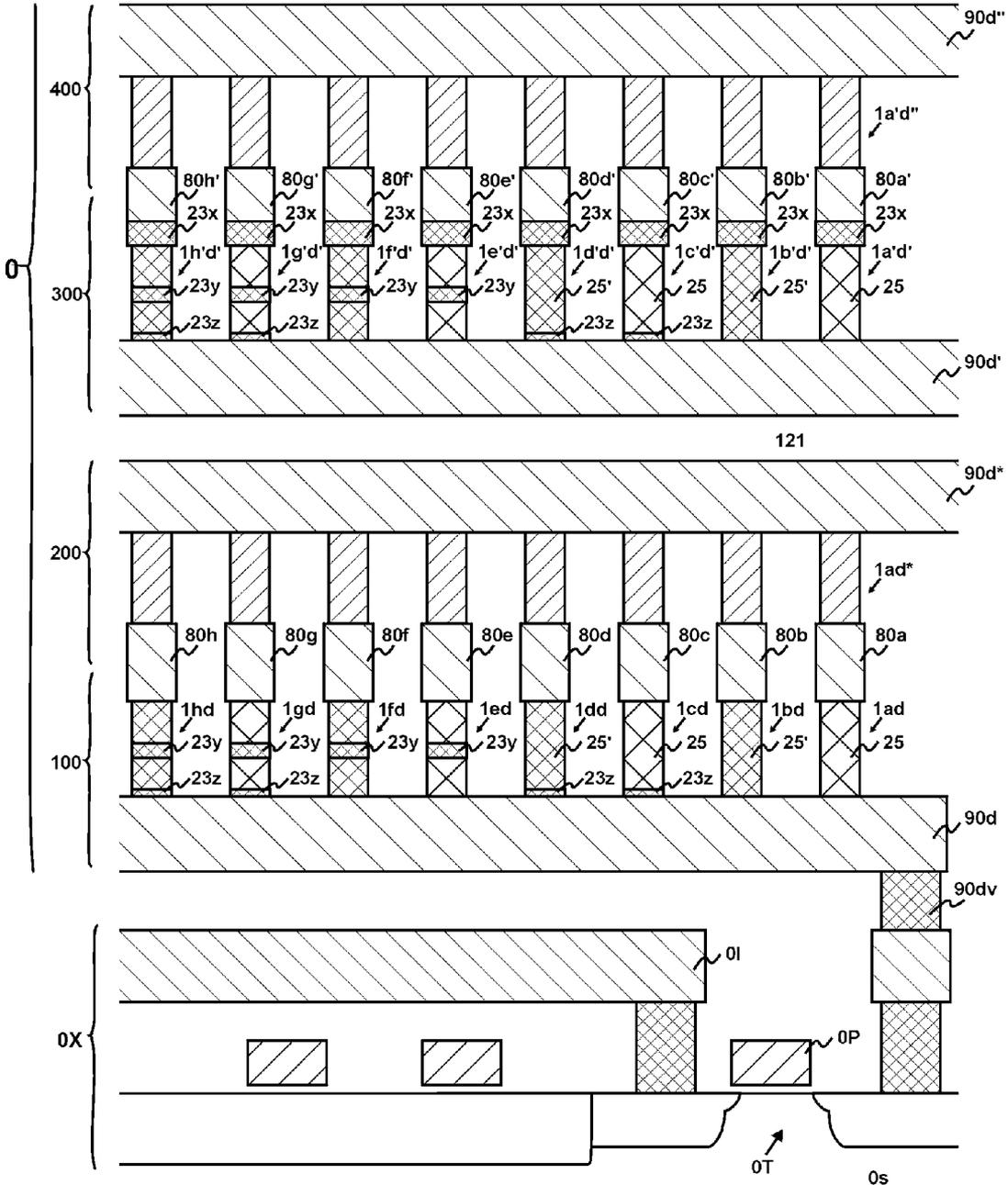
Fig. 15B

LARGE BIT-PER-CELL THREE-DIMENSIONAL MASK-PROGRAMMABLE READ-ONLY MEMORY

BACKGROUND

[0001] 1. Technical Field of the Invention

[0002] The present invention relates to the field of integrated circuits, and more particularly to mask-programmable read-only memory (mask-ROM).

[0003] 2. Prior Arts

[0004] Mask-programmable read-only memory (mask-ROM) refers to those types of memories into which data are written during manufacturing, preferably during the lithographic steps. Three-dimensional mask-programmable read-only memory (3D-MPROM) is a mask-ROM comprising a plurality of mask-ROM levels stacked above and coupled to a semiconductor substrate. Among all types of mask-ROM, 3D-MPROM has a very large capacity and a very low cost.

[0005] U.S. Pat. No. 5,835,396, issued to Zhang on Nov. 10, 1998, and U.S. Pat. No. 6,624,485, issued to Johnson on Sep. 23, 2003, disclose examples of 3D-MPROM. FIG. 1 illustrates a typical 3D-MPROM. It comprises a semiconductor substrate $0s$ and a 3D-MPROM stack 0. The semiconductor substrate $0s$ comprises transistors, which form the peripheral circuit for 3D-MPROM. The 3D-MPROM stack 0 is stacked above the substrate $0s$. In this example, it comprises two memory levels: 100 and 200; and the memory level 200 is stacked above the memory level 100. Each memory level (e.g. 100) comprises a plurality of address lines (e.g. $20a$, $20b$, $30a$ . . .) and memory cells (e.g. $1aa$, $1ab$ . . .). Contact vias (e.g. $30av$, $30av'$) couple memory levels (e.g. 100, 200) to the substrate $0s$.

[0006] Most 3D-MPROM's disclosed in prior arts are binary, i.e. memory cells have two states: '1' and '0': state '1' conducts current, whereas state '0' does not. Each binary cell can store one bit of data.

[0007] As illustrated in FIG. 2A, a '1' 3D-MPROM cell $1aa$ comprises an upper address line $20a$, a ROM-layer $3a$ and a lower address line $30a$. The ROM-layer $3a$ comprises a quasi-conduction layer 5, which is a non-linear resistor and conducts more current in one direction than in the other direction. The quasi-conduction layer 5 is generally a diode. Here, it is a p-i-n diode, including a p-layer 12, an i-layer 14 and an n-layer 16. It could also be other diodes, such as p-n diode or Schottky diode. Because there is a contact 18 in the insulating dielectric 11, a read current can be sensed in the lower address line $30a$ when a read voltage is applied to the upper address line $20a$. This corresponds to the state '1'.

[0008] As illustrated in FIG. 2B, a '0' 3D-MPROM cell $1ba$ comprises an upper address line $20b$, a ROM-layer $3b$ and a lower address line $30a$. The ROM-layer $3b$ further comprises an insulating dielectric 11. Because there is no contact in the insulating dielectric 11, no read current can be sensed in the lower address line $30a$ when a read voltage is applied to the upper address line $20b$. This corresponds to the state '0'.

[0009] Besides binary, 3D-MPROM can be N-ary (N is a positive integer and N>2), i.e. memory cells have N states and cells in different states have different current-voltage (I-V) characteristics. Each N-ary cell can store b bits of data, namely b-bit-per-cell (bpc). Here, $b=\log_2(N)$ and b can be an integer or a non-integer. U.S. Pat. No. 7,633,128, issued to Zhang on Dec. 15, 2009, and U.S. patent application Ser. No. 12/477,912, filed by Zhang on Jun. 4, 2009, disclose examples of N-ary 3D-MPROM. They include geometry-defined N-ary 3D-MPROM and junction-defined N-ary 3D-MPROM.

[0010] In a geometry-defined N-ary 3D-MPROM, cells in different states have different structures, e.g. different cell geometries. As illustrated in FIG. 2C, a geometry-defined cell $1ca$ comprises an upper address line $20c$, a ROM-layer $3c$ and a lower address line $30a$. The ROM-layer $3c$ further comprises an insulating layer 11, a partial contact $18'$ and a quasi-conduction layer 5. Compared with FIG. 2A, the partial contact $18'$ in the insulating layer 11 only partially couples the upper address line $20c$ to the quasi-conduction layer 25. Accordingly, memory cell $1ca$ has a different I-V characteristic than memory cell $1aa$.

[0011] In a junction-defined N-ary 3D-MPROM, cells in different states have different junctions, e.g. different doping profiles. As illustrated in FIG. 2D, a junction-defined cell $1da$ comprises an upper address line $20d$, a ROM-layer $3d$ and a lower address line $30a$. The ROM-layer $3d$ has a similar structure as the ROM-layer $3a$ in cell $1aa$ (FIG. 2A), but its diode $5'$ has a different doping profile than diode 5. This can be implemented by an extra implant. Accordingly, memory cell $1da$ has a different I-V characteristic than cell $1aa$.

[0012] The present invention makes further improvements to N-ary 3D-MPROM. By increasing the range of modulation for the cell I-V characteristics (e.g. to ~4.5V or more), large bit-per-cell (e.g. 4-bpc) can be achieved. Accordingly, the present invention discloses a large bit-per-cell 3D-MPROM ($3D\text{-}MPROM_B$).

Objects and Advantages

[0013] It is a principle object of the present invention to increase the storage capacity of 3D-MPROM.

[0014] It is a further object of the present invention to lower the manufacturing cost of 3D-MPROM.

[0015] It is a further object of the present invention to achieve large bit-per-cell (e.g. 4-bpc or more) for 3D-MPROM.

[0016] In accordance with these and other objects of the present invention, a large bit-per-cell 3D-MPROM (3D-$MPROM_B$) is disclosed.

SUMMARY OF THE INVENTION

[0017] An improved N-ary (N>2) three-dimensional mask-programmable read-only memory (3D-MPROM), having large bit-per-cell (e.g. 4-bpc or more), is disclosed. The large bit-per-cell 3D-MPROM ($3D\text{-}MPROM_B$) increases the range of modulation for the cell I-V characteristics by adding resistive layer(s) and/or resistive element(s) to the memory cells. Accordingly, $3D\text{-}MPROM_B$ can be categorized into $3D\text{-}MPROM_B$ with resistive layer ($3D\text{-}MPROM_{RL}$) and $3D\text{-}MPROM_B$ with resistive element ($3D\text{-}MPROM_{RE}$).

[0018] A $3D\text{-}MPROM_{RL}$ comprises a first cell and a second cell. The first cell is a base cell, which has the smallest threshold voltage among all states. Here, threshold voltage (V_T) refers to the voltage on a memory cell that generates a threshold current (I_T) through the memory cell. The second cell has a larger V_T than the base cell. Its memory cell comprises at least one resistive layer more than the base cell. The resistive layer could comprise a semiconductor layer (e.g. 45 nm amorphous silicon), or, a thin dielectric layer (e.g. 5 nm silicon oxide, or 9 nm silicon nitride). It preferably has a resistance comparable to or larger than the base cell at I_T.

Resistive layer(s) can significantly modulate V_T. As a result, memory cells have a wide total V_T window (TVW) and therefore, large bit-per-cell.

[0019] A 3D-MPROM$_{RE}$ comprises a first cell and a second cell. The first cell is a base cell; the second cell has a larger V_T than the base cell. Its quasi-conduction layer comprises more concentration of at least one resistive element than the quasi-conduction layer of the base cell. The resistive element (e.g. oxygen, nitrogen or carbon), when introduced into the semiconductor material (e.g. silicon) of the quasi-conductor layer (e.g. p-i-n diode) of the base cell, can increase its resistivity. In addition, more concentration of the resistive element leads to a higher resistivity. Resistive element(s) can also significantly modulate V_T. As a result, memory cells have a wide TVW and therefore, large bit-per-cell.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 is a cross-sectional view of a three-dimensional mask-programmable read-only memory (3D-MPROM);

[0021] FIGS. 2A-2D are cross-sectional views of prior-art binary '1' 3D-MPROM cell, binary '0' 3D-MPROM cell, geometry-defined N-ary 3D-MPROM cell, and junction-defined N-ary 3D-MPROM cell;

[0022] FIG. 3 illustrates the current-voltage (I-V) curves for 16 states of a preferred 4-bit-per-cell (bpc) 3D-MPROM$_B$ (b=4, N=16);

[0023] FIGS. 4A-4D are cross-sectional views of several preferred 3D-MPROM$_B$ cells with resistive layer (3D-MPROM$_{RL}$);

[0024] FIG. 5 compares the I-V curves for a base cell, a resistive layer, and a 3D-MPROM$_{RL}$ cell;

[0025] FIGS. 6A-6D are the cross-sectional views of four preferred resistive layers;

[0026] FIG. 7 is a plan view of a preferred resistive-layer mask for 3D-MPROM$_{RL}$, as well as the relative placement of the resistive layer and address lines during manufacturing;

[0027] FIGS. 8A-8C are the cross-sectional views along line AA' of FIG. 7 showing several manufacturing steps of the preferred 3D-MPROM$_{RL}$ cell;

[0028] FIGS. 9A-9C are cross-sectional view of three preferred 3D-MPROM$_B$ cells with partial resistive layer (3D-MPROM$_{PRL}$);

[0029] FIG. 10 is a cross-sectional view of a preferred 3D-MPROM$_B$ cell with resistive element (3D-MPROM$_{RE}$);

[0030] FIG. 11 compares the I-V curves for a Si-based diode, a SiO$_x$(x<2)-based diode, and a SiO$_2$ layer;

[0031] FIGS. 12A-12B illustrate several manufacturing steps of the preferred 3D-MPROM$_{RE}$ cell;

[0032] FIGS. 13A-13C are the cross-sectional views of three preferred 2-bpc 3D-MPROM$_B$'s (b=2, N=4);

[0033] FIG. 14A is a circuit diagram of the preferred 2-bpc 3D-MPROM$_B$; FIG. 14B is the timing diagram of a read operation for the preferred 2-bpc 3D-MPROM$_B$;

[0034] FIG. 15A is a table listing the configuration for 16 states in a preferred 4-bpc 3D-MPROM$_B$ (b=4, N=16); FIG. 15B is a cross-sectional view of the preferred 4-bpc 3D-MPROM$_B$.

[0035] It should be noted that all the drawings except FIG. 15A are schematic and not drawn to scale. Relative dimensions and proportions of parts of the device structures in the figures have been shown exaggerated or reduced in size for the sake of clarity and convenience in the drawings. The same reference symbols are generally used to refer to corresponding or similar features in the different embodiments.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0036] Those of ordinary skills in the art will realize that the following description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons from an examination of the within disclosure.

[0037] The present invention discloses a large bit-per-cell 3D-MPROM (3D-MPROM$_B$). Each 3D-MPROM$_B$ cell can store a large number of bits (e.g. 4 bits or more). FIG. 3 illustrates the cell current-voltage (I-V) curves for 16 states of a 4-bit-per-cell (bpc) 3D-MPROM$_B$ (b=4, N=16). The cell I-V curves 410-425 correspond to states '0'-'f', respectively. Note the vertical axis is on a log scale. A memory cell is considered "turned-on" when its current exceeds a threshold current (I_T). The cell voltage at I_T is referred to as threshold voltage (V_T). For example, V_T for state '0' is V_{T0}; V_T for state 'f' is V_{Tf}. In this disclosure, the assignment of state values follows this convention: the cell with a smaller V_T is assigned a lower state value, e.g. cells with the smallest V_T is assigned state '0'; cells with the second smallest V_T is assigned state '1'; . . . . It should be apparent to those skilled in the art that other conventions may also be followed.

[0038] To tolerate manufacturing variations and read tolerances, ΔV_T of the neighboring states generally needs to be ~0.3V or more. Hence, the total V_T window (TVW), which is the difference between the largest V_T (i.e. V_{Tf}) and the smallest V_T (i.e. V_{T0}), generally needs to be ~4.5V or more. To realize this wide TVW, the present invention suggests adding resistive layer(s) and/or resistive element(s) to the memory cells. Accordingly, 3D-MPROM$_B$ can be categorized into 3D-MPROM$_B$ with resistive layer (3D-MPROM$_{RL}$) and 3D-MPROM$_B$ with resistive element (3D-MPROM$_{RE}$).

[0039] Examples of 3D-MPROM$_{RL}$ are illustrated in FIGS. 4A-9C. Among them, FIGS. 4A-4D illustrate several preferred 3D-MPROM$_{RL}$ cells. Referring now to FIG. 4A, a typical base cell $1za$ is illustrated. The base cell $1za$ has the smallest V_T among all states, i.e. V_{T0}. It comprises a plurality of layers, including an upper address line 20z, the ROM-layer 3z and a lower address line 30a. These layers are collectively referred to as base layers. Among them, the address lines 20z, 30a comprise conductive material(s) such as highly-doped polysilicon, tungsten, titanium tungsten, titanium nitride, copper, or the like; the ROM-layer 3z only comprises a quasi-conduction layer 25, which is a non-linear resistor and conducts more current in one direction than in the other direction. The quasi-conduction layer 25 is generally a diode. Here, it is a p-i-n diode, including a p-layer 22, an i-layer 24 and an p-layer 26. More details on quasi-conduction layer are disclosed in U.S. Pat. No. 5,835,396.

[0040] Referring now to FIG. 4B, a first preferred 3D-MPROM$_{RL}$ cell $1ea$ is illustrated. It comprises an upper address line 20e, a ROM-layer 3e and a lower address line 30a. The address lines 20e, 30a comprise conductive material(s). The ROM-layer 3e comprises a resistive layer 23 in addition to the quasi-conduction layer 25 (including p-layer 22, i-layer 24 and n-layer 26). In this preferred embodiment, the resistive layer 23 is formed above the quasi-conduction layer 25. It preferably has a resistance comparable to or larger than the quasi-conduction layer 25 at I_T. Because the base cell $1za$

3

and the quasi-conduction layer **25** have the same I-V characteristics, the resistive layer **23** preferably has a resistance comparable to or larger than the base cell **1**za at I_T.

[0041] FIG. 4C illustrates a second preferred 3D-MPROM$_{RL}$ cell **1**fa. It comprises an upper address line **20**f, a ROM-layer **3**f and a lower address line **30**a. The address lines **20**f, **30**a comprise conductive material(s). The ROM-layer **3**f comprises a resistive layer **23** in addition to the quasi-conduction layer **25** (including p-layer **22**, i-layer **24** and n-layer **26**). In this preferred embodiment, the resistive layer **23** is formed in the quasi-conduction layer **25**, i.e. between the uppermost p-layer **22** and the middle i-layer **24**. It preferably has a resistance comparable to or larger than the base cell **1**za at I_T.

[0042] FIG. 4D illustrates a third preferred 3D-MPROM$_{RL}$ cell **1**ga. It comprises an upper address line **20**g, a ROM-layer **3**g and a lower address line **30**a. The address lines **20**g, **30**a comprise conductive material(s). The ROM-layer **3**g comprises a resistive layer **23** in addition to the quasi-conduction layer **25** (including p-layer **22**, i-layer **24** and n-layer **26**). In this preferred embodiment, the resistive layer **23** is formed below the quasi-conduction layer **25**. It preferably has a resistance comparable to or larger than the base cell **1**za at I_T.

[0043] To form a 3-D device structure, i.e. to stack multiple memory levels one above another, the 3D-MPROM$_{RL}$ cell (**1**ea/**1**fa/**1**ga, "/" here means "or") and the base cell **1**za on a same memory level should provide a good foundation upon which the next memory level can be built. In other words, their upper address lines (**20**e/**20**f/**20**g, **20**z) are preferably planarized (e.g. by chemical-mechanical polishing, or CMP). According, the thickness T_R of the resistive layer **23** should satisfy the following requirements: 1) in the preferred embodiments of FIGS. 4C-4D, if the ROM-layers (**3**f/**3**g, **3**z) are to be planarized, then T_R should be less than the thickness T_U of the uppermost layer **22** in the quasi-conduction layer **25** of the base cell **1**za, 2) in the preferred embodiments of FIGS. 4B-4D, if the ROM-layers (**3**e/**3**f/**3**g, **3**z) are not planarized, then T_R should be less than the thickness T_R of the upper address line **20**z of the base cell **1**za.

[0044] FIG. 5 compares the I-V curves **430**, **431**, **432** for a base cell **1**za, a resistive layer **23** and a 3D-MPROM$_{RL}$ cell lea. Because the resistive layer **23** and quasi-conduction layer **25** are connected in series in the 3D-MPROM$_{RL}$ cell lea, the I-V curve **432** for the 3D-MPROM$_{RL}$ cell **1**ea is shifted from the I-V curve **430** for the quasi-conduction layer **25** (or, the base cell **1**za) by an amount indicated by the I-V curve **431** of the resistive layer **23**. Hence, V_T of the 3D-MPROM$_{RL}$ cell **1**ea is the sum of V_{T0} of the base cell **1**za and the voltage V_r on the resistive layer **23**, i.e. $V_T = V_{T0} + V_r$.

[0045] FIGS. 6A-6D are the cross-sectional views of several preferred resistive layers. FIG. 6A illustrates a preferred resistive layer **23**. It comprises only a core resistive layer **502**. The core resistive layer **502** has an exponential I-V characteristic as shown in FIG. 5. It comprises a semiconductor layer, or a thin dielectric layer. The semiconductor layer could comprise silicon, carbon, germanium, silicon carbide, silicon germanium or others. It preferably takes a non-single-crystalline form, e.g. amorphous, microcrystalline, or polycrystalline. One example of the semiconductor layer is 45 nm amorphous silicon, which can shift V_T by ~4.5V or more. The thin dielectric layer could comprise silicon oxide, silicon nitride, or other protective ceramics (referring to U.S. Pat. No. 5,838,530, issued to Zhang, on Nov. 17, 1998). Although it is traditionally considered as an insulator, dielectric has an

exponential I-V characteristic when used in thin layer and therefore, is suitable for the resistive layer. Examples of the thin dielectric layer are 5 nm silicon oxide and 9 nm silicon nitride, either of which can shift V_T by ~4.5V or more.

[0046] Referring now to FIGS. 6B-6D, three alternate preferred resistive layers **23** are illustrated. In FIG. 6B, a barrier layer **501** is formed above the core resistive layer **502**; in FIG. 6C, a barrier layer **503** is formed below the core resistive layer **502**; in FIG. 6D, barrier layers **501**, **503** are formed above and below the core resistive layer **502**, respectively. The barrier layer provides a better interface for the resistive layer **23** and can also be used as etch-stop layer. It comprises conductive material(s) such as highly-doped polysilicon, tungsten, titanium tungsten, titanium nitride, copper, or the like.

[0047] FIG. 7 is a plan view of a preferred resistive-layer mask for 3D-MPROM$_{RL}$. It also illustrates the relative placement of the resistive-layer patterns **7**x, **7**y with respect to the upper address-line patterns **20**a, **20**b, **20**e and the lower address-line patterns **30**a, **30**b. Compared with the upper address-line patterns whose critical dimension is 1F, the resistive-layer pattern **7**x could have a large critical dimension, i.e. nF(n>1, preferably ~2). Moreover, adjacent resistive-layer patterns (e.g. **7**ab, **7**bb) can be merged into a larger single resistive-layer pattern **7**y. Accordingly, the resistive-layer mask is an nF-mask (n>1, preferably ~2). For example, a 20 nm-node 3D-MPROM can use a 40 nm-node resistive-layer mask.

[0048] FIGS. 8A-8C illustrate several manufacturing steps of the preferred 3D-MPROM$_{RL}$ cell **1**ea of FIG. 4B. First of all, the lower address-line **30**a is formed. This is followed by the deposition of the quasi-conduction layer **25**. The quasi-conduction layer **25** is then etched to form a plurality of individual pillars (FIG. 8A). Secondly, intra-layer dielectric **27** is deposited and planarized. Then the resistive layer **23** is deposited and etched using the resistive-layer mask of FIG. 7. Note that its dimension is nF(n>1, preferably ~2) (FIG. 8B). Finally, the upper address-line layer **20**e is deposited (FIG. 8C) and etched using the intra-diode dielectric **27** as etch stop. This step will remove a portion of the resistive layer **23**. As a result, the resistive layer **23** is self-aligned with the upper address line **20**e (FIG. 4B). It should be apparent to those skilled in the art the preferred MPROM$_{RL}$ cells **1**fa, **1**ga in FIGS. 4C-4D can be manufactured in a similar manner.

[0049] From the above description, the final shape of the resistive layer **23** is determined by the overlapping portion between the resistive-layer pattern **7**x and the upper-address-line pattern **20**e. Hence, this self-aligned process relaxes the edge-control requirements on the resistive-layer patterns. In other words, a 20 nm-node 3D-MPROM$_{RL}$ can not only use a 40 nm resistive-layer mask, but also this mask can be a non-high-precision mask. Adding the fact that this self-aligned process also relaxes the alignment requirements between the upper address line and the resistive layer, the total lithographic cost for 3D-MPROM$_{RL}$ is relatively low.

[0050] 3D-MPROM$_{RL}$ can be combined with geometry-defined N-ary 3D-MPROM (referring to U.S. Pat. No. 7,633, 128 and U.S. Pat. App. Ser. No. 12/477,912). By varying the geometry of the resistive layer, more states can be created. Accordingly, the present invention discloses a 3D-MPROM with partial resistive layer (3D-MPROM$_{PRL}$). FIGS. 9A-9C illustrate three preferred 3D-MPROM$_{PRL}$ cells.

[0051] Referring now to FIG. 9A, a preferred 3D-MPROM$_{PRL}$ cell **1**ha is illustrated. It comprises an upper address line **20**h, a ROM-layer **3**h and a lower address line

30a. The ROM-layer **3**h further comprises a blocking dielectric **29**, a partial resistive layer **23'** and a quasi-conduction layer **25**. The blocking dielectric **29** and the partial resistive layer **23'** are formed above the quasi-conduction layer **25**. The partial resistive layer **23'** only partially couples the upper address line **20**h to the quasi-conduction layer **25**. Because the partial resistive layer **23'** has a different geometry (i.e. smaller) than the resistive layer **23** of FIG. **4**B, cell **1**ha has a larger resistance than cell **1**ea of FIG. **4**B. To be more specific, the contact area **21** between the partial resistive layer **23'** and the quasi-conduction layer **25** is smaller than the cross-sectional area of the quasi-conduction layer **25**; whereas in FIG. **4**B, the contact area between the resistive layer **23** and quasi-conduction layer **25** is comparable to the cross-sectional area of the quasi-conduction layer **25**. By varying the width f of the contact area **21**, more resistance values can be obtained and therefore, more states can be created. Because f is defined by resistive-layer patterns, a single resistive-layer mask can program more than one bit of data into each cell. Similarly, the partial resistive layer **23'** preferably has a resistance comparable to or larger than the base cell **1**za at I_T. It should be apparent to those skilled in the art that all concepts disclosed in U.S. Pat. No. 7,633,128 and U.S. Pat. App. Ser. No. 12/477, 912 can be used for 3D-MPROM$_{PRL}$.

[0052] Referring now to FIGS. **9**B-**9**C, two alternate preferred 3D-MPROM$_{PRL}$ cells **1**ia, **1**ja are illustrated. They are similar to the 3D-MPROM$_{PRL}$ cell **1**ha of FIG. **9**A. The only difference is that their partial resistive layers **23'** are either in or below the quasi-conduction layer **25**. Similarly, by adjusting f, more resistance values can be obtained and therefore, more states can be created. A single resistive-layer mask can program more than one bit of data into each cell.

[0053] In a 3D-MPROM with resistive element (3D-MPROM$_{RE}$), the quasi-conduction layer of the memory cell comprises more concentration of at least one resistive element than the quasi-conduction layer of the base cell. Examples of 3D-MPROM$_{RE}$ are illustrated in FIGS. **10**-**12**B. FIG. **10** illustrates a preferred 3D-MPROM$_{RE}$ cell **1**ka. A base cell **1**za is drawn to the left for comparison. The preferred 3D-MPROM$_{RE}$ cell **1**ka comprises an upper address line **20**k, a ROM-layer **3**k and a lower address line **30**a. The ROM-layer **3**k comprises a quasi-conduction layer **25'**. Although the quasi-conduction layer **25'** is still a p-i-n diode **25'**, it comprises more concentration of at least one resistive element than diode **25** in the base cell **1**za. The resistive element (e.g. oxygen, nitrogen, or carbon), when introduced into the semiconductor material (e.g. silicon) of the quasi-conductor layer (e.g. p-i-n diode) of the base cell **1**za, can increase its resistivity. In addition, more concentration of the resistive element leads to a higher resistivity. This is opposite to the doping element (e.g. B, P, As) commonly used in semiconductor. The doping element decreases the semiconductor resistivity and more concentration of the doping element leads to lower resistivity.

[0054] FIG. **11** compares the I-V curves **440**, **441**, **442** for a Si-based diode (i.e. base cell), a SiO$_x$ (x<2)-based diode (i.e. 3D-MPROM$_{RE}$ cell), and a SiO$_2$ layer. Apparently, the I-V curve **441** for the SiO$_x$ (x<2)-based diode should be within the range defined by the I-V curve **440** for the silicon-based diode and the I-V curve **442** for the SiO$_2$ layer. This is because the SiO$_2$ layer can be considered as an extreme case of SiO$_x$ (x<2)-based diode, i.e. when the oxygen concentration becomes so high that SiO$_x$ (x<2) becomes SiO$_2$. Accordingly, V_T of the SiO$_x$ (x<2)-based diode should be between V_{T0} of

the silicon-based diode and V_{Tx} of the SiO$_2$ layer, i.e. $V_{T0}<V_T<V_{Tx}$. Because V_{Tx} could be very large, V_T of the 3D-MPROM$_{RE}$ cell can be modulated in a wide range. Similar to oxygen, nitrogen can modulate V_T in a wide range. Alternatively, carbon can also be used to modulate V_T. This is because carbon, when incorporated into silicon, forms SiC$_z$ (z<1), which has a larger bandgap than silicon. In general, the larger the bandgap of the semiconductor material, a larger V_T a diode has.

[0055] FIGS. **12**A-**12**B illustrate two manufacturing steps for the preferred 3D-MPROM$_{RE}$ cell **1**ka. First, the lower address-line **30**a and the quasi-conduction layer **25** are formed. Then a resistive-element mask is used to form an opening **28**o in the photoresist **28**. The resistive-element mask is similar to the resistive-layer mask of FIG. **7**. They are both nF-masks (n>1, preferably ~2). Here, the opening **28**o has a width of nF(n>1, preferably ~2), larger than the upper address line **20**k. This is followed by an ion implantation of resistive element (e.g. oxygen, nitrogen, carbon) (FIG. **12**A). This ion-implantation step increases the concentration of the resistive element under the opening **280**. After ion implantation, the photoresist **28** is removed. Then the quasi-conduction layer **25** is patterned and etched to form a pillar **25'**. The rest of manufacturing steps follows the steps described in FIGS. **8**B-**8**C for the base cell **1**za. Similar to 3D-MPROM$_{RL}$, a 20 nm-node 3D-MPROM$_{RE}$ can not only use a 40 nm resistive-element mask, but also this mask can be a non-high-precision mask. Overall, the data-programming cost for 3D-MPROM$_B$ is far lower than most people would like to believe.

[0056] 3D-MPROM$_{RL}$ (FIGS. **4**B-**4**D, FIGS. **9**A-**9**C) and 3D-MPROM$_{RE}$ (FIG. **10**) can be combined with geometry-defined N-ary 3D-MPROM and junction-defined N-ary 3D-MPROM (referring to U.S. Pat. No. 7,633,128 and U.S. Pat. App. Ser. No. 12/477,912) to further increase the number of bits stored in each cell. FIGS. **13**A-**14**B disclose several preferred 2-bpc 3D-MPROM$_B$ (b=2, N=4). FIGS. **15**A-**15**B disclose a preferred 4-bpc 3D-MPROM$_B$ (b=4, N=16).

[0057] FIGS. **13**A-**13**C illustrate three preferred 2-bpc 3D-MPROM$_B$'s. Referring now to FIG. **13**A, a first preferred 2-bpc 3D-MPROM$_B$ is illustrated. It combines 3D-MPROM$_{RL}$ of FIG. **4**B and 3D-MPROM$_{RE}$ of FIG. **10**. The four cells **1**za, **1**ma, **1**na, **1**oa represent four different states. The base cell **1**za comprises neither the resistive layer nor the resistive element. Cell **1**ma comprises at least one resistive element in the quasi-conduction layer **25'**. Cell **1**na comprises a resistive layer **23** above the quasi-conduction layer **25**. Cell **1**oa comprises both resistive element and resistive layer. Alternatively, cell **1**ma may have a different doping profile than the base cell **1**za. Apparently, this preferred embodiment needs two masks (i.e. a resistive-layer mask and a resistive-element mask) to program two bits of data into each cell.

[0058] Referring now to FIG. **13**B, a second preferred 2-bpc 3D-MPROM$_B$ is illustrated. It combines two preferred embodiments of 3D-MPROM$_{RL}$ in FIG. **4**B. Four cells **1**za, **1**pa, **1**qa, **1**ra represent four different states. For example, the resistive layer **23**a in cell **1**pa comprises 15 nm amorphous silicon; the resistive layer **23**b in cell **1**qa comprises 30 nm amorphous silicon; the resistive layer in cell **1**ra comprises both resistive layers **23**a, **23**b, i.e. 45 nm amorphous silicon. Alternatively, the resistive layer **23**a in cell **1**pa comprises 3 nm silicon nitride, the resistive layer **23**b in cell **1**qa comprises 6 nm silicon nitride; and the resistive layer in cell **1**ra comprises 9 nm silicon nitride. Similarly, this preferred

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embodiment needs two masks (i.e. two resistive-layer masks) to program two bits of data into each cell.

[0059] Referring now to FIG. 13C, a third preferred 2-bpc 3D-MPROM$_B$ is illustrated. It combines two preferred embodiments of 3D-MPROM$_{RL}$ in FIGS. 4B and 4D. Four cells 1za, 1sa, 1ta, 1ua represent four different states. The resistive layer 23c in cell 1sa is formed above the quasi-conduction layer 25; the resistive layer 23d in cell 1ta is formed below the quasi-conduction layer 25; and cell 1ua comprises two resistive layers 23c, 23d, with resistive layer 23c above the quasi-conduction layer 25 and resistive layer 23d below the quasi-conduction layer 25. Similarly, this preferred embodiment needs two masks (i.e. two resistive-layer masks) to program two bits of data into each cell.

[0060] The read operation of 3D-MPROM$_B$ involves application of a sequence of read voltages with successively increasing magnitude. Once the read voltage is large enough to stimulate a read current for a memory cell, an output signal is generated and the corresponding read voltage indicates the state of the memory cell. FIGS. 14A-14B describe the peripheral circuit and read operation of the preferred 2-bpc 3D-MPROM$_B$.

[0061] FIG. 14A is a circuit diagram for the preferred 2-bpc 3D-MPROM$_B$. It comprises two blocks: a memory stack 0 and a peripheral circuit 0K. The memory stack 0 comprises a data group 30DT (including data cells 1ca-1cz and data bit lines 30a-30z) and a dummy group 32DY (including dummy cells 1c0-1c3 and dummy bit lines 32a-32d). The data cells store data, while the dummy cells provide a reference signal during read. Both data cells and dummy cells have four states '0'-'3', e.g. both data cell 1ca and dummy cell 1c1 are in state '1', as indicated by the numbers in the parentheses. It is advantageous that, for the same state, the dummy cells use the same structure and material as the data cells, because no extra manufacturing cost will incur for the dummy cells.

[0062] The peripheral circuit 0K is formed in the substrate 0s and coupled to the memory stack 0 through contact vias. It comprises a word-line voltage generation circuit 50, a row decoder 52, a column decoder 54, a reference-signal generation circuit 56, a sense amplifier 58, a data buffer 60 and an N-ary-to-binary converter 62. The word-line voltage generation circuit 50 generates a read voltage associated with the read phase. The row decoder 52 supply this read voltage to a word line (e.g. 20c) based on row address 52A. The column decoder 54 couples a bit line to a first input 51 of the sense amplifier 58 based on column address 54A. The reference-signal generation circuit 56 generates a reference voltage 53 as a second input for the sense amplifier 58. It comprises a plurality of switch pairs (e.g. 56a'), each of which includes a pair of transistors sharing a gate signal (e.g. 56a).

[0063] FIG. 14B is a timing diagram of the read operation. Each read operation includes at least N−1 read phases. This preferred embodiment has 3 read phases: T0-T2. During each read phase, a read voltage is applied to a selected word line (e.g. 20c). Based on the cell states, different read currents flow though memory cells (1ca-1cz, 1c0-1c3). Accordingly, the bit-line voltages (30a-30z, 32a-32d) rise at different rates. At the end of each read phase, all bit-line voltages in the data group 30DT are read out one-by-one. If the voltage on a bit line (e.g. 30a) is larger than a trigger voltage V_x, the output 55 becomes high. In the mean time, the sense amplifier 58 sets the voltage on the corresponding bit line (30a) to a high voltage V_H in the remaining read phases. This can prevent diode in the associated cell (1ca) from being damaged when

higher read voltages are applied during the remaining read phases. More details on each read phase are described below.

[0064] A) During the first read phase T0, a first read voltage V_{R0} is applied to the word line 20c. Then the bit-line voltages (30a-30z, 32a-32d) rise at different rates based on the cell states. For state '0' (including cells 1ca, 1c0), the read voltage V_{R0} generates a large read current and the bit-line voltages (30a, 32a) rise fast; for state '1' (including cells 1cz, 1c1), the read voltage V_{R0} generates a small read current and the bit-line voltages (30z, 32b) stays almost flat . . . . In the mean time, only the gate signal 56a in the reference-signal generation circuit 56 is asserted. The switch pair 56a' is turned on and the dummy bit lines 32a, 32b are coupled together. As a result, the reference voltage 53 is effectively the average bit-line voltage for states '0' and '1'. At the end of T0, the bit-line voltages on all data bit lines (30a-30z) in the data group 30DT are compared one-by-one with the reference voltage 53 at the sense amplifier 58. The outputs 55 are sent to the data buffer 60.

[0065] B) During the second read phase T1, a second read voltage V_{R1} is applied to the word line 20c. For state '0' (including cells 1ca, 1c0), the bit-line voltages (30a, 32a) are already set to V_H during T0; for state '1' (including cells 1cz, 1c1), the read voltage V_{R1} generates a large read current and the bit-line voltages (30z, 32b) rise fast; for state '2' (including cells 1cb, 1c2), the read voltage V_{R1} generates a small read current and the bit-line voltages (30b 32c) stays almost flat . . . . In the mean time, only the gate signal 56b in the reference-signal generation circuit 56 is asserted and the reference voltage 53 is effectively the average bit-line voltage for states '1' and '2'. At the end of T1, the bit-line voltages on all data bit lines (30a-30z) are read out one-by-one and the outputs 55 are sent to the data buffer 60.

[0066] C) During the third read phase T2, a third read voltage V_{R2} is applied to the word line 20c. For states '0' and '1' (including cells 1ca, 1cz, 1c0, 1c1), the bit-line voltages (30a, 30z, 32a, 32b) are already set to V_H during T0 and T1; for state '2' (including cells 1cb, 1c2), the read voltage V_{R2} generates a large read current and the bit-line voltages (30b, 32c) rise fast . . . . In the mean time, only the gate signal 56c in the reference-signal generation circuit 56 is asserted and the reference voltage 53 is effectively the average bit-line voltage for states '2' and '3'. At the end of T2, the bit-line voltages on all data bit lines (30a-30z) are read out one-by-one and the outputs 55 are sent to the data buffer 60.

[0067] D) At the end of the read operation, all data stored in the data buffer 60 are converted into binary data by the N-ary-to-binary converter 62. Hence, the 4-ary data stored at cells 1ca-1cz are read out.

[0068] FIGS. 15A-15B illustrate a preferred 4-bpc 3D-MPROM$_B$. FIG. 15A is a table listing the configuration for its 16 states and FIG. 15B is its cross-sectional view. It should be apparent to those skilled in the art that the peripheral circuit and read operation in FIGS. 14A-14B for the 2-bpc 3D-MPROM$_B$ can be applied to the 4-bpc 3D-MPROM$_B$.

[0069] Referring now to FIG. 15A, to achieve 4-bpc, memory cells are modified in four dimensions: upper resistive layer 23x, middle resistive layer 23y, lower resistive layer 23z and resistive element. "Yes" in the table means inclusion of resistive layer or resistive element; "No" means otherwise. Binary choices ("Yes" or "No") in each of these four dimensions lead to 16 different states. Here, these four dimensions

can be realized by four masks, i.e. upper resistive-layer mask, middle resistive-layer mask, lower resistive-layer mask, and resistive-element mask.

[0070] Referring now to FIG. 15B, the preferred 4-bpc 3D-MPROM$_B$ comprises a semiconductor substrate 0s and a 3D-MPROM$_B$ stack 0. The semiconductor substrate 0s comprises transistors 0T (including gate 0P), which, together with interconnects 0I, form a peripheral circuit 0X for the 3D-MPROM$_B$ stack 0. The 3D-MPROM$_B$ stack 0 is stacked above the substrate 0s. In this preferred embodiment, it comprises four memory levels: 100-400: the memory level 100 comprises word lines (80a-80h . . .), bit lines (90d . . .) and memory cells (1ad-1hd . . .); the memory level 200 is stacked above the memory level 100 and comprises word lines (80a-80h . . .), bit lines (90d^* . . .) and memory cells (1ad^* . . .); the memory level 300 is stacked above the memory level 200 and comprises word lines (80a'-80h' . . .), bit lines (90d' . . .) and memory cells (1a'd'-1h'd' . . .); the memory level 400 is stacked above the memory level 300 and comprises word lines (80a'-80h' . . .), bit lines (90d'' . . .) and memory cells (1a'd'' . . .). Contact vias (e.g. 90dv) couple memory levels (e.g. 100) to the substrate 0s.

[0071] Memory cells 1ad-1hd and 1a'd'-1h'd' in memory levels 100, 300 represent states '0'-'f', respectively (also referring to FIG. 15A). For example, memory cell 1ad represents state '0'. It is the base cell and comprises neither resistive layer nor resistive element; memory cell 1bd represents state '1' and comprises at least one resistive element in diode 25'; memory cell 1cd represents state '2' and comprises a lower resistive layer 23z; memory cell 1ed represents state '4' and comprises a middle resistive layer 23y; memory cell 1a'd' represents state '8' and comprises an upper resistive layer 23x; memory cell 1h'd' represents state 'f' and comprises the upper resistive layers 23x, the middle resistive layers 23y, the lower resistive layers 23z and at least one resistive element. For reason of simplicity, memory cells in memory levels 200, 400 and contact vias for memory levels 200-400 are not drawn in this figure.

[0072] The preferred embodiment in FIG. 15B incorporates several advanced features for 3D-MPROM, including hybrid-level 3D-MPROM (referring to U.S. Pat. App. Ser. No. 12/476,263, filed by Zhang on Jun. 2, 2009) and small-pitch 3D-MPROM (referring to U.S. Pat. App. Ser. No. 11/936,069, filed by Zhang on Nov. 6, 2007). Hybrid-level 3D-MPROM refers to a 3D-MPROM where a portion of memory levels (e.g. 100, 200) share one level of address lines (e.g. 80a-80h . . .), while another portion of memory levels (e.g. 200, 300) are separated by an inter-level dielectric 121. Small-pitch 3D-MPROM refers to a 3D-MPROM whose address-line pitch is smaller than the transistor-gate pitch. Further combining three-dimension memory module (referring to U.S. Pat. App. Ser. No. 12/043,128, filed by Zhang on Mar. 5, 2008), a x8x8x4 3D-MPROM$_B$ module (i.e. 8 3D-MPROM$_B$ chips stacked in a module, 8 memory levels and 4-bpc in a 3D-MPROM$_B$ chip) can reach a capacity of ~1 TB at the 20 nm node.

[0073] In FIGS. 13A-13C, only two masks are needed to program two bits of data into each cell and realize 2-bpc; in FIGS. 15A-15B, only four masks are needed to program four bits of data into each cell and realize 4-bpc. In fact, in 3D-MPROM$_B$, each mask can program one additional bit into memory cell. For example, five masks can realize 5-bpc; six masks can realize 6-bpc . . . . If 3D-MPROM$_{PRL}$ of FIGS. 9A-9C is used, even fewer masks are needed. This is more advantageous than the prior-art binary 3D-MPROM, which needs one more memory level for each additional bit.

[0074] While illustrative embodiments have been shown and described, it would be apparent to those skilled in the art that may more modifications than that have been mentioned above are possible without departing from the inventive concepts set forth therein. The invention, therefore, is not to be limited except in the spirit of the appended claims.

What is claimed is:

1. A three-dimensional mask-programmable read-only memory, comprising:

a semiconductor substrate including transistors;

a plurality of mask-programmable read-only memory levels stacked above and coupled to said substrate, each memory level comprising a plurality of memory cells including a first cell and a second cell; each memory cell comprising a quasi-conduction layer, said conduction layer conducting more current in one direction than in the other direction; said memory cells having N (N>2) states, cells in different states having different current-voltage characteristics;

wherein, said first cell has the smallest threshold voltage among all states; said second cell has a larger threshold voltage than said first cell, said second cell comprises at least a first resistive layer more than said first cell.

2. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer has a resistance comparable to or larger than said first cell at threshold current.

3. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer comprises at least one semiconductor layer.

4. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer comprises at least one dielectric layer.

5. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer is formed above said quasi-conduction layer.

6. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer is formed in said quasi-conduction layer.

7. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer is formed below said quasi-conduction layer.

8. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said quasi-conduction layer comprises two oppositely doped layers.

9. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer is thinner than the upper address line of said first cell.

10. The three-dimensional mask-programmable read-only memory according to claim 1, wherein said resistive layer is thinner than the uppermost layer in the quasi-conduction layer of said first cell.

11. The three-dimensional mask-programmable read-only memory according to claim 1, further comprising a third cell, wherein said third cell has a larger threshold voltage than said first cell, said third cell comprises at least a second resistive layer more than said first cell, and said first and second resistive layers have different geometries.

12. The three-dimensional mask-programmable read-only memory according to claim 1, wherein the contact area

between said resistive layer and said quasi-conduction layer is smaller than the cross-sectional area of said quasi-conduction layer.

13. The three-dimensional mask-programmable read-only memory according to claim **1**, further comprising a fourth cell and a fifth cell, wherein:

said fourth cell has a larger threshold voltage than said first cell, said fourth cell comprises at least a third resistive layer more than said first cell;

said fifth cell has a larger threshold voltage than said second and fourth cells, said fifth cell comprises said first and third resistive layers.

14. The three-dimensional mask-programmable read-only memory according to claim **1**, further comprising a sixth cell, wherein the quasi-conduction layer of said sixth cell has a different junction than the quasi-conduction layer of said first cell.

15. The three-dimensional mask-programmable read-only memory according to claim **14**, wherein the quasi-conduction layer of said sixth cell comprises more concentration of at least one resistive element than the quasi-conduction layer of said first cell.

16. A three-dimensional mask-programmable read-only memory, comprising:

a semiconductor substrate including transistors;

a plurality of mask-programmable read-only memory levels stacked above and coupled to said substrate, each memory level comprising a plurality of memory cells including a first cell and a second cell; each memory cell comprising a quasi-conduction layer, said conduction layer conducting more current in one direction than in the other direction; said memory cells having N (N>2) states, cells in different states having different current-voltage characteristics;

wherein, said first cell has the smallest threshold voltage among all states; said second cell has a larger threshold voltage than said first cell, and the quasi-conduction layer of said second cell comprises more concentration of at least one resistive element than the quasi-conduction layer of said first cell.

17. The three-dimensional mask-programmable read-only memory according to claim **16**, wherein the quasi-conduction layer of said first cell comprises a semiconductor material and said resistive element increases the resistivity of said semiconductor material.

18. The three-dimensional mask-programmable read-only memory according to claim **16**, wherein the quasi-conduction layer of said first cell comprises a semiconductor material and said resistive element increases the bandgap of said semiconductor material.

19. The three-dimensional mask-programmable read-only memory according to claim **16**, wherein said resistive element is selected from a group of elements consisting of oxygen, nitrogen and carbon.

20. The three-dimensional mask-programmable read-only memory according to claim **16**, further comprising a third cell, wherein the quasi-conduction layer of said third cell has a different doping profile than the quasi-conduction layer of said first cell.

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