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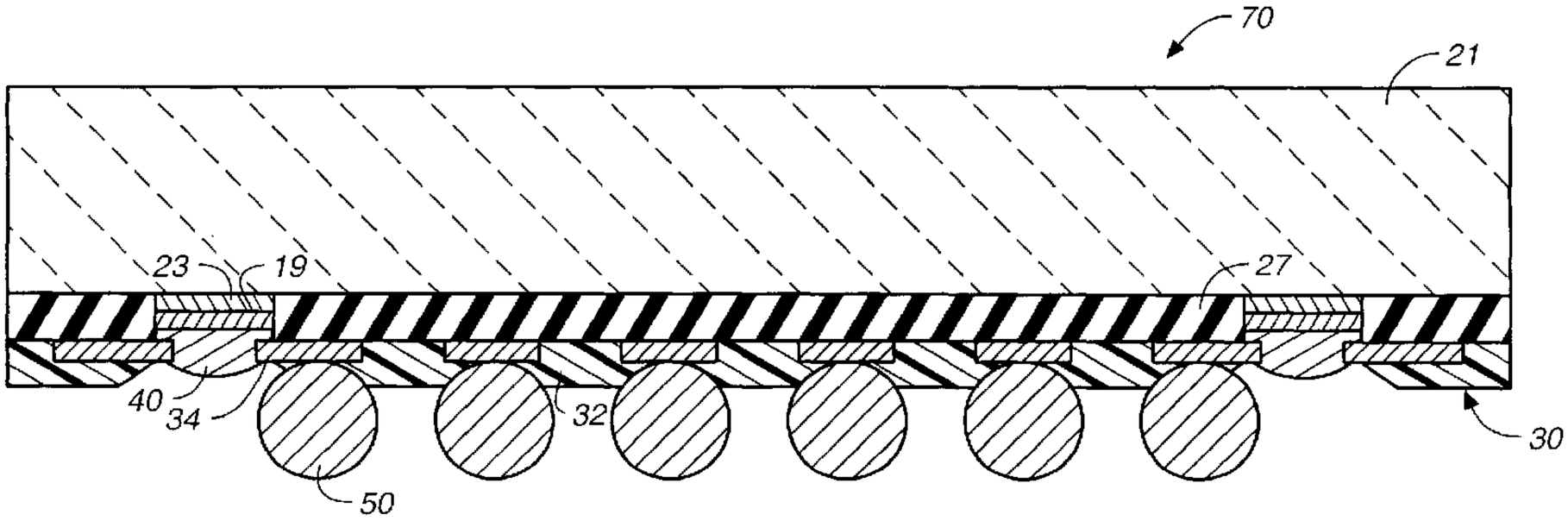
(54) Titre : BOITIER DE CIRCUIT INTEGRE FABRIQUE AU NIVEAU DE LA PLAQUETTE
(54) Title: INTEGRATED CIRCUIT PACKAGE FORMED AT A WAFER LEVEL



(57) Abrégé/Abstract:
An integrated circuit package (70) that is formed at the wafer level. The integrated circuit package (70) occupies a minimum amount of space on an end-use printed circuit board. A pre-fabricated interposer substrate (30), made of metal circuitry (34) and a dielectric base (32), has a plurality of metallized openings which are aligned with metallized wirebond pads (23) on the top surface of a silicon wafer (21). Solder (40), or conductive adhesive, is deposited through the metallized openings to form the electrical connection between the circuitry on the interposer layer (30) and the circuitry on the wafer (21). Solder balls (50) are then placed on the metal pad openings on the interposer substrate (30) and are reflowed to form a wafer-level BGA structure. The wafer-level BGA structure is then cut into individual BGA chip packages.

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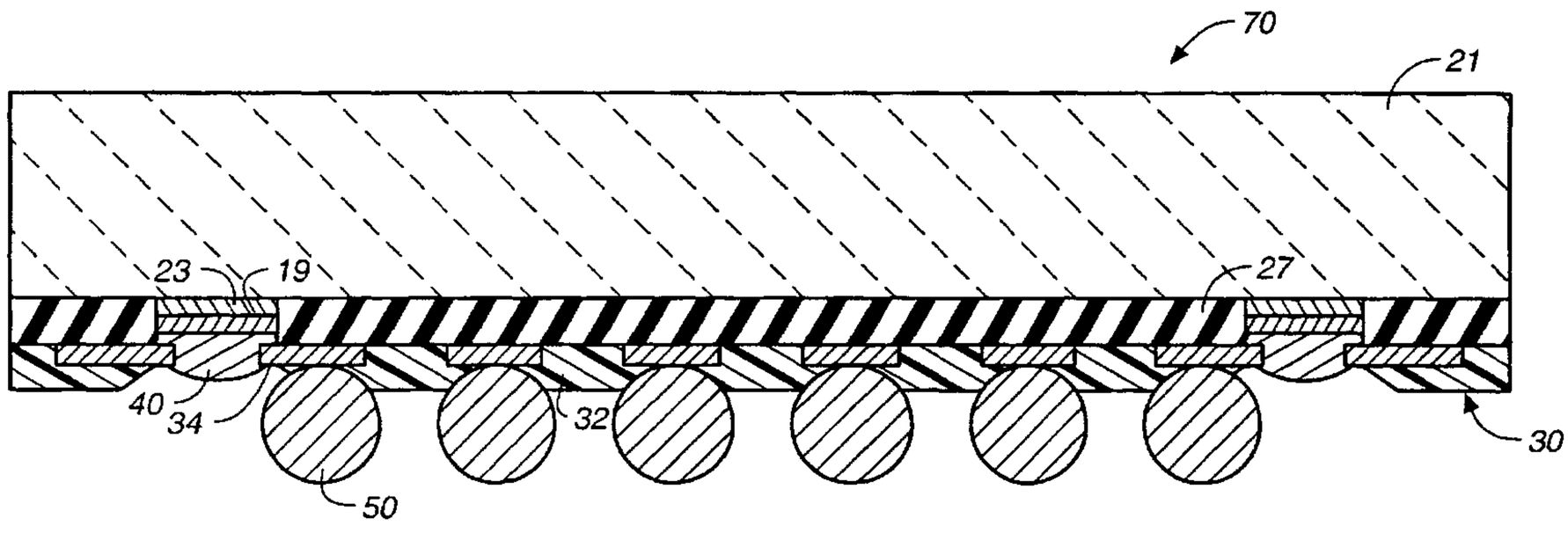
(54) Title: INTEGRATED CIRCUIT PACKAGE FORMED AT A WAFER LEVEL



(57) Abstract: An integrated circuit package (70) that is formed at the wafer level. The integrated circuit package (70) occupies a minimum amount of space on an end-use printed circuit board. A pre-fabricated interposer substrate (30), made of metal circuitry (34) and a dielectric base (32), has a plurality of metallized openings which are aligned with metallized wirebond pads (23) on the top surface of a silicon wafer (21). Solder (40), or conductive adhesive, is deposited through the metallized openings to form the electrical connection between the circuitry on the interposer layer (30) and the circuitry on the wafer (21). Solder balls (50) are then placed on the metal pad openings on the interposer substrate (30) and are reflowed to form a wafer-level BGA structure. The wafer-level BGA structure is then cut into individual BGA chip packages.

WO 01/45167 A3

Description

INTEGRATED CIRCUIT PACKAGE FORMED AT A WAFER LEVEL

TECHNICAL FIELD

The invention relates generally to integrated circuit packages, and more specifically to a ball-grid array integrated package formed at a wafer level.

BACKGROUND ART

The footprint of an integrated circuit package on a circuit board is the area of the board occupied by the package. It is generally desired to minimize the footprint and to place packages close together. In recent years, the ball-grid array (BGA) package has emerged as one of the more popular package types because it provides high density, minimum footprint, and shorter electrical paths, which means that it has better performance than previous types of semiconductor packages.

A typical BGA package is shown in Fig. 9. In the BGA package 110, an integrated circuit chip 122 is mounted by means of an adhesive on an upper surface of a base 112 made of a substrate material. Metal bonding wires or wirebond leads 120 electrically connect a plurality of metal chip pads 126 formed on the upper surface of the chip 122 with wire bonding pads 128 formed on the upper surface of the base 112. The base 112 includes plated through-hole vias 118 and metal traces 114 to connect the circuitry from the upper surface to the lower surface of the base 112. A plurality of solder balls 116 are placed on the bottom surface of the base 112 and are electrically connected to the metal traces 114 of the base. The solder balls 116 can be arranged in a uniform full matrix array over the entire bottom

surface, in a staggered full array, or around the perimeter of the bottom surface in multiple rows. The solder balls are then used to secure the chip package onto a printed circuit board in the end-use product.

While the BGA packages of the prior art provide a great improvement over earlier types of packages in terms of high density and high I/O capability, it is always desired to make the IC package even smaller to further decrease the amount of space needed on a printed circuit board to accommodate the package. Because the wirebond leads are of a predetermined length and require a minimum spacing between adjacent bonding sites to provide sufficient room for the bonding tool, the substrate base must be larger than the chip and it is not possible to fabricate a more compact package. Ideally, it is desired to make a package in which the substrate base does not have to be any larger than the size of the chip.

In the prior art, as described above, it is common to fabricate a package for each individual die. Others have realized that it would be advantageous to be able to form the IC package at the wafer level, that is, after the individual chips have been formed on the wafer but before the wafer has been diced into individual chips. This allows for easier mass production of chip packages and for several chip packages, arranged in a matrix format on the wafer, to be manufactured and tested all at one time. This can reduce time and cost in the process of packaging and testing IC chips.

Some examples of packaging methods in the prior art that are conducted at the wafer level include: U.S. Patent No. 5,604,160 to Warfield, which discloses using a cap wafer to package semiconductor devices on a device wafer; U.S. Patent No. 5,798,557 to Salatino et al., which describes a wafer level hermetically packaged

integrated circuit having a protective cover wafer bonded to a semiconductor device substrate wafer; and U.S. Patent No. 5,851,845 to Wood et al., which discloses a method of forming a semiconductor package by providing a wafer containing a plurality of dice, thinning a backside of the wafer by polishing or etching, attaching the thinned wafer to a substrate, and then dicing the wafer.

It is the object of the present invention to provide a ball-grid array IC package that has a minimum size such that the IC package takes up no more space than the area of the IC chip.

It is a further object of the invention to provide an IC package at the wafer level in order to take advantage of the greater efficiency in mass production and the ability to conduct parallel testing of the IC packages.

SUMMARY OF THE INVENTION

The above objects have been achieved in an integrated circuit package that is formed on the wafer level using a flip chip design with a single wafer. The integrated circuit package is formed by first providing a product silicon wafer having a plurality of microelectric circuits fabricated thereon and having a plurality of standard aluminum bonding pads exposed. The aluminum bonding pads are re-metallized to be solderable. Then, a layer of adhesive is deposited onto the wafer surface, the bonding pads remaining exposed. A pre-fabricated interposer substrate, having metallized openings, is aligned to the wafer and then the assembly is cured. Solder, or conductive adhesive, is then deposited through the openings in the substrate and the assembly is reflowed, or cured, to form the electrical connection between the circuitry on the substrate and the bonding pads on the silicon wafer. Solder balls are then placed

on the metal pads on the substrate and are then reflowed forming a BGA structure. The wafer is then diced and the individual BGA packages are formed. The BGA package is flipped for mounting on a circuit board.

The integrated circuit package of the present invention is smaller than BGA packages of the prior art in that the additional space usually required because of the use of wirebonding leads is not necessary. The whole wafer can be packaged all at one time which is more efficient than packaging each die individually and allows for parallel testing of the packaged dice while still in wafer form.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view of a silicon wafer having a plurality of chips formed on a top surface.

Fig. 2 is a cross-sectional view of a section 2-2 of the silicon wafer shown in Fig. 1.

Figs. 3-6 are cross-sectional views of the silicon wafer of Fig. 1 showing the various process steps used in forming the IC package of the present invention.

Fig. 7 is a cross-sectional view of the silicon wafer of Fig. 1, showing the finalized wafer assembly for the IC package of the present invention.

Fig. 8 is a cross-sectional view of the finalized IC package of the present invention.

Fig. 9 is a cross-sectional view of a ball-grid array package as known in the prior art.

BEST MODE FOR CARRYING OUT THE INVENTION

With reference to Fig. 1, a silicon wafer 21 has a plurality of microcircuits fabricated thereon. The microcircuits are arranged into a matrix of individual chips or dice 24, 25. A plurality of aluminum bonding pads 23 are arranged around the perimeter of each of the

chips. In prior art packaging operations, the wafer 21 is usually diced at this point into individual chips, and each of the individual chip is then packaged. In the present invention, the chips are formed on the wafer but are not diced until the packaging operation on the wafer has been completed, thus the packaging of the chip is conducted at the wafer level.

With reference to Fig. 2, a section 2-2 of the wafer 21 is shown, with the aluminum bonding pads 23 being disposed on a top surface of the wafer 21. The first step in the packaging process, is to re-metallize the aluminum bonding pads 23 in order to make the bonding pads solderable. Aluminum, which is commonly used for the wirebond pads of IC's, is a less than ideal metal for use in solder connections due to the fact that the aluminum tends to oxidize which creates bonding problems. In the forming of the IC package of the present invention, the aluminum bonding pads need to be wetable by solder or have a low ohmic contact resistance for application of a conductive adhesive. Therefore, the bonding pads need to be re-metallized. One process for re-metallizing the bonding pads, that is inexpensive and convenient to implement, is to use electroless nickel-gold plating. With reference to Fig. 3, first, a layer of zinc is deposited on the aluminum bonding pads 23, then a layer of electroless nickel plating is deposited on the layer of zinc and, then, a layer of electroless gold plating is deposited on top of the electroless nickel plating to form a nickel-gold plating 19 in order to make the bonding pads 23 conducive to soldering. Alternatively, a thin film metallization process can be carried out to re-metallize the bonding pads.

Next, referring to Fig. 4, a layer of adhesive 27 is deposited on the top surface of the wafer 21 such that the bonding pads 23 are left uncovered. The

adhesive can be made of a silicone elastomer. The adhesive layer 27 can be applied through a screen printing process in which the silicone elastomer material is pushed through the openings of a stencil or a mesh screen. The screen is mounted onto a screen printer and is precisely positioned with respect to the wafer. A certain amount of the silicone elastomer material is dispensed along one edge of the screen and an air-operated squeegee presses down on the screen as it sweeps across it, sheering the material at a constant pressure. The material acquires higher flowability above certain shear pressures, which allows it to go through the screen and fill the gaps left by the wire mesh of the screen. The area above the bonding pads 23 is blocked so that no material is laid on top of the bonding pads. The screen is removed and a uniform layer of the material is formed on top of the wafer. Alternatively, an adhesive layer preform can be used to adhere the adhesive layer 27 to the top surface of the wafer 21 or to the backside of an interposer substrate layer. The silicone elastomer acts as an encapsulant, providing environmental protection for the wafer. The silicone elastomer also acts as a buffer for the wafer 21 from external stresses, such as a thermal coefficient of expansion mismatch between the wafer and the package solder balls used for mounting the IC package, or a mismatch between the wafer and an end-use printed circuit board on which the IC package would be mounted.

With reference to Fig. 5, an interposer substrate layer 30 is then secured on top of the elastomer layer 27 to form a wafer assembly 39. The interposer substrate 30 is a preformed substrate consisting of metal circuitry 34 and a dielectric base 32. The metal circuitry 34 typically consists of copper traces formed throughout the substrate. The interposer

substrate 30 can also include solder resist coatings to help define solder wetable areas on the copper metal circuitry. The metal circuitry 34 can be formed on a single layer or on multiple layers of the interposer substrate 30. The copper metal circuitry can be nickel-gold plated or coated by an organic material. The dielectric base material 32 is typically made of a polyamide base substrate. Alternatively, BT resin and other epoxy-glass substrates can also be used as the dielectric base material 32. The metal circuitry 34 generally serves as interconnect circuitry, as the traces can be routed throughout the substrate to interconnect the circuits from the various bonding pads 23 to the Input/Output (I/O) interconnects which will be added to the wafer assembly 39, as described later with reference to Fig. 7.

A key feature of the interposer substrate 30 is a plurality of openings 36 on the copper circuitry. The interposer substrate 30 can be approximately the same size as the wafer 21 and is aligned to the wafer 21 such that the openings 36 line up with the bonding pads 23. A sufficient amount of copper must be present in the openings 36 to provide adequate connection for solder or for a conductive adhesive. A circular copper ring around the openings 36 or a copper strip across the openings 36 can be used to facilitate this requirement. The interposer substrate 30 is then adhered by a bonding adhesive to the elastomer layer 27 and the wafer assembly 39 is then cured. Thus, the interposer is aligned and bonded to the wafer.

With reference to Fig. 6, a layer of solder paste 40 is deposited through the openings 36 of the interposer substrate 30. This can be carried out by a screen or stencil printing process in the same manner as described above with reference to the depositing of the

elastomer layer 27. The interposer substrate base 32 layer is screened off and the solder paste 40 is deposited into the openings 36 by an air-operated squeegee so that the solder paste 40 is deposited on the wafer all at one time. The wafer 21 is then solder reflowed to form a plurality of electrical connections between the bonding pads 23 on the wafer 21 and the copper metal circuitry 34 in the interposer substrate layer 30. The solder paste can also be deposited through the openings of the interposer substrate by the use of automatic dispensing equipment or by solder preform placement. Alternatively, a conductive adhesive may be used, in lieu of the solder paste, to electrically connect the bonding pads 23 and the metal circuitry 34. The adhesive is deposited in the openings 36 and then is cured to form the electrical connections. Optionally, an epoxy material can be used to protect the solder connections. Application of the epoxy material would also be by the screen or stencil printing process described above and the protective coating would then be cured.

The next step is to place package solder balls on the wafer. The package solder balls serve as the I/O interconnects for the package and will be used to secure the completed IC package to an end-use printed circuit board. With reference to Fig. 7, the solder balls 50 are placed on the metallized openings 36 through a mechanical transfer of pre-formed solder balls. Alternatively, the solder balls 50 can be formed by screen or stencil printing solder paste. The solder is then reflowed to form the package solder balls. The solder balls 50 are applied in whatever type of pattern is desired, such as in a uniform full matrix over the entire surface.

At this point, electrical testing may be conducted on the wafer assembly 39 since the wafer

assembly 39 contains finished dice arranged in a matrix format. This allows for parallel testing, which can be conducted at the wafer level and can provide savings in testing time and cost. Then the wafer assembly 39 is diced, or singulated, to form individual chip-size BGA packages 70, 72. A common technique for the singulation is to use a wafer saw with diamond or resinoid saw blades. With reference to Fig. 8, the finished BGA package 70 can then be mounted on the end-use printed circuit board in the same manner as prior art BGA packages. The BGA package 70 of the present invention has the same footprint as the individual silicon die, as no extra space is needed to accommodate wirebond leads or larger substrate bases. In this way, the integrated circuit package of the present invention provides the advantages of a smaller package size and the convenience of packaging at the wafer level.

Claims

1. An integrated circuit package formed at a wafer level, comprising:

a silicon die having an area and having a plurality of bonding pads arranged on a first surface,

an adhesive layer covering a substantial portion of the first surface of the die, the plurality of bonding pads remaining exposed,

an interposer substrate disposed on the adhesive layer and including a plurality of metal circuit traces and a plurality of metallized openings, the openings being aligned with the plurality of bonding pads of the die,

means for electrically connecting the plurality of metallized openings of the interposer substrate and the plurality of bonding pads on the die, and

a plurality of I/O interconnects formed on the plurality of metallized openings of the interposer substrate.

2. The integrated circuit package of claim 1 wherein the plurality of I/O interconnects are solder balls formed on the interposer substrate.

3. The integrated circuit package of claim 1 wherein the means for electrically connecting the plurality of metallized openings and the plurality of bonding pads is solder.

4. The integrated circuit package of claim 1 wherein the means for electrically connecting the plurality of metallized openings and the plurality of bonding pads is a conductive adhesive.

5. The integrated circuit of claim 1 wherein the interposer substrate has an area of a same size as the area of the die.

6. A method of forming an integrated circuit chip package on a wafer level, comprising:

providing a silicon wafer having a plurality of bonding pads disposed on a first surface thereof,

re-metallizing the plurality of bonding pads,

depositing a layer of an adhesive material on the first surface of the wafer, the plurality of bonding pads remaining exposed,

securing an interposer substrate, composed of a dielectric material and a plurality of metallized traces, to the layer of adhesive material to form a wafer assembly, the interposer substrate including a plurality of metallized openings which are aligned to the plurality of bonding pads,

forming an electrical connection between the plurality of metallized openings and the plurality of bonding pads,

attaching a plurality of I/O interconnects on the plurality of metallized openings on the surface of the interposer substrate, and

dicing the wafer assembly into a plurality of individual integrated circuit chip packages.

7. The method of claim 9 wherein the step of securing the interposer substrate to the layer of adhesive material further comprises, curing the wafer assembly.

8. The method of claim 9 wherein the plurality of I/O interconnects are a plurality of solder balls.

9. The method of claim 11 wherein the step of attaching the plurality of I/O interconnects on the plurality of metallized opening includes:

placing the plurality of solder balls on the plurality of metallized openings, and

reflowing the plurality of solder balls to form a plurality of interconnections.

10. The method of claim 9 wherein the step of re-metallizing the plurality of bonding pads includes:

depositing a layer of zinc on each of the bonding pads,

depositing a layer of electroless nickel plating on top of the layer of zinc on each of the bonding pads, and

depositing a layer of electroless gold plating over the layer of electroless nickel plating on each of the bonding pads.

11. The method of claim 9 wherein the step of depositing the layer of adhesive material on the first surface of the wafer is implemented by a screen-printing process.

12. The method of claim 9 wherein the layer of adhesive material is made of a silicone elastomer.

13. The method of claim 9 wherein the step of forming an electrical connection between the plurality of metallized openings and the plurality of bonding pads includes:

depositing a layer of solder on the metallized openings, and

reflowing the layer of solder to form an electrical connection.

14. The method of claim 9 wherein the step of forming an electrical connection between the plurality of metallized openings and the plurality of bonding pads includes:

depositing a layer of a conductive adhesive on the metallized openings, and

curing the layer of conductive adhesive to form an electrical connection.

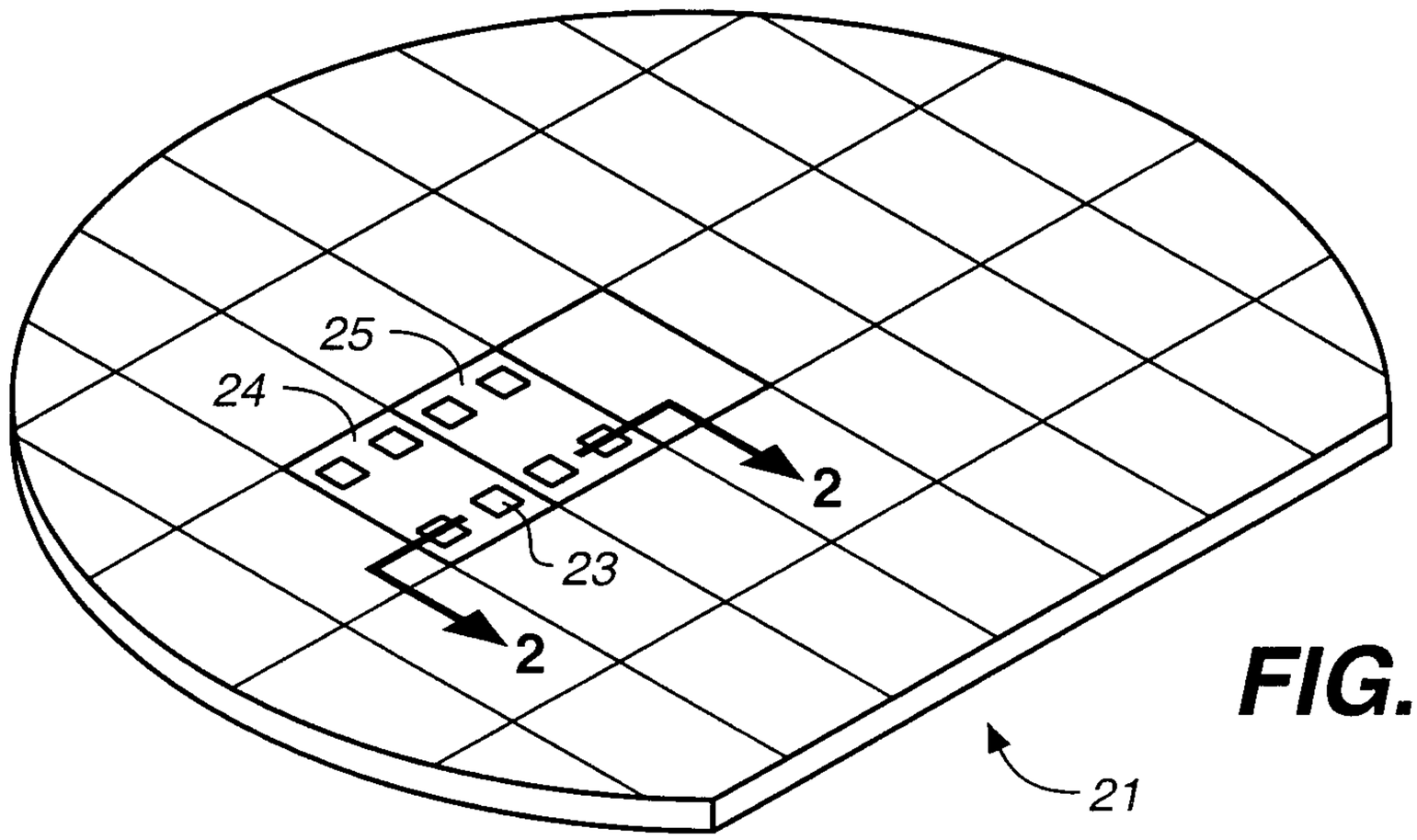


FIG._1

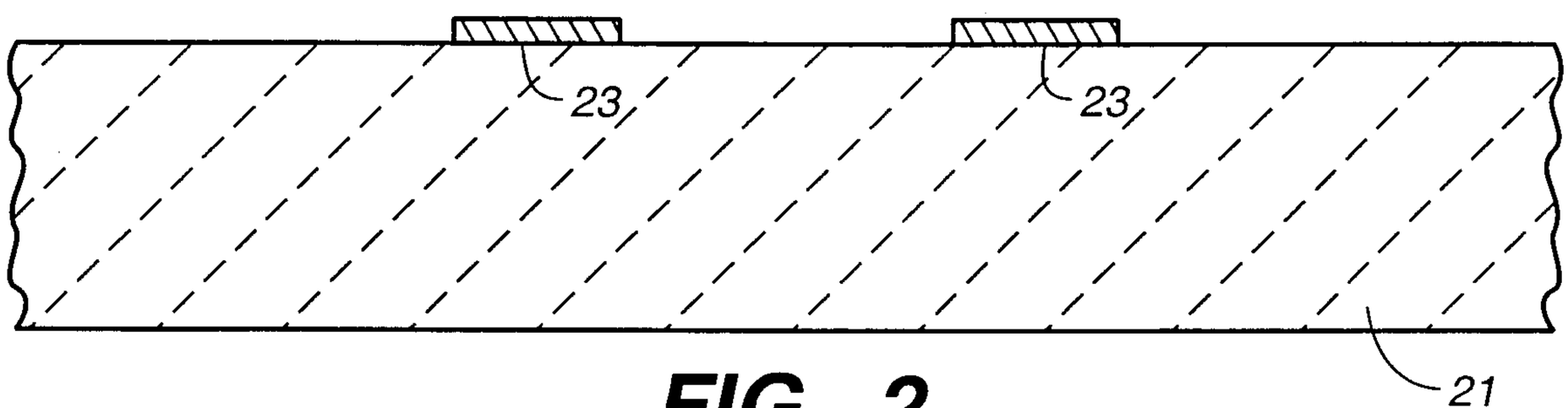


FIG._2

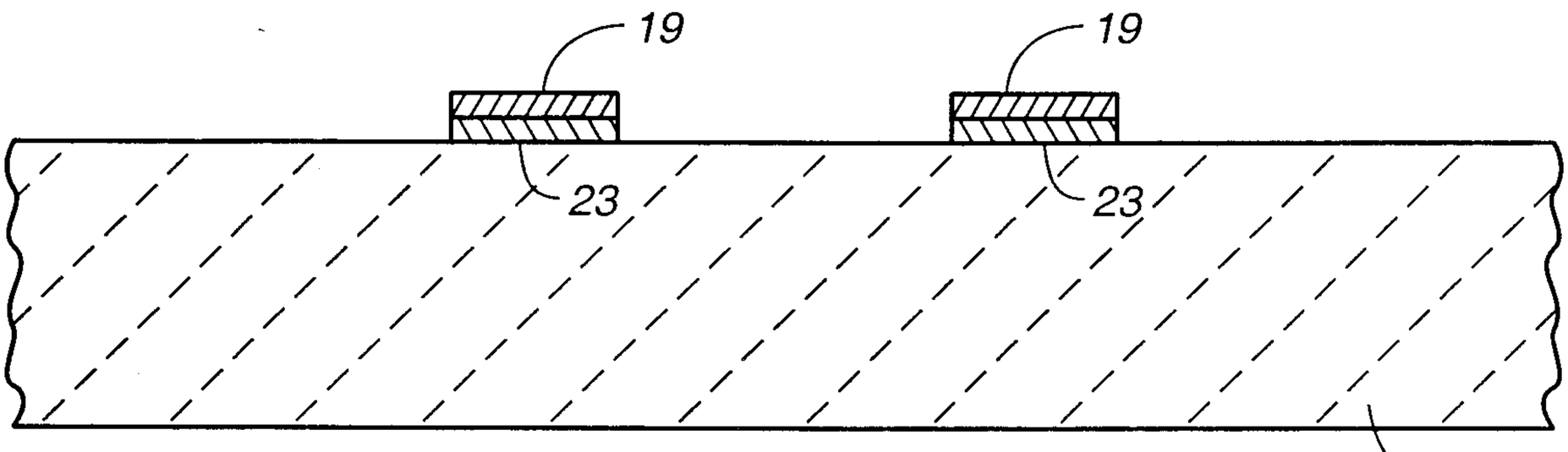


FIG._3

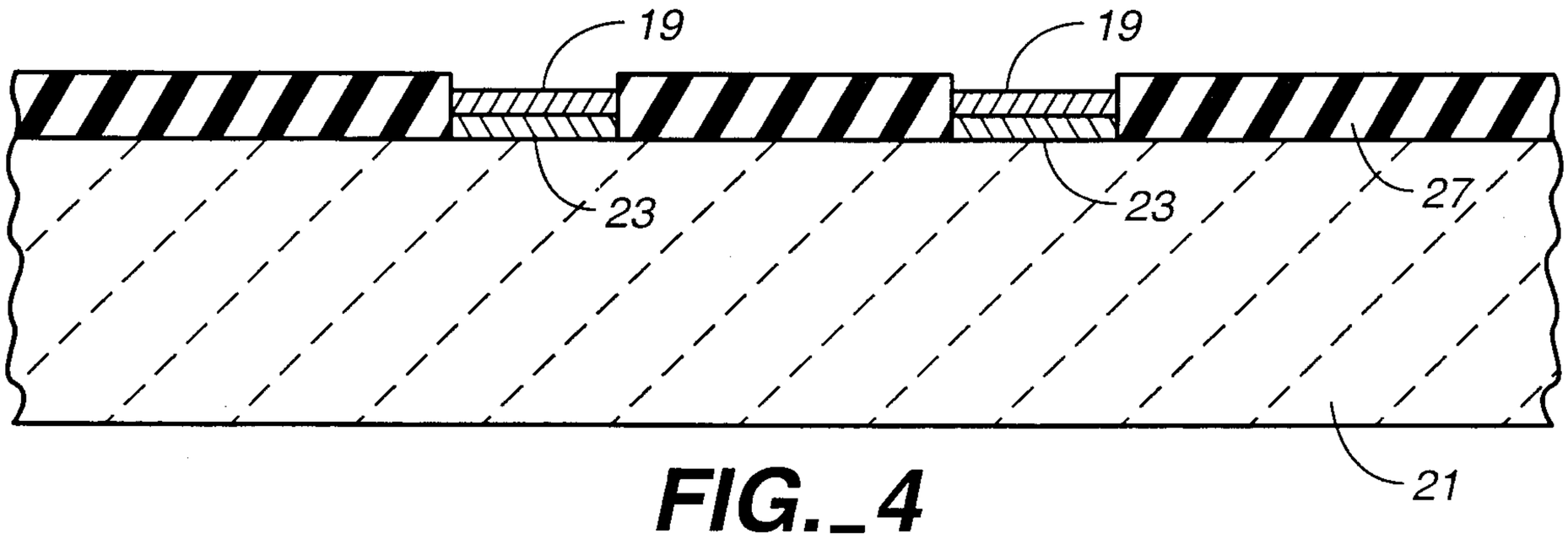


FIG._4

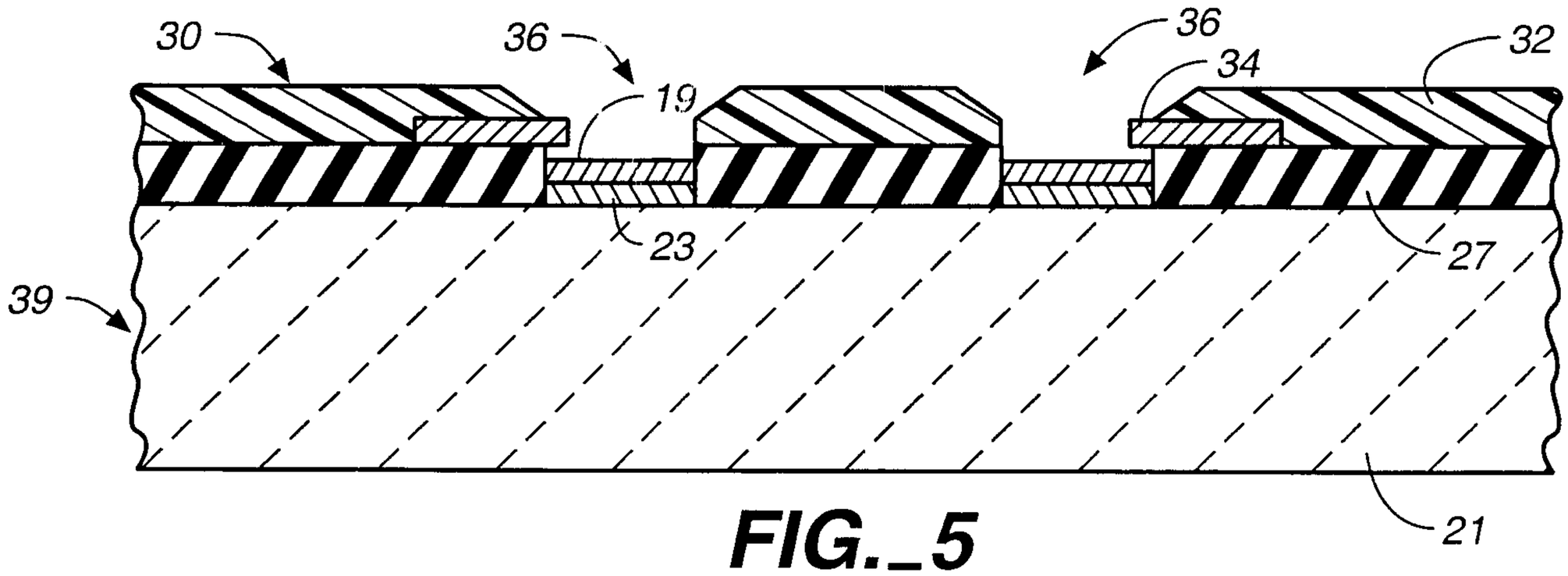
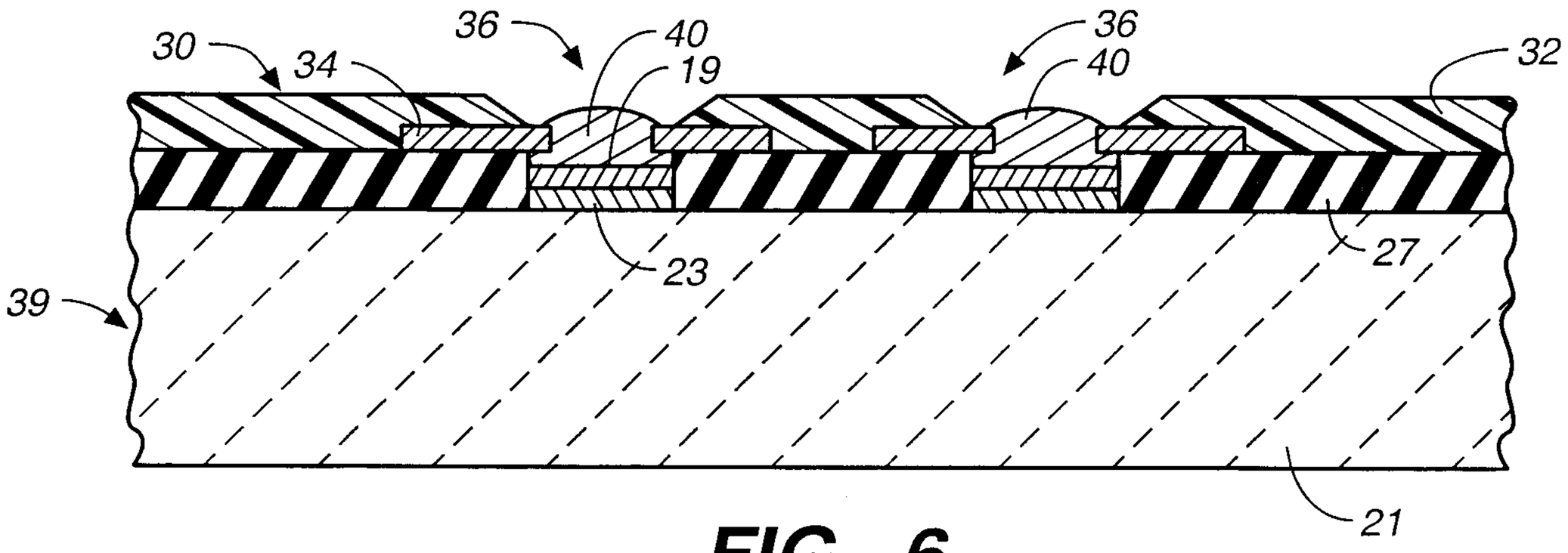


FIG._5



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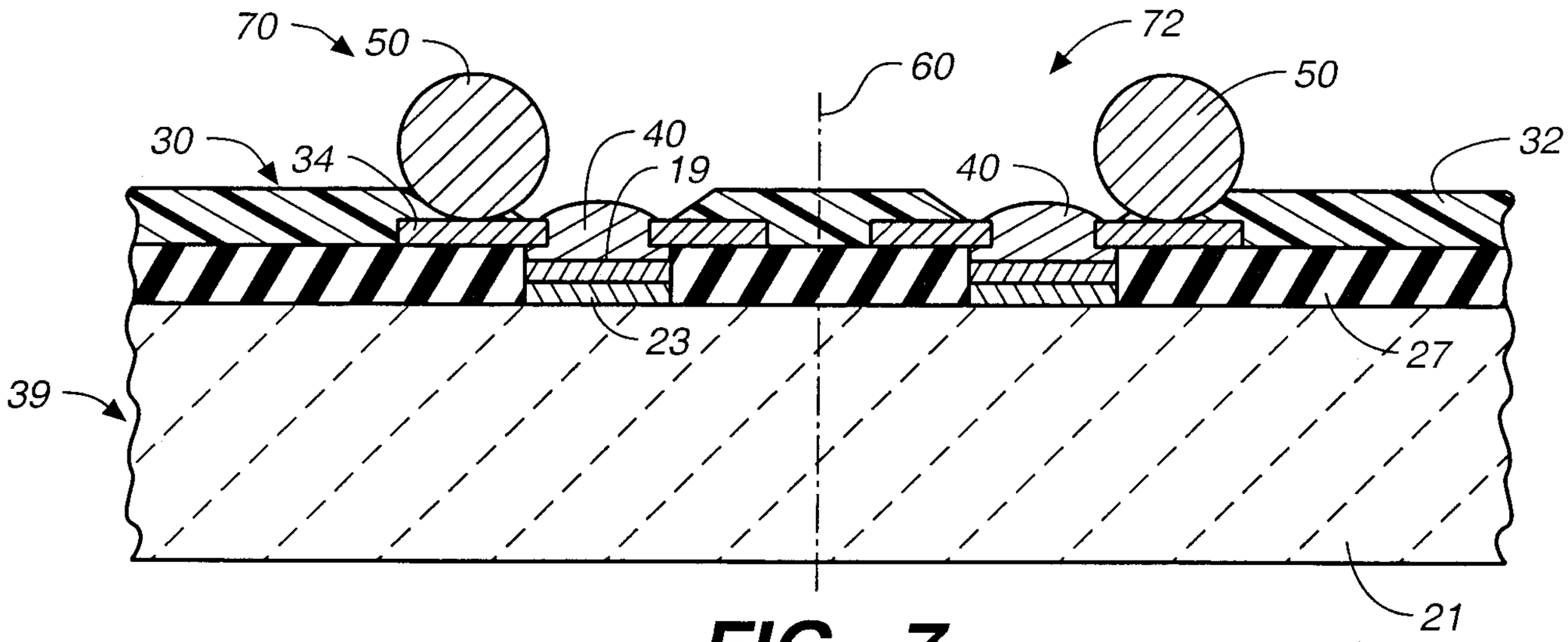


FIG._7

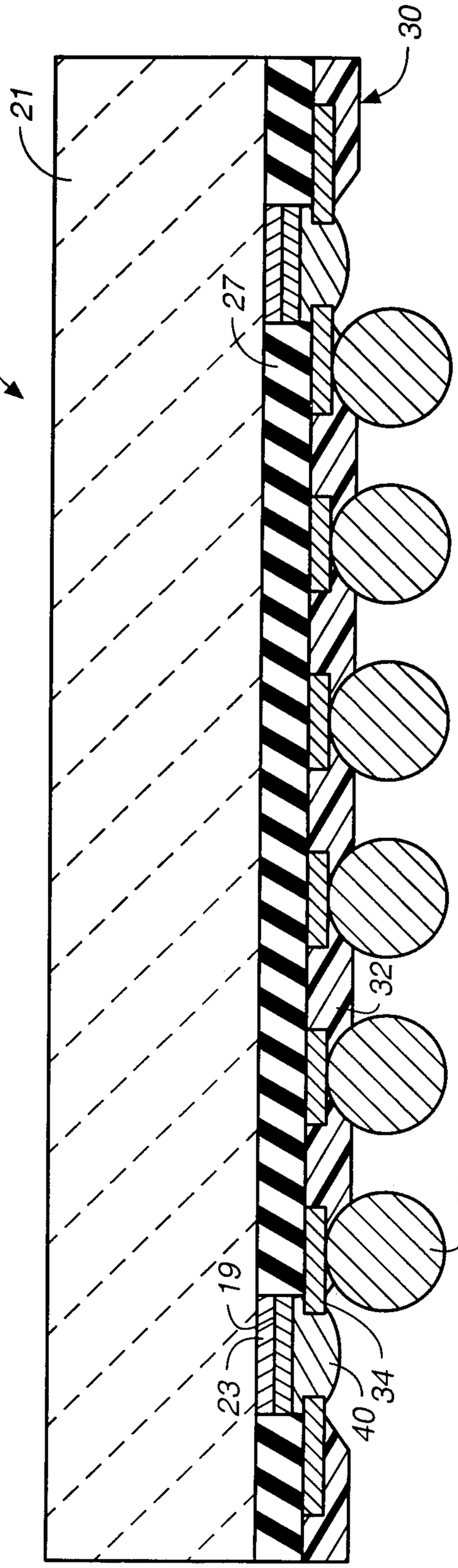


FIG._8

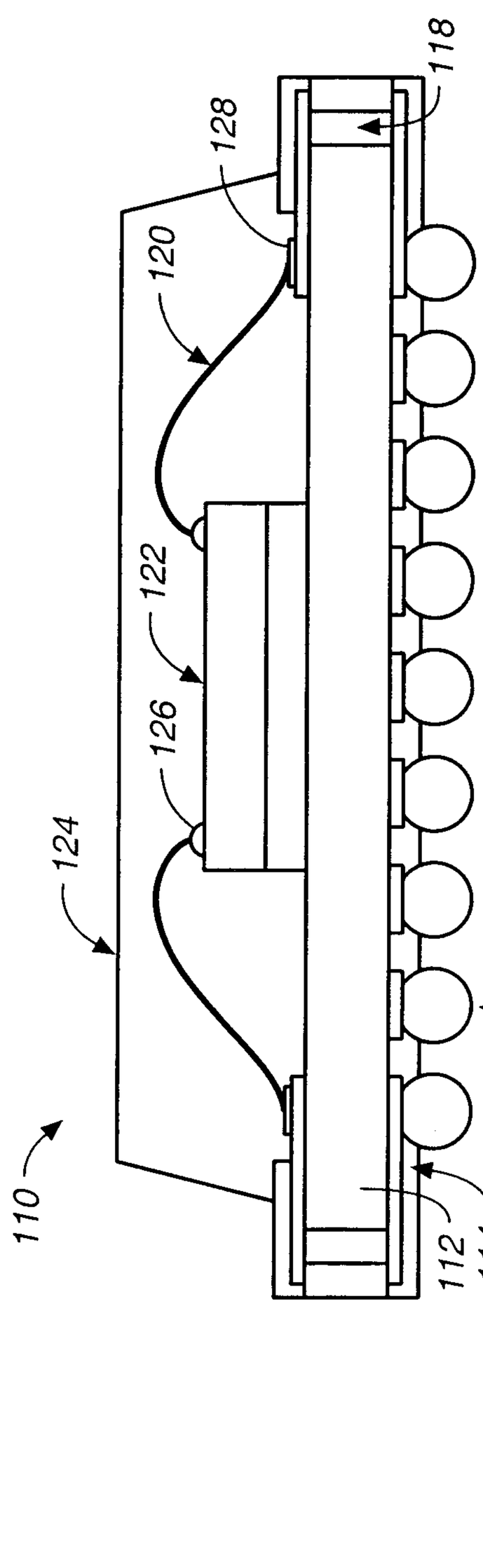
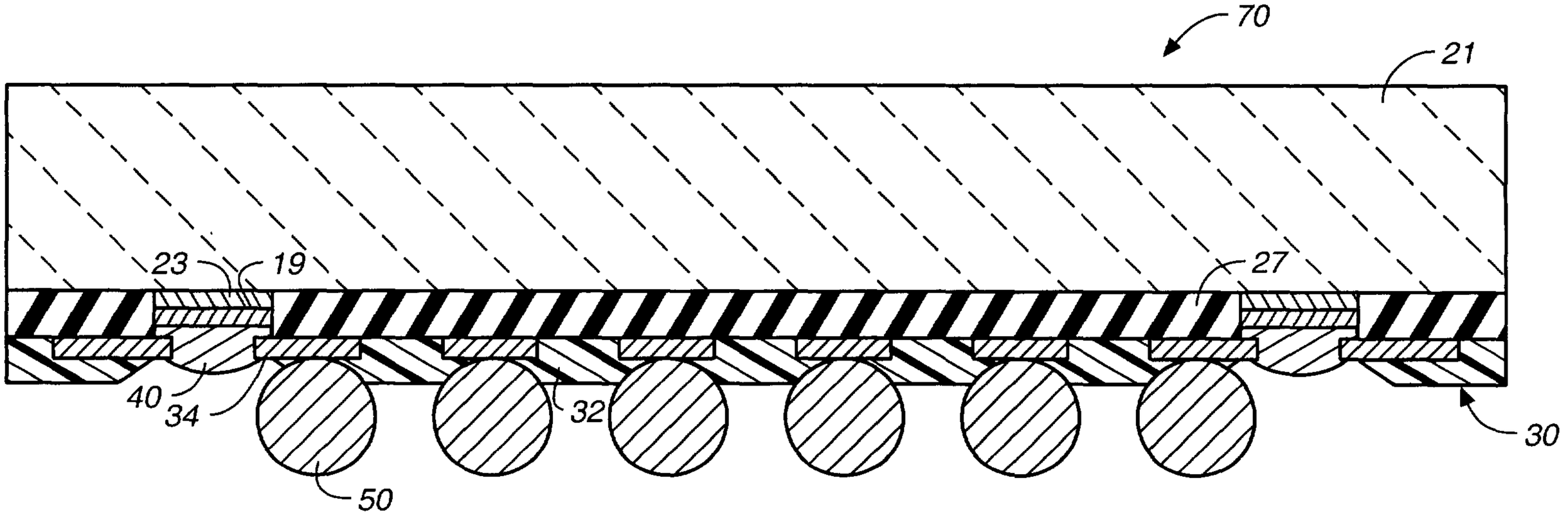


FIG._9
(PRIOR ART)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