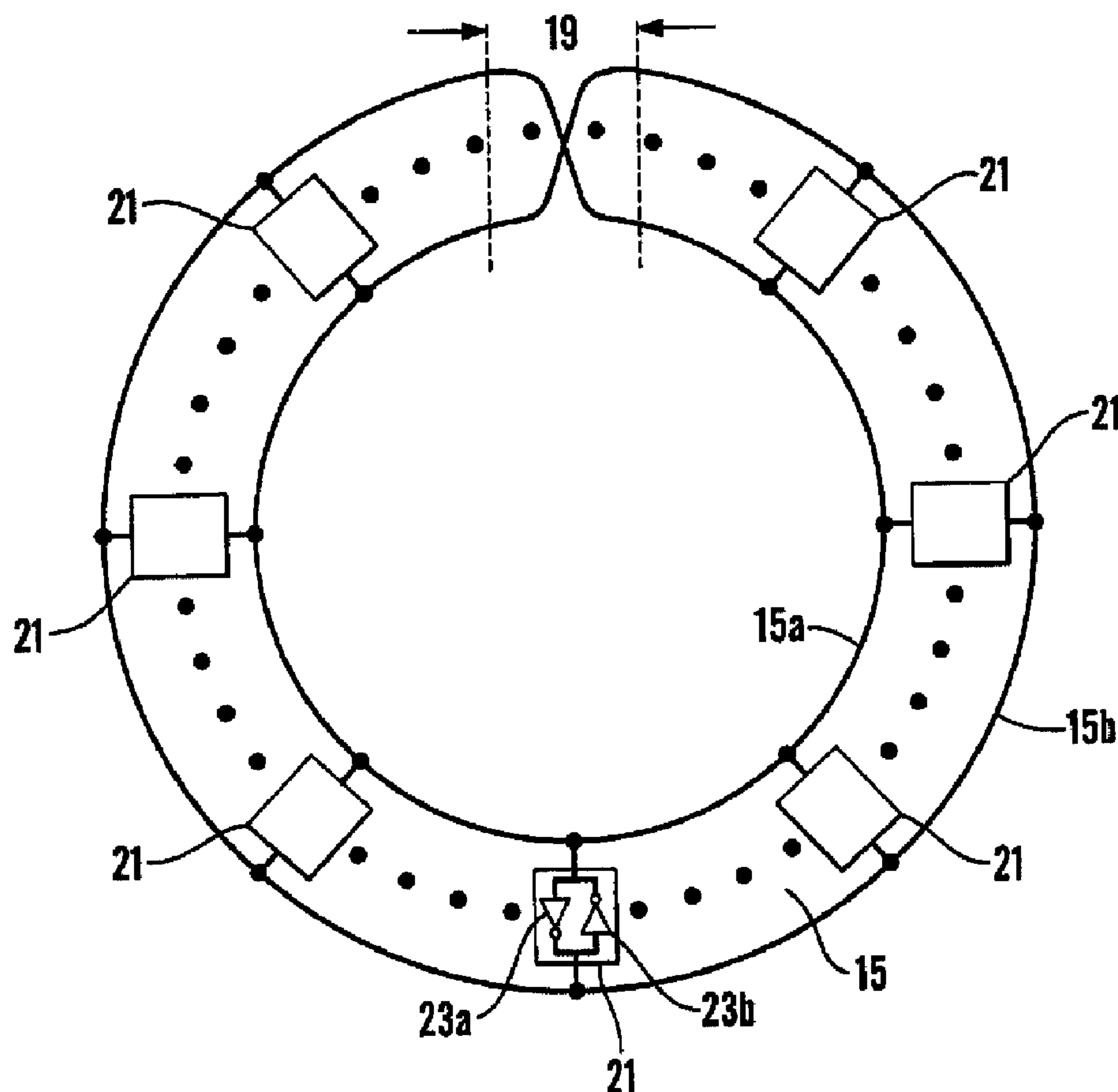




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(57) Abrégé/Abstract:

Timing signal generation and distribution are combined in operation of a signal path (15) exhibiting endless electromagnetic continuity affording signal phase inversion and having associated regenerative active means (21). Two or more phases of



(57) **Abrégé(suite)/Abstract(continued):**

substantially square-wave bipolar signals arise directly in travelling wave transmission-line embodiments compatible with semiconductor fabrication including CMOS. Coordination by attainable frequency synchronism with phase coherence for several such oscillating signal paths has intra-IC inter-IC and printed circuit board impact, as does two-way simultaneous data transfer.



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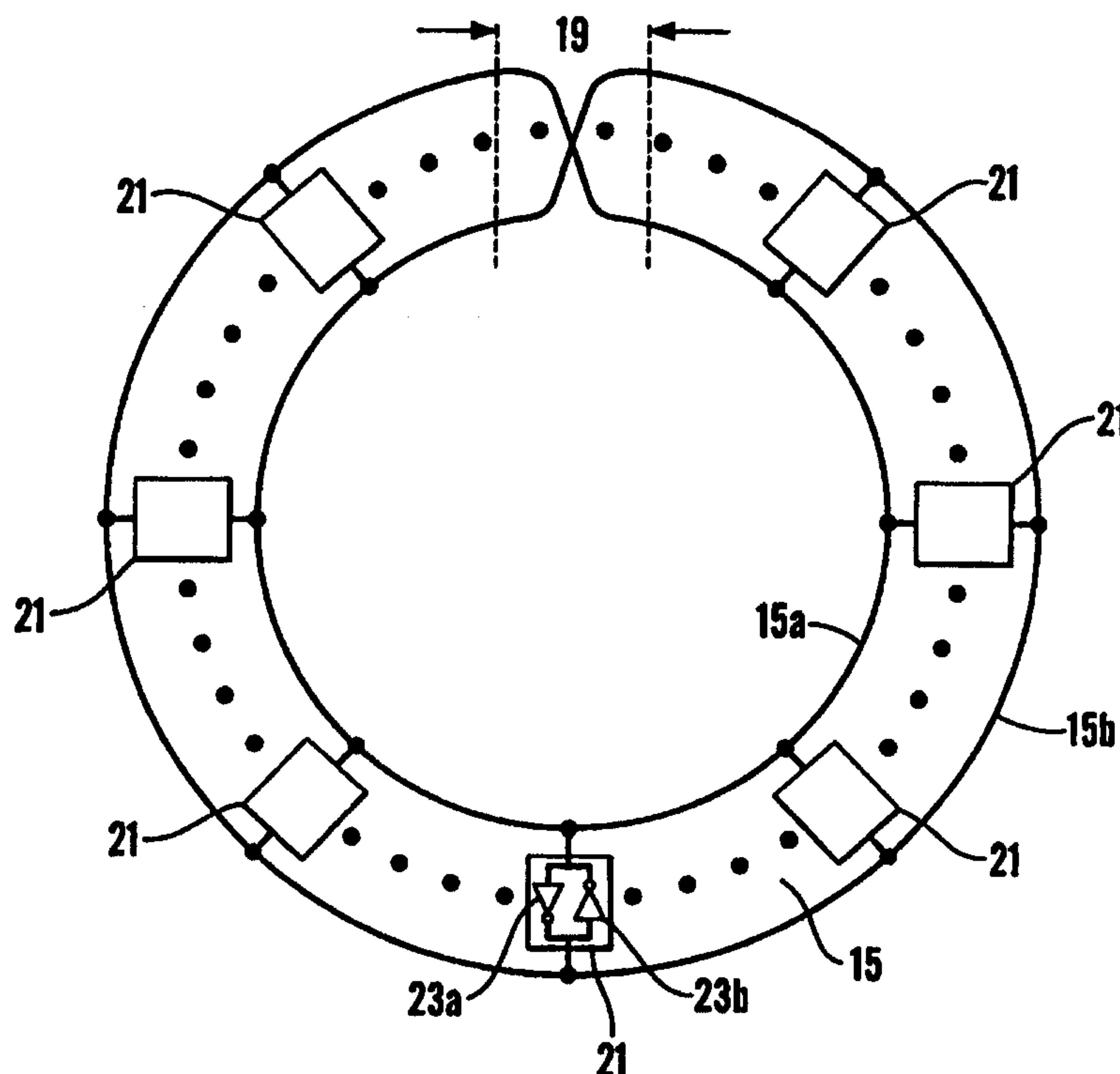
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(54) Title: ELECTRONIC CIRCUITRY**(57) Abstract**

Timing signal generation and distribution are combined in operation of a signal path (15) exhibiting endless electromagnetic continuity affording signal phase inversion and having associated regenerative active means (21). Two or more phases of substantially square-wave bipolar signals arise directly in travelling wave transmission-line embodiments compatible with semiconductor fabrication including CMOS. Coordination by attainable frequency synchronism with phase coherence for several such oscillating signal paths has intra-IC inter-IC and printed circuit board impact, as does two-way simultaneous data transfer.



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ELECTRONIC CIRCUITRY**20 FIELD OF INVENTION**

The invention relates to electronic circuitry concerning timing signals and their production and distribution; oscillators as sources of such as timing signals; and communications according to timing signals.

BACKGROUND TO INVENTION

25 Digital electronic data processing circuitry and systems require timing signals to synchronise data processing activities. Customarily, such timing signals include a master timing signal from which other timing signals can be derived. Such a master timing signal is commonly referred to as a 'clock' signal. It is often desirable to have a clock signal that is available in more than one phase.

30 An example of a two-phase clock signal is where available clock signals have a phase difference of 180-degrees as often used for dynamic logic and shift register circuitry. An example of a four-phase clock signal is where available clock signals have successive phase differences of 90-degrees. Semiconductor integrated circuits (ICs or chips) are typical host environments, often very large scale (VLSI) chips as for microprocessors or memories.

35 Historically, modest operating clock frequencies up to about 50MHz were satisfied by use as off-chip quartz crystal clock oscillator with simple point-to-point on-chip clock signal

distribution. Nowadays, at much higher operating frequencies, typically aiming for 300MHz to 1GHz, inherent on-chip distribution problems associated with clock signal reflection and skew have become highly significant as binary signal widths/durations are no longer so much shorter than clock signal pulses. Natural progression of IC designs is for chips to become physically bigger and functionally more complex, which compounds these problems.

Clock signal generation is presently typically by frequency multiplication from off-chip crystal clock oscillators using on-chip phase locked loop (PLL) control circuitry which occupies valuable chip area, consumes considerable power, and experiences problems with signal reflections, capacitive loading and power dissipation that effectively limit maximum operating frequency. Related clock signal distribution usually involves tree-like arrangement of operational circuitry with chains of clock signal boosting buffers at intervals. Even so, variability of semiconductor process parameters, including in the buffers, leads to undesirable and unpredictable phase delays (skew) at different positions on the chip, thus can adversely affect reliable synchronous operation and communication even for neighbouring areas of a chip. As a result, ICs often have to be rated and run at lower than maximum designed-for clock rates. Indeed, IC manufacturers are even reversing long-standing trends by use of smaller chip sizes for latest ICs.

The development of ever more comprehensive 'systems-on-silicon' chips is being hampered by lack of viable provisions for reliably clocking large area high-density chips. It is noteworthy that clock rates tend to be limited to less than about 1 GigaHertz despite such as Mosfet IC transistor features being capable of switching at 25 GigaHertz or more.

This invention arises basically from looking for some alternative approach that at least reduces areal and/or power demands of on-chip PLL provisions, if possible further addresses and to some useful extent resolves clock signal distribution problems.

25 SUMMARY OF INVENTION

One broad view or aspect of this invention resides in the concept and realisation of method and means for effectively integrating or synergistically combining distribution of repeating pulse or cyclic signals with active means for producing and maintaining those signals. A composite electromagnetic/semiconductor structure is facilitated that

simultaneously generates and distributes timing signals, including a master clock. A suitable said signal path exhibits endless electromagnetic continuity affording signal phase inversion of an electromagnetic wave type signal, conveniently with path-associated regenerative means.

5 A successful inventive rationale aspect hereof has been evolved in which time constant for repeating pulse or cyclic signals is related to and effectively defined by electrical length of said signal path in the signal distribution means. A travelling electromagnetic wave recirculating endlessly electromagnetically continuous said signal path is preferred, when its traverse time of the signal path determines said time constant.

10 Interestingly and quite surprisingly, this has been found to be conducive to particular inventive direct production of pulse-like cyclic signals inherently having fast rise and fall characteristics, i.e. already "square" as produced, rather than requiring resort to "squaring" action on a basic inherently substantially sinusoidal signal as hitherto conventional. Indeed, such inventive electrical length/signal traverse time-constant-defining rationale hereof leads
15 conveniently and advantageously to said electrical length or one said signal traverse effectively first defining one unipolar half-cycle signal excursion and next, or at next said signal traverse, effectively completing definition of a full bipolar cycle comprising two opposite half-cycle excursions. Said electrical length thus corresponds to 180-degrees for each of two successive pulse excursions for such full bipolar cycle.

20 Specific inventive aspects hereof to achieve such rationale are viewed as involving signals of a travelling wave nature with the signal distribution path involved having a suitably propagating nature therefor, typically of endless transmission-line form, further with transposing effect and inverting action associated with re-circulations of desired signals.

 In one specific inventive aspect hereof, desired repeating cyclic signals involve re-
25 circulatory travelling wave propagation means effectively affording rotation thereabout by a desired travelling wave and setting duration of each signal excursion, with active regenerative means that can be of switching and amplifying nature, conveniently bidirectional inverting amplifier, supplying energy requirements and setting relatively short rise and fall at ends of each signal excursion.

Suitable travelling wave propagation means with desired transposing effect relative to active inverting means is exemplified, as seen by the traversing travelling wave, by physical width twisted along its length to connect opposite sides to input and output of the inverting means, say as though a Moebius band or ribbon. Indeed, an integrated circuit made on a flexible substrate could be of elongate form with said path following its length and its ends interconnected as a Moebius band or ribbon, even with functional circuitry blocks to either or both sides of or straddling its travelling wave propagation feature. At least then, integration of inverting and travelling wave propagating features of cyclic signal means hereof could be to the extent of up to all its length being of continuous semiconductor inverter nature, at least using CMOS technology.

However, for planar implementation of travelling wave propagation means, a typical transmission-line form uses spaced path-following conducting features, aforesaid Moebius twist effect being afforded by way of no more than a mutually insulated cross-over of those spaced conducting features. An alternative would be use of a transmission-line inverting transformer in or associated with otherwise transmission-line form of the travelling propagation means.

An inventive aspect of exemplary implementation hereof uses spaced conductive features as trace formations each having substantially the same length and being transposed on the way between output and input of at least one inverter feature connected to, preferably between, those conductive traces. In practice, at least where the inverter feature is of extent less than about 1% along the conductive features, there will preferably be plural inverter features spaced along the conductive features or traces – unless this invention is adapted to operation as a standing wave oscillator.

Preferred inverter means is of bidirectional nature, such as a pair of opposite inverters side-by-side or back-to-back; and such provision facilitates direct simultaneous production of similar or substantially identical anti-phase cyclic signal components.

Particularly interesting and advantageous results available from this invention include timing signal provision with extremely low power consumption that can effectively be limited to transmission-line and inverter action losses, i.e. to near-negligible topping-up via the inverter

provision(s), and take-off to operational circuitry is readily made, e.g. by way of light bidirectional connection paths of passive resistive and/or capacitive and/or inductive or transmission-line nature, or unidirectional say using diodes or inverters, etc as will be described in more detail.

5 Another such available result is that, at least in principle and absent fabrication imperfections, cyclic signal provision hereof has no innate preference for either direction or rotation of travelling wave propagation, though either may be predisposed or imposed by such as prescribed spacings or other differences between or within inverter means.

Inventive proposals and aspects hereof as to pulse generators and oscillators as such
10 include transmission-line structures using conductive metal and insulating dielectric layers in a manner compatible with IC production generally and particularly together with regenerative circuitry associated with the transmission-line as such, typically and conveniently formed below and connected by vias; required insulated cross-overs or spaced transmission-line transformer parts are likewise readily formed including such as via jump connections for the
15 cross-overs; and resulting advantageously DC unstable interconnection of terminals of such as bidirectional inverters as the regenerative means; synchronous detection and bridge rectifier action of preferred bidirectional inverters; reinforcing sequential action of such bidirectional inverters including recycling electrical energy relative to supplies; etc.

Moreover, there are inventive aspects in interconnection/intercoupling of timing signal
20 generating and distribution circuitry hereof, whether by direct connection or by sharing magnetic and/or electrical fields; and doing so on a self-synchronising basis with extension to different frequencies particularly in odd-harmonic relationship. Intercoupling and coordinating between ICs as such and further with transferring data also have important innovative and inventive merit.

25 Other aspects and features of the present invention arise later in this Description, and/or are as set out in independent and dependent Claims wording of which is to be taken as incorporated here too.

BRIEF DESCRIPTION OF DRAWINGS

Specific exemplary implementation for the invention is now described and shown by reference to the accompanying diagrammatic drawings, in which

Figure 1 is an outline diagram for a transmission-line structure hereof;

Figure 2 shows a Moebius strip;

5 Figure 3 is an outline circuit diagram for a travelling wave oscillator hereof;

Figure 4 is another outline circuit diagram for a travelling wave oscillator hereof;

Figures 5a and 5b are equivalent circuits for distributed electrical models of a portion of a transmission-line hereof;

Figure 6a shows idealised graphs for respective differential output waveforms hereof;

10 Figure 6b illustrates relationship between propagation delay, electrical length and physical length of a transmission-line hereof;

Figures 7(i)-7(ix) are idealised graphs illustrating the phase of signal waveforms hereof;

Figures 8a-8c illustrate instantaneous phasing of one waveform in a transmission-line oscillator hereof;

15 Figure 9 is a cross sectional view of part of a transmission-line on an IC;

Figures 10a and 10b are outline circuit and idealised graphs for a standing wave version;

Figure 11 is a scrap outline of a transmission-line with inverting transformer;

Figure 12 shows a pair of back-to-back inverters connected across part of a transmission-line;

20 Figures 13a and 13b are outline and equivalent circuit diagrams of CMOS back-to-back inverters;

Figure 14a details capacitive elements of a transmission-line together with CMOS transistors;

Figure 14b is on an equivalent circuit diagram for Figure 14a;

Figure 15 shows capacitive stub connections to a transmission-line;

Figure 16 shows one connection for self-synchronising transmission-line oscillators;

25 Figures 17a-17c show other connections for self-synchronising transmission-line oscillators;

Figure 18 is a diagrammatic equivalent representation for Figure 13a;

Figures 19a and 19b show connection of four transmission-line oscillators;

Figure 20 and 21 show magnetically coupled self-synchronised transmission-line oscillators;

Figure 22 shows three magnetically couple self-synchronised transmission-line oscillators;

Figure 23 shows connection of self-synchronising transmission-lines oscillators of different frequencies:

Figure 24 shows an example of a clock distribution network for a monolithic IC;

Figure 25 shows 3D implementation for timing systems hereof;

5 Figure 26a and 26b show examples of dual phase tap-off points;

Figure 27 shows three concentrically arranged transmission-line oscillators;

Figure 28a and 28b show a transmission-line having a cross-loop connection;

Figure 29a shows a transmission-line configuration for four-phase signals;

Figure 29b shows idealised resulting four-phase signal waveforms;

10 Figure 30 shows an open-ended transmission-line connection;

Figure 31 concerns co-ordinating frequency and phase for two IC's;

Figure 32a concerns data transfer for frequency and phase co-ordinated IC's;

Figures 32b-32e concern data latches for the system of Figure 32a;

Figure 33 shows digitally selectable shunt capacitors of Mosfet type; and

15 Figure 34 shows capacitive loading and routing data and/or power across a transmission-line.

DETAILED DESCRIPTION FOR ILLUSTRATED EMBODIMENTS

Known transmission-lines broadly fall into two categories in that they are either open-ended or specifically terminated either partially or fully. Transmission-lines as proposed herein are different in being neither terminated nor open-ended. They are not even
20 unterminated as such term might be understood hitherto; and, as unterminated herein, are seen as constituting a structural aspect of invention, including by reason of affording a signal path exhibiting endless electromagnetic continuity.

Figure 1 shows such a transmission-line 15 as a structure that is further seen as physically endless, specifically comprising a single continuous "originating" conductor
25 formation 17 shown forming two appropriately spaced generally parallel traces as loops 15a, 15b with a cross-over at 19 that does not involve any local electrical connection of the conductor 17. Herein, the length of the originating conductor 17 is taken as S, and corresponds to two 'laps' of the transmission-line 15 as defined between the spaced loop traces 15a, 15b and through the cross-over 19.

This structure of the transmission-line 15 has a planar equivalence to a Moebius strip, see Figure 2, where an endless strip with a single twist through 180° has the remarkable topology of effectively converting a two-sided and two-edged, but twisted and ends-joined, originating strip to have only one side and one edge, see arrows endlessly tracking the centre line of the strip. From any position along the strip, return will be with originally left- and right-hand edges reversed, inverted or transposed. The same would be true for any odd number of such twists along the length of the strip. Such a strip of conductive material would perform as required for signal paths of embodiments of this invention, and constitutes another structural aspect of invention. A flexible substrate would allow implementing a true Mobius strip transmission-line structure, i.e. with graduality of twist that could be advantageous compared with planar equivalent cross-over 19. A flexible printed circuit board so formed and with its ICs mounted is seen as a feasible proposition.

Figure 3 is a circuit diagram for a pulse generator, actually an oscillator, using the transmission-line 15 of Figure 1, specifically further having plural spaced regenerative active means conveniently as bi-directional inverting switching/amplifying circuitry 21 connected between the conductive loop traces 15a, 15b. The circuitry 21 is further illustrated in this particular embodiment as comprising two inverters 23a, 23b that are connected back-to-back. Alternatives regenerative means that rely on negative resistance, negative capacitance or are otherwise suitably non-linear, and regenerative (such as Gunn diodes) or are of transmission-line nature. It is preferred that the circuitry 21 is plural and distributed along the transmission-line 15, further preferably evenly, or substantially evenly; also in large numbers say up to 100 or more, further preferably as many and each as small as reasonably practical.

Inverters 23a, 23b of each switching amplifier 21 will have the usual operative connections to relatively positive and negative supply rails, usually V_{+} and GND, respectively. Respective input/output terminals of each circuit 21 are shown connected to the transmission-line 15 between the loops 15a, 15b at substantially maximum spacing apart along the effectively single conductor 17, thus each at substantially halfway around the transmission-line 15 relative to the other.

Figure 4 is another circuit diagram for an oscillator using a transmission-line structure hereof, but with three cross-overs 19a, 19b and 19c, thus the same Moebius strip-like reversing/inverting/transposing property as applies in Figure 3.

The rectangular and circular shapes shown for the transmission-line 15 are for convenience of illustration. They can be any shape, including geometrically irregular, so long as they have a length appropriate to the desired operating frequency, i.e. so that a signal leaving an amplifier 21 arrives back inverted after a full 'lap' of the transmission-line 15, i.e. effectively the spacing between the loops 15a,b plus the crossover 19, traversed in a time T_p effectively defining a pulse width or half-cycle oscillation time of the operating frequency.

Advantages of evenly distributing the amplifiers 21 along the transmission-line 15 are twofold. Firstly, spreading stray capacitance effectively lumped at associated amplifiers 21 for better and easier absorbing into the transmission-line characteristic impedance Z_0 thus reducing and signal reflection effects and improving poor waveshape definition. Secondly, the signal amplitude determined by the supply voltages V_+ and GND will be more substantially constant over the entire transmission-line 15 better to compensate for losses associated with the transmission-lines dielectric and conductor materials. A continuous closed-loop transmission-line 15 with regenerative switching means 21 substantially evenly distributed and connected can closely resemble a substantially uniform structure that appears the same at any point. A good rule is for elementary capacitance and inductance (C_e and L_e) associated with each regenerative switching means and forming a resonant shunt tank LC circuit to have a resonant frequency of $1/2 \cdot \pi \cdot \sqrt{L_e \cdot C_e}$ that is greater than the self-sustaining oscillating frequency F (F_3 , F_5 etc.) of the transmission-line 15.

Figure 5a is a distributed electrical equivalent circuit or model of a portion of a transmission-line 15 hereof. It shows alternate distributed resistive (R) and inductive (L) elements connected in series, i.e. R_0 connected in series with L_1 in turn connected in series with R_2 and so on for a portion of loop 15a, and registering L_0 connected in series with R_1 in turn connected in series with L_2 and so on for the adjacent portion of loop 15b; and distributed capacitive elements C_0 and C_1 shown connected in parallel across the transmission-line 15 thus to the loops 15a and 15b between the resistive/inductive elements

R_0/L_1 and the inductive/resistive elements L_0/R_1 , respectively for C_0 and between the inductive/resistive elements L_1/R_2 and the resistive/ inductive elements R_1/L_2 , respectively for C_1 ; where the identities $R_0=R_1=R_2$, $L_1=L_2=L_3$ and $C_0=C_1$ substantially hold and the illustrated distributed RLC model extends over the whole length of the transmission-line 15.

5 Although not shown, there will actually be a parasitic resistive element in parallel with each capacitive element C, specifically its dielectric material.

Figure 5b is a further simplified alternative distributed electrical equivalent circuit or model that ignores resistance, see replacement of those of Figure 5a by further distribution of inductive elements in series at half ($L/2$) their value (L) in Figure 5a. This model is useful for

10 understanding basic principles of operation of transmission-lines embodying the invention.

During a 'start-up' phase, i.e. after power is first applied to the amplifiers 21, oscillation will get initiated from amplification of inherent noise within the amplifiers 21, thus begin substantially chaotically though it will quickly settle to oscillation at a fundamental frequency F , typically within nano-seconds. For each amplifier 21, respective signals from its

15 inverters 23a and 23b arrive back inverted after experiencing a propagation delay T_p around the transmission-line 15. This propagation delay T_p is a function of the inductive and capacitive parameters of the transmission-line 15; which, as expressed in henrys per metre (L) and in farads per metre (C) to include all capacitive loading of the transmission-line, lead to a characteristic impedance $Z_0 = \sqrt{L/C}$ and a line traverse or propagation or phase

20 velocity $P_v = 1/\sqrt{L/C}$. Reinforcement, i.e. selective amplification, of those frequencies for which the delay T_p is an integer sub-divisor of a half-cycle time gives rise to the dominant lowest frequency, i.e. the fundamental frequency $F = 1/(2 \cdot T_p)$, for which the sub-divisor condition is satisfied. All other integer multiples of this frequency also satisfy this sub-divisor condition, but gain of the amplifiers 21 'falls off', i.e. decreases, for higher frequencies, so the

25 transmission-line 15 will quickly settle to fundamental oscillation at the frequency F .

The transmission-line 15 has endless electromagnetic continuity, which, along with fast switching times of preferred transistors in the inverters 23a and 23b, leads to a strongly square wave-form containing odd harmonics of the fundamental frequency F in effectively reinforced oscillation. At the fundamental oscillating frequency F , including the odd harmonic

frequencies, the terminals of the amplifiers 21 appear substantially unloaded, due to the transmission-line 15 being 'closed-loop' without any form of termination, which results very desirably in low power dissipation and low drive requirements. The inductance and capacitance per unit length of the transmission-line 15 can be altered independently, as can
 5 also be desirable and advantageous.

Figure 6a shows idealised waveforms for a switching amplifier 21 with inverters 23a and 23b. Component oscillation waveforms $\Phi 1$, $\Phi 2$ appear at the input/output terminals of that amplifier 21 shortly after the 'start-up' phase, and continue during normal operation. These waveforms $\Phi 1$ and $\Phi 2$ are substantially square and differential, i.e. two-phase inverse
 10 in being 180 degrees out-of-phase. These differential waveforms $\Phi 1$ and $\Phi 2$ cross substantially at the mid-point ($V+/2$) of the maximum signal amplitude ($V+$). This mid point ($V+/2$) can be considered as a 'null' point since the instant that both the waveforms $\Phi 1$ and $\Phi 2$ are at the same potential, there is no displacement current flow present in nor any differential voltage between the conductive loop traces 15a and 15b. For the preferred
 15 recirculating travelling wave aspect of this invention, this null point effectively sweeps round the transmission line 15 with very fast rise and fall times and a very 'clean' square-wave form definition. This null point is also effectively a reference voltage for opposite excursions of a full cycle bipolar clock signal.

For the transmission-line 15, it is convenient to consider complete laps as traversed
 20 by a travelling wave, and also total length S of the originating conductive trace 17, both in terms of 'electrical length'. Figure 6b shows relationships between the propagation delay or traverse time (T_p), electrical length in degrees, and physical length (S) of originating conductive line/trace 17. For each of the out-of-phase waveforms $\Phi 1$ and $\Phi 2$, and as seen by a travelling wave repeatedly traversing the transmission-line 15, each substantially square
 25 wave excursion corresponds to one complete lap, i.e. one traverse time T_p , and successive opposite wave excursions require two consecutive laps, i.e. two traverse times ($2 \times T_p$). One lap of the transmission-line 15 thus has an 'electrical length' of 180 degrees, and two laps are required for a full $0^\circ - 360^\circ$ bipolar signal cycle, i.e. corresponding to the full lengths of the originating conductor 17.

By way of example, an electrical length of 180° corresponding to one lap and $1/2$ wavelength at 1GHz could be formed from a 50mm transmission-line having a phase velocity (P_v) that is 30% that of the speed of light (c), i.e. $P_v=0.3*c$, or 5mm where $P_v=0.03*c$, or 166mm in free space, i.e. where $P_v=1*c$.

5 Figures 7(i) - 7(ix) show waveforms Φ_1 , Φ_2 through a full cycle to start of the next cycle, specifically at eight equal electrical-length spacings of 45 degrees between sample positions along the conductor line or trace 17. Phase labellings are relative to Fig 7(i) which can be anywhere along the trace 17, i.e. twice round the transmission line 15, as such, and 0/360-degrees for rise/fall of the Φ_1 , Φ_2 waveforms 15 is arbitrarily marked. Taking Figure
10 7(i) as time t_0 , Figure 7(ii) shows the waveforms Φ_1 , Φ_2 at time $t_0+(0.25T_p)$ after one-eighth (0.125S) traverse of total length S of the line 17, thus traverse of one-quarter of the transmission line 15, and 45-degrees of electrical length. Times $t_0+(0.5T_p)$, $t_0+(0.75T_p)$, $t_0+(0.75T_p)$ $t_0+(2T_p)$; traverses 0.25S, 0.375S, 0.5S.....1.0S and 90, 135, 180.....360-degrees should readily be seen self-evidently to apply to Figures 7(iii) - (ix),
15 respectively.

 Figures 8a and 8b show snap-shots of excursion polarity (shown circled), displacement current flow (shown by light on-trace arrows), and instantaneous phasing from an arbitrary 0/360-degree position on the electromagnetically endless transmission line 15 covering two laps thereof (thus the full length the continuous originating conductor 17). Only
20 one differential travelling electromagnetic (EM) waveform (say Φ_1) of Figure 7 is shown, but for rotation propagation around the transmission-line 15 in either of opposite directions, i.e. clockwise or counter-clockwise. The other waveform (Φ_2) will, of course be 180° out of phase with the illustrated waveform (Φ_1). The actual direction of rotation of the EM wave will be given by Poyntings' vector, i.e. the cross product of the electric and magnetic vectors. The
25 crossover region 19 produces no significant perturbation of the signals Φ_1 or Φ_2 as the EM wave traverses this region 19. In effect, the fast rise/fall transitions travel round the transmission-line at phase velocity P_v , the switching amplifiers 21 serving to amplify the transitions during first switching between supply voltage levels.

- 13 -

The phases of the waveforms $\Phi 1$ and $\Phi 2$ can, for a transmission-line 15 hereof, be accurately determined from any arbitrary reference point on the transmission-line 15, thus have strong coherence and stability of phasing.

Suitable (indeed preferred in relation to present IC manufacturing technology and practice) switching amplifiers 21 for bidirectional operation are based on back-to-back Mosfet inverters 23a,b, for which up to well over 1,000 switching inverting amplifier pairs could be provided along typical lengths of transmission-line structures hereof.

The bidirectional inverting action of the switching amplifiers 21 is of synchronous rectification nature. The rise and fall times of the waveforms $\Phi 1$ and $\Phi 2$ are very fast indeed compared with hitherto conventional timing signals, being based on electron-transit-time of preferred Mosfet transistors of the inverters 23a,b. Moreover, reinforcement is related to the transmission-line 15 having lower impedance than any 'on' transistor in inverters of preferred bidirectional switching amplifiers 21, though total paralleled is usefully of the same order. Switching of such inverters means that each amplifier 21 contributes to the resulting wave polarity by way of a small energy pulse which, by symmetry, must propagate in both directions, the forwardly directed EM wave pulse thus contributing as desired. The reverse EM wave pulse that travels back to the previously switched amplifier 21 is of the same polarity as already exists there, thus reinforces the pre-existing switched state. Ohmic paths between power supply rails and the transmission line 15 through 'on' transistors of the preferred inverters of amplifiers 21 ensure that energy of such reverse EM wave pulses is absorbed into those power supply rails V+,GND, i.e. there is useful power conservation.

It should be appreciated that implementation could be by other than CMOS, e.g. by using N-channel pull-ups, P-channel pull-downs, bipolar transistors, negative resistance devices such as Gunn diodes, Mesfet, etc

Regarding the transmission-lines 15 as such, a suitable medium readily applicable to ICs and PCBs and interconnects generally is as commonly referred to as microstrip or coplanar waveguide or stripline, and well known to be formable lithographically, i.e. by patterning of resists and etching. Practical dielectrics for an on-IC transmission-line include silicon dioxide (SiO_2) often referred to as field oxide, inter-metal dielectrics, and substrate

dielectrics (which can be used at least for semi-insulating structures, e.g. of silicon-on-insulator type).

Figure 9 is a cross-section through a portion of one exemplary on-IC transmission-line formation comprising three metal layers 56, 58 and 60 and two dielectric layers 62 and 64. Middle metal layer 58 is illustrated as comprising the two transmission-line loop conductive traces 15a and 15b that are at least nominally parallel. Upper metal layer 60 could be used as an AC 'ground' plane and could be connected to the positive supply voltage $V+$, lower metal 56 being a 'ground' plane that could be connected to the negative supply voltage GND. The dielectric layers 62 and 64 between the metal transmission-line traces at 58 and 'ground' planes 56 and 58 are typically formed using silicon dioxide (SiO_2). The full illustrated structure is seen as preferable, though maybe not essential in practice, i.e. as to inclusion of either or both of the 'ground' planes and the dielectric layers 62, 64. The physical spacing 66 between the conductive traces 15a, 15b affects the differential and common modes of signal propagation, which should preferably have equal, or substantially equal, velocities in order to achieve minimum dispersion of the electromagnetic field from the spacing 66. Screening properties improve with use of 'ground planes', as does the ability for the structure to drive non-symmetrical, i.e. unbalanced, loads applied to the conductive traces 15a, 15b.

Inter-metal dielectric layers on a typical IC CMOS process are thin, typically about $0.7\mu\text{m}$, so microstrip transmission-line features with low signal losses must have a low characteristic impedance Z_0 (as hitherto for unterminated, partially terminated or series terminated lines acting to reduce signal reflections to a manageable level). Self-sustaining, non-terminated, closed-loop transmission-lines 15 hereof inherently have very low power consumption for maintained travelling EM wave oscillation as the dielectric and conductor losses to be overcome are typically low. From Figure 5b, it will be appreciated that, if there were no resistive losses associated with the transmission-line 15 and amplifiers 21, the transmission-line 15 would require no more energy than required initially to 'charge-up' the transmission-lines inductive L_e and capacitive C_e elements. The EM wave would continually travel around the transmission-line with all energy in the transmission-line 15 simply

transferred, or recycled between its electric and magnetic fields, thus capacitive C_e and inductive L_e elements. Whilst there must be some resistive losses associated with the transmission-line 15 and amplifiers 21, see transmission-line resistive elements R_0 - R_2 in Figure 5a, the resistance is typically low and associated resistive losses will be also low.

5 There is no penalty herein from for using low-impedance transmission-lines 15, even advantage from being less affected by capacitive loading, thus resulting in 'stiffer' drive to logic gates.

A crossover 19 can be implemented on an IC using 'vias' between the metal layers, preferably with each via only a small fraction of total length S of the transmission-line 15.

10 A variant is available where a transmission-line 15 hereof has only one amplifier 21 connected to the transmission-line, and the EM wave no longer travels around the transmission-line 15 so that a standing wave oscillation results, see Figure 10a for single amplifier 21 and Figure 10b for differential waveforms. Such amplifier should not extend over more than approximately 5° of the electrical length of the transmission-line 15. If the single

15 amplifier 21 never goes fully 'on' or 'off' a standing sine wave oscillation will result in the transmission-line 15, which will have varying amplitude with the same phases at the same positions including two stationary, two 'null regions'.

It follows that travelling wave operation will be available using a few spaced or just one lengthy CMOS bidirectional inverter formation, though plural small inverters will produce

20 smoother faster results. Offsetting formations of the amplifiers 21, even just its input/output terminals, can predispose a travelling EM wave to one direction of transmission-line traversal, as could specific starter circuit such as based on forcing first and slightly later second pulses onto the transmission-line at different positions, or incorporation of some known microwave directional coupler.

25 Inverting transmission-line transformers can be used instead of the crossovers (19) and still yield a transmission line having endless electromagnetic continuity, see Figure 11 for scrap detail at 21T.

Figure 12 shows a pair of back-to-back inverters 23a, 23b with supply line connectors and indications of distributed inductive ($L/2$) and capacitive (C) elements of a transmission-

line as per Figure 5b. Figure 13a shows N-channel and P-channel Mosfet implementation of the back-to-back inverters 14a and 14b, see out of NMOS and PMOS transistors.

Figure 13b shows an equivalent circuit diagram for NMOS (N1, N2) and PMOS (P1, P2) transistors, together with their parasitic capacitances. The gate terminals of transistors P1 and N1 are connected to the conductive trace 15a and to the drain terminals of transistors P2 and N2. Similarly, the gate terminals of transistors P2 and N2 are connected to the conductive trace 15b and to the drain terminals of transistors P2 and N2. The PMOS gate-source capacitances C_{gsP1} and C_{gsP2} , the PMOS gate-drain capacitances C_{gdP1} and C_{gdP2} , and the PMOS drain-source and substrate capacitances C_{dbP1} and C_{dbP2} , also the NMOS gate-source capacitances C_{gsN1} and C_{gsN2} , the NMOS gate-drain capacitances C_{gdN1} and C_{gdN2} , and the NMOS drain-source and substrate capacitances C_{dbN1} and C_{dbN2} are effectively absorbed into the characteristic impedance Z_0 of the transmission-line, so have much less effect upon transit times of the individual NMOS and PMOS transistors. The rise and fall times of the waveforms $\Phi 1$ and $\Phi 2$ are thus much faster than for prior circuits.

For clarity Figures 12-14 omit related resistive (R) elements. Figure 23a shows only the capacitive elements (as per Figures 12 and 13b) of the transmission-line 15 together with those of the N/PMOS transistors. Figure 14b illustrates another equivalent circuit diagram for Figure 14a including the transmission-line distributed inductive (L/2) elements and the effective capacitance C_{eff} given by:

$$C_{eff} = C + C_{gdN} + C_{gdP} + [(C_{gsN} + C_{dbN} + C_{gsP} + C_{dbP}) / 4];$$

Where:

$$C_{gdN} = C_{gdN1} + C_{gdN2};$$

$$C_{gdP} = C_{gdP1} + C_{gdP2};$$

$$C_{gsN} = C_{gsN1} + C_{gsN2};$$

$$C_{dbN} = C_{dbN1} + C_{dbN2};$$

$$C_{gsP} = C_{gsP1} + C_{gsP2}; \text{ and}$$

$$C_{dbP} = C_{dbP1} + C_{dbP2}.$$

Capacitance loading due to gate, drain, source and substrate junction capacitances are preferably distributed as mentioned previously.

An advantage of having a differential- and common-mode, transmission-line, is that 'parasitic' capacitances inherent within mosfet transistors can be absorbed into the transmission-line impedance Z_0 , as illustrated in Figures 14a and 14b, and can therefore be used for energy transfer and storage. The gate-source capacitances (C_{gs}) of the NMOS and PMOS transistors appear between the signal conductor traces 15a, 15b and their respective supply voltage rails and can be compensated for by removing the appropriate amount of respective capacitance from connections of the transmission-line 15 to the supply voltage rails, say by thinning the conductor traces 15a, 15b by an appropriate amount. The gate-drain capacitance (C_{gd}) of the NMOS and PMOS transistors appear between the conductive traces 15a and 15b and can be compensated for by proportionally increasing the spacing 66 between the conductive traces 15a, 15b at connections to the NMOS and PMOS transistors of the inverters 23a/b.

By way of a non-restrictive example, on a 0.35 micron CMOS process, a usable 5GHz non-overlapping clock signal should result with transmission-line loop length ($S/2$) of 9mm for a phase velocity of 30% of speed-of-light, as determined by capacitive shunt loading distribution and dielectric constants, the total length (S), of the conductor 17 thus being 18mm.

The substrate junction capacitances (C_{db}) of the NMOS and PMOS transistor could be dramatically reduced by using semi-insulating or silicon-on-insulator type process technologies.

There is a continuous DC path that directly connects the terminals of each of the amplifiers 21, i.e. the respective input/output terminals of each and all of the inverters 23a, 23b, but this path is characterised by having no stable DC operating point. This DC instability is advantageous in relation to the regenerative action of each of the respective amplifiers 21, 21₄ and their positive feedback action.

Transmission-lines 15 hereof can be routed around functional logic blocks as closed-loops that are 'tapped into' to get 'local' clock signals. CMOS inverters can be used as 'tap amplifiers' in a capacitive 'stub' to the transmission-line 15, which can be 'resonated out' by removing an equivalent amount of 'local' capacitance from the transmission-lines, say by local

thinning of conductor traces (15a/15b) as above. Capacitive 'clock taps' can be spread substantially evenly along a transmission-line 15 hereof having due regard as a matter of design to their spacings, which, if less than the wavelength of the oscillating signal, will tend to slow the propagation of the EM wave and lower the characteristic impedance Z_0 of the transmission-line (15), but will still result in good signal transmission characteristics.

Within functional logic blocks that are small relative to clock signal wavelength, unterminated interconnects work adequately for local clocking with phase coherence, see Figure 15. For clarity, the pairs of connections to the transmission-line 15 are shown slightly offset, though they would typically be opposite each other in practice. Alternative tap-off provisions include light bidirectional or passive resistive, inductive or transmission-line nature, or unidirectional or inverting connections, including much as for what will now be described for interconnecting transmission-lines 15 themselves.

Plural oscillators and transmission-lines 15 can readily be operatively connected or coupled together in an also inventive manner, including synchronising with each other both in terms of phase and frequency provided that any nominal frequency mismatch is not too great. Resistive, capacitive, inductive or correct length direct transmission-line connections/ couplings, or any combinations thereof, can make good bidirectional signal interconnections. Signal connection or coupling between transmission-lines can also be achieved using known coupling techniques as used for microwave micro-strip circuits, generally involving sharing of magnetic and/or electrical flux between adjacent transmission lines. Unidirectional connections can also be advantageous. Connectors and couplings hereof are capable of maintaining synchronicity and coherency of plural transmission-line oscillators throughout a large system, whether within ICs or between IC's say on printed circuit boards (PCBs).

Connection/coupling of two or more transmission-lines and cross-connection rules are similar to Kirchoff's current law but based on the energy going into a junction, i.e. a connection or coupling, of any number of the transmission-lines being equal to the energy coming out of the same junction, i.e. there is no energy accumulation at the junction. When the supply voltage V_+ is constant, the rule is, of course, precisely Kirchoff's current law. By way of a practical example, if there is a junction common to three transmission-lines, the simplest,

but not the only, solution is that one of the transmission-lines has half the characteristic impedance of the other two transmission-lines. Where there are any even number of coupled transmission-lines, their respective characteristic impedances can all be equal. However, there are an infinite number of combinations of impedances which will satisfy Kirchoff's
 5 current law. The cross-connection rule, within a transmission-line, is the same as the rules for coupling two or more transmission-lines described above.

There will be high quality differential signal waveforms $\Phi 1$ and $\Phi 2$, in terms of phase and amplitude, at all points around a transmission-line network 15 when the following criteria are met :

- 10 (i) the transmission-lines have substantially matching electrical lengths
- (ii) above Kirchoff-like power rules are satisfied
- (iii) there is phase inversion.

There are, of course, an infinite number of coupled network designs and supply voltages that will fulfil the above three criteria, such as for example: short sections of slow, low impedance
 15 transmission-lines that are coupled to long fast, high impedance transmission-lines; and one- and/or three-dimensional structures etc. However, for the best wave-shapes and lowest parasitic power losses, the phase velocities of the common-mode and the differential-mode, i.e. even and odd modes, should be substantially the same. The same, or substantially the same, phase velocities can be designed into a system by varying the capacitances of the
 20 transmission-lines.

The supply voltage $V+$ does not have to be constant throughout a system, provided that above Kirchoff-like power/impedance relationships are maintained and result in an inherent voltage transformation system that, when combined with the inherent synchronous rectification of the inverters 23a and 23b, allows different parts of the system to operate at
 25 different supply voltages, and power to be passed bi-directionally between such different parts of the system.

Figure 16 shows two substantially identical transmission-line oscillators hereof that are operatively connected such that they are substantially self-synchronising with respect to frequency and phase. The transmission-lines 15_1 and 15_2 are shown 'siamesed' with the

common part of their loop conductive traces meeting above Kirchoff-like power/impedance rule by reason of its impedance being half the impedances (20) of the remainders of the transmission-lines 15_1 and 15_2 , because the common parts carry rotating wave energy of both of the two transmission-lines 15_1 and 15_2 . As noted above, the originating trace length S of a transmission-line is one factor in determining the frequency of oscillation so transmission-lines 15_1 and 15_2 using the same medium and of substantially identical length S will have substantially the same frequency of oscillation F and will be substantially phase coherent. In Figure 10, respective EM waves will travel and re-circulate in opposite directions around the transmission-lines 15_1 and 15_2 , see marked arrows 1L, 2L (or both opposite), in a manner analogous to cog wheels. Such siamesing connection of transmission-lines can readily be extended sequentially to any number of such 'cogged' transmission-line oscillators.

Figure 17a shows another example of two substantially identical transmission-line oscillators with their transmission lines 15_1 and 15_2 operatively connected to be substantially self-synchronising in frequency and phase by direct connections at two discrete positions 40 and 42. Figure 17b shows such direct connections via passive elements 44, 46 that could be resistive, capacitive or inductive or any viable combination thereof. Figure 17c shows such direct connections via unidirectional means 48 that can be two inverters 50_1 and 50_2 . The unidirectional means 48 ensures that there is no coupling or signal reflection from one of the transmission-lines (15_2) back into the other (15_1), i.e. only the other way about. Directions of travel of re-circulating EM waves are again indicated by arrows 1L, 2L that are solid but arbitrary for transmission-line oscillator 15_1 and dashed for 15_2 in accordance with expectations as to a 'parallel'-coupled pair of transmission-lines yielding contra-directional travelling waves. Figure 18 is a convenient simplified representation of the two self-synchronised transmission-line oscillators of Figure 17a, and similar representations will be used in following Figures.

Figure 19a shows four self-synchronised transmission-line oscillators $15_1 - 15_4$ connected together basically as for Figures 17a - 17c, but so as further to afford a central fifth effective transmission-line timing signal source of this invention affording a re-circulatory travelling EM wave according to indicated EM wave lapping directions 1L - 4L of the four

transmission-line oscillators $15_1 - 15_4$. As shown the central fifth transmission-line oscillator physically comprises parts of each of the other four, and has a lapping direction $5L$ that is opposite to theirs, specifically clockwise for counter-clockwise $1L - 4L$. It will be appreciated that this way of connecting transmission-line oscillators together can also be extended to any
 5 desired number and any desired variety of overall pattern to cover any desired area.

An alternative is shown in Figure 19b where the central fifth transmission-line oscillator is not of re-circulating type, but is nonetheless useful and could be advantageous as to access to desired phases of timing signals.

Figure 20 shows two self-synchronising oscillators with their transmission-lines 15_1
 10 and 15_2 not physically connected together, rather operatively coupled magnetically; for which purpose it can be advantageous to use elongated transmission-lines to achieve more and better magnetic coupling. Figure 21 shows another example of magnetically coupled self-synchronising oscillators with transmission-lines 15_1 and 15_2 generally as for Figure 20, but with an coupling enhancing ferromagnetic strip 52 operatively placed between adjacent parts
 15 to be magnetically coupled.

Figure 22 shows three self-synchronising oscillators with their transmission-lines 15_1 , 15_2 and 15_3 magnetically coupled by a first ferrous strip 52 placed between transmission-lines 15_1 and 15_2 and a second ferrous strip 54 placed between transmission-lines 15_2 and 15_3 . As a source of oscillating signals, the transmission-line 15_2 does not need any regenerative
 20 provisions 21 so long as enough energy for oscillation is magnetically coupled from the other transmission-lines 15_1 and 15_3 that are complete with provisions 21. It is considered practical for the transmission-line 15_2 to be longer and circumscribe a larger area but not to need or have regenerative provisions 21, nor a cross-over 19; and is then preferably an odd multiple (3S, 5S, 7S etc) of the length (S) or at least the electrical length of at least one of the
 25 transmission-lines 15_1 and 15_3 . This, of course, has further implications for self-synchronising frequency- and phase-locking of oscillators (say as using transmission-lines 15_1 and 15_3), at a considerable spacing apart.

Further alternatives include use of a dielectric material (not illustrated) that spans over and/or under the portions of the conductive traces to be electromagnetically coupled.

It is feasible and practical to synchronise transmission-line oscillators operating at different frequencies. In Figure 24, transmission-lines of two self-synchronising oscillators are of different electrical lengths. Specifically, using same transmission-line structure/materials, first transmission-line 15₁ has a total conductive length S for a fundamental oscillating frequency $F=F_1$ and is operatively connected and synchronised to a second transmission-line 15₂ having a total conductive length that is one third of that of the first transmission-line 15₁, i.e. $S/3$, thus an oscillating frequency of $3F$. The dashed lines with arrows indicate the direction of rotation of the EM waves. Operative connection is as for Figures 17a - c, though any other technique could be used. Self-synchronising is due to above-mentioned presence in the highly square first transmission-line signal of a strong third harmonic ($3F$). Similar results are available for higher odd harmonics, i.e. at frequencies of $5F$, $7F$ etc.

Preferred coupling between transmission-lines of oscillators operating at such different odd harmonic related frequencies, is unidirectional so that the naturally lower frequency line (15₁) is not encouraged to try to synchronise to the naturally higher frequency line (15₂). Any number of transmission-line oscillators of different odd-harmonically related frequencies can be coupled together and synchronised as for Figure 24.

Re-circulatory transmission-line oscillators hereof can be used in and for the generation and distribution of reference, i.e. clock, timing signal(s) in and of a semiconductor integrated circuit (IC); and is also applicable to a printed-circuit-board (PCB), e.g. as serving to mount and interconnect circuitry that may include plural ICs, or indeed, any other suitable apparatus/system where timing reference signal(s) is/are required.

For ICs as such, simulations using the industry standard SPICE techniques show potential for supplying clock signals of very high frequencies indeed, up to several tens of GHz, depending upon the IC manufacturing process employed and projections for their development. Generation and distribution can effectively be at, and service, all parts of an IC with predictable phases at and phase relationships between such parts, including as multiple clock signals that may have the same or different frequencies. Moreover, principles of operation of transmission-line oscillators hereof and their self-synchronising inter-coupling extend or lead readily not only to reliable service of timing signals to operational circuitry

within any particular IC and between ICs, but further and it is believed also importantly and inventively to data transfer between ICs etc.

The entire transmission-line 15 structure and network involving regenerative circuits 21 oscillates. The transmission-line 15 operates unterminated, i.e. the transmission-line forms
 5 a closed-loop. The characteristic impedance Z_0 of the transmission-line is low and only 'top-up' energy is required to maintain oscillation.

Impedance between the two conductor traces 15a, 15b is preferably evenly distributed, thus well balanced, which helps achieve well defined, differential signal waveforms (Φ_1 , Φ_2). Coherent oscillation occurs when the signals Φ_1 , Φ_2 on the
 10 transmission-line 15 meet this 180° , or substantially a 180° , phase shift requirement for all inverting amplifiers 21 connected to the transmission-line 15 i.e. when all the amplifiers 21 operate in a co-ordinated manner with known phase relationship between all points along the transmission-line 15. Signal energy is transmitted into the transmission-line 15 both inductively and capacitively, i.e. magnetically and electrically, between the signal conductors
 15 15a, 15b for the differential-mode, also between each signal conductor and the ground reference for the two individual common-mode (not present if the upper and lower 'ground' planes are absent, nor for connections via unshielded twisted-pair cables).

CMOS inverters as non-linear, operative switching and amplifying circuit elements have low losses from cross-conduction current as normally lossy transistor gate 'input' and
 20 drain 'output' capacitances are absorbed into the characteristic impedance Z_0 of the transmission-line 15, along with the transistor substrate capacitances, so power consumption is not subject to the usual $\frac{1}{2}CV^2$ formula.

It is quite often assumed that the power dissipation due to capacitive charging and discharging of MOS transistor gates, for example, is unavoidable. However, the self
 25 sustaining oscillating nature of the transmission-line 15 is able to 'drive' the transistor gate terminals with low power loss. This is due to the fact that the required 'drive' energy is alternating between the electrostatic field, i.e. the capacitive field of the MOS gate capacitances, and the magnetic field, i.e. the inductive field elements of the transmission-line 15. Therefore, the energy contained within the transmission-line 15 is not being completely

dissipated, it is in fact being recycled. Energy saving applies to all operatively connected transistor gates of the transmission-line 15.

It is envisaged that low loss efficiency of transmission-line oscillator hereof could well be used to 'clock' ICs for many previously popular logic systems that have since been
 5 overshadowed or abandoned as non-viable options for reasons attributed to problems associated with clock skew, clock distribution, power consumption etc. Non-exhaustive examples of such logic arrangements include poly-phase logic and charge recovery or adiabatic switching logic, such logic arrangements being known to those skilled in the art.

Figure 24 shows a possible clock distribution network hereof as applied to a
 10 monolithic IC 68 (not to scale, as is other Figures hereof) . The IC 68 has a plural transmission-lines hereof shown as loops 1L-13L, of which loops 1L-10L and 13L all have the same effective lengths (say as for S above) and oscillate at a frequency F, and loops 11L and 12L each have shorter loop lengths (say as for S/3 above) and oscillate at a frequency 3F. Loops 1L-8L and 11L-13L are full transmission-line oscillator complete with regenerative
 15 means, and loops 9L and 10L arise as parts of four of the former transmission-lines, namely 1L, 3L, 4L and 5L; 4L, 5L, 6L and 8L respectively.

The transmission-line (15) of the loop 13L is elongated with a long side close to the edge (i.e. scribe line) of the IC 68, so that it is possible to couple to another similarly set up separate monolithic IC for inter-coupling by such as flip-chip technology for frequency and
 20 phase locking by such as magnetic coupling, as described above. Phase and frequency locking of separate monolithic IC's can be very useful in such as hybrid systems.

Figure 25 indicates feasibility of a three-dimensional network of interconnected transmission line oscillators hereof for signal distribution, specifically for a simple pyramidal arrangement, though any other structure could be serviced as desired, no matter how
 25 complex so long as interconnect rules hereof are met regarding electrical length, impedance matching, any phasing requirements for data transfer, etc.

ICs hereof can be designed to have whatever may be desired up to total frequency and phase locking, also phase coherence, including for and between two or more self-sustaining transmission-line oscillators greatly to facilitate synchronous control and operation

of data processing activities at and between all the various logic and processing blocks associated with such IC.

Figure 26a shows an example of dual phase tap-off using a pair of CMOS inverters 70₁ and 70₂ connected to the transmission-line conductive traces 15a and 15b respectively to provide local clock to and/or to be distributed about a logic block 72₁. Whilst the logic block 72₁ is shown as being 'enclosed' within the transmission-line 15 alternatives include it being outside any area enclosed by the transmission-line 15, as for the logic block 72₂ and its associated inverters 70₃, 70₄, and/or it spanning the conductive traces 15a, 15b of the transmission line 15. If desired, say for large logic blocks 72₁ and/or 72₂ plural pairs of inverters 70 can 'tap' into the transmission-line 15, including for any desired phasing needed locally in the logic block 72, see dashed line. Capability accurately to select the phase of the oscillating clock signals Φ_1 , Φ_2 allows complex pipeline logic and poly-phase logic (see Figure 29 below) to be operatively designed and controlled.

Figure 26b differs in that the logic blocks 71₁, 72₂ are replaced by respective processing elements 73₁, 73₂, though there could be more, and for which one or more transmission-lines can be used to clock one or more of the processing elements. Two or a greater plurality of processing elements can operate independently and/or together, i.e. in parallel to achieve very fast and powerful data processing ICs/systems.

Figure 27a shows concentrically arranged transmission-lines 15₁-15₃ of progressively less physical lengths. However, each of the three transmission-lines 15₁-15₃ can be made so that they all oscillate at the same frequency, whether as a matter of structure or by respective velocities of the EM waves rotating around each of the shorter transmission-lines 15₂ and 15₃ being suitably retarded by increasing their inductance and/or capacitance per unit length. Moreover, the transmission-lines 15₁-15₃ can optionally have one or more operative connections 70 and 72 that will serve to synchronise the three transmission-lines 15₁-15₃. The advantages, apart from synchronicity, of having these connections 70, 72 ~~are that the~~ transmission-lines 15₁-15₃ will or can

- (i) act as a single multi-filament transmission-line;
- (ii) have smaller conductive traces (15a, 15b);

- (iii) cover a larger clocking area;
- (iv) produce lower skin effect losses; and
- (v) produce lower crosstalk and coupling.

Figure 28a shows a transmission-line having a cross-loop connection between
 5 positions A, B, C and D, which comprises further transmission-line 15c, 15d that has, in this
 particular example, an electrical length of 90° to match spacing of the positions A, B and C, D.
 Other cross-connection electrical length could be chosen, then operatively connected at
 correspondingly different spacings of the positions A, B and C, D. Cross-loop connections
 allow further tap-off positions within area enclosed by the transmission-line 15. The
 10 transmission-line part 15d is shown connected in parallel, between points A and C, and part
 of the transmission-line 15 represented by line 74. Likewise, the transmission-line part 15c is
 shown connected in parallel, between points B and D, with part of the transmission-line 15
 represented by line 76. The transmission-line parts 15c, 15d, 74 and 76 will be satisfactory if
 they each have an impedance that is half that associated with the remainder of the
 15 transmission-line 15, as above. The transmission-lines 15 and 15c,d will have operatively
 connected amplifiers 21. Figure 28b shows the cross-loop connection 15c,d and the positions
 A, B, C and D set up relative to parts 78 and 80 of the transmission-line 15, i.e. instead of
 parts 74 and 76, respectively; but with Kirchoff-type rules applying again to result in parts
 15c, 15d, 78 and 80 each having an impedance of half that associated with the remainder of
 20 the transmission-line 15. Introduction of plural additional transmission-lines such as 15c,d
 across a transmission-line 15 is feasible as required.

Figure 29a shows one way to produce four-phase clock signals. Effectively, a
 transmission-line 15 makes a double traverse of its signal carrying boundary, shown as
 rectangular, and further repeated traverses could produce yet more phases. In the example
 25 shown, the positions A1, A2, B1 and B2 will yield localised four-phase clock signals, as will
 the positions C1, C2, D1, and D2. The repeated boundary traverses will be with suitable
 mutual spacing/separation of the transmission-line 15 to avoid inter-coupling. Figure 29b
 shows idealised four-phase signal waveforms at points A1, A2, B1 and B2 and at C1, C2, D1
 and D2.

Figure 30 shows addition of an open-ended passive transmission-line (15e, 15f) connected to the closed-loop transmission-line 15 and having the characteristics, of having an electrical length of 180° , of producing no adverse effect at the tap point, since it acts as an open-circuit oscillating stub. Amplifiers 21 will not be present along this open-ended line 15e,f
 5 but inverters 23 could be far ends of each of the traces 15c and 15d to reduce risk of spurious oscillations. Indeed, turned oscillation in such stubs 15e,f can have useful regenerative effects for the transmission-line 15 and thus serve for reinforcement and/or stability purposes.

Passive transmission-line connections with no particular requirement for impedance matching can be used to connect oscillating transmission-lines of the same, or substantially
 10 the same, frequency together, at least provided that enough inter-connections are established between two systems, at connection positions with the same relative phases in the inter-connected networks. Such connections can assist in synchronising high speed digital signals between IC's and systems because non-clock signals (i.e. the IC/system data lines) will have similar delay characteristics if they are incorporated into the same routing (e.g. ribbon cable,
 15 twisted pair, transmission-line) as the clock connections, thus making data and clocking coherent between different systems.

Figure 31 shows one example of coherent frequency and phase operation of two clock distribution networks of two monolithic ICs 68_1 , 68_2 each having a clock generation and distribution hereof and pairs of inter-IC connections E, F and G, H. The two ICs concerned
 20 will operate coherently, i.e. at the same frequency and with the same phase relationships, where each of the connections is substantially of 180° -degrees electrical lengths, or a multiple satisfying $360^\circ \cdot n + 180^\circ$ where n is zero or an integer.

A single pair of inter-IC connections (E, F or G, H) will result in frequency and phase 'locking'. More than one pair of inter-IC connections (E, F and G, H as shown) will result
 25 further in clock wave direction or rotation locking.

Also shown in Figure 31 is a first and second 'stub' connections 82 and 83, though there could be more of either or each. The first stub connection 82 has a total electrical length of 180° to assist in stabilising operation. The second stub connection 83 is open-ended and also of 180° electrical length and helpful for stabilisation. Such stubs 82, 83 can

be particularly useful for non-IC applications of the invention where conductive trace definition may be less precise than for ICs.

Impedance of the pairs of connections E, F and G, H and connections 82, 83 can have any value since, in normal operation and once these connections are energised, there
 5 will be no net power flow therein for correct phasing thereof. It is, however, preferred that the impedance of these connections E, F and G, H and 82, 83 is greater than that of oscillator transmission-lines 15 to which they are connected. These connections will support a standing EM wave rather than a travelling EM wave.

Such Figure 31 inter-connections can be applied equally well to intra-IC, inter-IC, IC-
 10 to-PCB and/or any non-IC, i.e. PCB-to-PCB system connections.

Figure 32a shows two interconnected monolithic IC's 68₁, 68₂ that are phase and rotation locked and that further have a plurality of bidirectional data latches 84 and links 86 between them inventively affording separate data processing system connection to act as one coherent structure as to phasing and further as to data transfer. Interconnection positions on
 15 the transmission-lines 15 concerned here substantially, a 180° phase difference between ends J, K of each line inter-IC connection, though there is usually a tolerance of at least 1°. The plurality of inter-IC connections 86 can be of 'twisted pair' nature connected between corresponding transmission-lines 15 of both IC's 68₁, 68₂. Impedances of these inter-IC connections 86 are again preferably higher than that associated with the clock generation
 20 transmission-lines 15.

It is not necessary for there to be equal numbers of clock/phase and data connections. Moreover, the data and clock transmission mediums 86 are of the same length and electrically matched, so both exhibit the same propagation delays, which is advantageous. The nominal 180° phase difference represents a half clock cycle, i.e. T_p , so a
 25 data pulse transmitted from either IC to the other by the rising edge of the clock waveform Φ_1 , will be received during, or just after, the rising edge of the clock waveform Φ_2 .

Figure 32b shows the preferred inventive data latch 84 of Figure 32a as a block. The data latch 84 is edge triggered by the differential clock signals Φ_1 and Φ_2 for transmission

(TX) and receiving (RX); and has differential bidirectional input/output lines, data pulse control lines labelled TX Data and RX Data, and the clock signal waveforms $\Phi 1$, $\Phi 2$.

Techniques hereof greatly facilitate communicating data latches 84 on different IC's 68₁, 68₂ being clocked with the same relative phasing. Moreover, Figure 32a indicates that
 5 respective communicating pairs of latches 84 are triggered on different phases, which results in wholly advantageous multi-phase data transfer that eliminates need for simultaneous switching of the transmission-lines 86, thus results in reduction of 'ground bounce' and positive supply voltage dips.

In half duplex data transfer wherein, two data bits are transferred, one each way,
 10 during each clock cycle. For data transfer (TX) from one IC to the other, and for local logic control where $\Phi 1=1$, $\Phi 2=0$ and logic 1= $V+$ and logic 0=GND, the corresponding latches 84 at each IC both transmit a single bit of data for the period where $\Phi 1=1$, one data bit going from IC 68₁ to IC 68₂, and another data bit going from IC 68₂ to IC 68₁ in each half cycle. The data signals pass each other on the transmission-line 86, and do not interfere in the twisted pair
 15 nature of the transmission-line 86. The last received data signal is usable in this half cycle. When $\Phi 1$ and $\Phi 2$ are 180° from going high and low, respectively, data is received and the local logic states are $\Phi 1=0$, $\Phi 2=1$. The same latches 84 at each of the two IC's now both receive a single bit of data that was sent during the previous half cycle, when $\Phi 2=1$.

Figure 32c shows a circuit to implement the data latch 84. Transistors P1, N1, P5
 20 and N5 are operatively arranged and controlled to produce the differential output signals and are only active, i.e. switched 'on', when $\Phi 1=1$. Either P1 and N5 turn on for a positive differential output signal, or P5 and N1 turn on for a negative differential output signal. Transistors N4, P4, N8 and P8 are operatively arranged and controlled to allow transistors P1, N1, P5 and N5 to switch 'on' only when $\Phi 1=1$, i.e. during the transmit time. Transistors
 25 P2, N2, P6 and N6 are operatively arranged and controlled to switch 'off' the output transistors P1, N1, P5 and N5 when $\Phi 2=1$, i.e. during the receive time.

Transistor N3 is operatively arranged and controlled by the TX Data control signal for its associated differential bidirectional output to go positive, i.e. $V+$, via transistors N4 and P1, when the TX Data control signal is a logic 1. Transistor P3 is operatively arranged and

controlled by the TX Data control signal for its associated differential bidirectional output to go negative, i.e. GND, via transistors P4 and N1, when the TX Data control signal is a logic 0. The inverter I1 is operatively arranged and controlled such that it produces the inverse logic state of the TX Data control signal.

5 Transistor N7 is operatively arranged and controlled by the TX Data control signal for its associated differential bidirectional output to go positive, via transistors N8 and P5, when the TX Data control signal is a logic 0. Transistor P7 is operatively arranged and controlled by the TX Data control signal for its associated differential bidirectional output to go negative, via transistors P8 and N5, when the TX Data control signal is a logic 1.

10 Transistor N13 is operatively arranged and controlled to terminate the differential transmission-line 86 correctly during the receipt (RX) of a data signal. Transistor T13 has an operative "on-resistance" that approximately equals the characteristic impedance of the transmission-line 86.

Transistors N1-8 and P1-8 together with inverter I1 constitute the transmit circuitry
15 TX1 of the bidirectional latch 84.

Transistors N9 and N10 are operatively arranged and controlled to 'sample' for a whole half cycle, onto capacitor C1, the differential signal during the receipt (RX) of a data signal. Transistors N11 and N12 are operatively arranged and controlled to switch the stored charge sample of capacitor C1 onto the operatively arranged and controlled differential-to-
20 single ended converter. This differential-to-single ended converter is made up by the operatively arranged and controlled inverters I2, I3 and capacitor C2. Inverter I3 and capacitor C3 are operatively arranged as a voltage reference and inverter I2 is operatively arranged and controlled such that it acts as a single ended logic output buffer/amplifier for the sampled received (RX'd) data signal.

25 Transistors N9-N11 and inverters I2 and I3 together with capacitors C1 and C2 constitute the receiving circuitry RX1 of the bidirectional latch 84.

The following is a truth table that summarises the operation of the data latch 84 during the transmit (T) and receipt (RX) of data signals.

TX Data	$\Phi 1$	$\Phi 2$	+ve Differential Output	-ve Differential Output
0	0	1	Hi-Z (receiving)	Hi-Z (receiving)
0	1	0	0	1
1	0	1	Hi-Z (receiving)	Hi-Z (receiving)
1	1	0	1	0

It is noted that, for data link transmission-lines 86 with $(360^\circ \cdot n + 180^\circ)$ electrical length there is an additional n cycle latency (delay), but subsequent data is received once per cycle. Furthermore, the phasing could be slightly different from different 180° for TX and RX circuitry within the I/O data latch 84 circuit so as to improve the timing and therefore 'hold times' etc on the data latches 84 and therefore compensate somewhat for switching delays.

The circuit diagram illustrated in Figure 32c does not include additional waveshaping circuitry that may well be required in practice, but could be of well-known nature.

With clean differential waveshapes, package inductance problems are minimised since GND and V+ package connection currents do not arise through the output switching action of the transmission-lines 86 since, the return currents are via the opposite signal of the differential pair and not through the supply pins. The matching of the package impedance to the transmission-lines 86 is therefore easier.

Figure 32d shows an intra-connected IC having plural unidirectional receive and transmit data latches. see 85 and 87. A first pair of unidirectional transmit and receive latches 87_1 , 85_1 are operatively connected to two different transmission-lines for operatively transmitting data from one transmission-line to the other. The first receive latch 85_1 has a 'delay correction through placement' of 45° : where 45° represents the electrical length of respective clock signal connections to the latches 87_1 , 85_1 .

Two pairs of unidirectional transmit/receive latches 85_2 , 87_2 and 85_3 , 87_3 operate in the same manner as 87_1 and 85_1 except that their delay correction through placement is approximately 10° , which represents the electrical length of their clock signal connections.

Figure 32e shows unidirectional transmit and receive latches 85, 87 able to transmit and receive two bits of data per clock cycle if these latches 87, 85 respectively comprise two

co-phase transmit or receive circuits respectively TX1 and RX1, as opposed to each having a transmit and receive circuitry TX1 and RX1.

Figure 33 illustrates digitally selectable shunt capacitors that are formed out of mosfet transistors.

5 Digitally selectable shunt capacitors illustrated in Figure 33 can be operatively connected to the transmission-line 15 and controlled for the travelling EM wave to be delayed slightly, i.e. the frequency of oscillation can be controlled. Such delays are useful for fine tuning the frequency of a transmission-line(s). As shown, eight shunt capacitors are implemented by means of mosfet transistors. The mosfets transistors M1, M2, M5 and M6 are
10 PMOS transistors and mosfet transistors M3, M4, M7 and M8 are NMOS transistors.

The mosfets M1, M3, M5 and M7 have their drain and source terminals connected to the 'inner' transmission-line conductor 15a. for example, and the mosfets M2, M4, M6 and M8 have their drain and source terminals connected to the 'outer' transmission-line conductor 15b. The substrate terminals of mosfets M1, M2, M5 and M6 are connected to the positive
15 supply rail V+ and the substrate terminals of mosfets M3, M4, M7 and M8 are connected to the negative supply rail GND.

The gate terminals of mosfets M1 and M2 are connected together and controlled by a control signal CS0 and the gate terminals of mosfets M3 and M4 are connected together and controlled by the inverse of control signal CS0. Likewise, the gate terminals of mosfets M5
20 and M6 are connected together and controlled by a control signal CS1 and the gate terminals of mosfets M7 and M8 are connected together and controlled by the inverse of control signal CS1.

The following truth table illustrates which mosfet shunt capacitors (M1-M8) contribute capacitance, i.e. 'Mosfets On', to the transmission-line 15.

25

CS0	CS1	Mosfets 'On'	Mosfets 'Off'
0	0	M1-M8	-
0	1	M1-M4	M5-M8
1	0	M5-M8	M1-M4
1	1	-	M1-M8

It is preferred that the respective sizes and numbers of shunt capacitors connected to the 'inner' and 'outer' transmission-line conductive traces 15a, 15b are the same, i.e. balanced. Whilst eight mosfet shunt capacitors M1-M8 are shown, any number of mosfet shunt capacitors having suitable sizes, and hence capacitances, can be used, provided that the transmission-line 15 is balanced, as per Figure 33.

There are other configurations for producing digitally controllable shunt capacitors that, may or may not be formed using mosfet transistors. One known example, again using mosfets, could be the use of binary weighted mosfet capacitors for example. Alternatives to MOS capacitors affording variable capacitance include varactors and P/N diodes for example.

It can be advantageous for the 'capacitor arrays' to be replicated at regular intervals around the transmission-line(s) so as to distribute the impedance.

Figure 34 shows how to route data and/or power across a transmission-line 15 and for altering its capacitive loading by way of formations 88 resembling railway sleepers deposited, preferably at regular intervals below the conductive traces 15a, 15b. Alternatively, formations such as 88 could be deposited above and/or below the transmission-lines conductive traces 15a, 15b. As can be seen from the cross sectional view, the traces 15a, 15b are preferably on a metal layer that is isolated from the formation 88 e.g. by a silicon dioxide 92 layer. These formations 88 have the effect of increasing the transmission-lines capacitance and can therefore be used to alter the transmission-line impedance thus the velocity of the travelling EM wave. These formations 88 can also be used to route data and/or power 99. One advantage of routing data and/or power 99, as illustrated, is that since the clock signals $\Phi 1$, $\Phi 2$ on the transmission-line 15 are differential, these clock signals $\Phi 1$, $\Phi 2$ have no effect upon the routed data and/or power signals.

The bi-directional switches (21) using inverters 23a, 23b inherently act as synchronous rectifiers of the clock frequency as can be deduced by the ohmic path from these inverters most negative supply rail to GND and their most positive supply rail to V+. Therefore, the NMOS and PMOS transistors that constitute the back-to-back inverters 23a

and 23b (see Figure 22b) will always be switched by an incident EM wave on the transmission-line 15 to a state where the two 'on' transistors (an NMOS and PMOS respectively) will connect the most negative transmission-line conductive trace to the local GND supply for an NMOS transistor and the local V+ supply for a PMOS transistor. The two

5 NMOS/PMOS pairs of transistors alternate as the incident EM wave signal polarity reverses for oscillation in the manner of bridge rectification that is synchronous and exemplifies the bi-directionality of the DC-AC-DC conversion mode involved. The transmission-line 15 is thus able to extract and redirect power bi-directionally to supply power to the transmission-line 15 when the local supply rail voltage is greater than the transmission-line voltage and to remove

10 power when the local supply rail voltage is less than the transmission-line voltage, and the transmission-line 15 acts as a power conductor in this mode, see following table:

Inputs	PMOS 'on'	NMOS 'on'	P/NMOS 'off'
15a=GND 15b=V+	P1 (15b connected to local V+)	N2 (15a connected to local GND)	N1, P2
15a=V+ 15b=GND	P2 (15a connected to local V+)	N1 (15b connected to local GND)	N2, P1

This power recycling is particularly appropriate to IC process technologies where the gate length is less than approximately 0.1 microns when the parallel 'on-resistance' will be

15 comparable to the series DC resistance of the supply connections. Such synchronous rectification can act as the basis of power distribution in the absence or impossibility of power supply routing to certain area's of an IC, particularly can be used for 'charge pump' circuitry, i.e. DC-to-DC power conversion. There is also inherent capability for converting DC-to AC power conversion and visa versa. Alternatively, of course, known 'on-chip' transformers could

20 be employed.

The possibility is envisaged of achieving highest possible operating frequencies consistent with disconnectable switching of logic circuitry, including as semiconductor fabrication technology is bound to develop.

Indeed, transmission-line formations themselves should scale with IC process

25 technology, thus smaller and faster transistor formations lead naturally to shorter and faster transmission-line oscillators for yet higher clock frequencies.

Other possibilities include maintaining low power consumption; regardless of applications, which could be as to any resonating of capacitive and inductive connections to a transmission-line, and specifically use relative to such as shift registers or 'precharge'/evaluate' logic.

5 Whilst there is evident advantage in not having to use external timing reference such as a quartz crystal, nor PLL techniques, there may be situations and applications where this invention is applied in conjunction with such external timing crystals etc.

 Whilst detailing herein has been within the context of currently dominant CMOS technology for ICs, it will be appreciated by those skilled in the art that principles are involved
10 that are also applicable to other semiconductor technologies, e.g. Silicon-Germanium (Si-Ge), Gallium-Arsenide (Ga-As) etc.

 Finally, highly beneficial particular utility in overcoming the problems associated with high frequency clocking, e.g. where $F > 1\text{GHz}$, no other applicability of combined timing signal generation and distribution is to be excluded from intended scope hereof, say for systems and
15 apparatus to operate at frequencies less than 1GHz.

20

What is claimed is:

1. **Electronic circuitry comprising active switching operational circuits requiring timing signals, and a conductive distribution means for distributing said timing signals to the operational circuits, wherein the distribution means includes a signal path exhibiting endless electromagnetic continuity**
5 **affording a signal phase inversion and having an associated regenerative active means so as to serve as a source of said timing signals.**
2. **Electronic circuitry according to claim 1, comprising a semiconductor integrated circuit having an active area with features presenting the operational circuits and the distribution means, including**
10 **the signal path and its associated regenerative active means together serving as the source of said timing signals.**
3. **Semiconductor integrated electronic circuit comprising an operational circuitry of active switching nature requiring timing signals, and a conductive distribution means for distributing said timing**
15 **signals to the operational circuitry, wherein a part of the distribution means is a signal path exhibiting endless electromagnetic continuity affording signal phase inversion and having an associated regenerative active means so as to serve as a source of said timing signals.**
4. **Electronic circuitry according to any one of claims 1 to 3, wherein the regenerative active means**
20 **provides switching action relative to two supply voltage levels.**
5. **Electronic circuitry according to claim 4, wherein the regenerative active means provides amplifying action during said switching.**
- 25 6. **Electronic circuitry according to any one of claims 1 to 5, wherein the regenerative active means provides inverting action relative to said timing signals in the signal path.**

7. Electronic circuitry according to any one of claims 1 to 6, wherein the regenerative active means is a bidirectional active means so that said timing signals will have bipolar differential components available anywhere along the signal path at 180° out-of-phase.

5 8. Electronic circuitry according to claim 7, wherein the signal path makes more than one loop in its endless electromagnetic continuity so that said timing signal is available in poly-phase components including quadrature for one additional loop of the same sense.

10 9. Electronic circuitry according to any one of claim 1 to 8, wherein the regenerative active means is physically localized at one position along length of the signal path so that said timing signal will be of standing wave nature.

15 10. Electronic circuitry according claim 7, wherein the bidirectional active means never reaches fully "on" or fully "off" states so that said timing signal is substantially sinusoidal, and the regenerative active means is physically localized at one position along length of the signal path so that said timing signal will be of standing wave nature.

20 11. Electronic circuitry according to any one of claims 1 to 8, wherein the regenerative active means is physically distributed along length of the signal path so that said timing signal is a recirculating travelling wave timing signal.

12. Electronic circuitry according to claim 11, wherein the regenerative active means further comprises plural inverting amplifiers spaced along the signal path.

25 13. Electronic circuitry according to claim 12, wherein the regenerative active means is a bidirectional active means so that said timing signals will have bipolar differential components available anywhere along the signal path at 180° out-of-phase, and the bidirectional active means reaches fully "on" and fully "off" states in relatively short parts of time taken for said travelling wave timing signal to traverse the signal path so that such timing signal is substantially rectangular.

14. Electronic circuitry according to any one of claims 11 to 13, wherein the regenerative active means has input/output terminals connected across the signal path affording endless electromagnetic continuity of DC interconnection of the terminals with no stable DC operating point.

5 15. Electronic circuitry according to any one of claims 1 to 14, wherein the signal path is of transmission-line nature for signals of transverse electromagnetic wave form.

10 16. Electronic circuitry according to any one of claims 1 to 15, wherein the regenerative means serves to top up low energy losses from low impedance of electromagnetically endless said signal path.

15 17. Electronic circuitry according to any one of claims 1 to 14, wherein the signal path is of transmission-line nature and includes a transmission-line transformer means affording said signal phase inversion.

18. Electronic circuitry according to any one of claims 1 to 14, wherein the signal path is a transmission-line signal path comprising spaced generally parallel conductive formations on a substrate with cross-over connection of conductor formations providing a single endless conductive length.

20 19. Electronic circuitry according to claim 18, wherein the transmission-line signal path is a structure of co-planar microstrip/microstrip nature.

25 20. Electronic circuitry according to claim 19, wherein the transmission-line signal path comprises spaced conductive traces sandwiched by dielectric layers and affording differential-mode timing signals.

21. Electronic circuitry according to claim 20, wherein the dielectric layers are sandwiched by conductive layers affording shielding and/or enabling common-mode timing signals.

22. Electronic circuitry according to claims 20 or 21, wherein capacitive and/or inductive reactance of the transmission-line signal path is determined by particular geometry of the conductive traces and their spacing along their lengths.

5 23. Electronic circuitry according to claim 22, wherein the geometry is locally varied as may be required to accommodate reactance of connections to the traces.

10 24. Electronic circuitry according to any one of claims 17 to 23, wherein the signal path has an electrical length of substantially 180-degree and the regenerative means is bidirectional inverting switching and amplifying means.

25. Electronic circuitry according to claim 24, wherein the regenerative means comprises back-to-back inverters.

15 26. Electronic circuitry according to claim 25, wherein the inverters are P-channel and N-channel Mosfet circuits.

20 27. Electronic circuitry according to claim 26, wherein the inverters switch sequentially in one direction around the signal path and are connected to supply voltage lines for passage thereto of energy received from next inverter switching so as to reinforce recirculating traversal of the signal path.

25 28. Electronic circuitry according to any one of claims 1 to 27, wherein the signal path further comprises a cross-connection having an electrical length of substantially half that of the signal path.

29. Electronic circuitry according to any one of claims 1 to 28, wherein the signal path has extent affording physical adjacency to the operational circuits and close electrical connectivity therefor directly to the signal path.

30. Electronic circuitry according to claim 29, further comprising electrical connections to the signal path for signal supply to the operational circuits.

5 31. Electronic circuitry according to claim 30, wherein the connections are by way of capacitive stubs from the signal path, which is a transmission-line signal path.

32. Electronic circuitry according to claim 31, wherein the capacitive stubs are spaced evenly along the transmission-line signal path.

10 33. Electronic circuitry according to claim 30, wherein the connections are by way of Mosfet inverters.

34. Electronic circuitry according to any one of claims 1 to 33, comprising plural signal paths.

15 35. Electronic circuitry according to claim 34, wherein at least two of said plural signal paths are intercoupled to operate synchronously by sharing of magnetic and/or electric fields.

36. Electronic circuitry according to claim 34, wherein at least two said signal paths have a common part with an impedance substantially half that of remainders of the two signal paths.

20 37. Electronic circuitry according to claim 34, wherein at least two said signal paths are interconnected to operate synchronously.

25 38. Electronic circuitry according to claim 37, wherein a self-synchronizing interconnection between said signal paths intended to operate at substantially same frequency is provided via passive circuit means affording light bidirectional coupling.

39. Electronic circuitry according to claim 37, wherein a self-synchronizing interconnection between said signal paths intended to operate at different frequencies having odd harmonic relation is

provided via inverter means poled so that a higher frequency is not affecting a lower frequency.

5 40. Electronic circuitry according to any one of claims 37 to 39, wherein said interconnected signal paths have impedances to assure substantial match of energy into and out of an interconnection concerned.

41. Electronic circuitry according to any one of claims 37 to 40, wherein the signal paths have spaced conductors in loops that are interconnected or intercoupled at matching positions along electrical lengths of their loops relative to means for imposing signal phase inversion.

10 42. Electronic circuitry according to claim 37, wherein said plural signal paths are interconnected directly at mutual electrical lengths of matching multiples of 45-degrees.

15 43. Electronic circuitry according to claim 37, wherein the signal paths are located one within another and have parameter differences to harmonize times of signal traverse.

20 44. Electronic circuitry according to claims 42 to 43, wherein said operational circuits are located in an area corresponding to a nominally rectangular grid array, and said signal paths correspond with areas along rows and columns of said rectangular grid that alternate with intervening areas also serviceable for signal supply for timing purposes.

25 45. Electronic circuitry according to any one of claims 34 to 44, wherein at least one of said signal paths is connected to another path or to an array thereof by way of at least one transmission-line connection having an electrical length nominally of 180 degrees or an odd multiple so as substantially to secure a frequency and phase lock.

46. Electronic circuitry according to claim 45, wherein two said transmission-line connections serve substantially to secure desired lock of direction of signal path traversing by respective timing signals.

47. Electronic circuitry according to any one of claims 11 to 46, wherein at least one connection made to said signal path is of short-circuit nature with an electrical length of substantially 90 degrees.

48. Electronic circuitry according to any one of claims 11 to 47, wherein at least one connection made to said signal path is of open-circuit nature with an electrical length of substantially 180 degrees.

49. Electronic circuitry comprising at least two semiconductor integrated circuits (ICs), each in accordance with any one of claims 1 to 48, for similar signal for timing purposes, and having an IC-interconnection between the signal paths of the ICs over an electrical length and at positions of the signal paths to coordinate frequency and phase coherence of the ICs and to obtain coordinated timing signals.

50. Electronic circuitry according to claim 49, wherein the IC interconnection has an electrical length substantially equal to the electrical length of the signal paths or an odd multiple thereof.

51. Electronic circuitry according to claims 49 or 50, wherein a phase difference at said positions of said interconnection of the ICs corresponds to the electrical length of their signal paths.

52. Electronic circuitry according to claims 49, 50 or 51, further comprising a second different IC interconnection, which serves further to define directions of said timing signals along their signal paths.

53. An electronic pulse generator circuit comprising a signal path exhibiting endless electromagnetic continuity affording signal phase inversion in setting a pulse duration within time of signal traversal of the signal path which has an associated regenerative active means for setting relatively short pulse rise and fall times at ends of each said signal traversal.

54. A travelling wave electronic oscillator circuit comprising recirculatory travelling wave

propagation means affording a closed signal path for imposing phase inversion for each travelling wave circulation, and a regenerative active bidirectional switching and amplifying means operative during each circulation so that opposite voltage excursions result in successive travelling wave circulations.

5

55. Electronic circuitry according to claims 53 to 54, wherein the signal path is of transmission-line nature for signals of transverse electromagnetic wave form.

10

56. Electronic circuitry according to any one of claims 53 to 55, wherein the regenerative means serves to top up low energy losses from low impedance of electromagnetically endless said signal path.

15

57. Electronic circuitry according to claims 53 or 54, wherein the signal path is of transmission-line nature and includes a transmission-line transformer means affording said signal phase inversion.

58. Electronic circuitry according to claims 53 or 54, wherein the signal path is a transmission-line signal path comprising spaced generally parallel conductive formations on a substrate with cross-over connection of conductor formations providing a single endless conductive length.

20

59. Electronic circuitry according to claim 58, wherein the transmission-line signal path is a structure of co-planar microstrip/microstrip nature.

25

60. Electronic circuitry according to claim 59, wherein the transmission-line signal path comprises spaced conductive traces sandwiched by dielectric layers and affording differential-mode timing signals.

61. Electronic circuitry according to claim 60, wherein the dielectric layers are sandwiched by conductive layers affording shielding and/or enabling common-mode timing signals.

62. Electronic circuitry according to claims 60 or 61, wherein capacitive and/or inductive reactance of the transmission-line signal path is determined by particular geometry of the conductive traces and their spacing along their lengths.

5 63. Electronic circuitry according to claim 62, wherein the geometry is locally varied as may be required to accommodate reactance of connections to the traces.

10 64. Electronic circuitry according to any one of claims 57 to 63, wherein the signal path has an electrical length of substantially 180-degree and the regenerative means is bidirectional inverting switching and amplifying means.

65. Electronic circuitry according to claim 64, wherein the regenerative means comprises back-to-back inverters.

15 66. Electronic circuitry according to claim 65, wherein the inverters are P-channel and N-channel Mosfet circuits.

20 67. Electronic circuitry according to claim 66, wherein the inverters switch sequentially in one direction around the signal path and are connected to supply voltage lines for passage thereto of energy received from next inverter switching so as to reinforce recirculating traversal of the signal path.

25 68. Electronic circuitry according to any one of claims 53 to 67, wherein the signal path further comprises a cross-connection having an electrical length of substantially half that of the signal path.

69. Electronic circuitry according to any one of claims 53 to 68, comprising plural signal paths.

70. Electronic circuitry according to claim 69, wherein at least two of said plural signal paths are intercoupled to operate synchronously by sharing of magnetic and/or electric fields.

71. Electronic circuitry according to claim 69, wherein at least two said signal paths have a common part with an impedance substantially half that of remainders of the two signal paths.

72. Electronic circuitry according to claim 69, wherein at least two said signal paths are
5 interconnected to operate synchronously.

73. Electronic circuitry according to claim 72, wherein a self-synchronizing interconnection between said signal paths intended to operate at substantially same frequency is provided via passive circuit means affording light bidirectional coupling.

10 74. Electronic circuitry according to claim 72, wherein a self-synchronizing interconnection between said signal paths intended to operate at different frequencies having odd harmonic relation is provided via inverter means poled so that a higher frequency is not affecting a lower frequency.

15 75. Electronic circuitry according to any one of claims 72 to 74, wherein said interconnected signal paths have impedances to assure substantial match of energy into and out of an interconnection concerned.

20 76. Electronic circuitry according to any one of claims 72 to 75, wherein the signal paths have spaced conductors in loops that are interconnected or intercoupled at matching positions along electrical lengths of their loops relative to means for imposing signal phase inversion.

77. Electronic circuitry according to claim 72, wherein said plural signal paths are interconnected directly at mutual electrical lengths of matching multiples of 45-degrees.

25 78. Electronic circuitry according to claim 72, wherein the signal paths are located one within another and have parameter differences to harmonize times of signal traverse.

79. Electronic circuitry according to any one of claims 69 to 78, wherein at least one of said signal

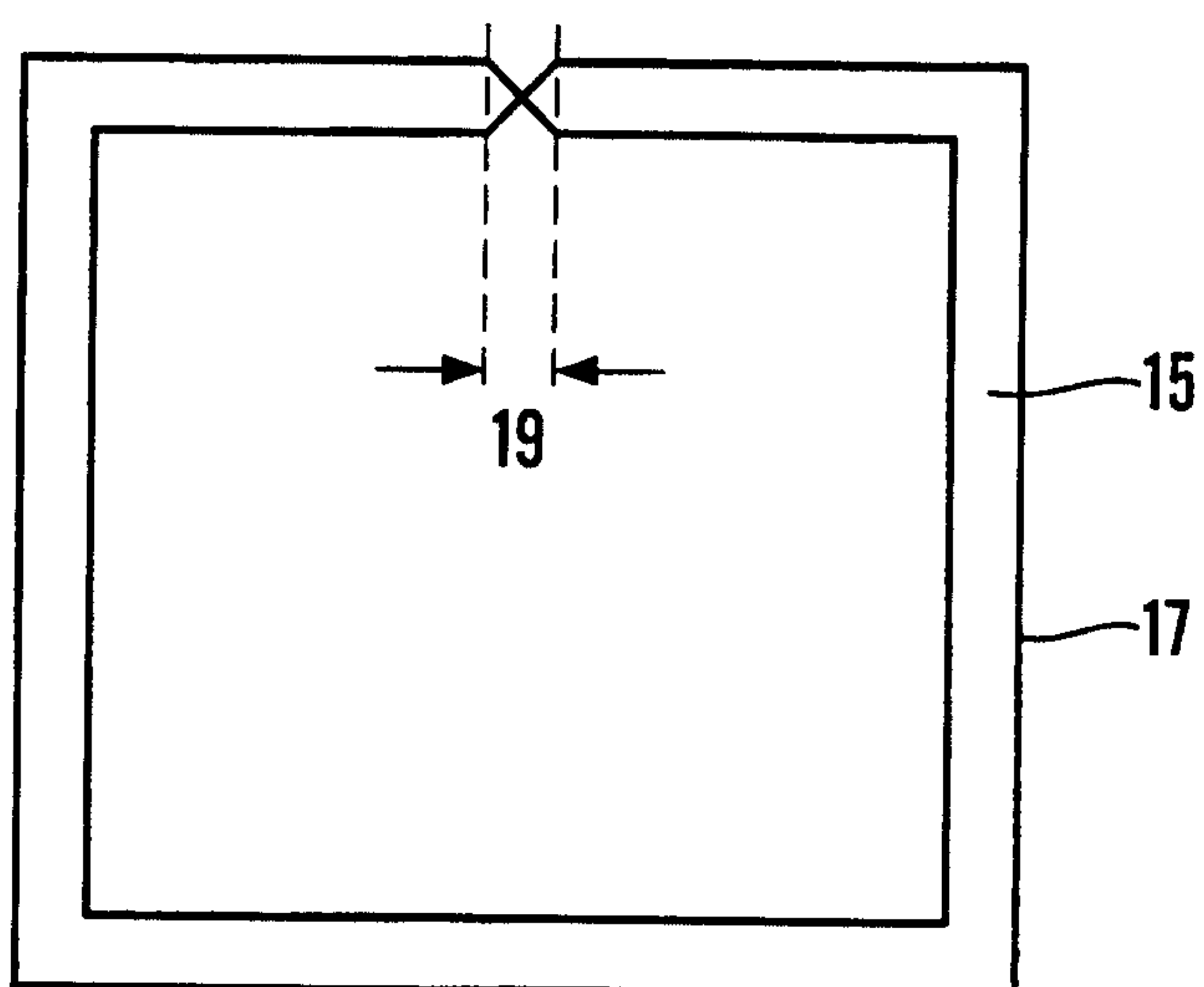
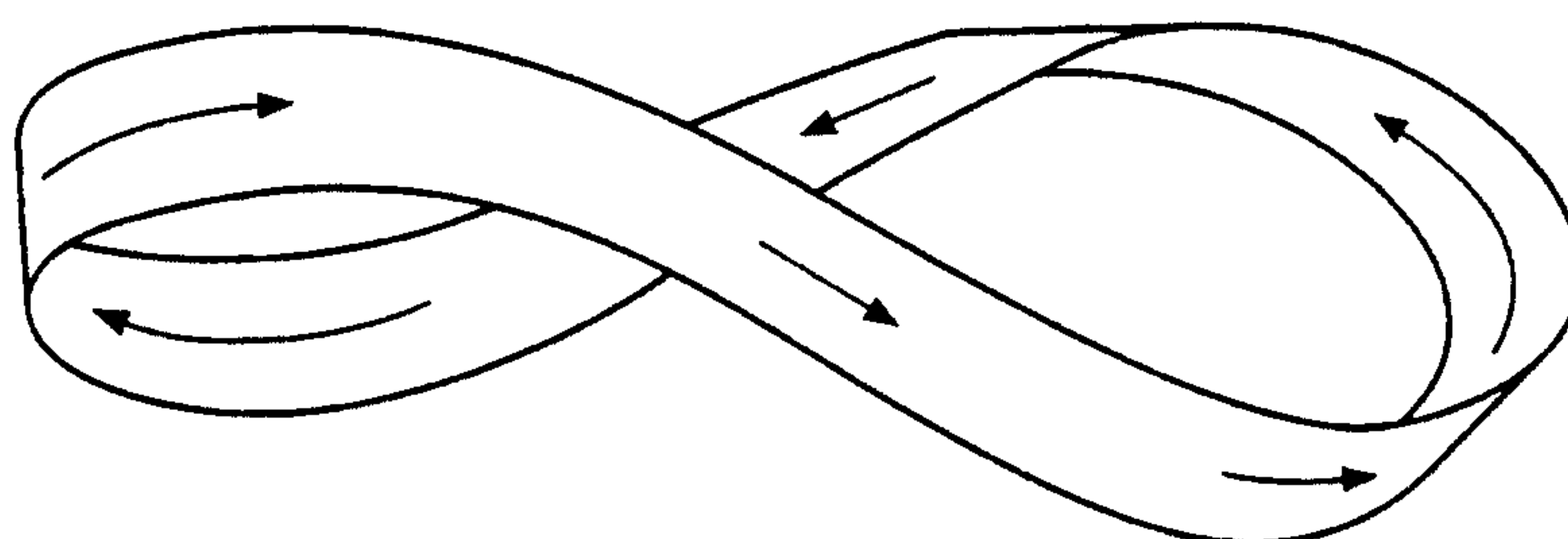
paths is connected to another path or to an array thereof by way of at least one transmission-line connection having an electrical length nominally of 180 degrees or an odd multiple so as substantially to secure a frequency and phase lock.

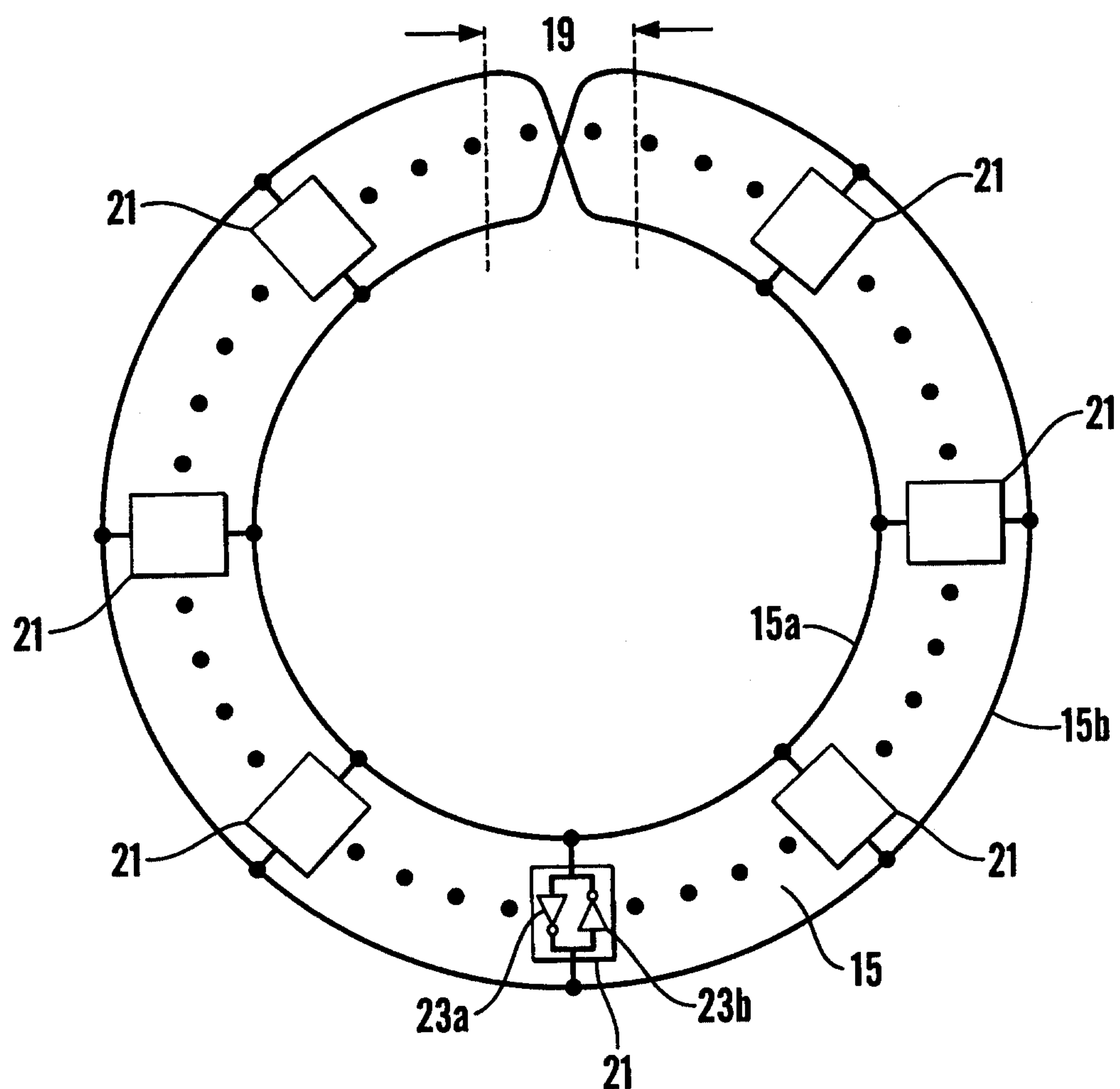
5 80. Electronic circuitry according to claim 79, wherein two said transmission-line connections serve substantially to secure desired lock of direction of signal path traversing by respective timing signals.

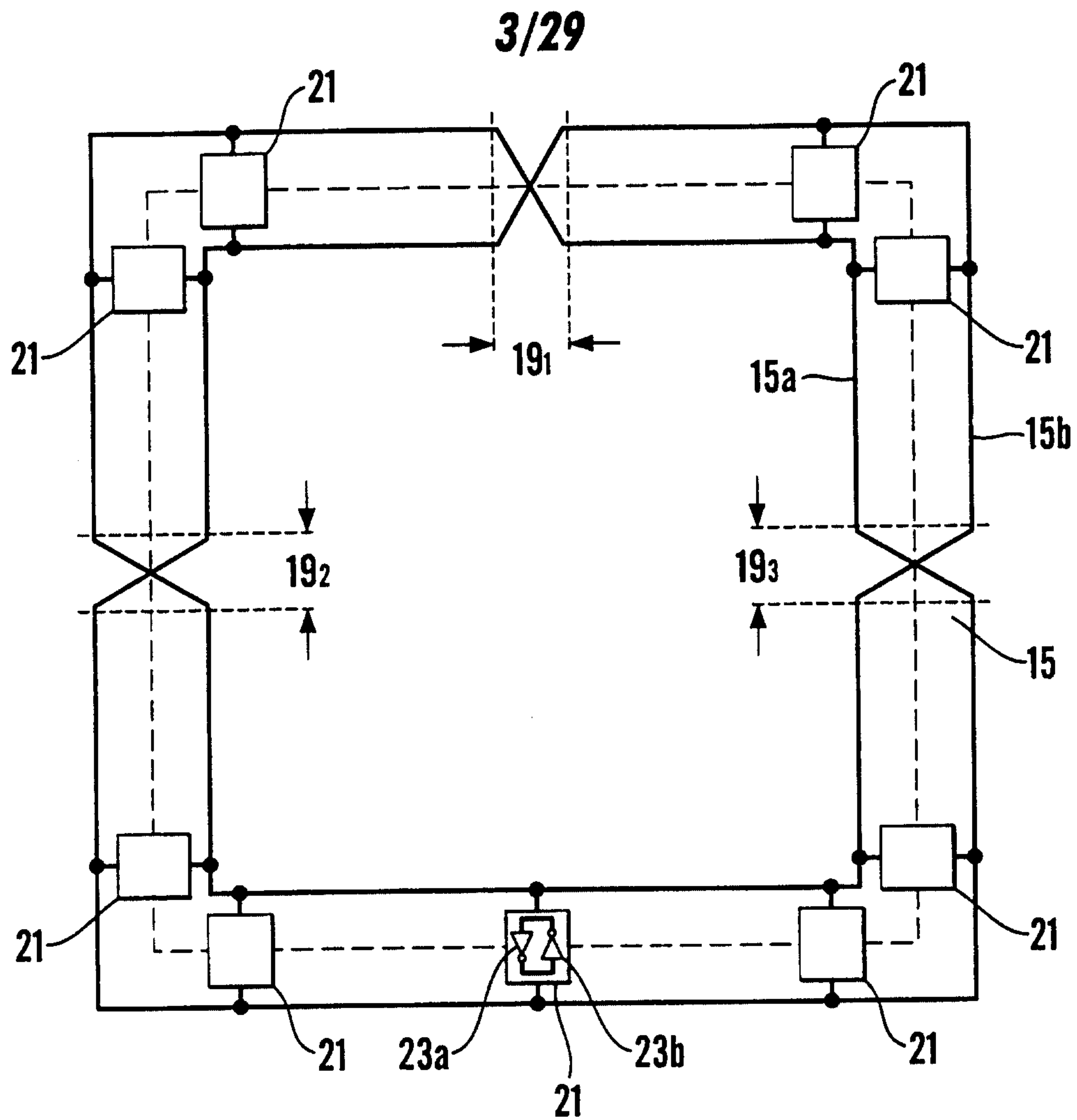
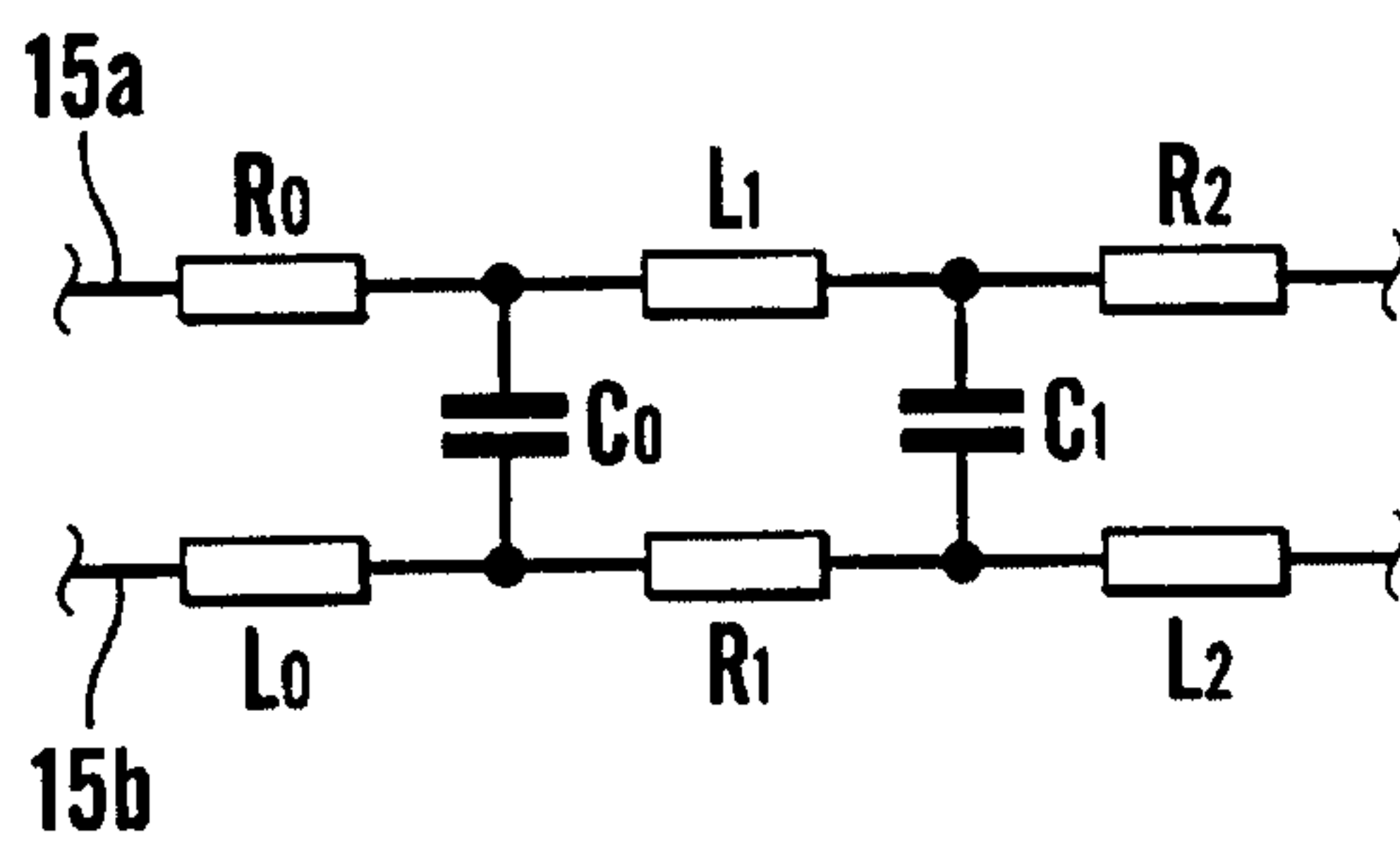
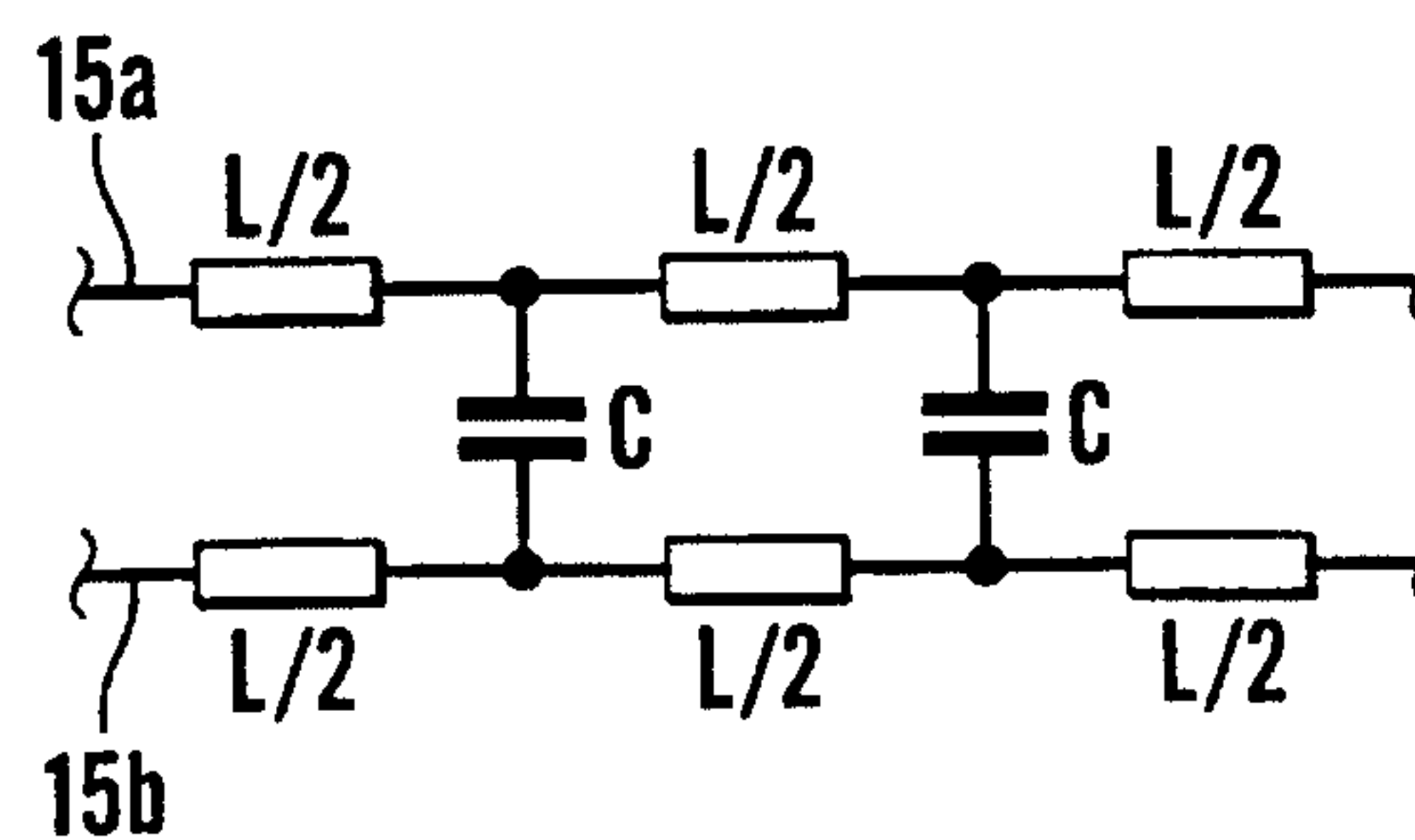
81. Electronic circuitry according to any one of claims 53 to 80, wherein at least one connection made to said signal path is of short-circuit nature with an electrical length of substantially 90 degrees.

10

82. Electronic circuitry according to any one of claims 53 to 81, wherein at least one connection made to said signal path is of open-circuit nature with an electrical length of substantially 180 degrees.

1/29**Fig. 1****Fig. 2**

2/29**Fig.3**

*Fig. 4**Fig. 5a**Fig. 5b*

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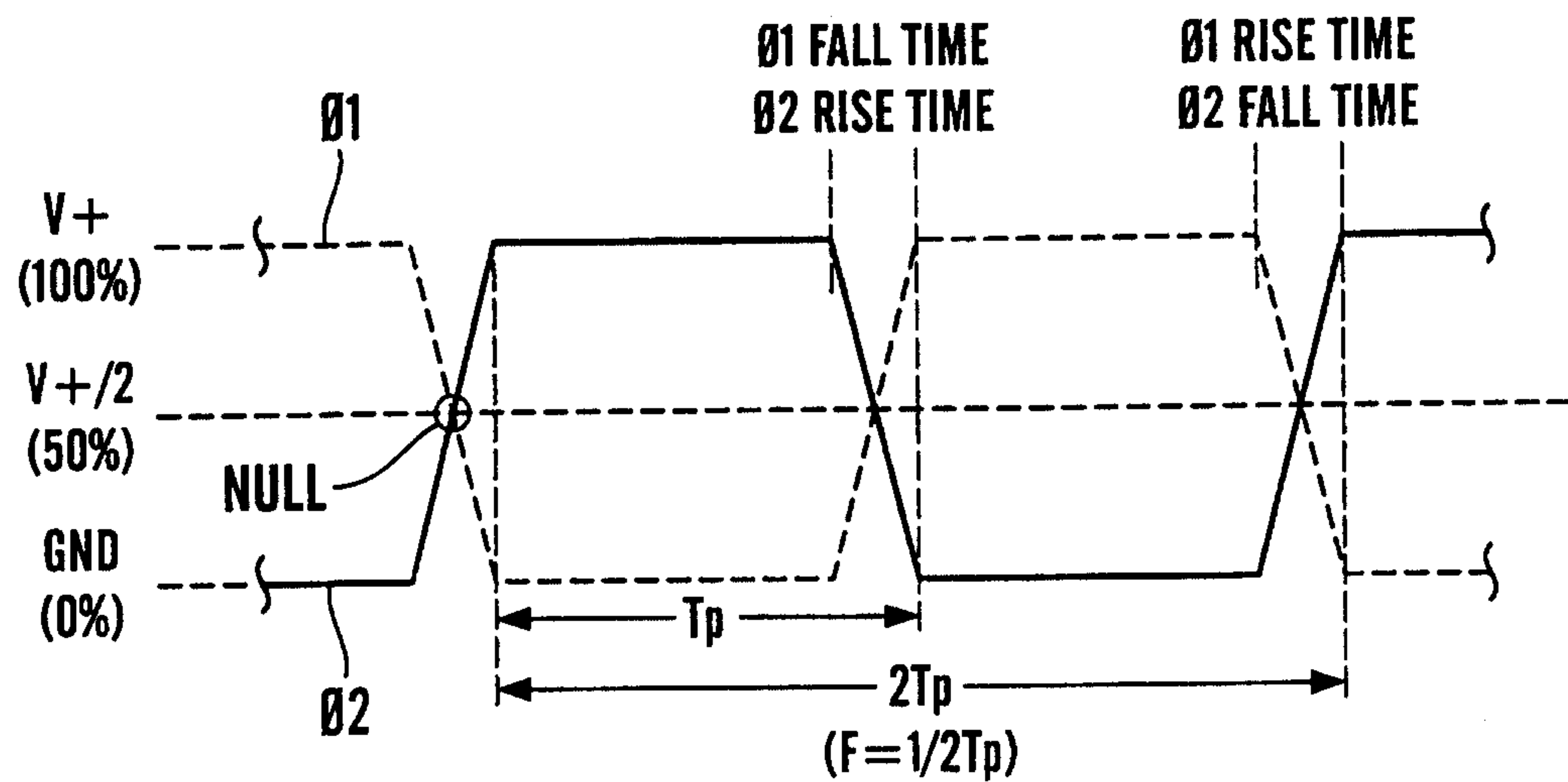


Fig.6a

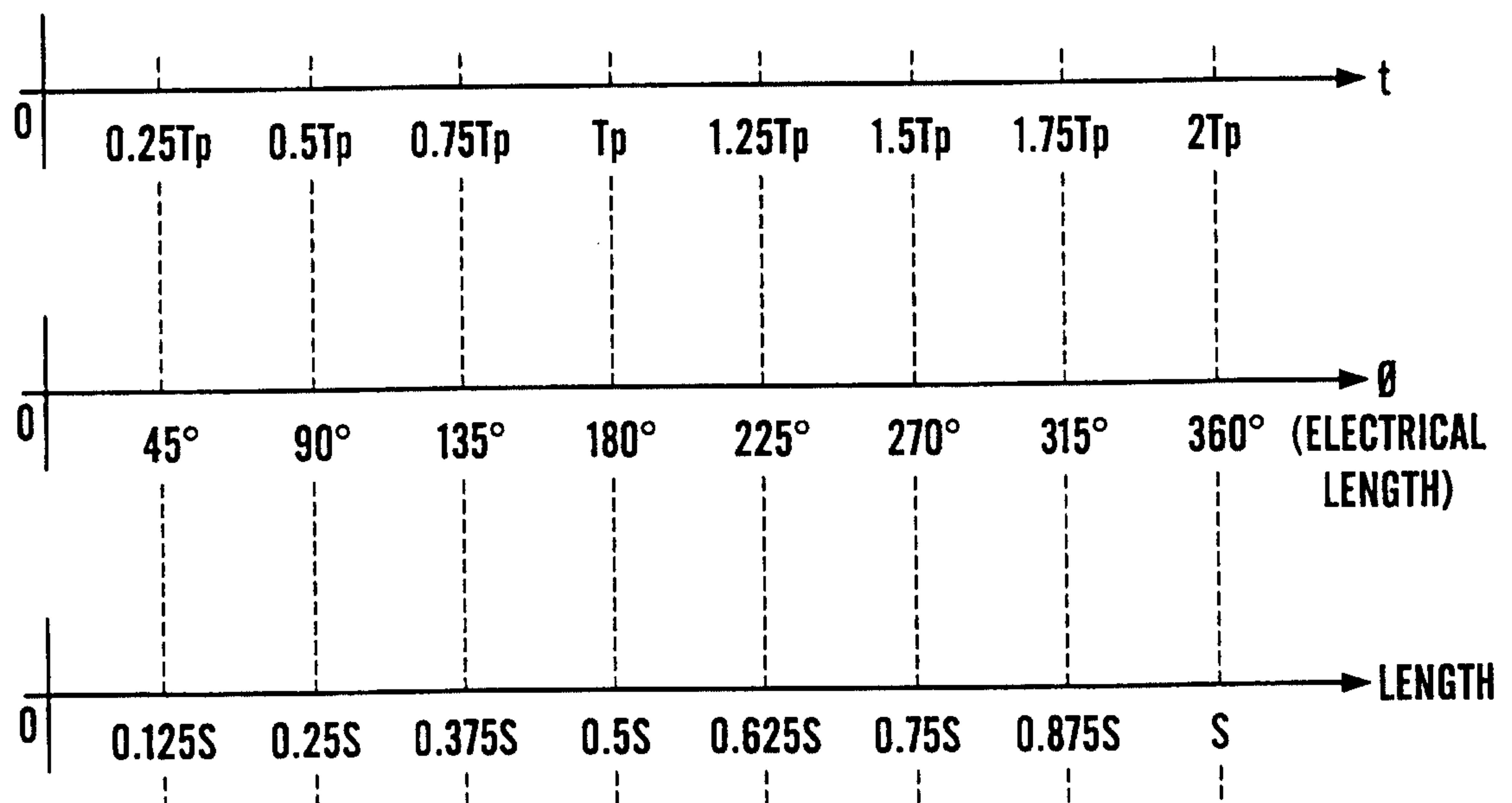


Fig.6b

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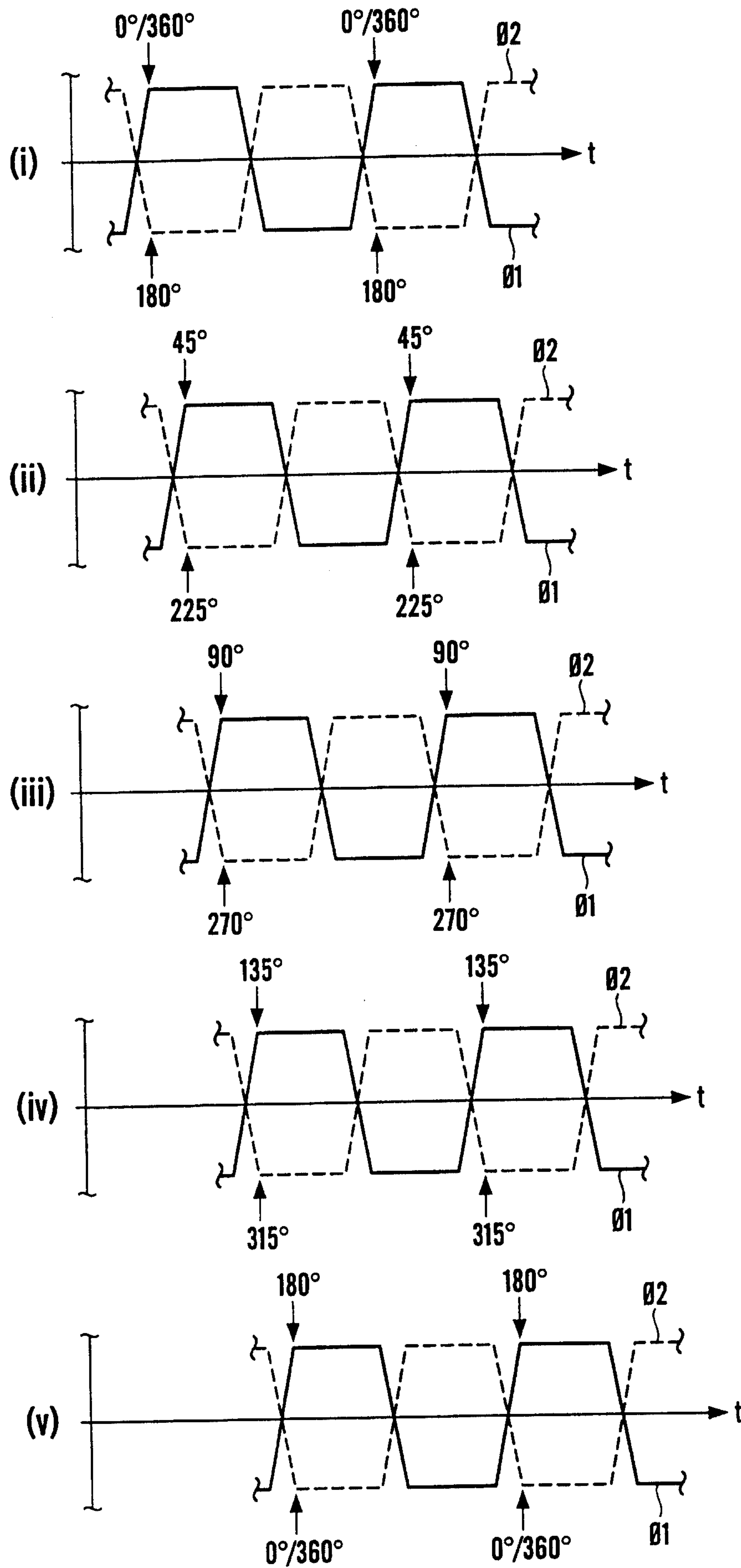


Fig.7

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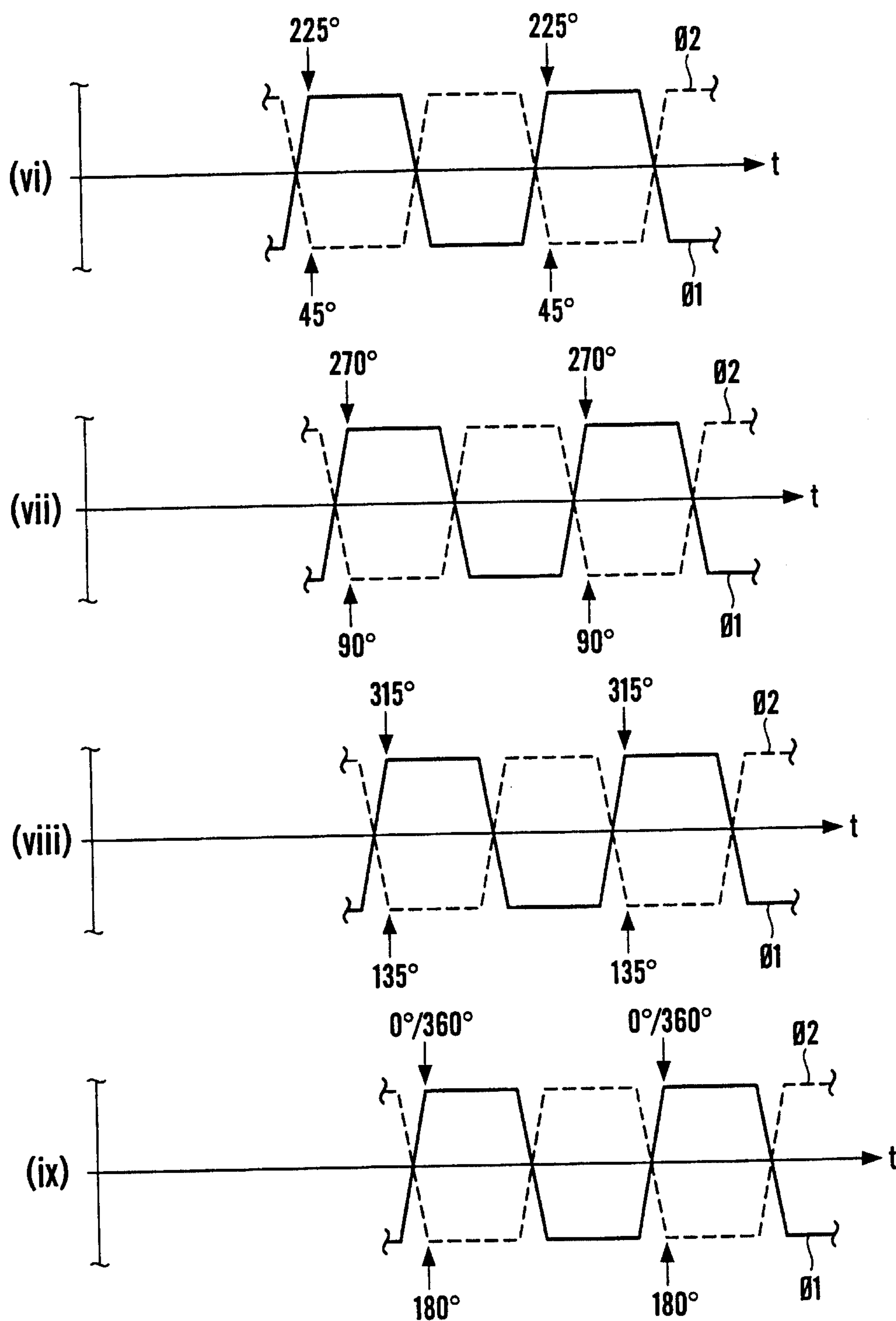
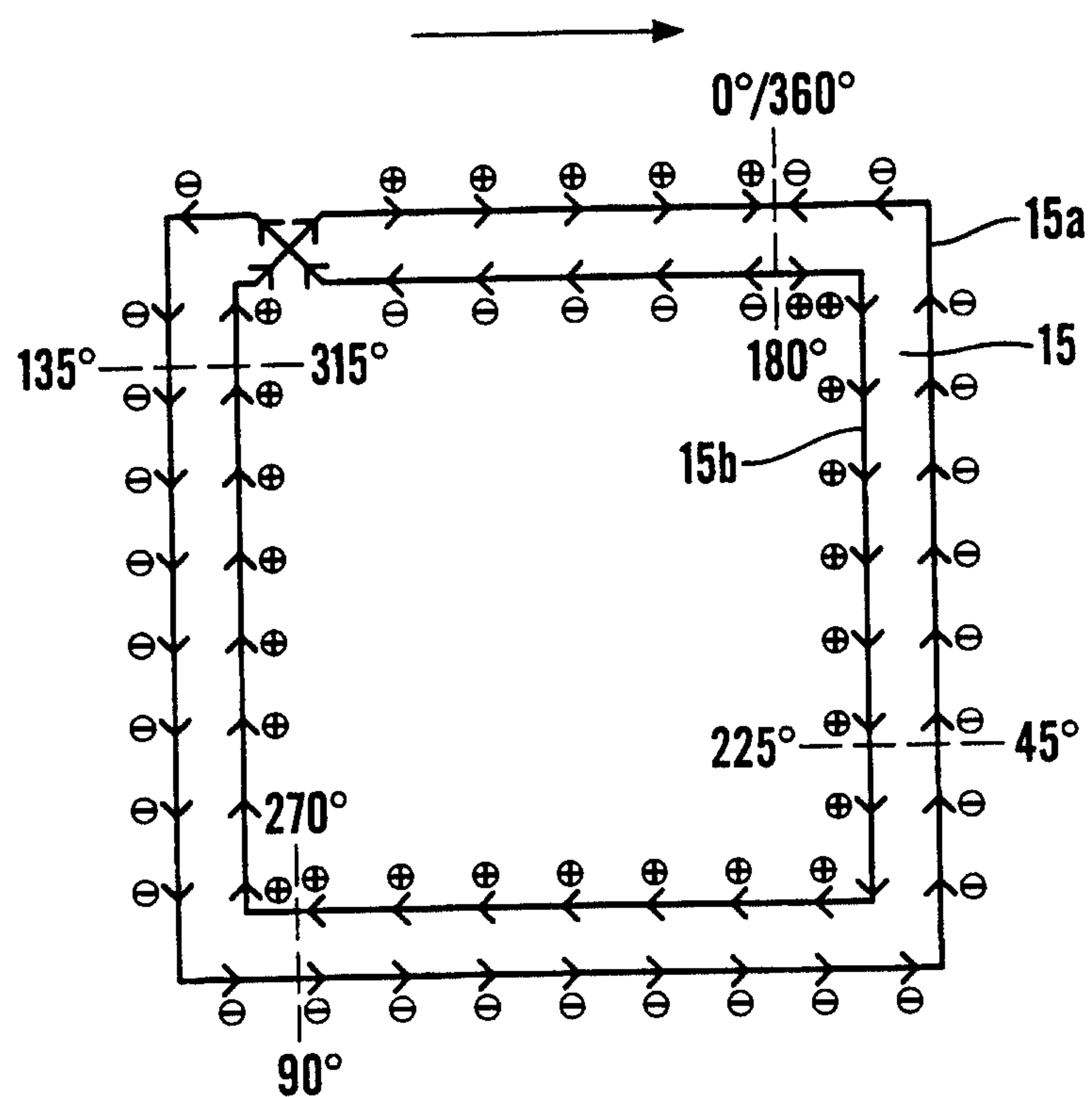
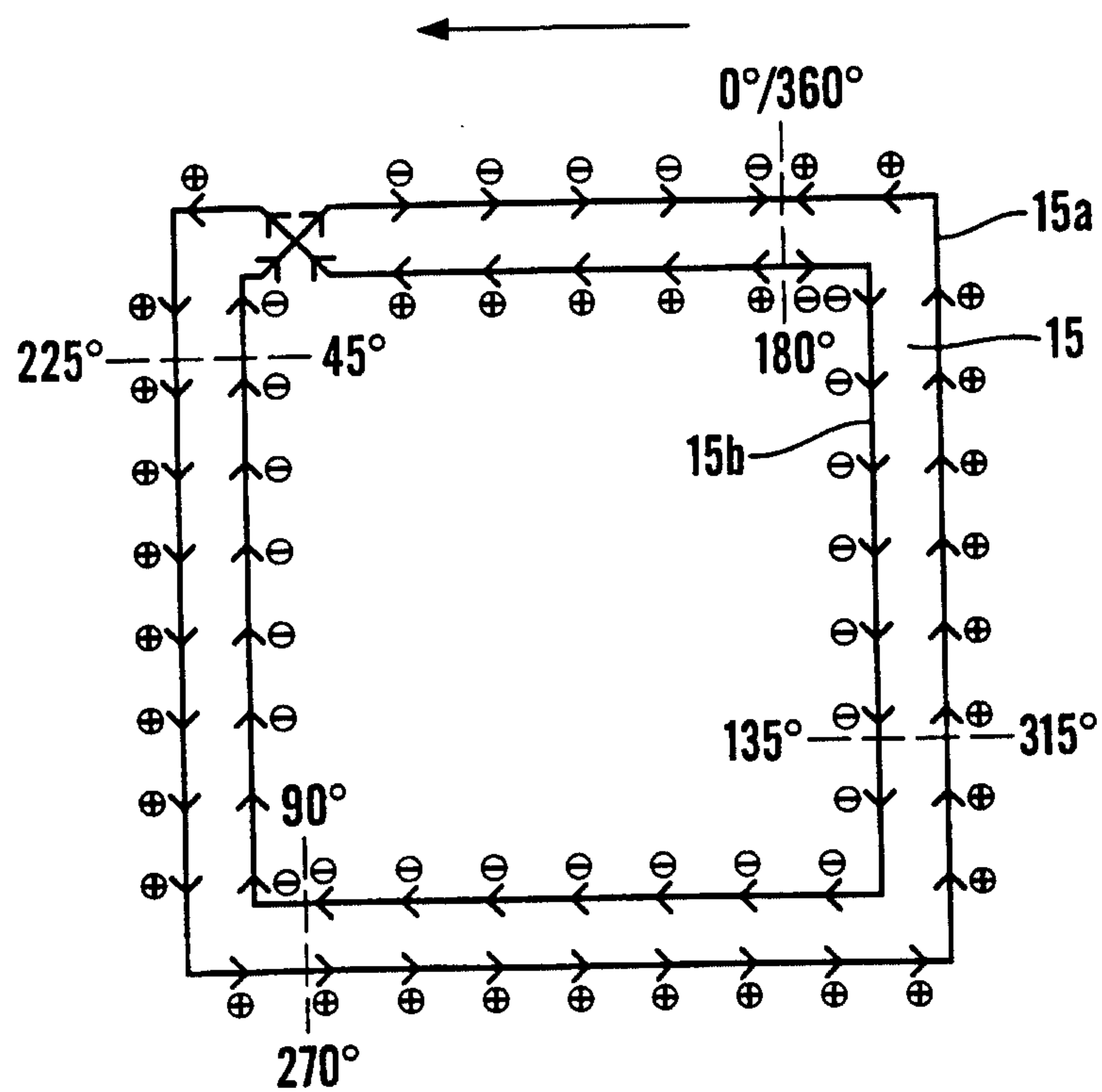


Fig.7(cont.)

7/29**DIRECTION OF ROTATION OF THE
ELECTROMAGNETIC WAVE****Fig.8a****DIRECTION OF ROTATION OF THE
ELECTROMAGNETIC WAVE****Fig.8b**

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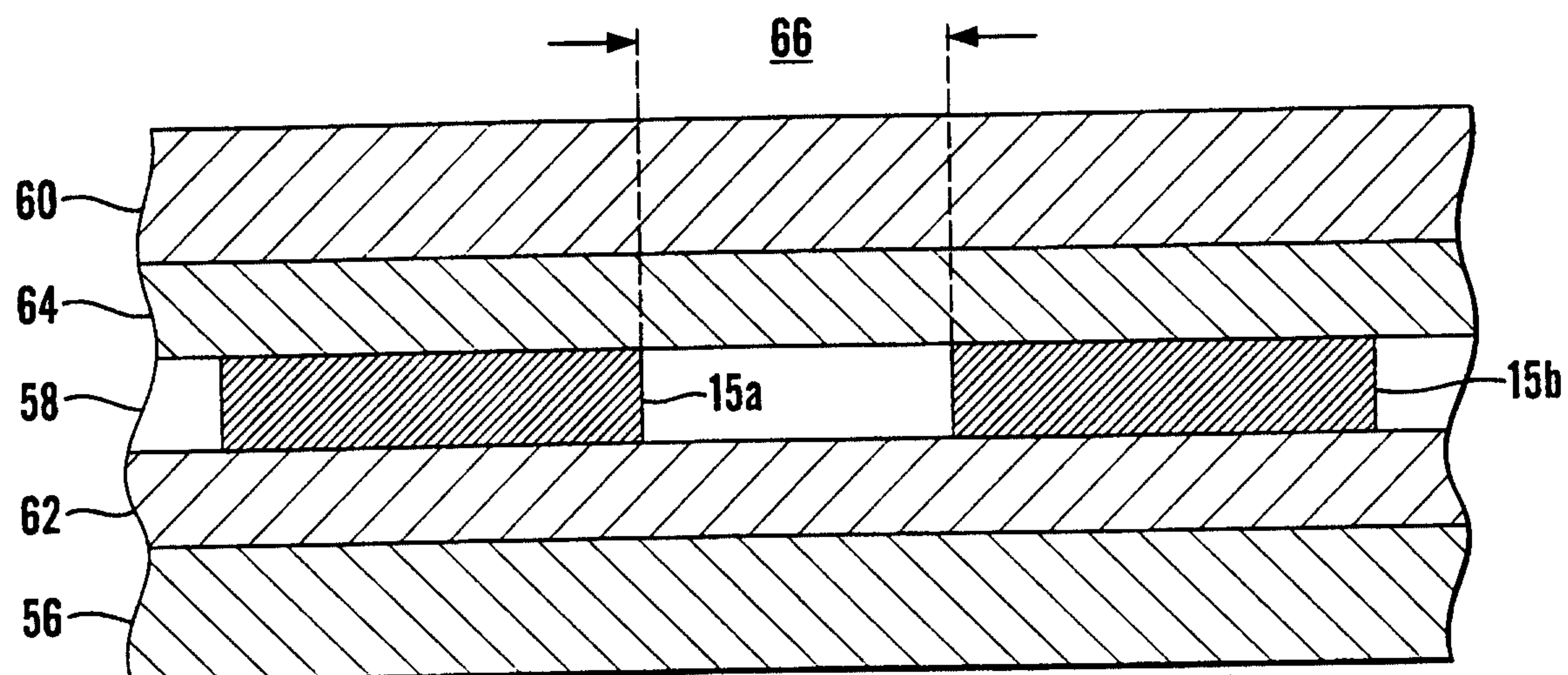


Fig. 9

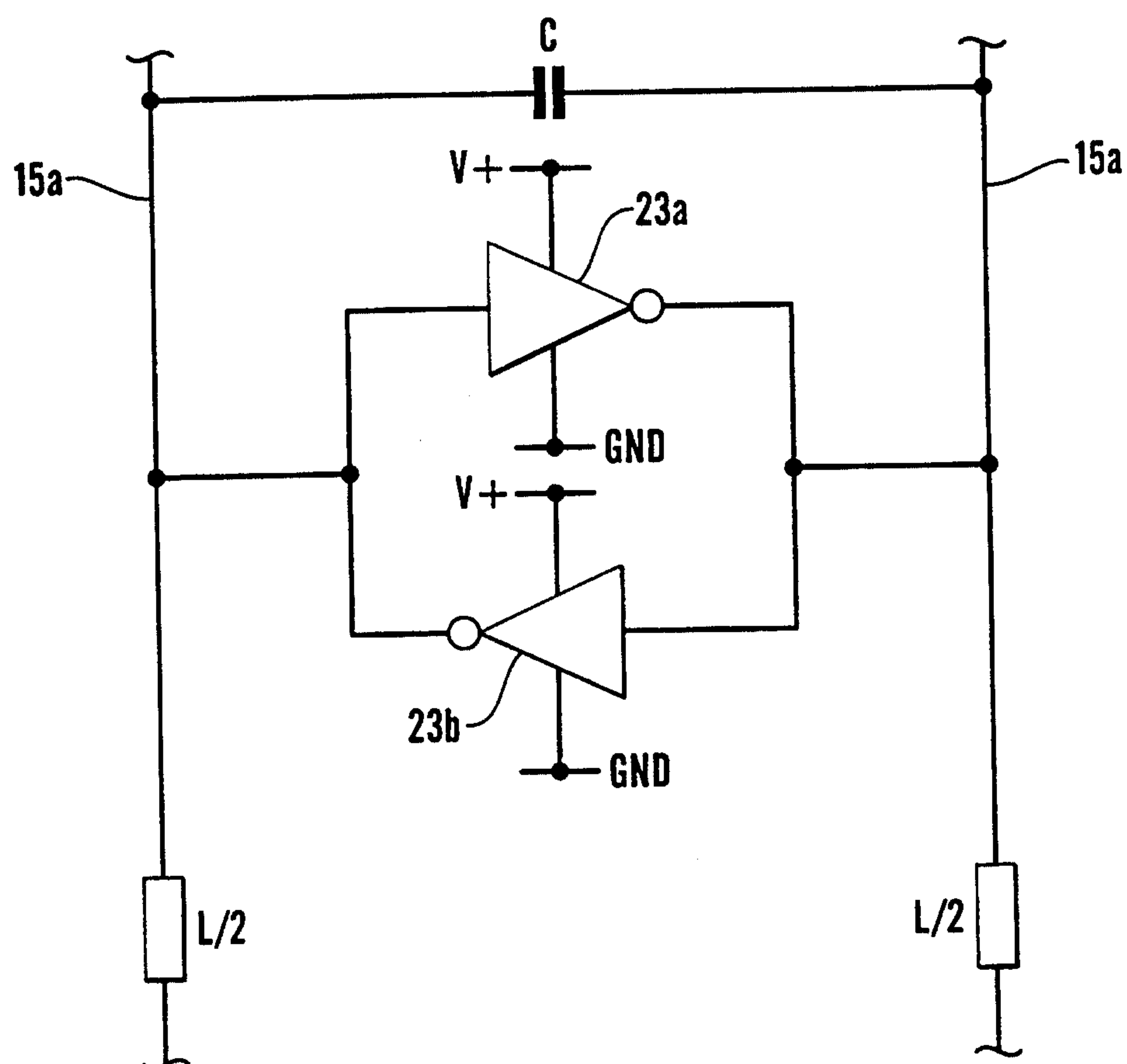


Fig. 12

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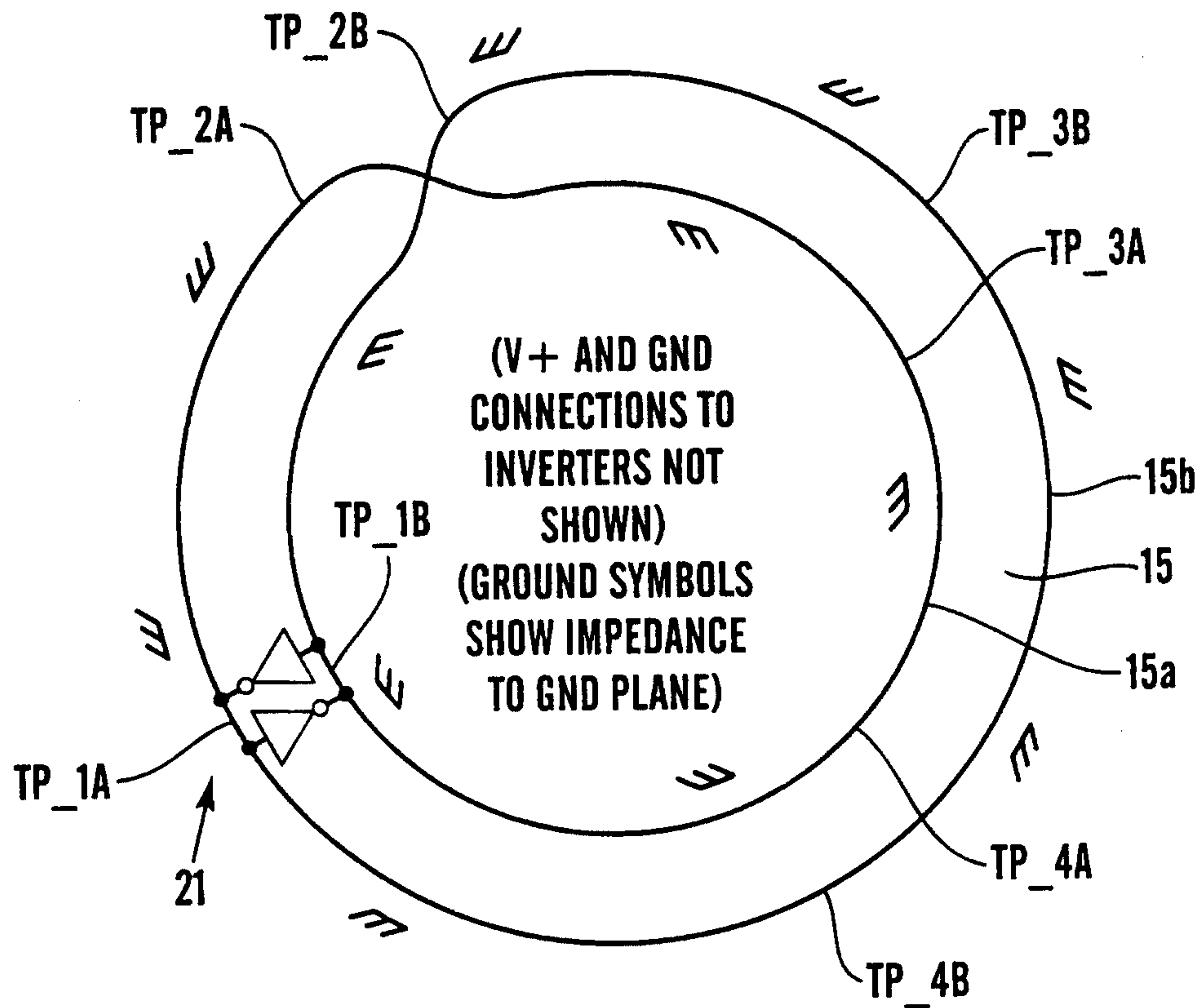


Fig. 10a

WAVEFORM (TIME DOMAIN)

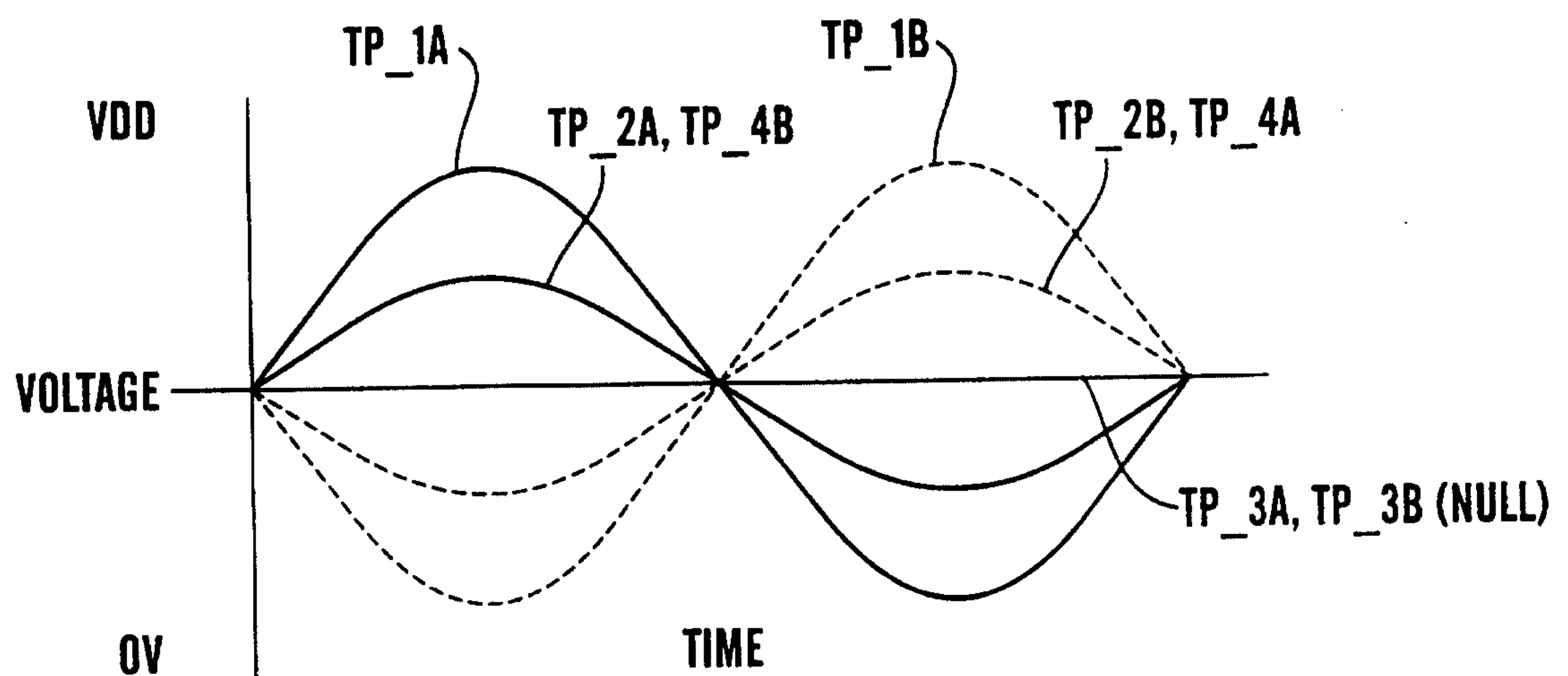


Fig. 10b

Diagram illustrating a two-terminal device structure. The central region is labeled $21T$. The left and right regions are labeled $+$ and $-$ respectively. The top and bottom lines are labeled $-$ and $+$ respectively.

Fig. 11

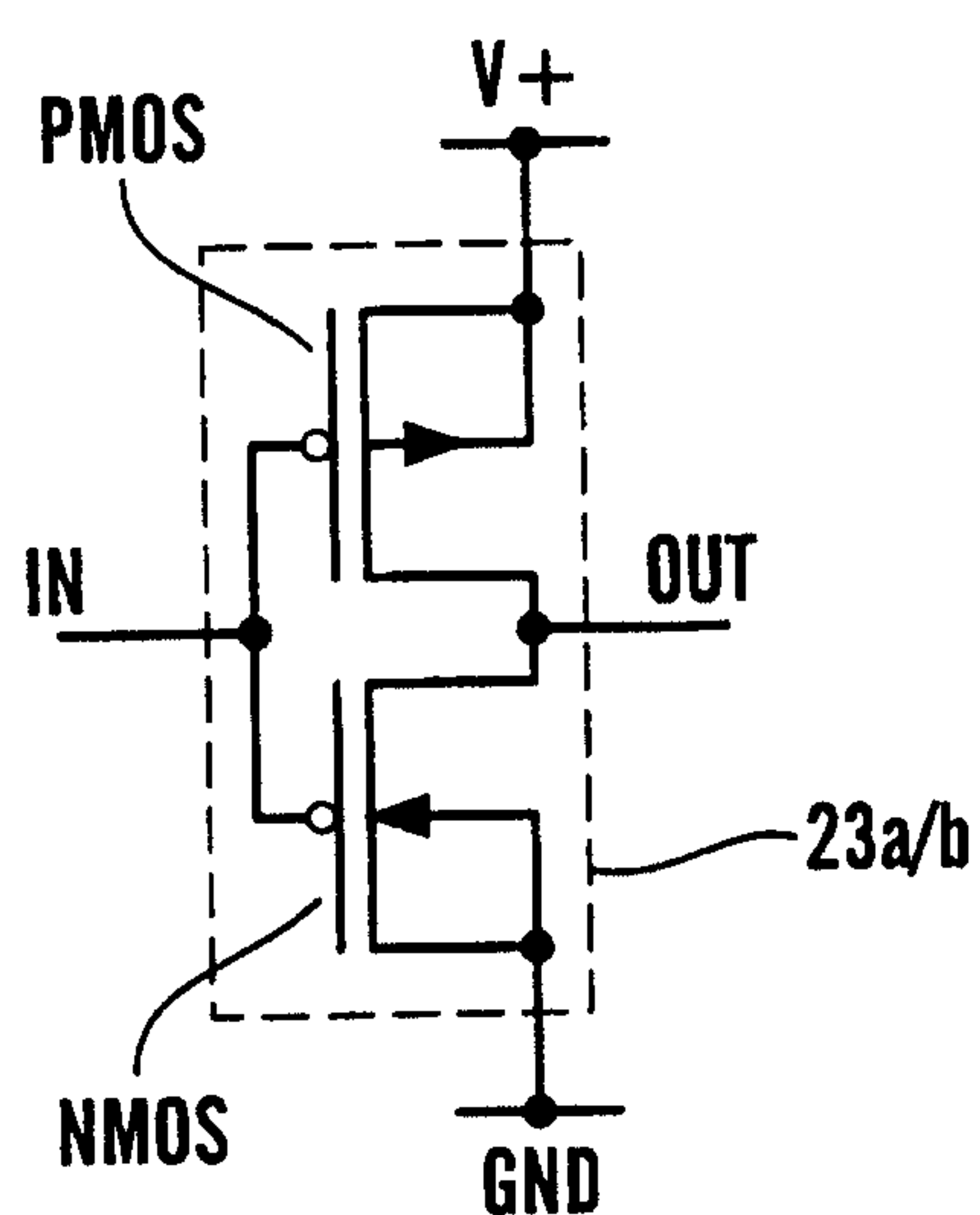


Fig. 13a

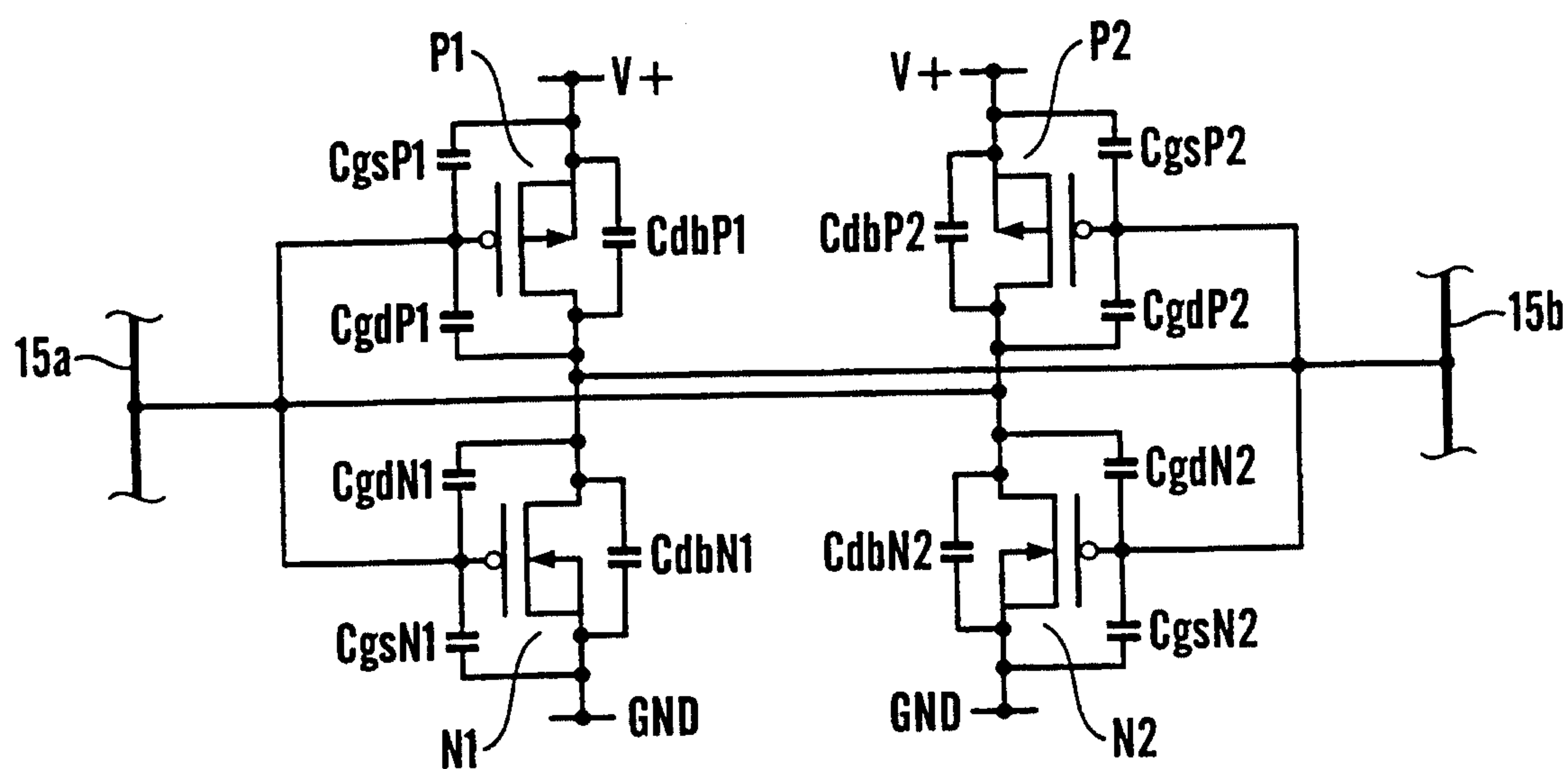


Fig. 13b

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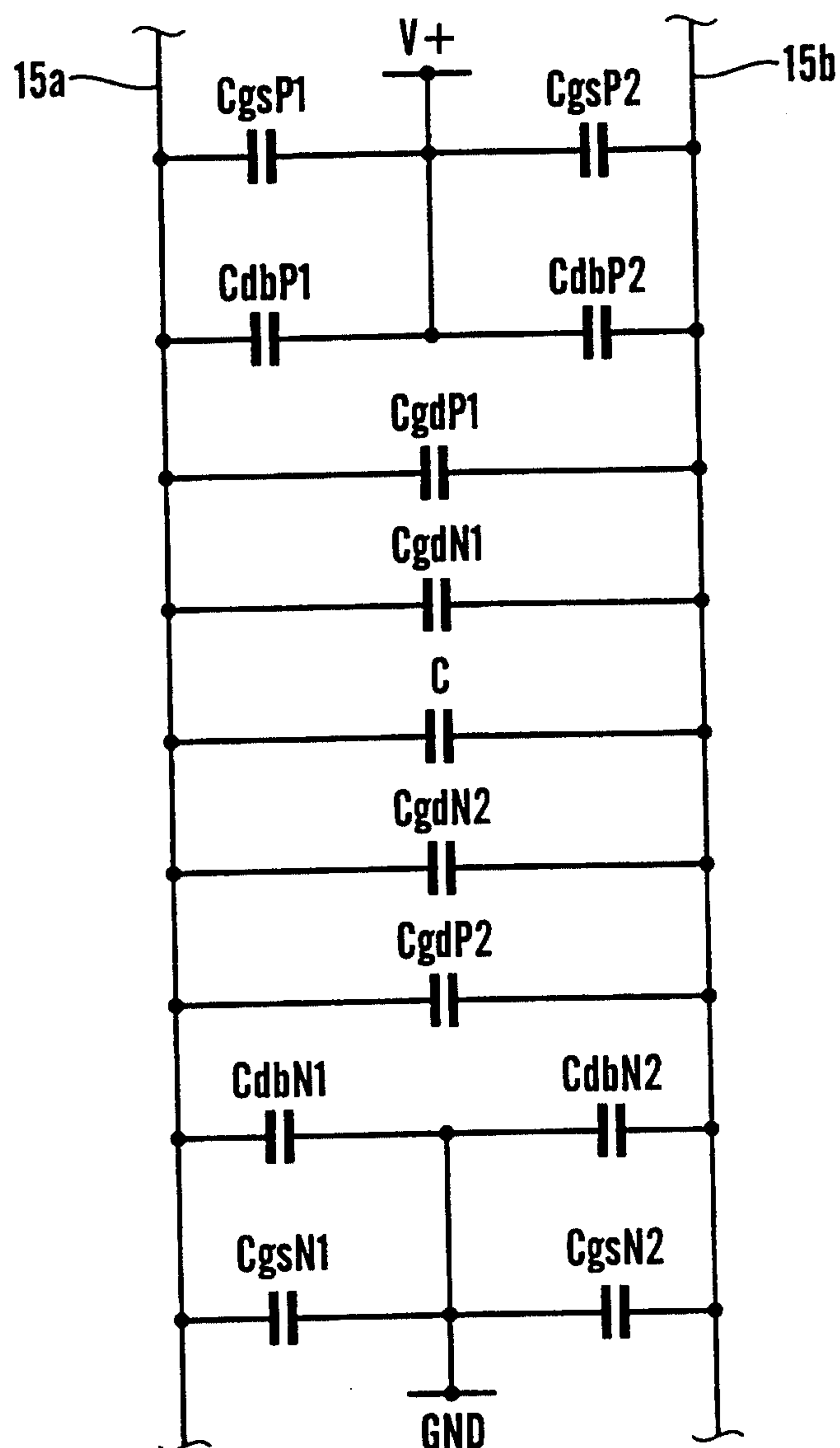


Fig. 14a

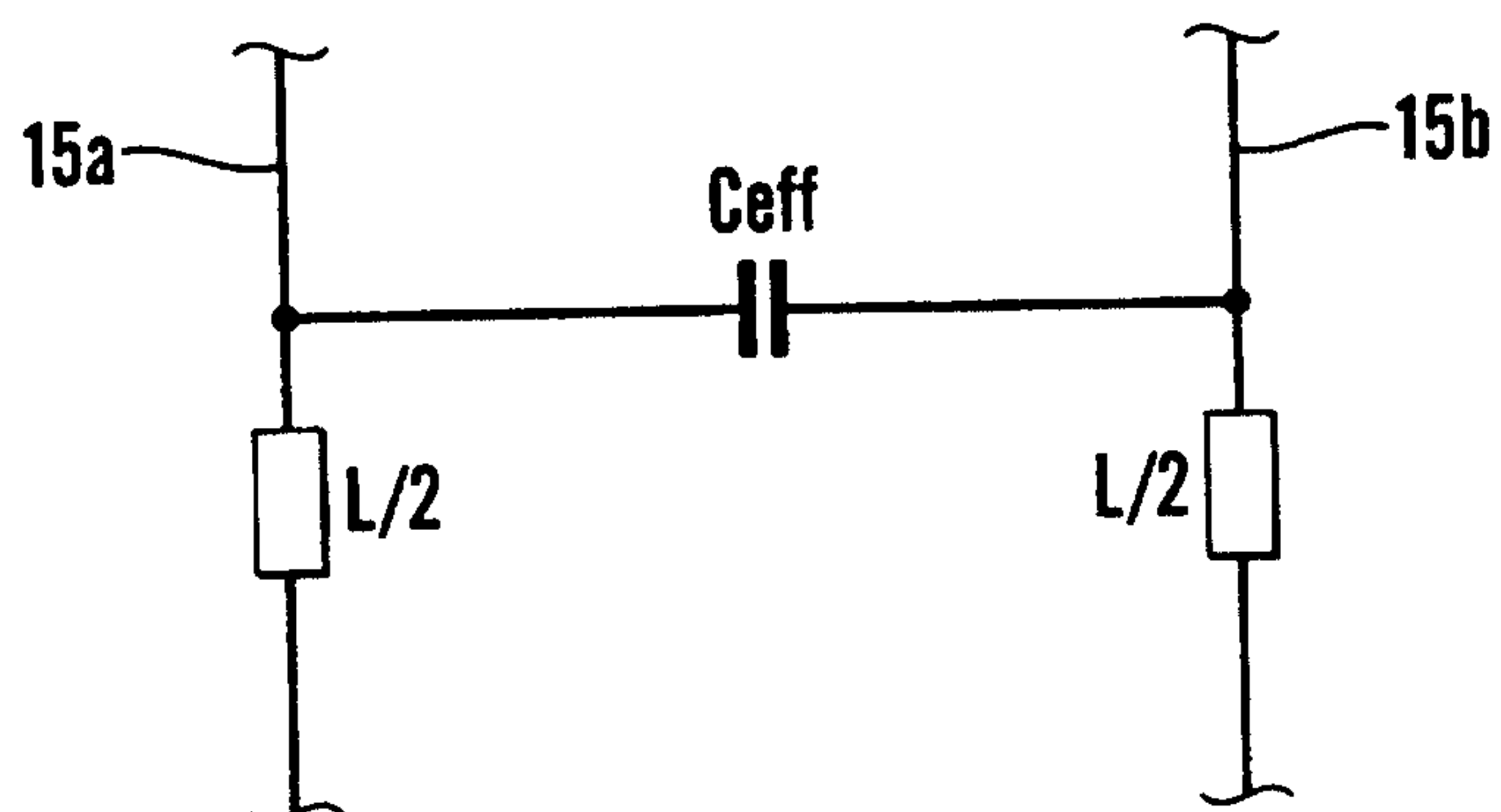


Fig. 14b

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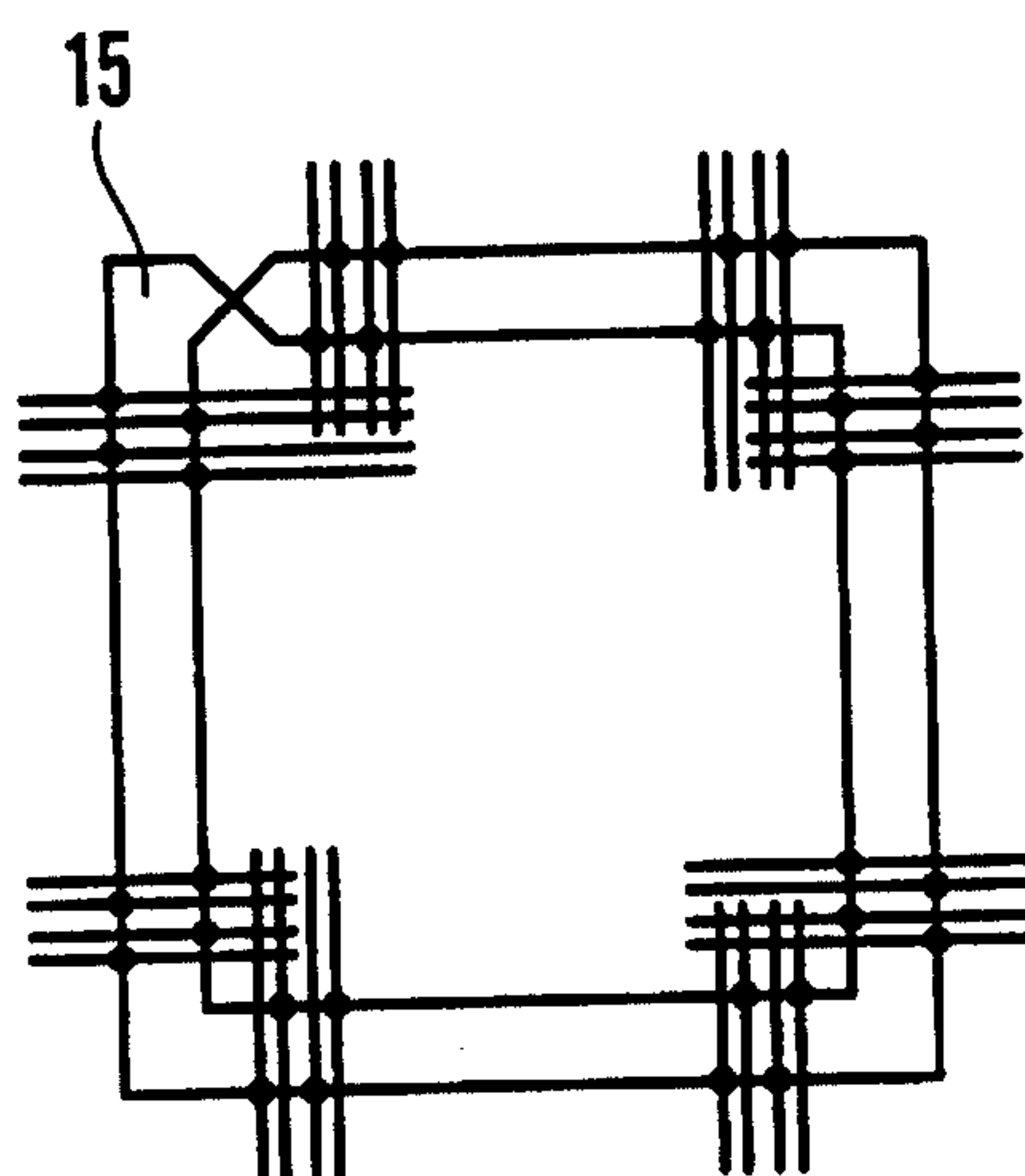


Fig. 15

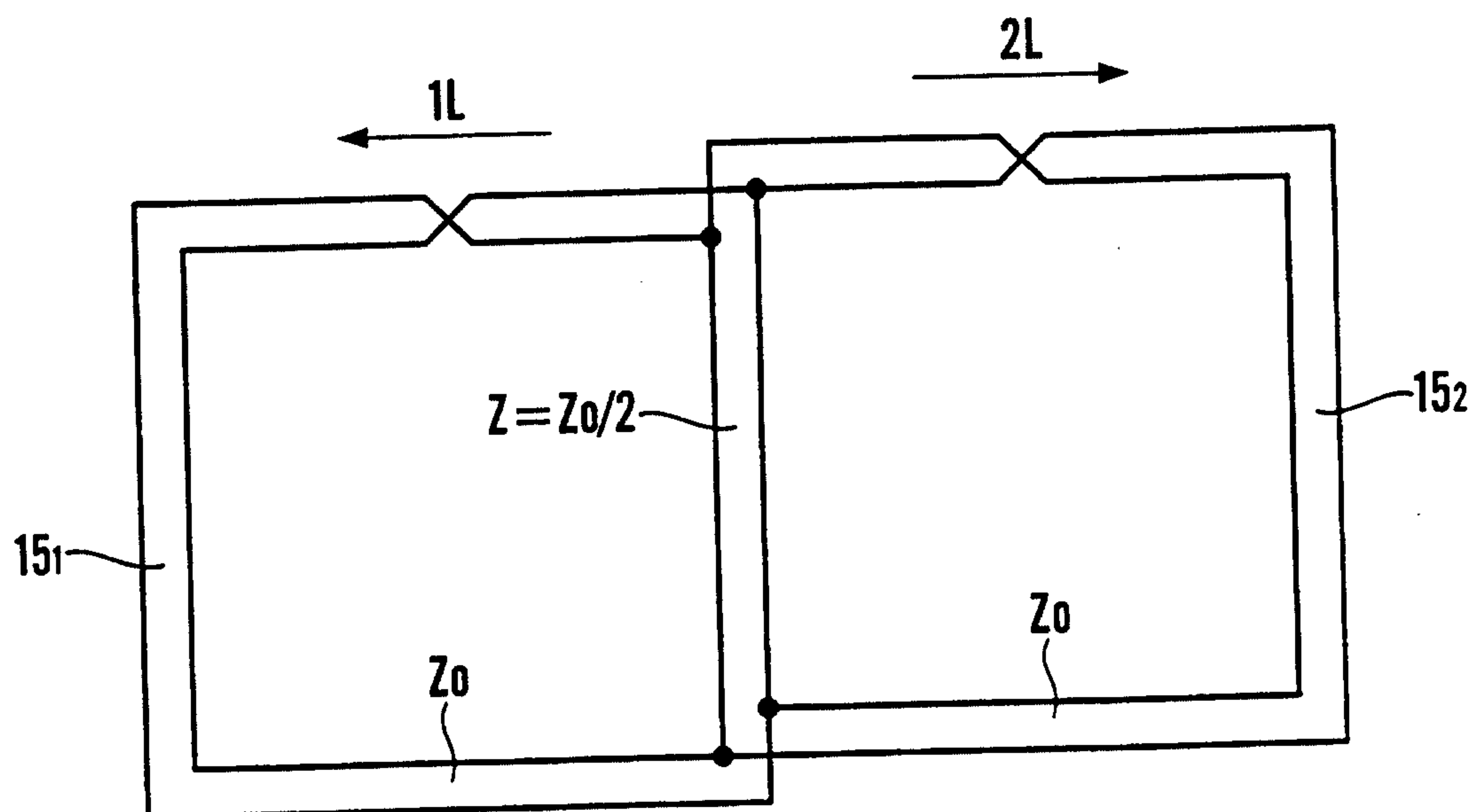


Fig. 16

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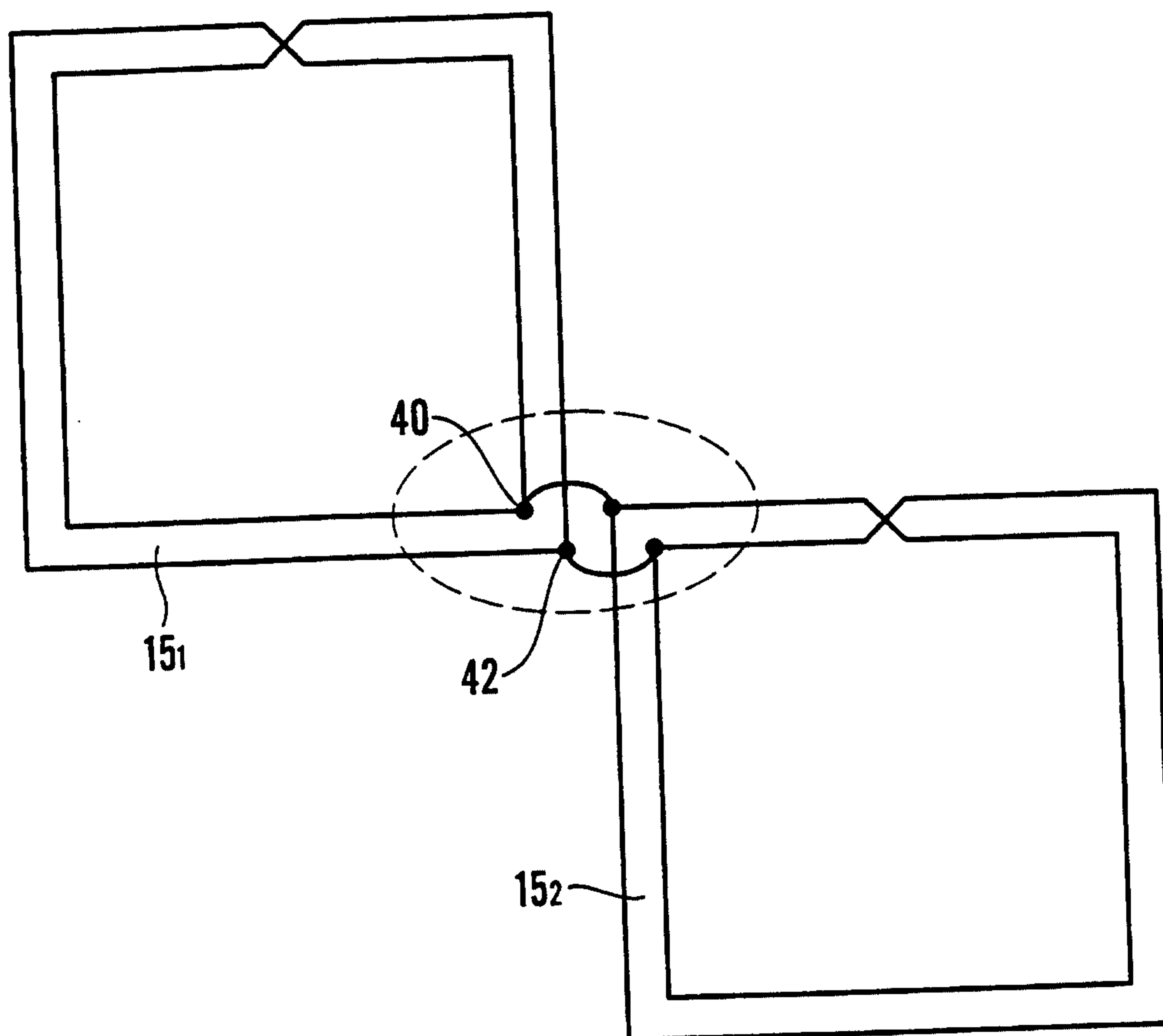


Fig. 17a

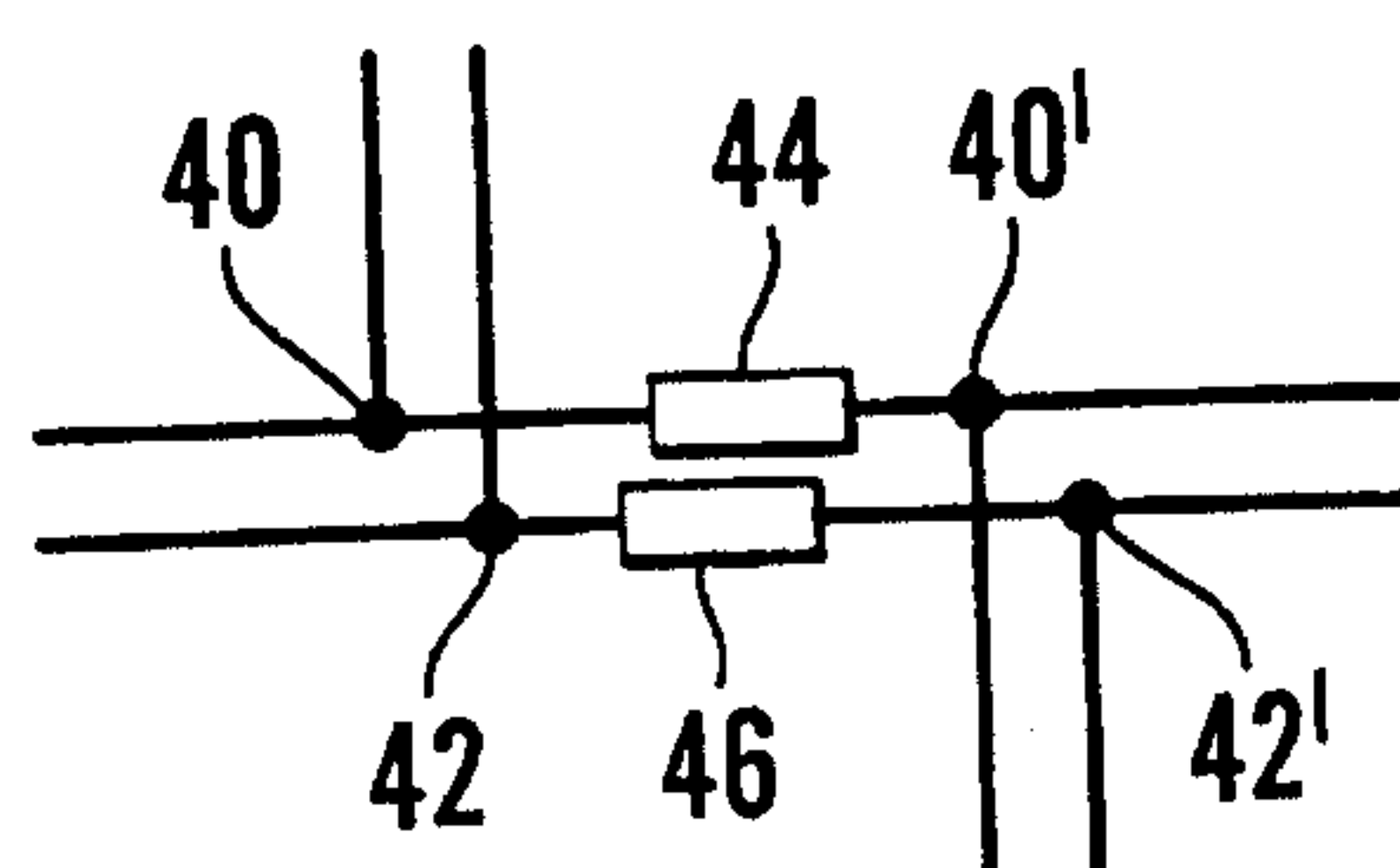


Fig. 17b

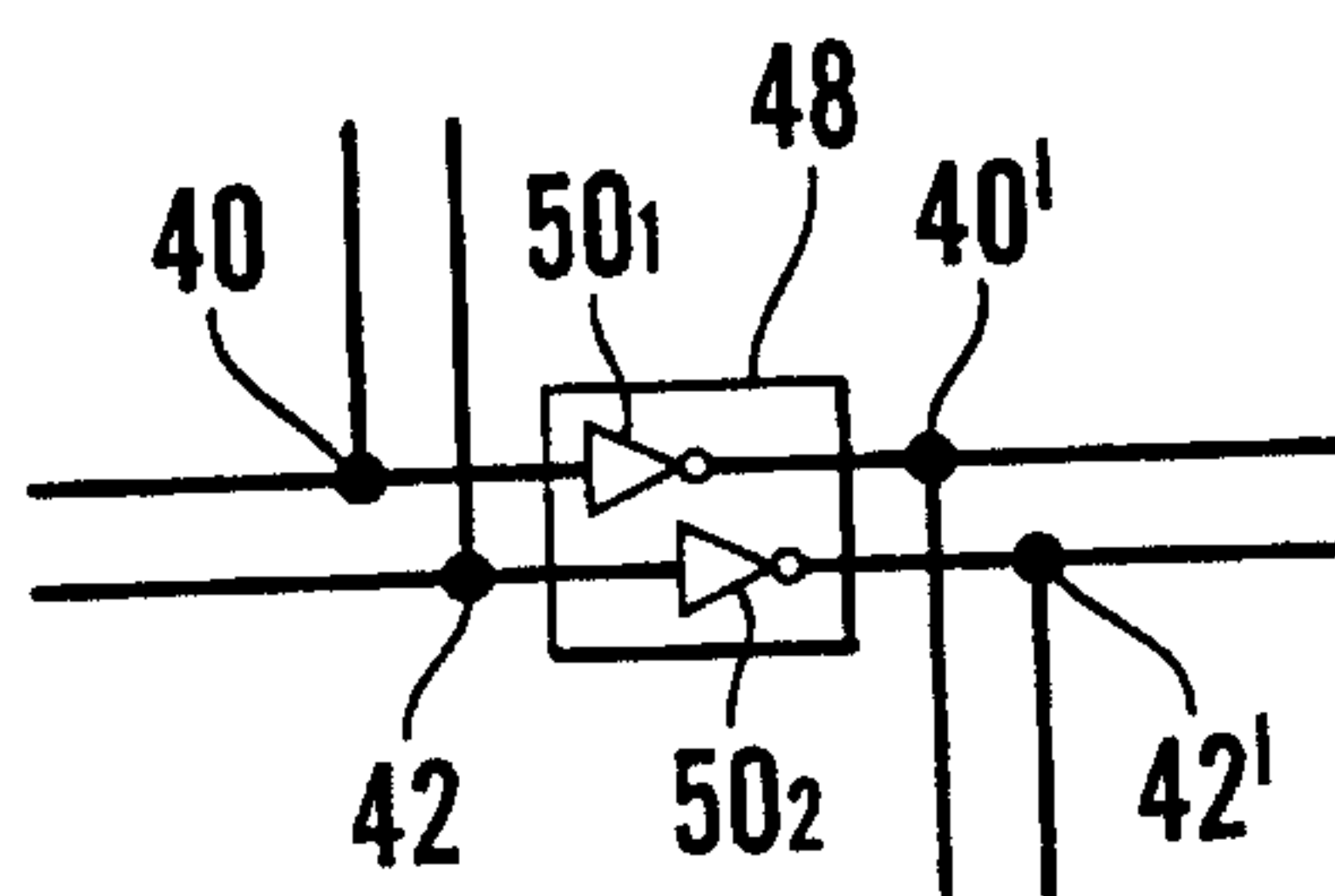
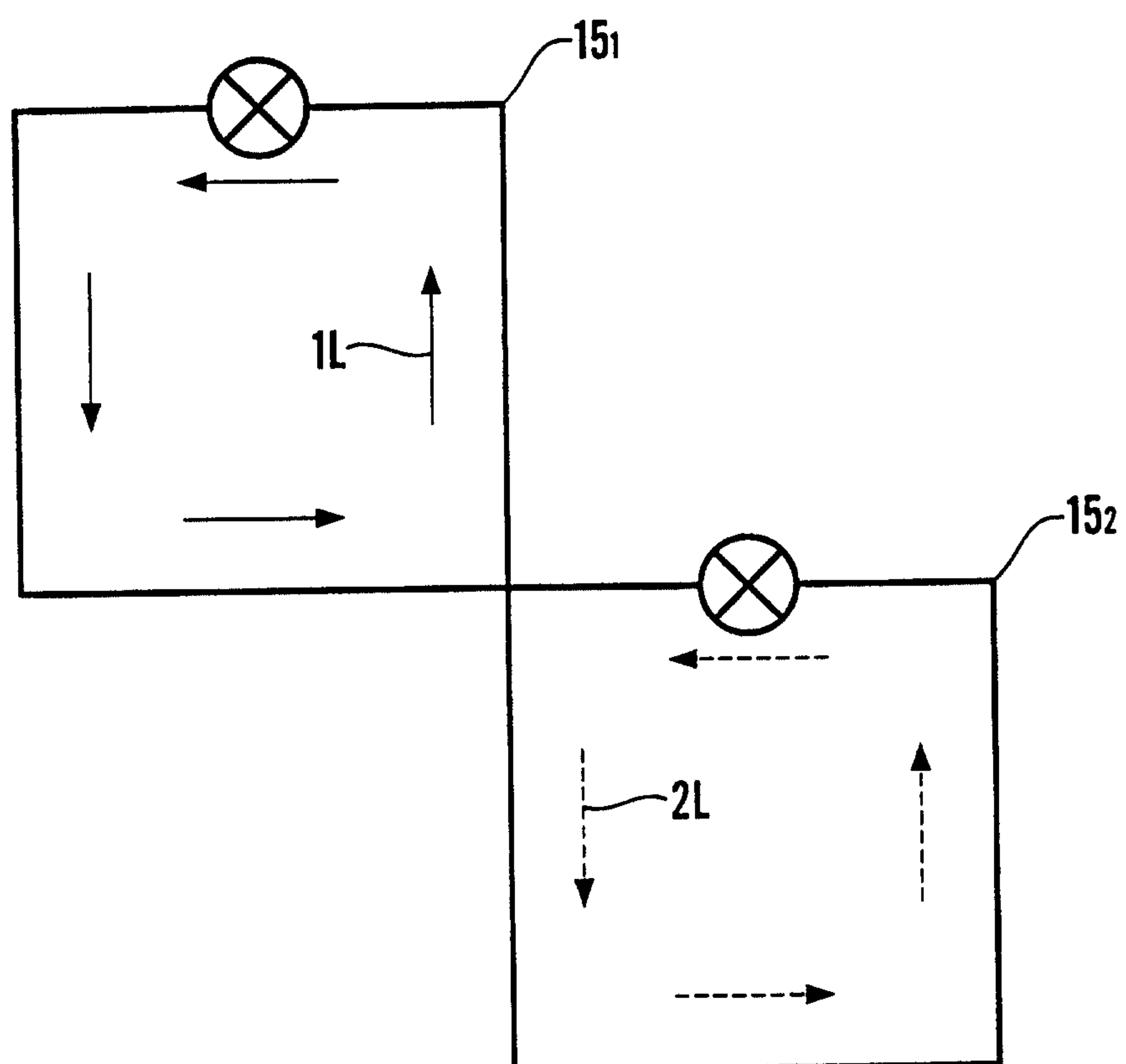
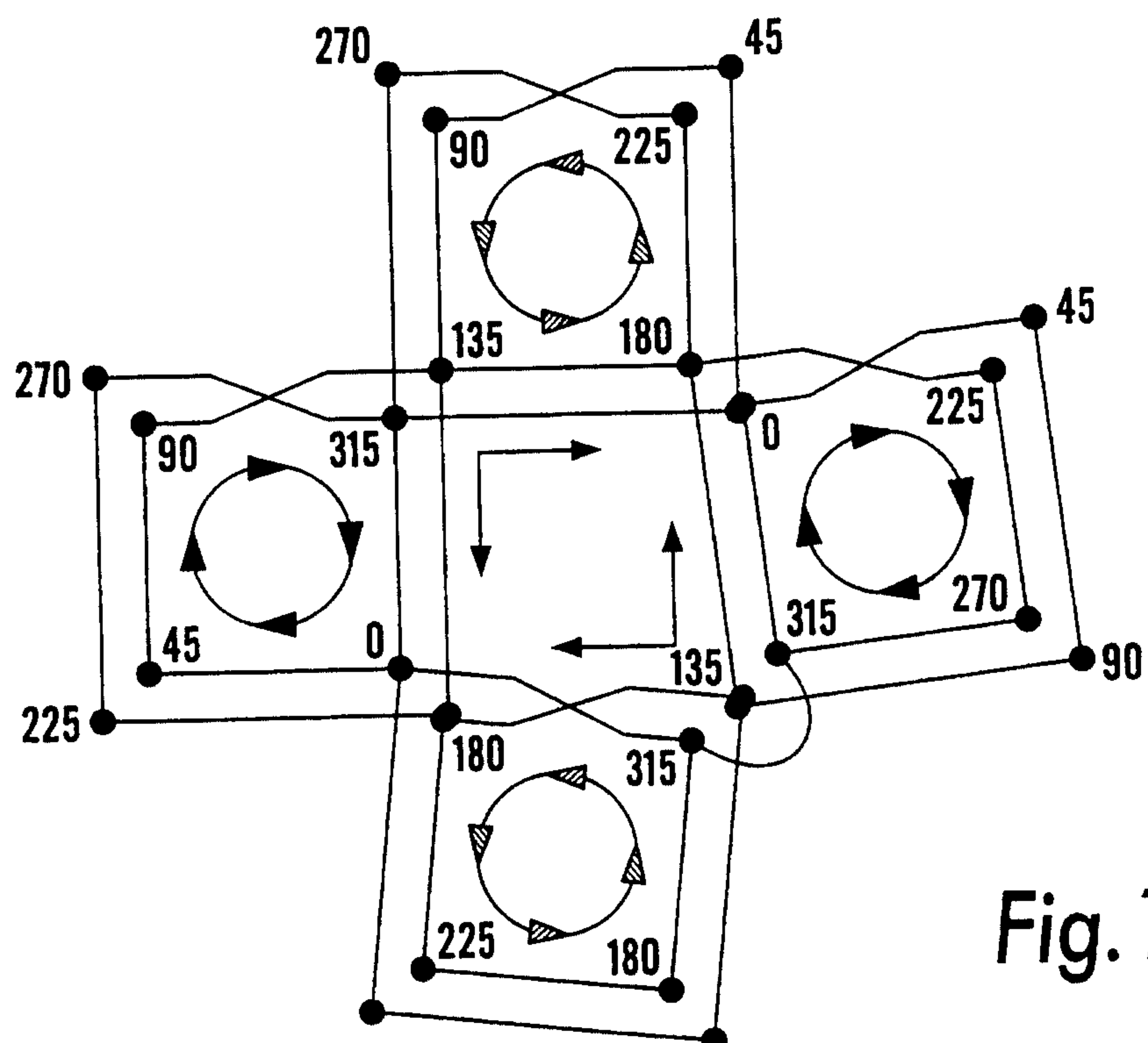
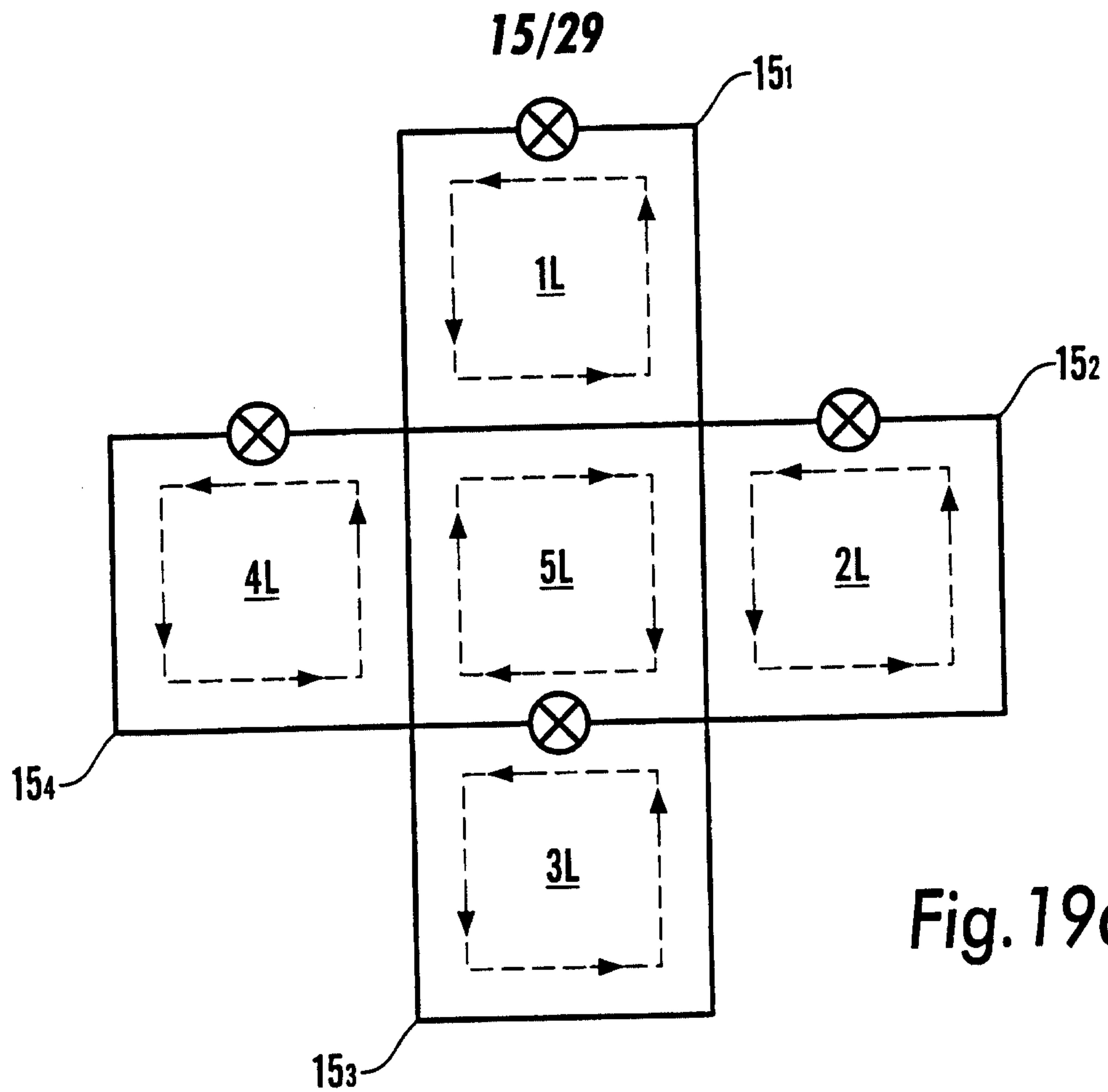


Fig. 17c

14/29**Fig. 18**



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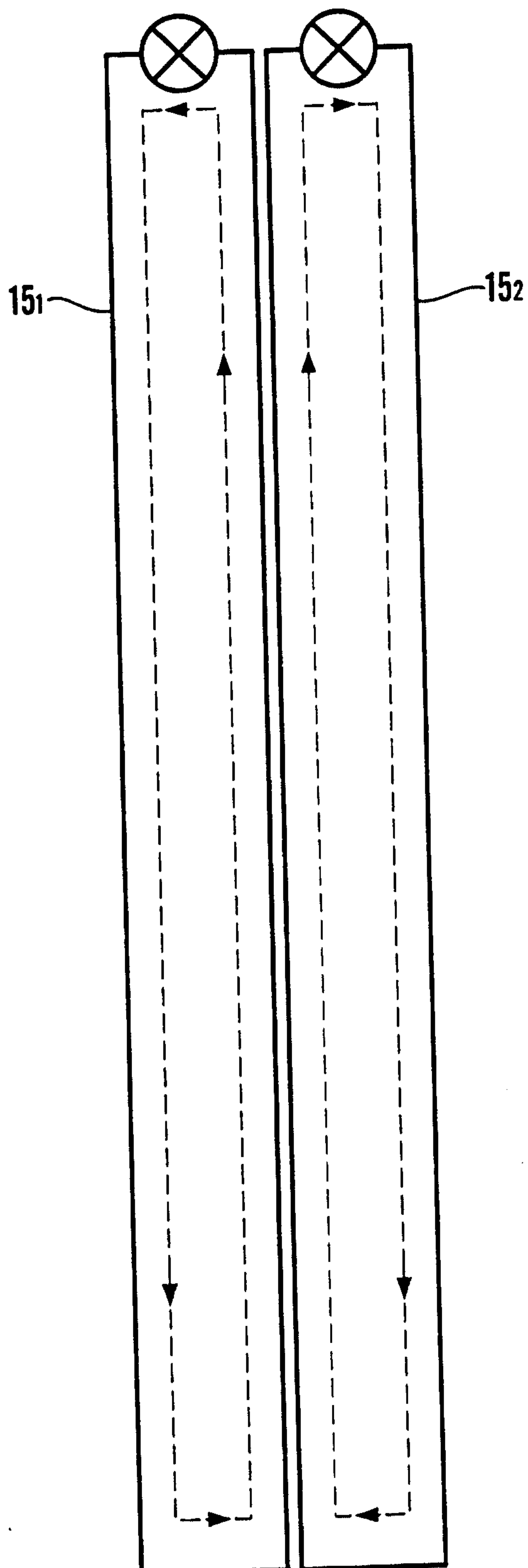


Fig. 20

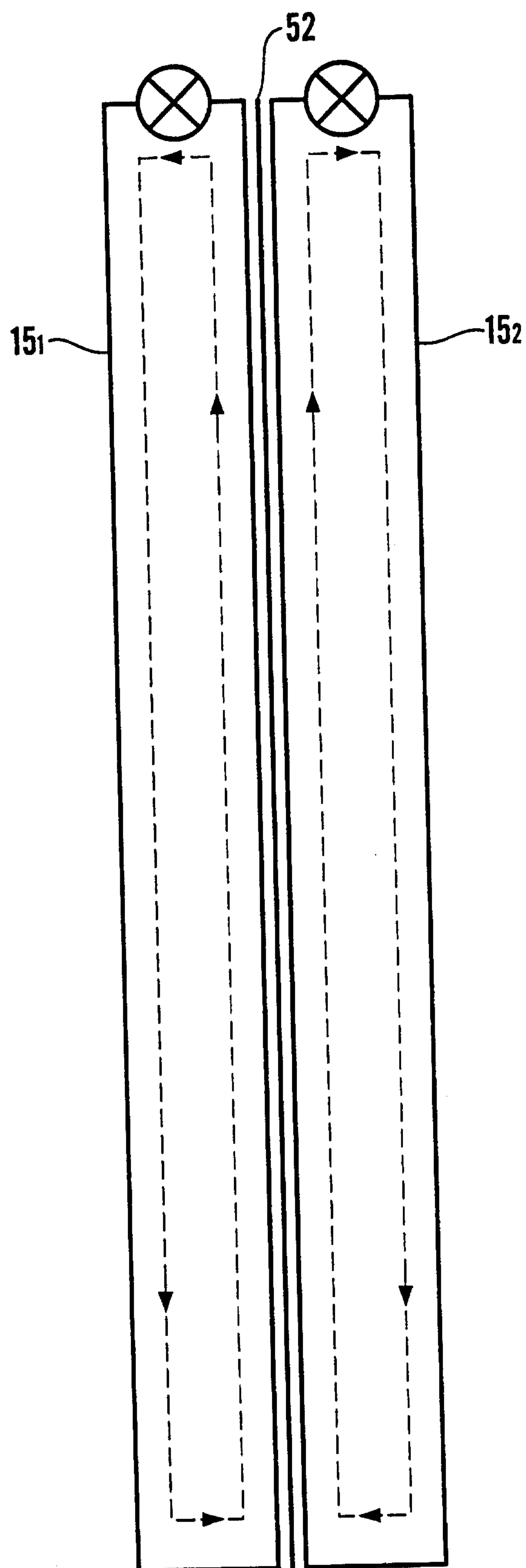


Fig. 21

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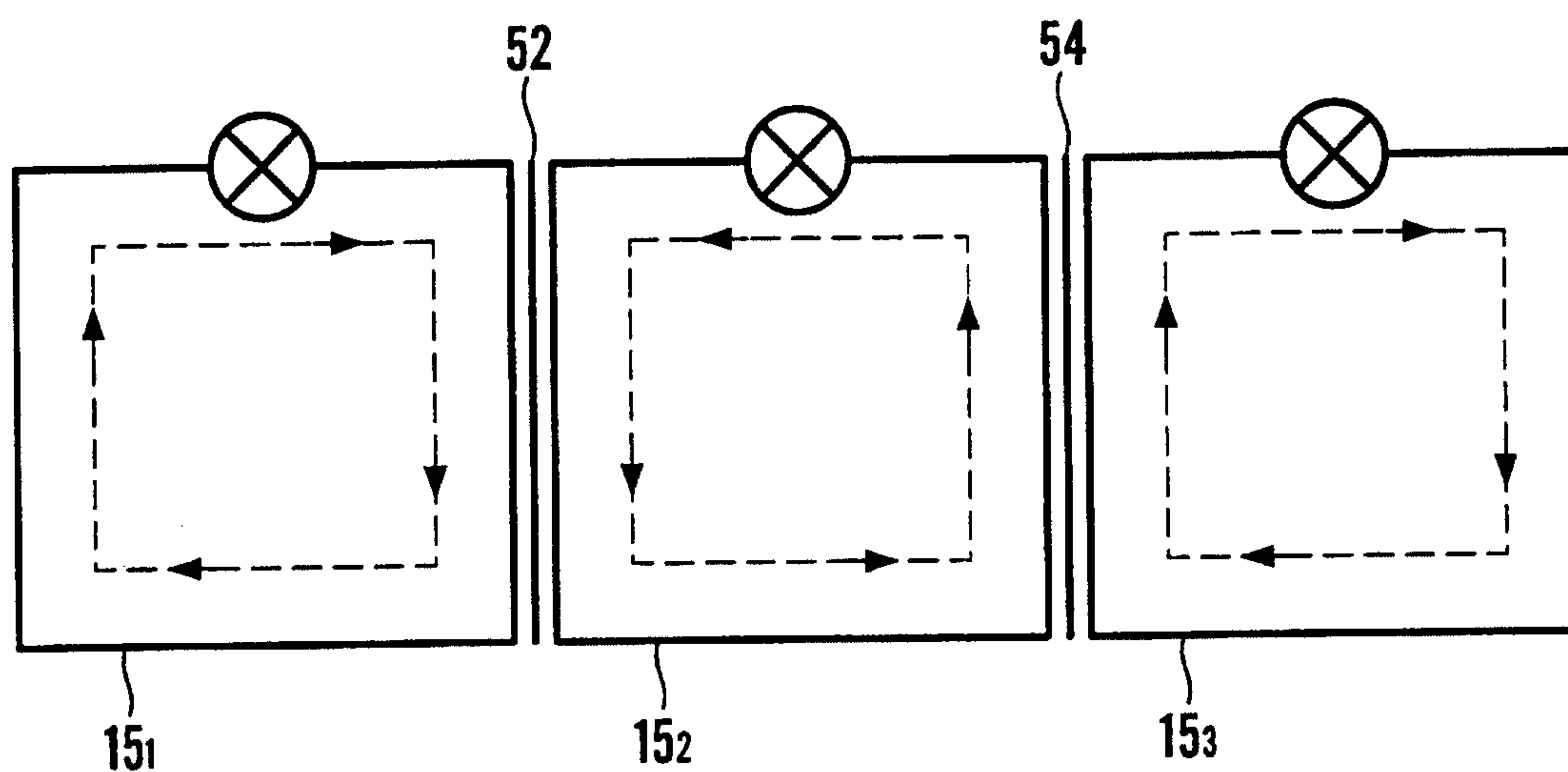


Fig.22

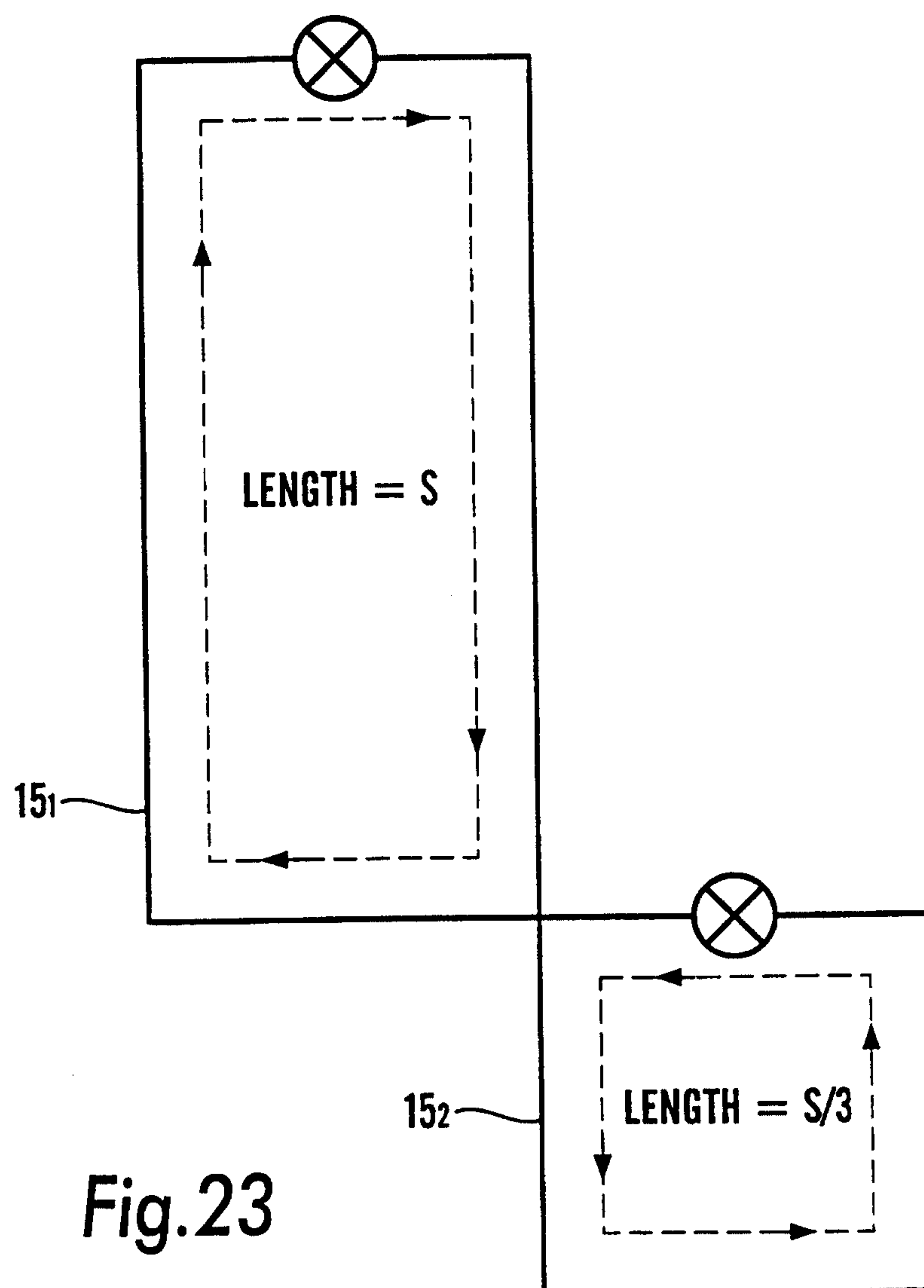


Fig.23

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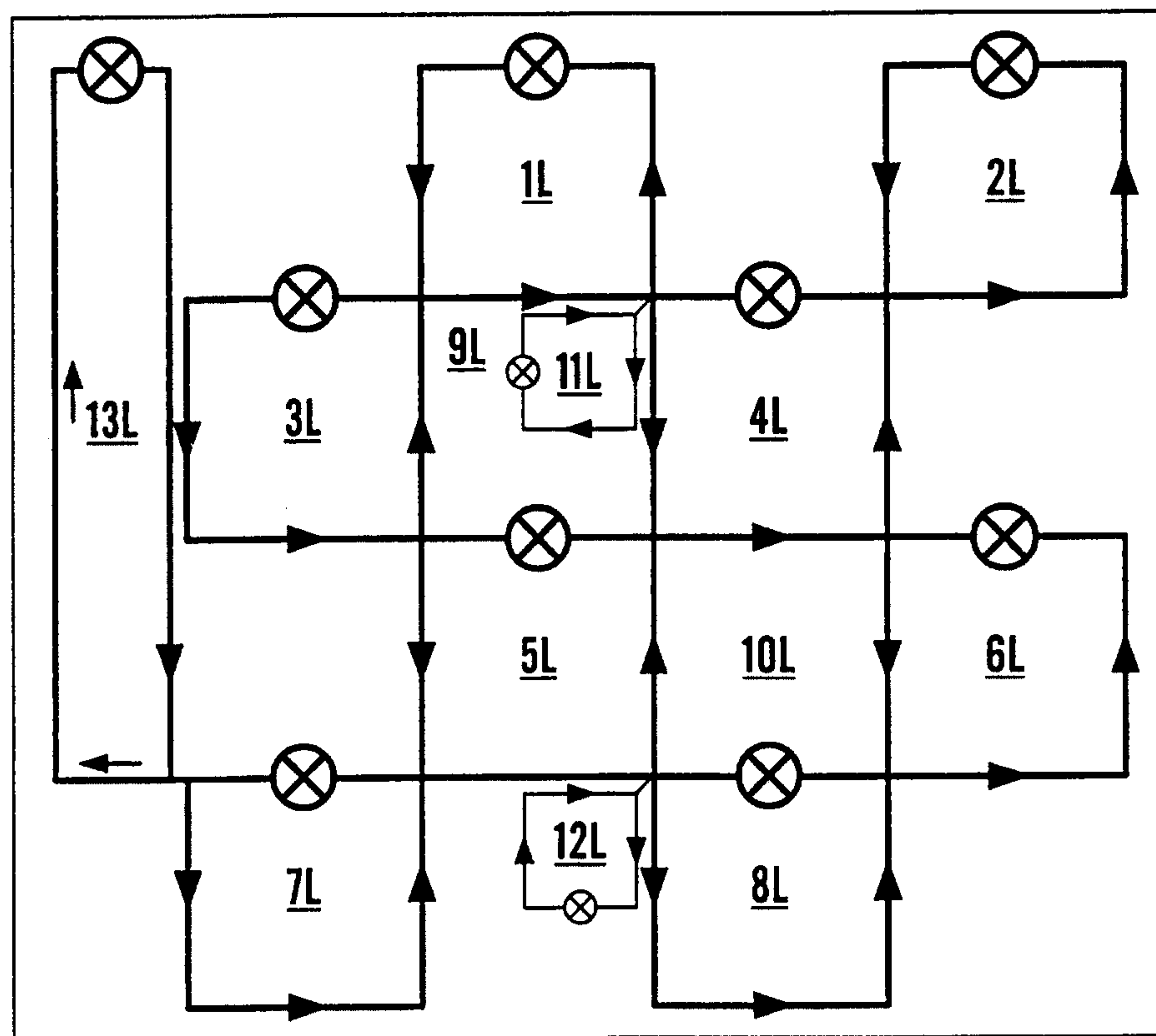


Fig.24

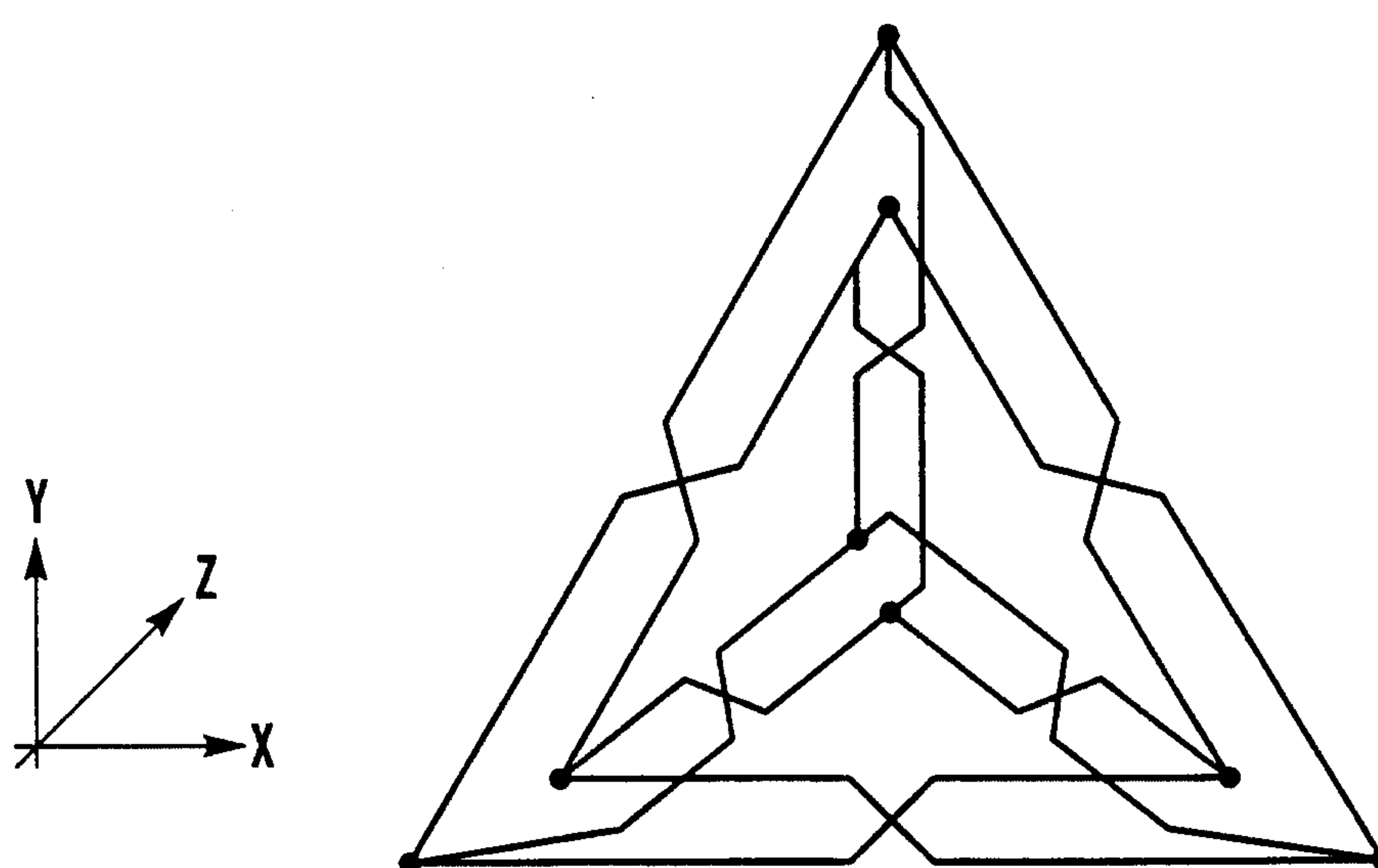


Fig.25

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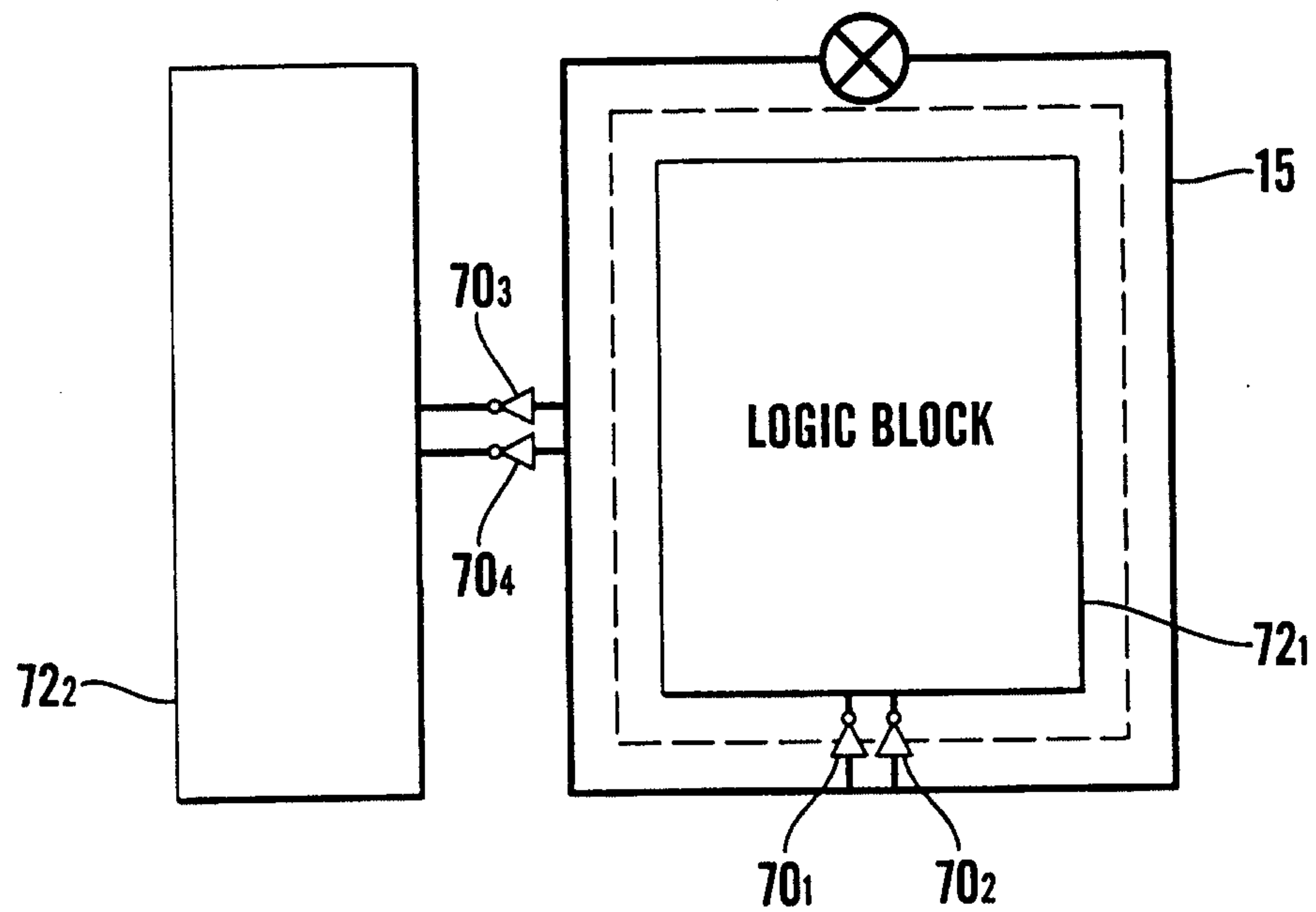


Fig. 26a

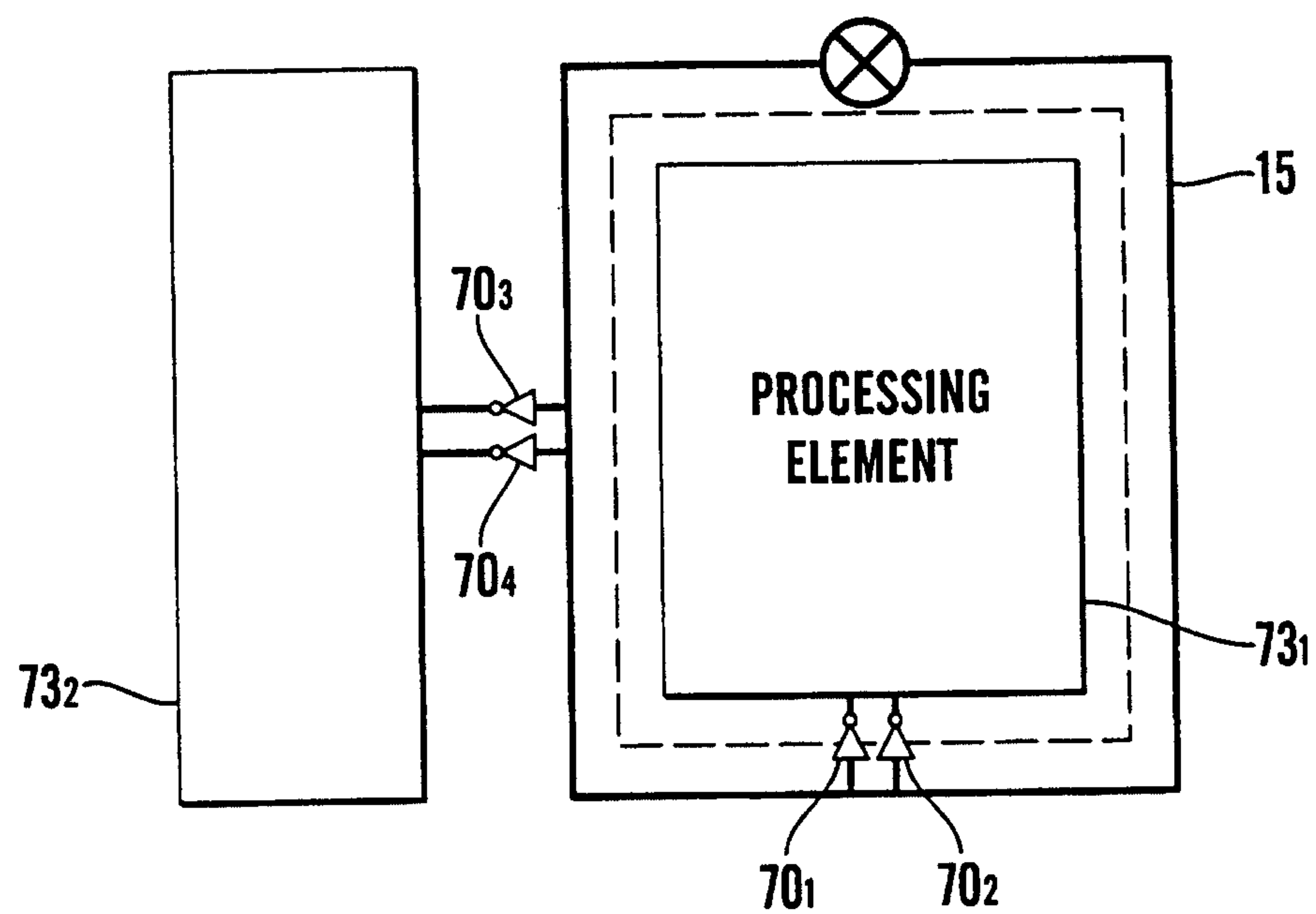
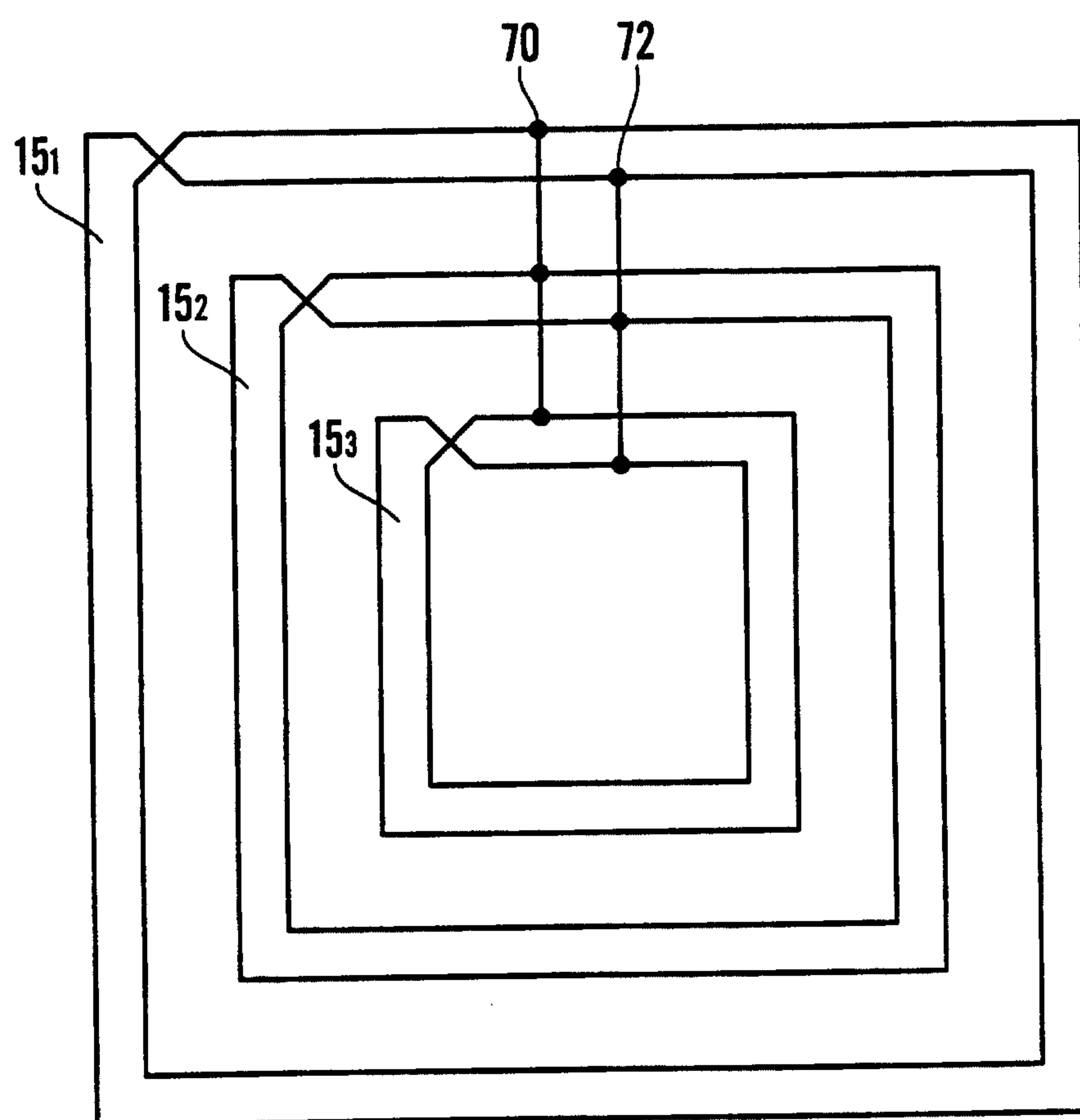


Fig. 26b

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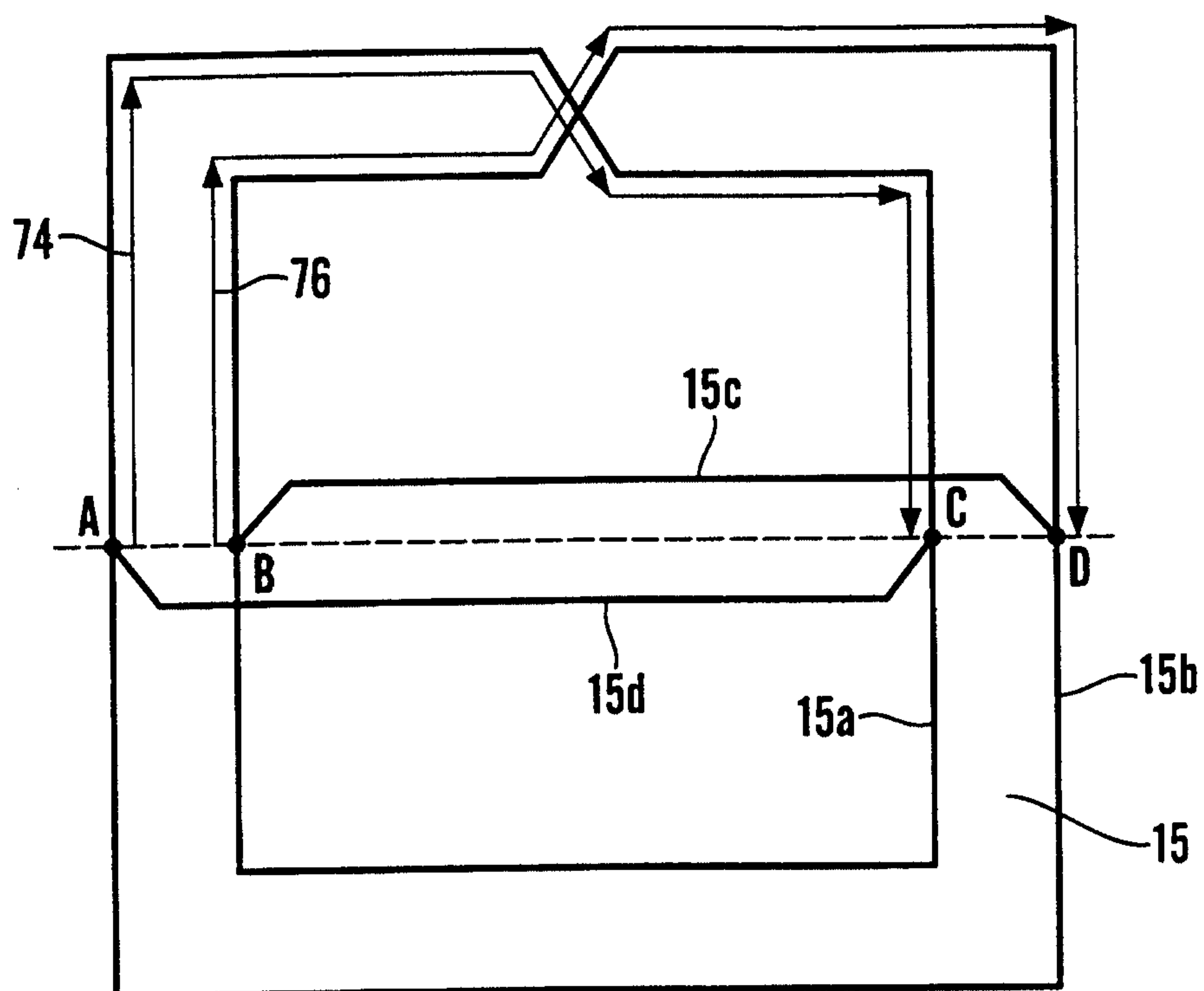


Fig. 28a

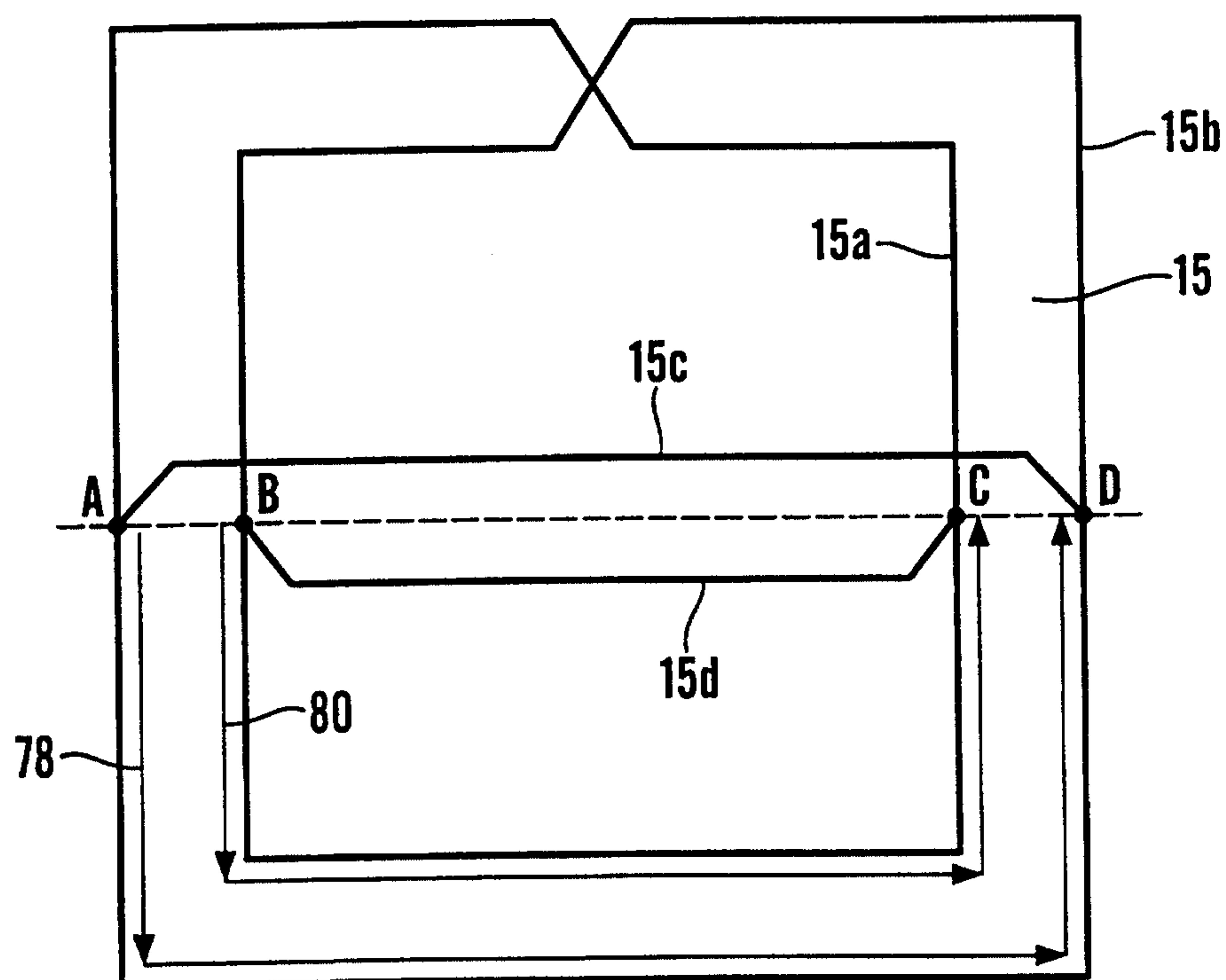
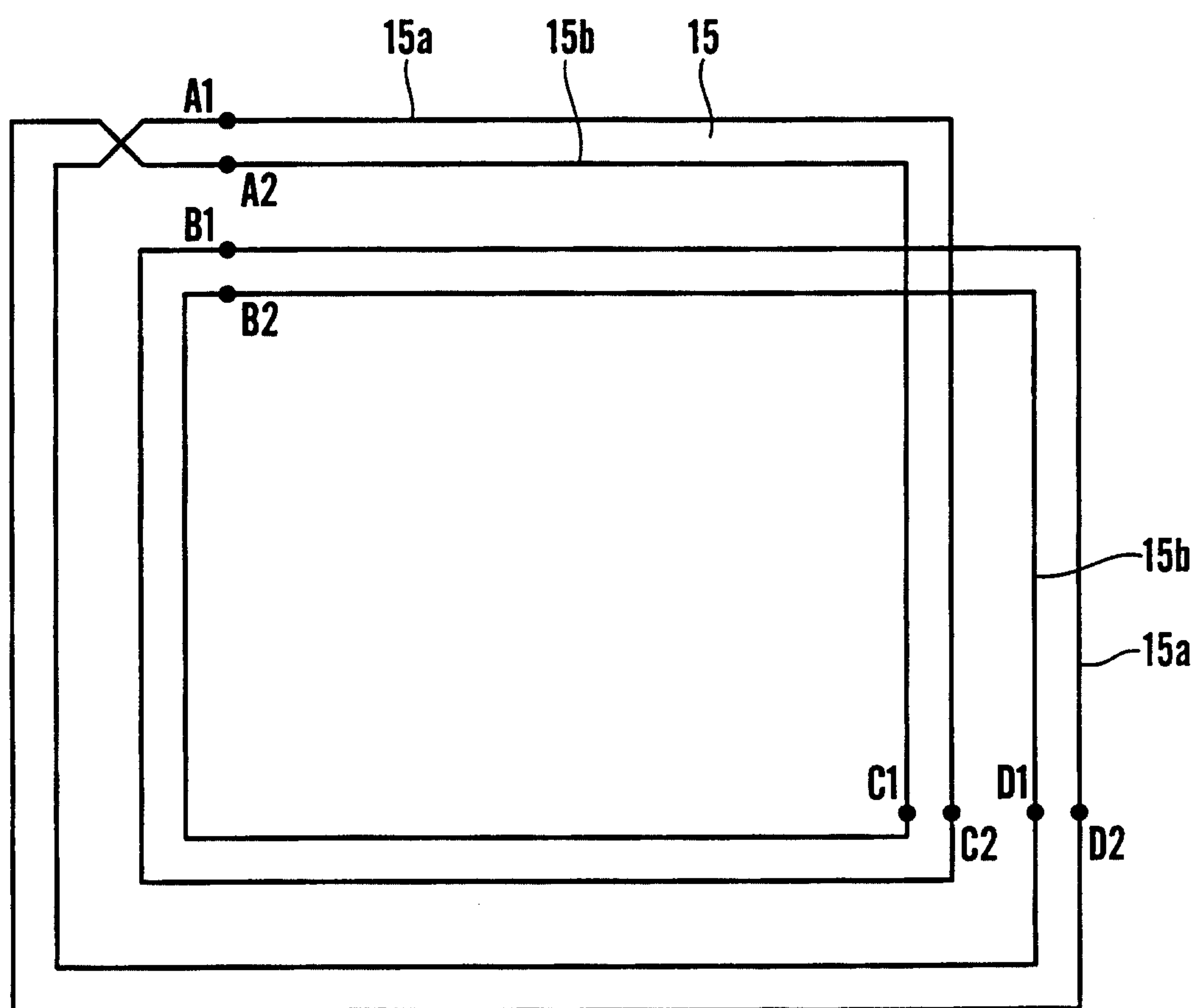
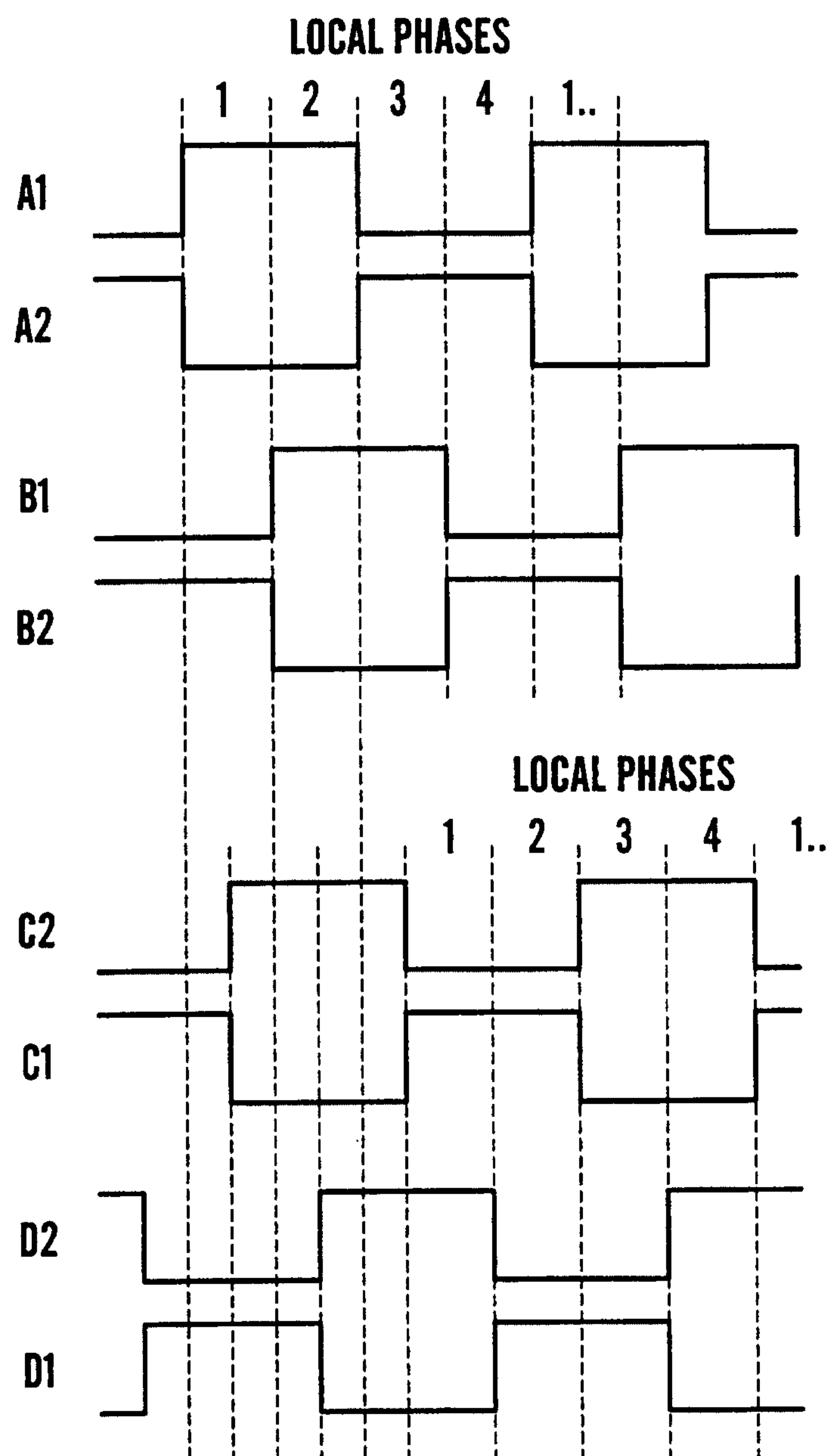
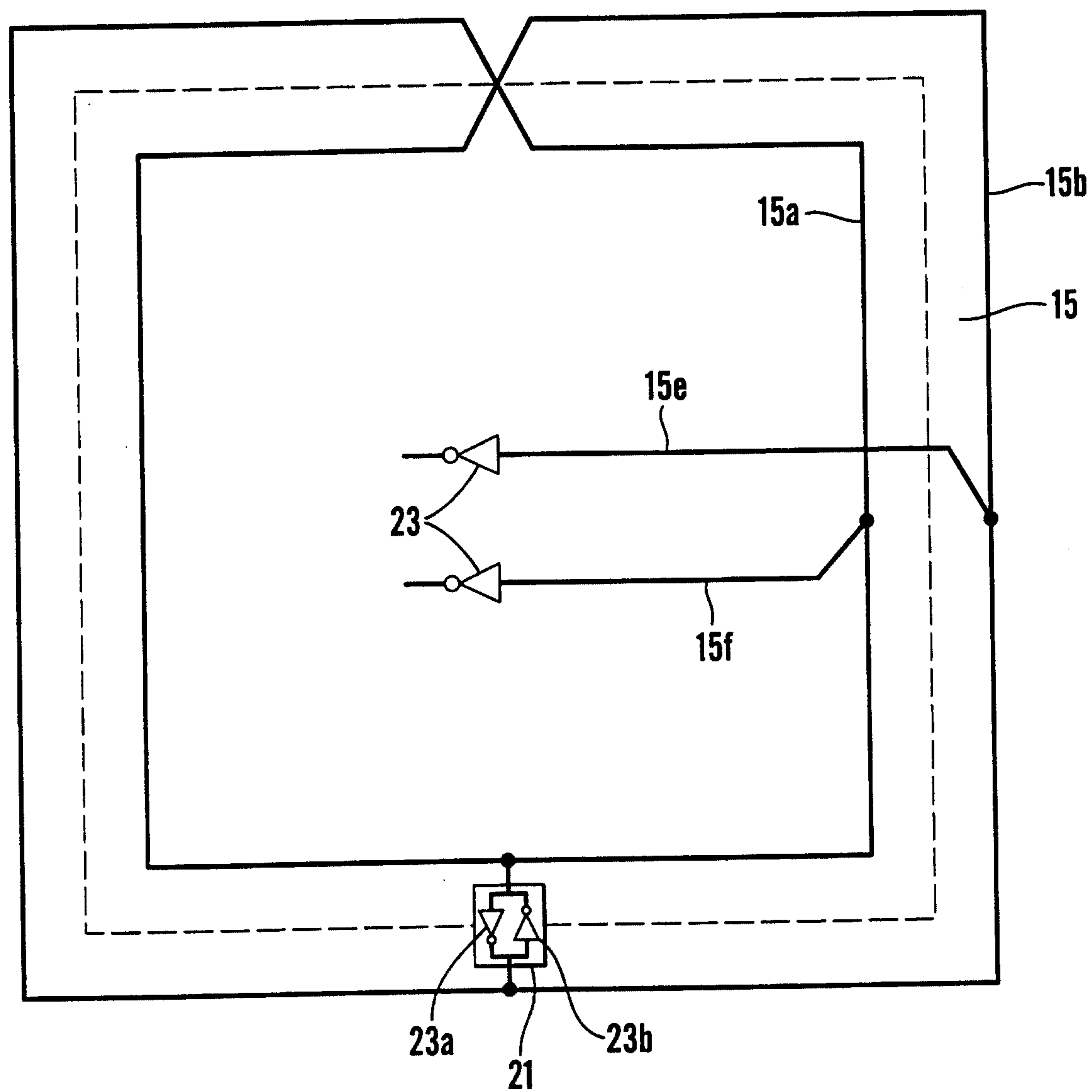


Fig. 28b

22/29**Fig.29a**

23/29**Fig.29b**

24/29**Fig.30**

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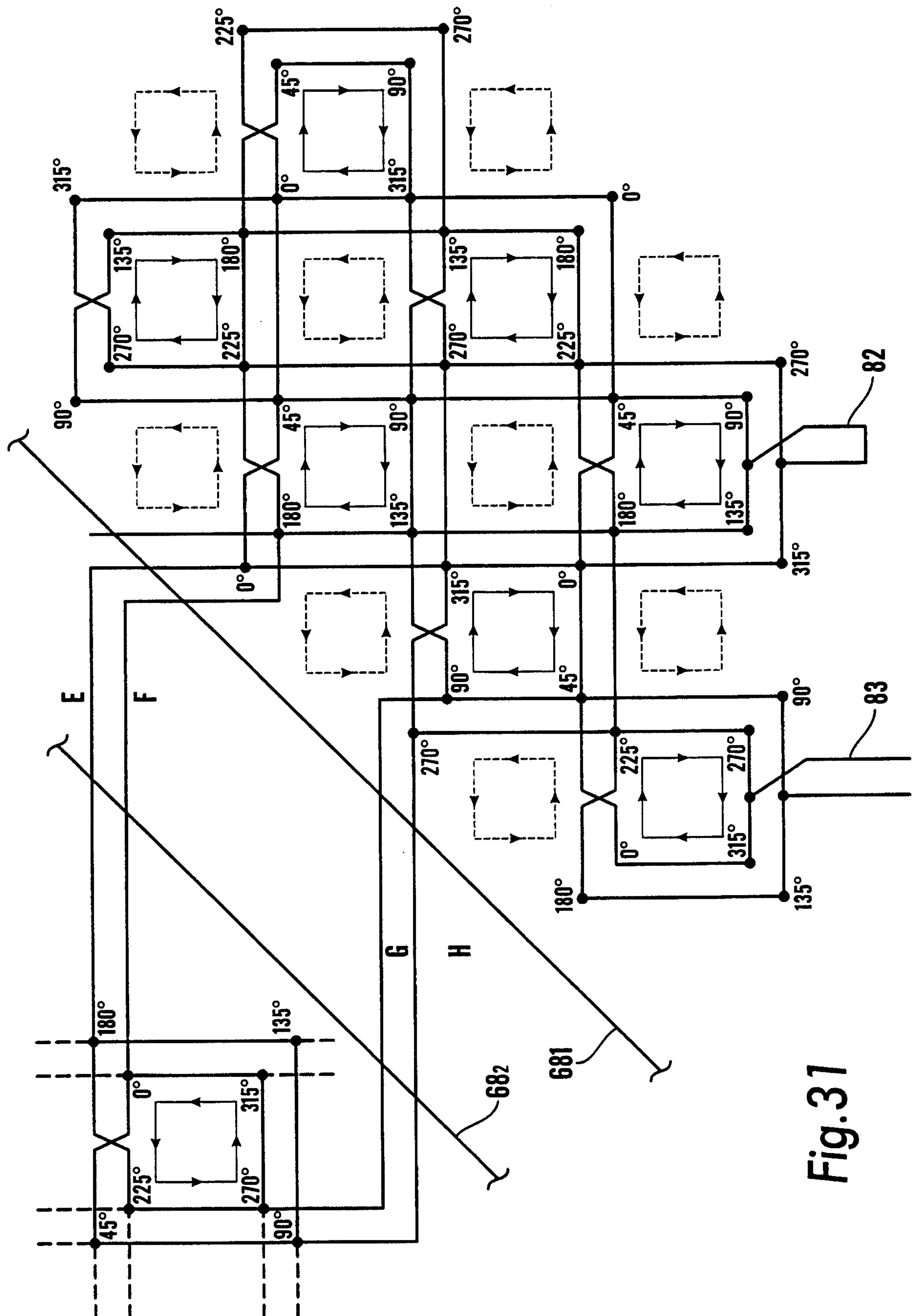


Fig. 31

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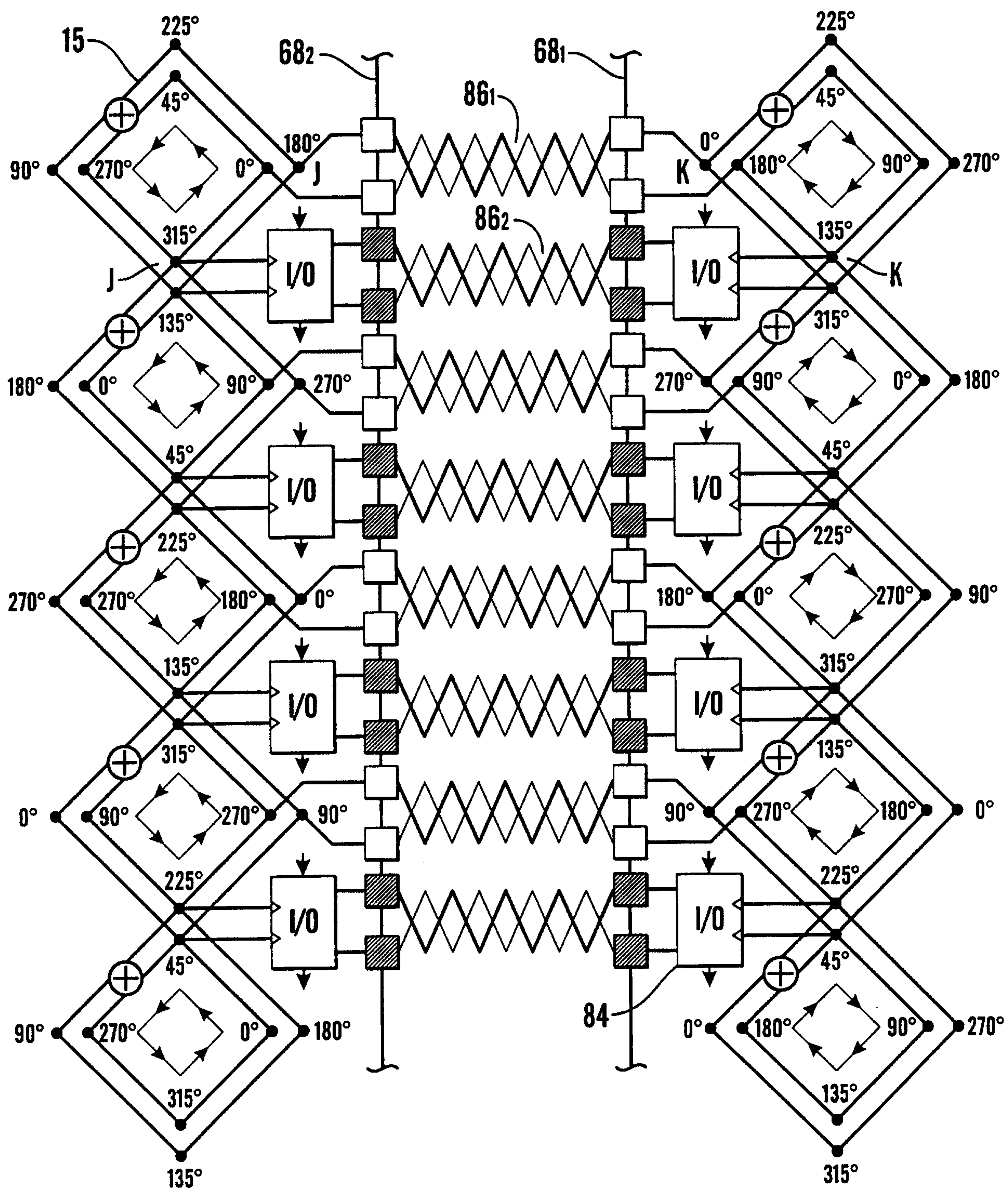


Fig.32a

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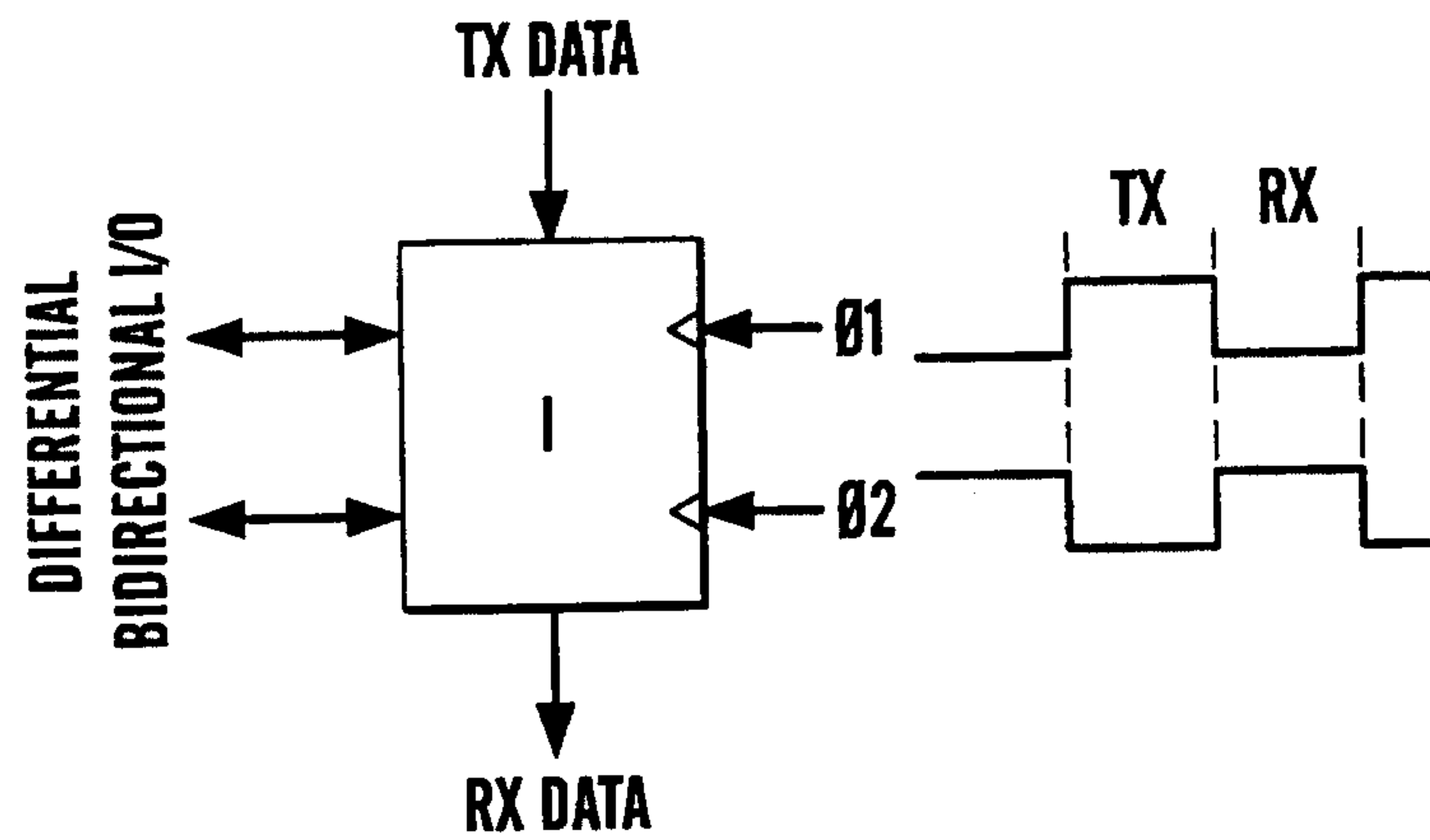


Fig.32b

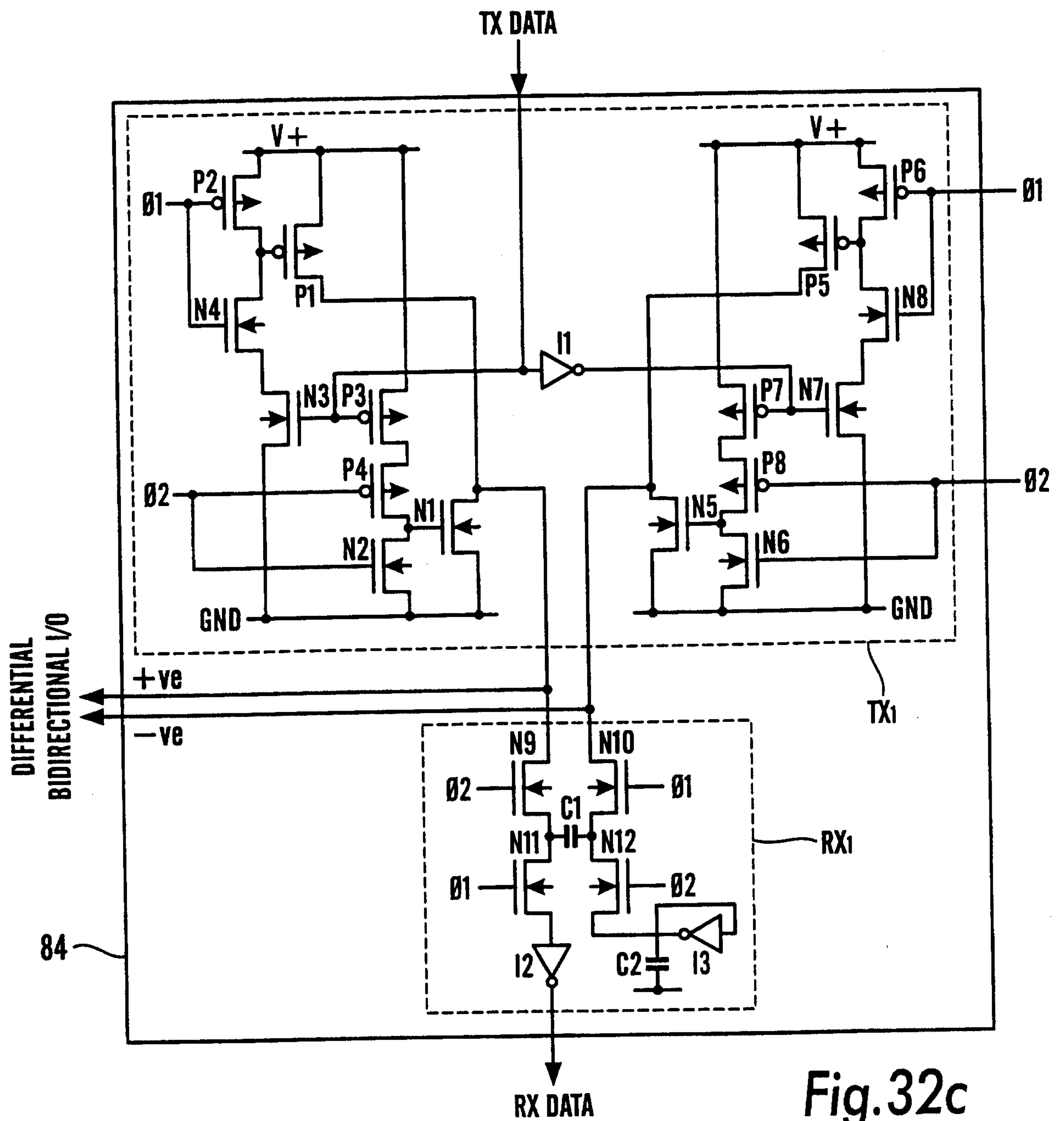


Fig.32c

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Fig.32d

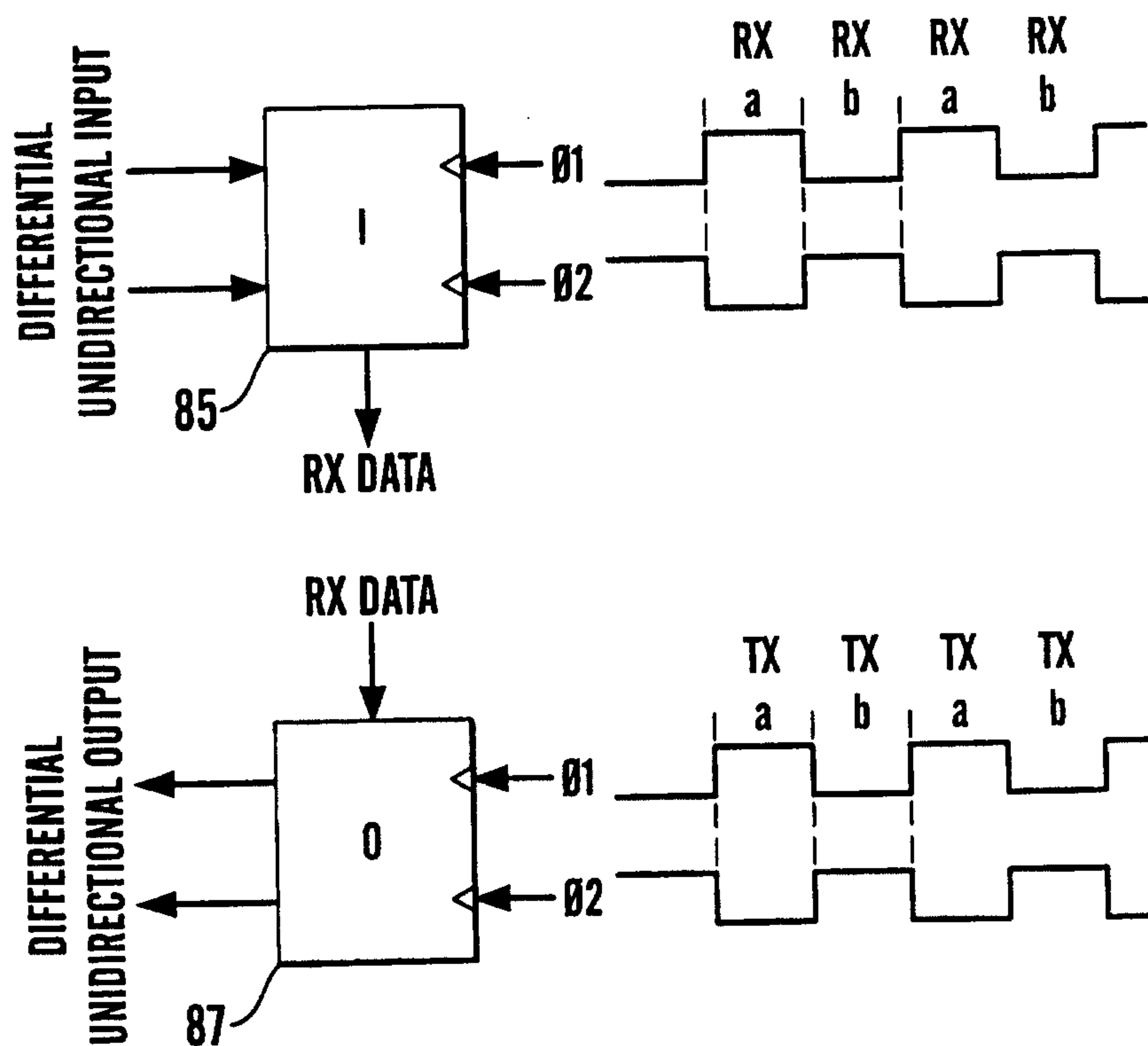
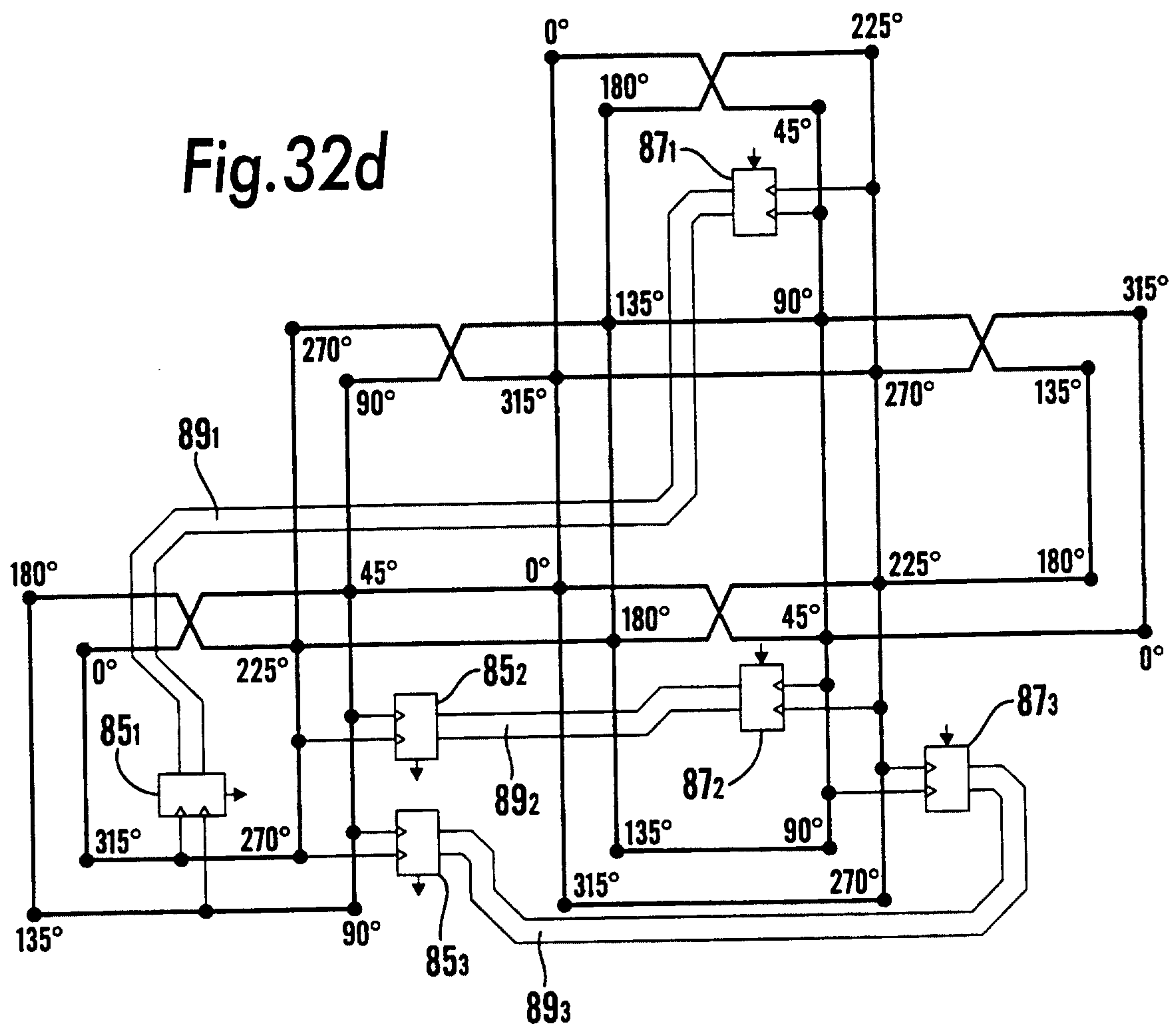


Fig.32e

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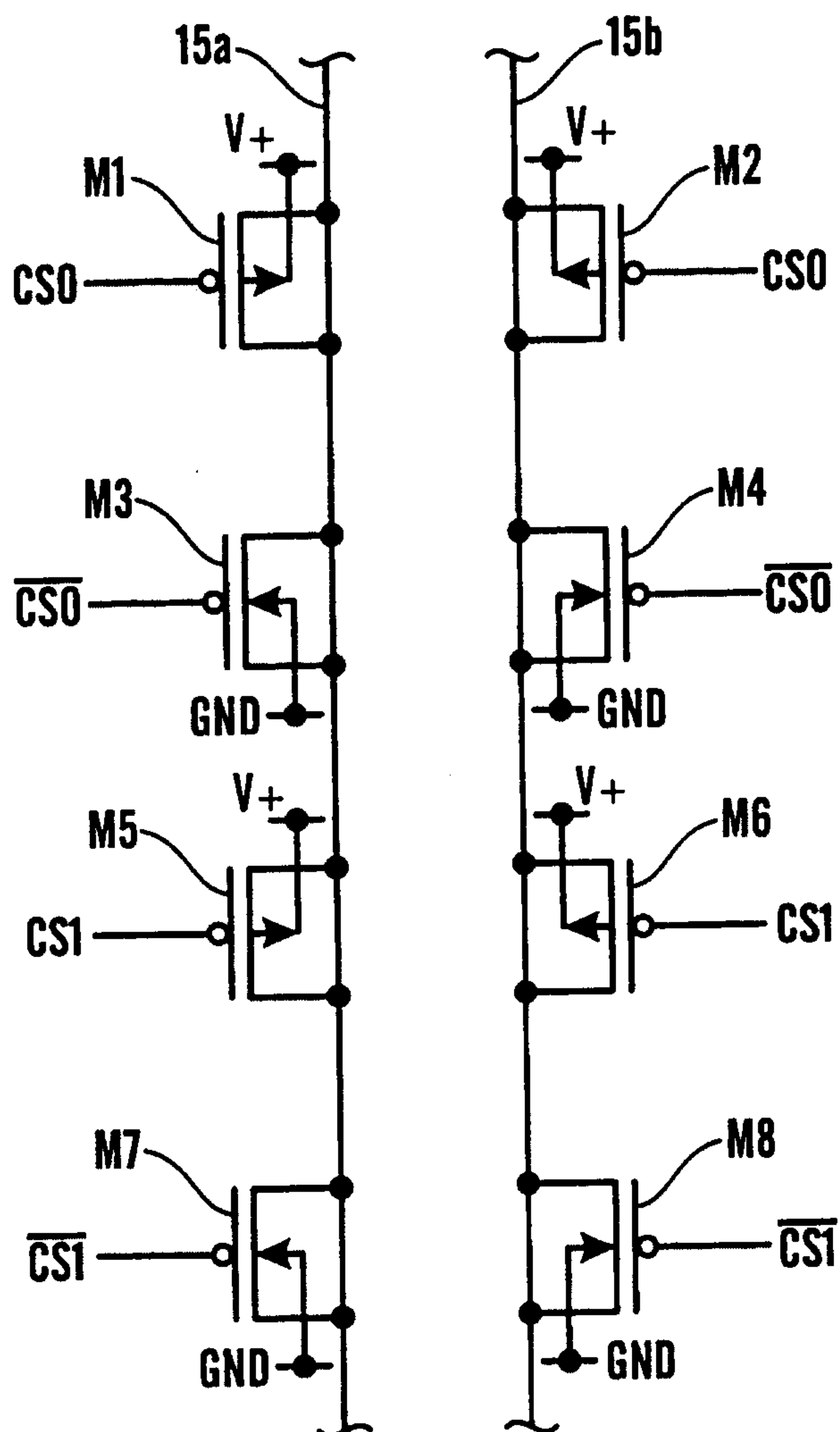


Fig.33

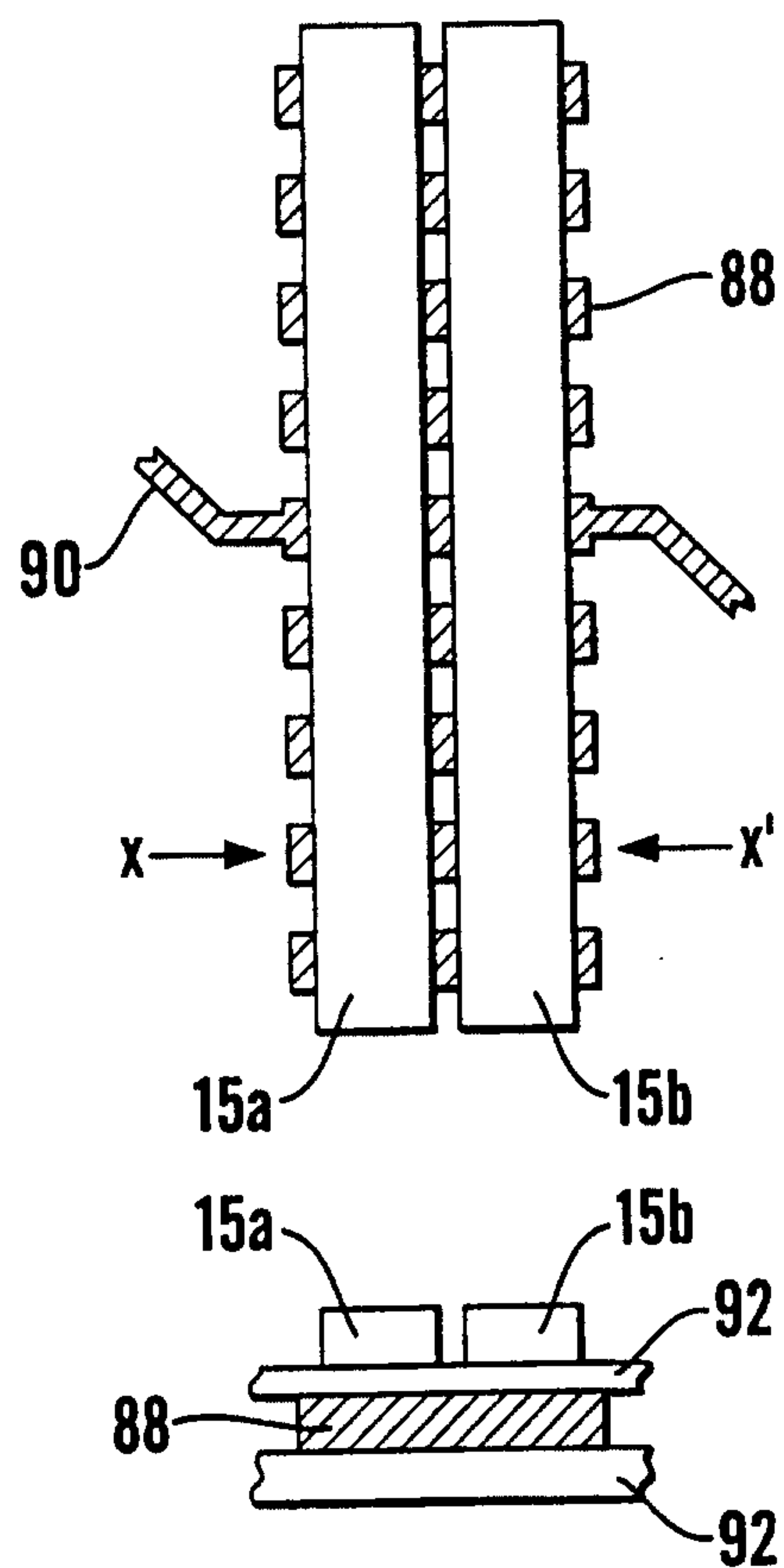


Fig.34

