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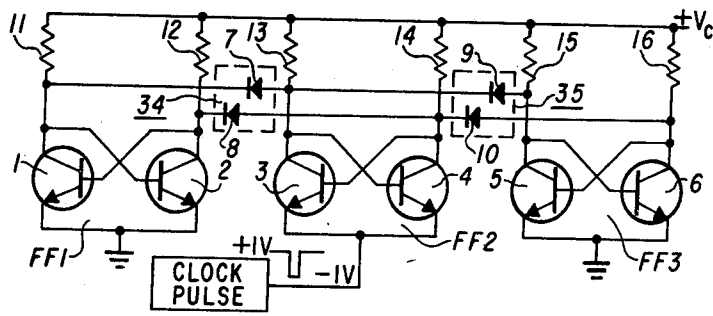
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[54] **INFORMATION TRANSFER SYSTEM**
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307/238, 328/37
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11/40, H03k 3/286
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(FF), 173; 328/37; 307/221, 224, 299 (A), 291;
317/235 (22)

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ABSTRACT: An information transfer system for transferring binary information from a first storage unit to a second storage unit in successive steps utilizing an intermediate storage unit and gates differently responsive to various conditions of an energizing source. During one condition of the energizing source, the binary information is transferred from the first storage unit to the intermediate storage unit, gates allowing communication between the first storage unit and the intermediate storage unit while blocking communication between the intermediate storage unit and the second storage unit. During another condition of the energizing source, the binary information is transferred from the intermediate storage unit to the second storage unit, gates allowing communication between the intermediate storage unit and the second storage unit while blocking communication between the intermediate storage unit and the first storage unit. The gates are differently responsive to two predetermined conditions of the energizing source in order to effect the desired communication and transfer of information between the storage units while these gates are non responsive to the energizing source when it is changing between these predetermined conditions so that the desired operation of the system is achieved only during two predetermined conditions of the energizing source.



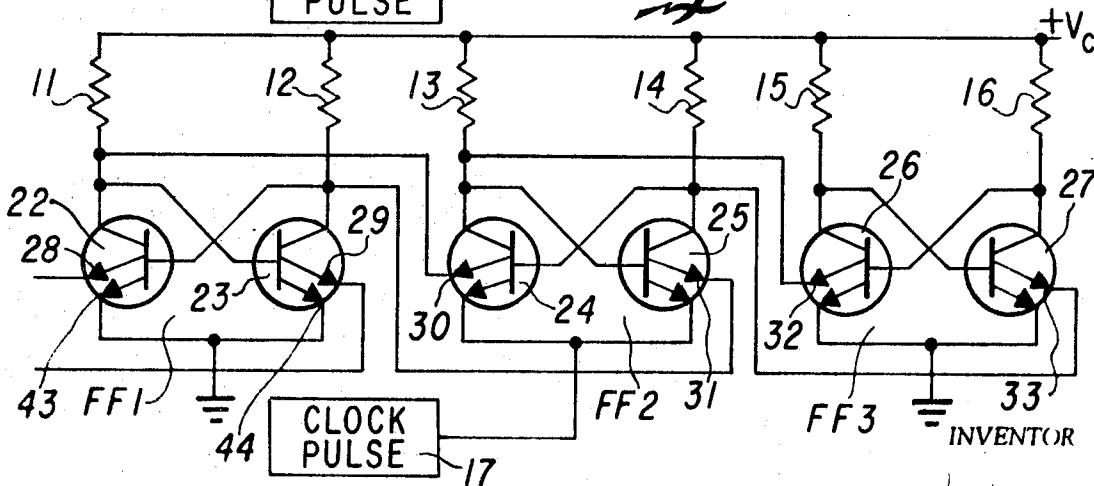
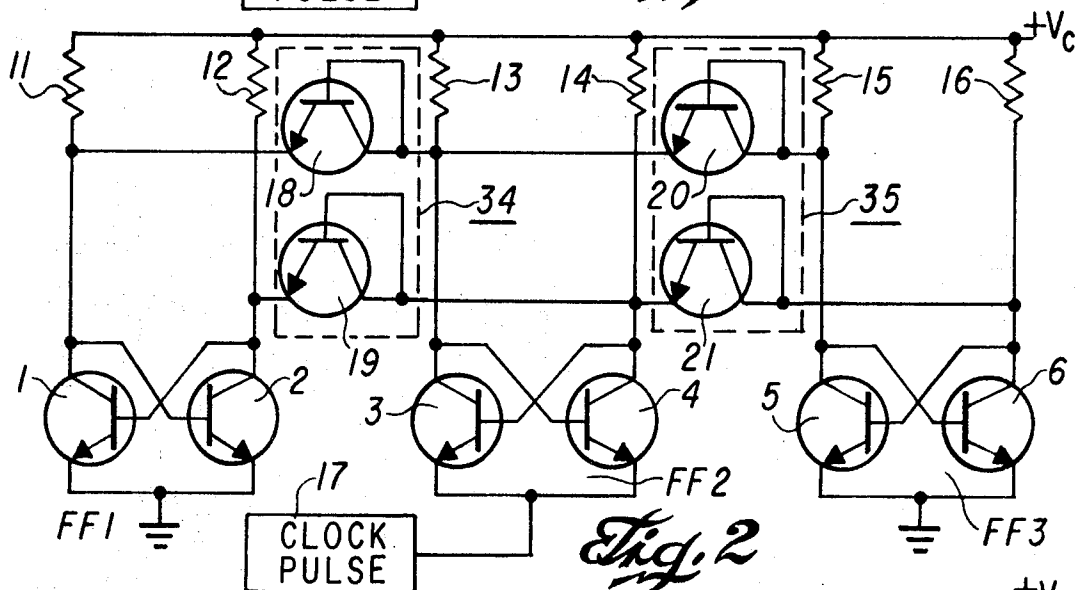
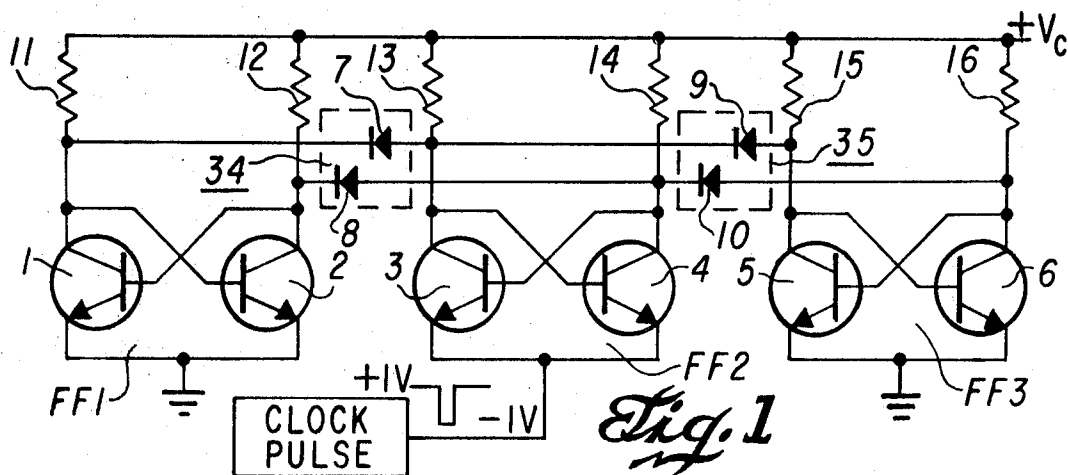
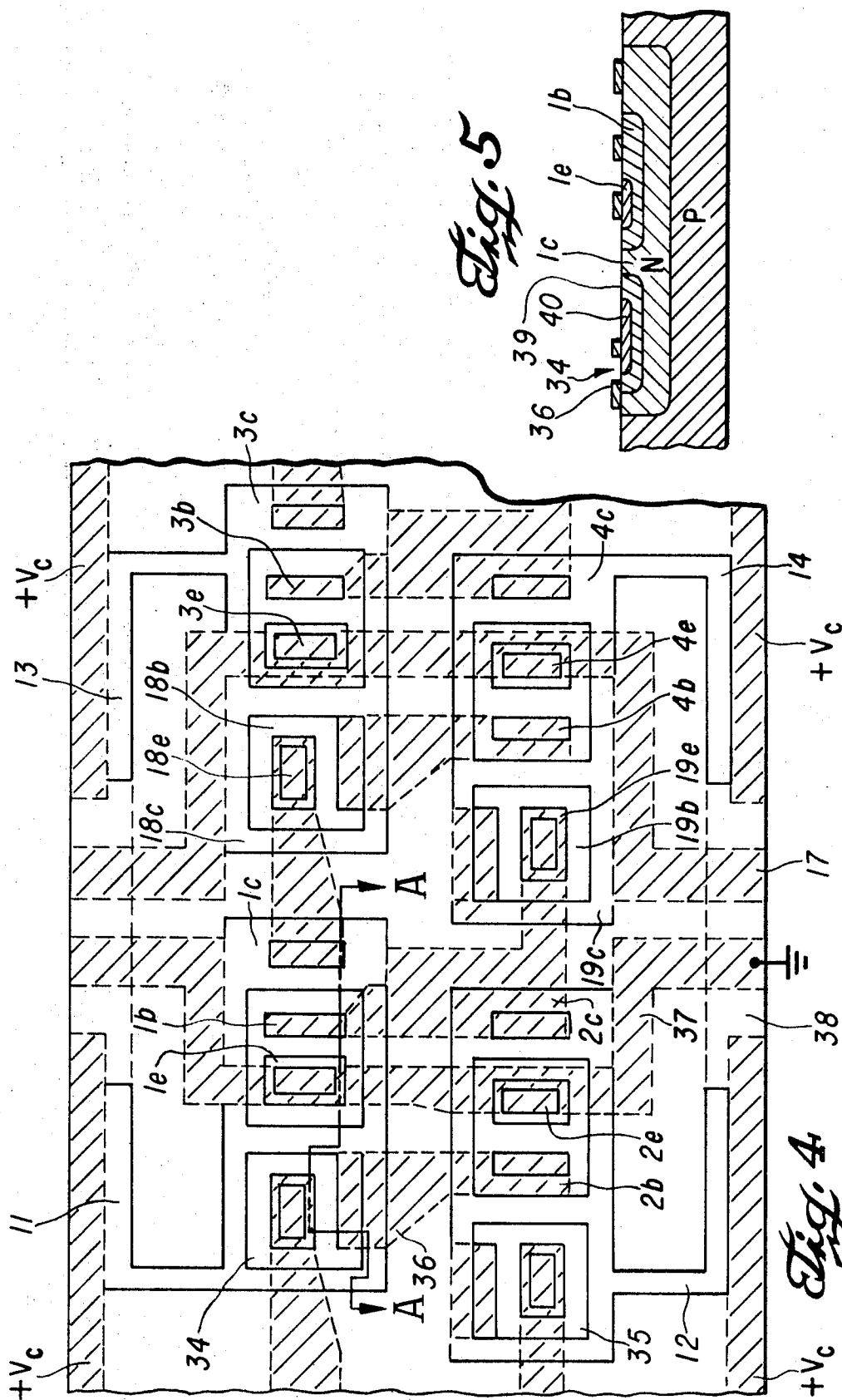
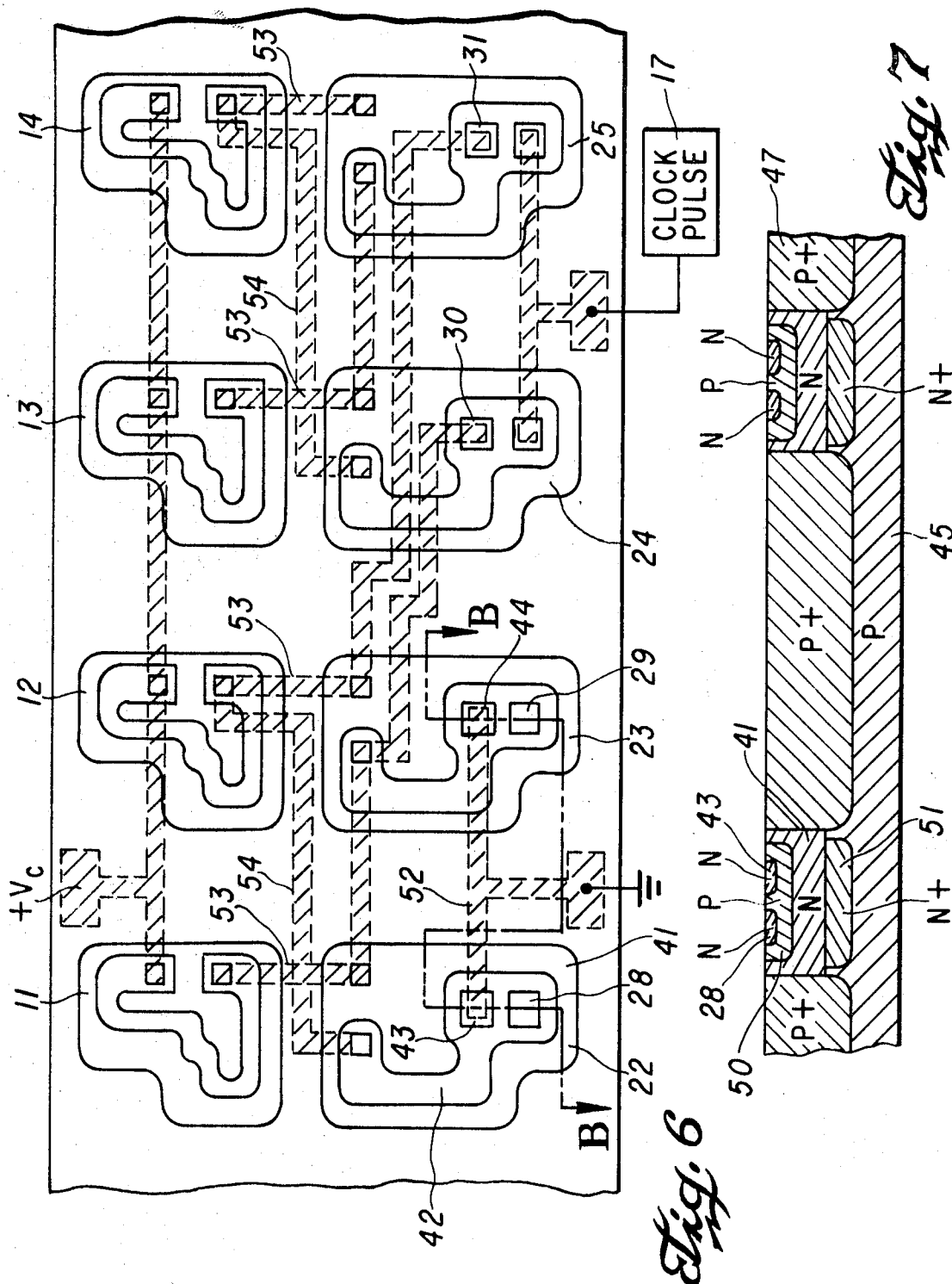


Fig. 3

BY

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INFORMATION TRANSFER SYSTEM

The present invention relates to information transfer systems and more particularly to shift registers wherein binary is transferred from one storage unit to another under the control of an energizing source.

In shift registers, binary information or a bit represented as a 1 or a 0 is transferred from one storage unit to another successively under the control of a clocking pulse or energizing source. The storage units are generally permanent bistable memory elements such as flip-flops, PNP switches, or thyratrons. In transferring the binary information from one storage unit to another, different kinds of intermediate storage units are utilized. One kind of intermediate storage unit is a temporary memory element such as a resistance capacitance network which eliminates active devices as part of the intermediate storage device but requires large capacitors which cause timing difficulties and are not compatible with present day miniaturized monolithic semiconductor circuit techniques. Another kind of intermediate storage unit is a permanent bistable memory element the same as that utilized for the other storage units of the shift register. However, permanent intermediate storage units heretofore utilized to effect two step or two phase transfer of binary information from one storage unit to another has required complicated electrical circuitry.

Accordingly, one object of the present invention is to transfer binary information from one storage unit to another utilizing a simple system and circuitry.

Another object is to provide an information transfer system suitable for high or low speed two step transfer of the binary information between the storage units utilizing low power.

Still another object is to provide an information transfer system especially suitable for miniaturization utilizing monolithic semiconductor circuit technique and suitable for large scale integration in or on a single semiconductor material.

A feature of the present invention is an intermediate storage unit and gates differently responsive to various conditions of an energizing source for effecting two step transfer of binary information from one storage unit to another.

The foregoing and other objects, features and advantages of the invention will be apparent from the following detailed description taken in connection with the appended claims and attached drawings wherein like reference numerals indicate like components and in which:

FIG. 1 is an embodiment of the present invention;

FIG. 2 is another embodiment of the present invention;

FIG. 3 is still another embodiment of the present invention;

FIG. 4 illustrates the top view of a monolithic integrated semiconductor circuit embodying the storage units FF1, FF2, gate 34 and resistors 11-14 of the embodiment illustrated in FIG. 2;

FIG. 5 illustrates a cross section of the FIG. 4 embodiment taken along the lines A-A.

FIG. 6 illustrates the top view of a monolithic integrated semiconductor circuit embodying the storage units FF1, FF2, gates 28-29, 30-31, and resistors 11-14 of the embodiment illustrated in FIG. 3; and

FIG. 7 illustrates a cross section of the FIG. 6 embodiment taken along the lines B-B.

Referring to FIG. 1, binary information contained in the storage unit FF1 is to be transferred to the storage unit FF3 by way of the intermediate storage units FF2. The storage units FF1, FF2 and FF3 are identical bistable flip-flops each comprising two transistors. Each transistor of a storage unit has its collector directly connected to the base of the other. The emitters of transistors 1, 2, 5 and 6 are connected to ground and the emitters of transistors 3 and 4 are connected to the energizing source of clock pulse 17. The collector bias voltage $+V_c$ is connected to the collectors of transistors 1-6 by way of the resistors 11-16. Gate 34 comprises diodes 7 and 8. The diode 7 has its cathode connected to the collector of transistor 1 and its anode connected to the collector of transistor 3 while

diode 8 has its cathode connected to the collector of transistor 2 and its anode connected to the collector of transistor 4. Gate 35 comprises diodes 9 and 10. Diode 9 has its cathode connected to the collector of transistor 3 and its anode connected to the collector of transistor 5 while diode 10 has its cathode connected to the collector of transistor 4 and its anode connected to the collector of transistor 6.

The embodiment of FIG. 1 represents one and one-half bits of a shift register. That is to say, one bit comprises storage unit FF1 and intermediate storage unit FF2. Storage unit FF3 and another intermediate storage units would be a second bit of the shift register.

The information transfer system of FIG. 1 operates as follows:

For the purpose of this description, the 1 state of a storage unit shall be defined as the collector voltage of the right-hand transistor being higher than the collector voltage of the left-hand transistor of a storage unit. Thus, if storage unit FF1 is in the 1 state, transistor 1 is on and transistor 2 is off. Conversely, if storage unit FF1 is in the 0 state, transistor 1 is off and transistor 2 is on.

Assume that storage unit FF1 is in the 1 state (transistor 1 on and transistor 2 off) and the clock pulse 17 is at +1 volts. Consequently, the cathode of diode 7 is at about +0.1 volts and the cathode of diode 8 is at about +0.7 volts. At this point it is not material whether the intermediate storage unit FF2 is in the 1 or 0 state since if it is in the 0 state it will be driven into the 1 state or if it is in the 1 state it will be maintained there. For example, assume that intermediate storage unit FF2 is in the 0 state (transistor 3 off, transistor 4 on). The collector voltage of transistor 3 is higher than the collector voltage of transistor 4 and the collector voltage of transistor 3 is sufficient to forward bias diode 7 and turn it on while the collector voltage of transistor 4 is insufficient to forward bias the diode 8. When diode 7 turns on, it drives the collector voltage of transistor 3 lower which in turn lowers the voltage on the base of transistor 4. Transistor 4 begins to conduct less heavily, increasing the positive voltage on the base of transistor 3 whereby transistor 3 turns on and transistor 4 turns off. Diode 8 remains off since the collector voltage of transistor 4, even when on, is insufficient to forward bias the diode 8. However, when transistor 3 is on, its collector voltage is still sufficient to maintain diode 7 forward biased. In this manner, intermediate storage unit FF2 is driven into the 1 state corresponding to the 1 state of storage unit FF1.

During these conditions both diodes 9 and 10 are off since the positive voltage, appearing at their cathodes, is sufficiently great to prevent forward biasing of either diode 9 or 10 regardless of the state of storage unit FF3. Consequently, during the +1 volt condition of the clock pulse 17, gate 35 blocks communication between the intermediate storage unit FF2 or storage unit FF1 and the storage unit FF3 while gate 34 allows communication between the storage unit FF1 and the intermediate storage FF2 to cause the state of intermediate storage unit FF2 to be driven into correspondence with that of storage unit FF1.

Assume now that storage unit FF1 is in the 1 state, clock pulse 17 is at +1 volts and intermediate storage unit FF2 is in the 1 state. The voltage at the cathode of diode 8 is greater than the voltage at the cathode of diode 7. The collector voltage of transistor 4 is higher than the collector voltage of transistor 3 but the collector voltage of transistor 4 is not sufficiently great to forward bias the diode 8 while the collector voltage of transistor 3 is sufficiently great to slightly forward bias the diode 7 thereby maintaining transistor 3 and transistor 4 off. Under these conditions, the positive voltages at the cathodes of diodes 9 and 10 are sufficiently great to prevent forward biasing of either diode 9 or 10 regardless of the state of storage unit FF3. Consequently, the action of gate 34 in response to the voltage levels caused by the +1 condition of the clock pulse 17 allows the storage unit FF1 to communicate with the intermediate storage unit FF2 and maintain the state of the intermediate storage unit FF2 in correspondence with

the state of the storage unit FF1 while the gate 35 blocks communication between the intermediate storage unit FF2 or the storage unit FF1 and the storage unit FF3.

Assume now that the storage unit FF1 is in the 1 state, the intermediate storage unit FF2 is in the 1 state, and the clock pulse is at -1 volts. The collector voltages of transistors 3 and 4 decrease and becomes negative, the collector voltage of transistor 3 more negative than the collector voltage of transistor 4. Both diodes 7 and 8 are reverse biased thereby preventing any communication between storage unit FF1 and intermediate storage unit FF2. At this point storage unit FF3 may be in the 1 or 0 state and it will be driven or maintained in the 1 state. Whether transistor 5 is on or off, the collector voltage of transistor 5 is sufficient to forward bias the diode 9 since the cathode of diode 9 is sufficiently more negative than the cathode of diode 10. Assume that storage unit FF3 is in the 0 state (transistor 5 off, transistor 6 on), diode 9 turns on since the collector voltage of transistor 5 is sufficiently positive with respect to the cathode of diode 9 to forward bias diode 9 thereby decreasing the collector voltage of transistor 5, decreasing the base voltage of transistor 6, and causing transistor 6 to conduct less heavily. Consequently, the collector voltage of transistor 6 increases and causes the base voltage of transistor 5 to increase. Transistor 5 now turns on and transistor 6 turns off placing storage unit FF3 in the 1 state. Diode 10 remains off since the negative voltage at its cathode is insufficiently negative with regard to the voltage swing at the collector of transistor 6 to reverse bias diode 10. In this manner, gate 35 allows intermediate storage unit FF2 to communicate with storage unit FF3 and drive the state of storage unit FF3 into correspondence with the state of the intermediate storage unit FF2.

Similarly, assume storage unit FF1 in the 1 state, intermediate storage unit FF2 in the 1 state, storage unit FF3 in the 1 state and the clock pulse 17 at -1 volts. The collector voltages of transistors 3 and 4 become negative, the collector voltage of transistor 3 more negative than the collector voltage of transistor 4. Gate 34 block communication between the storage unit FF1 and the intermediate storage unit FF2 or the storage unit FF3. The collector voltage of transistor 6 is not sufficiently positive with regard to the negative cathode voltage of diode 10 to forward bias diode 10. However, the diode 9 is forward biased and maintains transistor 5 on.

The gates 34 and 35 respond differently to the two predetermined conditions of the energizing source 17 to allow and prevent communication between the desired storage units.

Moreover there is an intermediate or third condition of the energizing source 17 (about 0 ± 0.2 volts) between the two predetermined conditions where the gates 34 and 35 are non-responsive since during this third condition of the energizing source, the voltage swings at the collectors of transistors 3 and 4 are insufficient to significantly influence the forward or reverse biasing of the diodes 7-10.

For example, assume that the storage unit FF1 is in the 1 state and the clock pulse 17 is at $+1$ volts. The diode 7 is on and diodes 8-10 are off. When the clock pulse decreases from $+1$ volts to -1 volts, gate 34 continues to allow communication between the storage units FF1 and FF2 only until the clock pulse reaches a certain lower voltage level (about $+0.7$ volts) at which time the gate 34 ceases to allow communication, and at an even lower voltage level (about 0.2 volts) the gate 35 responds if necessary i.e. storage unit FF3 in the 0 state, to allow communication between the intermediate storage unit FF2 and the storage unit FF3. However, if storage unit FF3 is already in the 1 state, the gate 35 responds at about -0.7 volts and maintains the already existing 1 state of the storage unit FF3.

Furthermore, when the voltage of the clock pulse 17 increases from -1 volts to $+1$ volts, there is a certain higher voltage level (about -0.7 volts) at which the gate 35 ceases to allow communication between the intermediate storage unit FF2 and the storage unit FF3 and at an even higher voltage level about $+0.2$ volts the gate 34 responds if necessary i.e. in-

intermediate storage unit FF2 in the 0 state, to allow communication between the intermediate storage unit FF2 and the storage unit FF1. However if the intermediate storage unit FF2 is already in the 1 state, the gate 34 responds at about $+0.7$ volts and maintains the already existing 1 state of the intermediate storage unit FF2.

Thus, during one condition of the energizing source 17, the gate 35 is in a blocking condition and isolates the storage unit FF3 from the preceeding storage unit and the gate 34 drives or maintains the state of the intermediate storage unit FF2 in correspondence with the state of the storage unit FF1. When the condition of the energizing source is changing that is, the energizing source is in the third condition, both gates 34 and 35 are nonresponsive that is, there is no communication between the storage units, until certain levels of the energizing source are reached at which time the gates 34 and 35 become responsive to the second condition of the energizing source and the gate 34 blocks and isolates storage unit FF1 from the succeeding storage unit while gate 35 drives or maintains the state of storage unit FF3 in correspondence with the state of the intermediate storage unit FF2.

The energizing source may take the form of a clock pulse as illustrated in the drawings or may be any wave shape that rises and falls above and below a predetermined voltage range which in the case described is about 0 ± 0.2 volts. During this predetermined range or third condition, the gates 34 and 35 are nonresponsive to the energizing source. If the storage unit FF1 and the storage unit FF2 are in the same state, this conformity of the states is maintained at about $+0.7$ volts. However, if the storage unit FF1 and the intermediate storage unit FF2 are in different states, the intermediate storage unit FF2 is driven into the opposite state at about $+0.2$ volts. If the intermediate storage unit FF2 and the storage unit FF3 are in the same state, this conformity of the states is confirmed at about -0.7 volts. However, if the intermediate storage unit FF2 and the storage unit FF3 are in opposite states, the storage unit FF3 is driven into the opposite state at about -0.2 volts.

The information transfer system of the present invention thereby senses and responds to two conditions of the energizing source to effect the two step transfer of binary information from one storage unit to another while being essentially insensitive or non responsive to the third condition of the energizing source when it is changing between the first and second predetermined conditions.

The embodiment of FIG. 2 is similar to that of FIG. 1 and operates in the same manner. However, gates 34 and 35 of FIG. 2 comprise transistors each having its collector and base electrodes electrically shorted together. This construction is especially suitable for incorporation into a miniaturized monolithic semiconductor circuit since all the transistors 1-6 and 18-21 are identical and can be fabricated and processed at the same time and in like manner in a single semiconductor material. Moreover, the embodiment and circuit figuration of FIG. 2 are especially suitable for lower speed applications where high f_t is desired and incorporation into a monolithic integrated semiconductor circuit utilizing triple diffused processing techniques as will more fully be described later in connection with FIGS. 4 and 5.

The embodiment of FIG. 3 is similar to the embodiment of FIGS. 1 and 2 except that multi emitter transistors 22-27 are employed in place of the transistors 1-6 and gates 34 and 35 of FIGS. 1 and 2. The embodiment of FIG. 3 operates in the same manner as the embodiments of FIGS. 1 and 2 except that the intermediate storage unit of FIG. 3 has a state which is inverted with respect to the state of the storage unit FF1. For example, assume that the storage unit FF1 is in the 1 state and the clock pulse 17 is at the -1 volt condition. The emitter 31 is more positive than the emitter 30. Assume that intermediate storage unit FF2 is in the 1 state (transistor 24 on, transistor 25 off) the collector voltage of transistor 25 is more positive than the collector voltage of transistor 24 whereby the PN junction represented by the base of transistor 24 and the emitter 30 is forward biased, lowering the collector voltage

of transistor 25 and causing transistor 24 to turn on and transistor 25 to turn off. Consequently, intermediate storage unit FF2 is driven into the 0 state so that it inversely corresponds to the state of storage unit FF1. When the clock pulse 17 is at -1 volts, the gate represented by emitters 30 and 31 is blocked and emitter 33 becomes more negative than emitter 32. Regardless of whether storage unit FF3 is in the 1 or 0 state, it will be driven or maintained in the 1 state. Assume that storage unit FF3 is in the 0 state. The collector voltage of transistor 26 is more positive than the collector voltage of transistor 27. The PN junction represented by the base of transistor 27 and the emitter 33 is forward biased while the PN junction represented by the base of transistor 26 and the emitter 32 is reversed biased. Accordingly, the collector voltage of transistor 26 decreases and turns transistor 26 on while driving transistor 27 off. The forward biased PN junction represented by the base of transistor 27 and the emitter 33 in effect adds current to the transistor 26 which is initially off. On the other hand, in the embodiments of FIGS. 1 and 2 current is taken away from a transistor which is on in order to drive a storage unit into the opposite state.

Returning now to FIG. 3, the storage unit FF3 has been driven into the 1 state and now corresponds with the original state of storage unit FF1 from which the binary information was transferred. The only inversion that takes place is in the intermediate storage unit FF2.

The embodiment and circuit construction of FIG. 3 are especially suitable for microminiaturized monolithic integrated semiconductor circuits since the multiemitter transistors 22-27 are identical and can be fabricated and processed at the same time and in like manner in a single semiconductor material. Moreover, the embodiment of FIG. 3 is especially suitable for incorporation in monolithic integrated semiconductor circuits of the single or double epitaxial type which will be more fully described later in connection with FIGS. 6 and 7.

FIG. 4 illustrates the top view of a monolithic integrated semiconductor circuit of the triple diffused type embodying transistors 1-4, resistors 11-14 and gate 34 illustrated in FIG. 2. Referring to FIG. 4, transistor 1 comprises a diffused collector 1c, diffused base 1b and diffused emitter 1e, transistor 2 comprises diffused collector 2c, diffused base 2b, and diffused emitter 2e, transistor 3 comprises diffused collector 3c, diffused base 3b and diffused emitter 3e, and transistor 4 comprises diffused collector 4c, diffused base 4b and diffused emitter 4e. The transistors 18 and 19 of gate 34 are formed respectively in the diffused collectors 3c and 4c of transistors 3 and 4. Transistor 18 comprises collector region 18c which is integral with the diffused collector 3c and ohmically connected therewith in the semiconductor material. The base 18b of transistor 18 is formed within the collector 3c or 18c, the diffused emitter of transistor 18 being 18e. Similarly, the transistor 19 is formed within the diffused collector 4c. Whereas, transistor 19 comprises collector region 19c integral with the collector 4c and ohmically connected therewith within the semiconductor material, diffused base 19b and diffused emitter 19e. Transistor 1-4 and transistors 18 and 19 interconnected in the manner shown comprise one bit of a shift register. FIG. 4 additionally illustrates transistors 34 and 35 formed within the diffused collectors 1c and 2c which transistors 34 and 35 are identical to 18 and 19 and would comprise the gate coupled to a preceding intermediate storage unit of the shift register for controlling the inputs to the storage unit FF1. The resistors 11-14 are diffused resistors made at the same times as the collector diffusion so that one end of each resistor is integral with and ohmically connected to the collector of its corresponding transistor.

The monolithic integrated semiconductor circuit is fabricated by the planar process in which an oxide film is thermally grown on a P-type silicon substrate of the desired resistivity by placing it in a furnace at an elevated temperature and passing an oxidizing agent over it. The silicon dioxide produced acts as a masking medium against the impurities

which are later diffused into the substrate. Holes are produced in the oxide film to allow subsequent diffusion processes to form the isolation, resistor and transistor functions. These holes which are patterns of the desired circuit elements are produced by photolithographic techniques. Contacts and interconnections to the circuit elements are made by similar photolithographic techniques using for example evaporated aluminum over the oxide to form a pattern connecting the circuit elements together. The connecting pattern comprises conductive strips 36, 37, etc. and where conductive strips need to crossover each other "tunnels" or multilevel interconnections can be formed as is described more fully in copending patent application, filed Jun. 5, 1967, entitled "Method of Making Semiconductor Devices" by Jack S. Kilby which is assigned to the assignee of the present application and which is a continuation application of Ser. No. 420,031, now abandoned. For example, a "tunnel" is provided at 38 so that the conductive strips to which ground and the clock pulse 17 are attached can crossover the "tunnel" which interconnects within the semiconductor material the two conductive strips labeled $+V_c$ to which the collector supply voltage is attached.

FIG. 5 is a cross section taken along the lines A-A of FIG. 4 and illustrates principally the semiconductor portion of the structure to show the transistor 1 and gate transistor 34 formed in its collector region. Referring to FIG. 5, transistor 1 comprises the N-type collection region 1c, the P-type base region 1b, and the N-type emitter region 1e. The gating transistor 34 is identical to the transistors 18 and 19 and comprises the N-type collector region 1c. The P-type base region 39 and the N-type emitter region 40. The metal contact 36 is deposited on the P-N junction formed by the zones 1c and 39 and shorts out this P-N junction so that the base and collector electrodes of transistor 34 are shorted together as is illustrated in FIG. 2 with respect to the transistor 18 and 19.

FIG. 6 illustrates the top view of a monolithic integrated semiconductor circuit of the single epitaxial type embodying the multiemitter transistors 22 through 25 and resistor 11-14 illustrated in FIG. 3. The monolithic integrated semiconductor circuit of the epitaxial type comprises a P-type silicon substrate having a N-type epitaxial layer deposited on one surface thereof. The multiemitter transistors 22-25 are formed by silicon oxide masking, diffusion techniques and photolithographic techniques to form the isolation, resistor and transistor functions whereby the transistor 22, for example comprises an N-type collector region 41 comprised of the epitaxial layer, a P-type diffused base region 42 and diffused multiemitters 28 and 43. The diffused emitter 43 is ohmically connected to the emitter 44 of transistor 23 and to ground by the metallic strip 52. The additional emitter 28 of transistor 22 would be connected to a preceding stage of the shift register. The resistors 11-14 are diffused resistors having one end respectively connected to the collectors of transistors 22-25 by metallic strips 53. The circuit elements illustrated in FIG. 6 are interconnected utilizing a connecting pattern in the form of strips over the silicon oxide insulating layer to interconnect the various components and where the metal strips need to crossover one another to effect the circuit interconnections, multi level interconnections are utilized as is more fully described in the aforementioned copending application. For example, strips 53 are illustrated as crossing over the strips 53 which connect the base of transistor to a resistor. This crossover can be effected using multilevel connections, strips 54 being formed on a first level pattern and strips 53 being formed on a second higher level.

FIG. 7 is a cross section of FIG. 6 taken along the lines B-B and illustrated the semiconductor portion of the structure wherein 45 is the P-type silicon substrate. 41 is the N-type epitaxial layer deposited on the surface of the P-type substrate 45, 47 represents the p^+ isolation diffusions made by selectively diffusing a P-type impurity through the N-type epitaxial layer in order to leave islands of N-type material 41 in which the circuit elements are to be formed. 50 is the P-type diffused base region of transistor 22 formed in the N-type epitaxial col-

lector region 41 and 28 and 43 are the N-type diffused multi-emitter regions. 51 represents an N+ buried diffused region under the collector region 41 to provide lower collector saturation resistance as is known from U.S. Pat. No. 3,211,972.

It is to be understood that the above-described embodiments are merely illustrative of the invention. Numerous other embodiments may be devised by those skilled in the art without departing from the spirit and scope of the invention as defined by the appended claims.

I claim:

1. An information transfer system comprising: a first storage unit containing binary information, a second storage unit, a variable energizing source, transfer means including an intermediate storage unit responsive to said variable energizing source for transferring binary information from said first storage unit to said second storage unit, said transfer means including gate means responsive to one condition of said variable energizing source for transferring said binary information from said first storage unit to said intermediate storage unit, while blocking the transfer of binary information into said second storage unit and responsive to a different condition of said energizing source for transferring said binary information from said intermediate storage unit into said second storage unit while blocking the transfer of binary information from said first storage unit into said intermediate storage unit and nonresponsive to said energizing source when it is changing from said one condition to said different condition and wherein said first storage unit comprises first and second transistors, the collector of said first transistor being directly connected to the base of said second transistor, the collector of said second transistor being directly connected to the base of said first transistor, the emitters of said first and second transistor being connected together, said intermediate storage unit comprising third and fourth transistors, the collector of said third transistor being directly connected to the base of said fourth transistor, the collector of said fourth transistor being directly connected to the base of said third transistor, and the emitters of said third and fourth transistors being connected together, said second storage unit comprising fifth and sixth transistors, the collector of said sixth transistor being directly connected to the base of said sixth transistor, the collector of said sixth transistor being directly connected to the base of said fifth transistor, and the emitters of said fifth and sixth transistors being connected together, and a biasing voltage being connected to the collectors of said transistors.

2. An information transfer system comprising a first storage unit containing binary information, said first storage unit comprising first and second transistors, the collector of said first transistor being directly connected to the base of said second transistor, the collector of said second transistor being directly connected to the base of said first transistor and the emitters of said first and second transistors being connected together, a second storage unit comprising third and fourth transistors, the collector of said third transistor being directly connected to the base of said fourth transistor, the collector of said fourth transistor being directly connected to the base of said third transistor, and the emitters of said third and fourth transistors being connected together, a variable energizing source, transfer means including an intermediate storage unit responsive to said variable energizing source for transferring binary information from said first storage unit to said second storage unit, said transfer means including gate means responsive to one condition of said variable energizing source for transferring said binary information from said first storage unit to said intermediate storage unit while blocking the transfer of binary information into said second storage unit and responsive to a different condition of said energizing source for transferring said binary information from said intermediate storage unit into said second storage unit while blocking the transfer of binary information from said first storage unit into said intermediate storage unit and nonresponsive to said energizing source when it is changing from said one condition to said dif-

ferent condition, said intermediate storage unit comprising fifth and sixth transistors, the collector of said fifth transistor being directly connected to the base of said sixth transistor, the collector of said sixth transistor being directly connected to the base of said fifth transistor and the emitters of said fifth and sixth transistors being connected to said variable energizing source and wherein said gate means comprises a first asymmetrically conductive means directly coupled between the collector of said first transistor and the collector of said third transistor, a second asymmetrically conductive means directly coupled between the collector of said second transistor and the collector of said fourth transistor, a third asymmetrically conductive means connected between the collector of said third transistor and the collector of said fifth transistor, and a fourth asymmetrically conductive means connected between the collector of said fourth transistor and the collector of said sixth transistor.

3. An information transfer system according to claim 2 wherein said first, second, third and fourth asymmetrically conductive means each comprise a transistor having its base and collector electrodes connected together.

4. An information transfer system comprising a semiconductor wafer, a first storage unit containing binary information formed at one surface of said semiconductor wafer, a second storage unit formed at said one surface of said semiconductor wafer, a variable energizing source, transfer means formed at said one surface of said semiconductor wafer, said transfer means including an intermediate storage unit responsive to said variable energizing source for transferring binary information from said first storage unit to said second storage unit, said transfer means including gate means responsive to one condition of said variable energizing source for transferring said binary information from said first storage unit to said intermediate storage unit while blocking the transfer of binary information into said second storage unit and responsive to a different condition of said energizing source for transferring said binary information from said intermediate storage unit into said second storage unit while blocking the transfer of binary information from said first storage unit into said intermediate storage unit and nonresponsive to said energizing source when it is changing from said one condition to said different condition and wherein said first storage unit, said second storage unit and said intermediate unit each comprise a direct coupled collector to base triple diffused transistors in said semiconductor wafer and said gate means comprises a triple diffused transistor in said semiconductor wafer having its base and collector electrodes connected together and being directly connected between the collectors of transistors in different storage units.

5. An information transfer system comprising a semiconductor wafer, a first storage unit containing binary information formed at one surface of said semiconductor wafer, a second storage unit formed at said one surface of said semiconductor wafer, a variable energizing source, transfer means formed at said one surface of said semiconductor wafer, said transfer means including an intermediate storage unit responsive to said variable energizing source for transferring binary information from said first storage unit to said second storage unit, said transfer means including gate means responsive to one condition of said variable energizing source for transferring said binary information from said first storage unit to said intermediate storage unit while blocking the transfer of binary information into said second storage unit and responsive to a different condition of said energizing source for transferring said binary information from said intermediate storage unit into said second storage unit while blocking the transfer of binary information from said first storage unit into said intermediate storage unit and nonresponsive to said energizing source when it is changing from said one condition to said different condition and wherein said semiconductor wafer comprises a semiconductor substrate of one conductivity type and an epitaxial layer of opposite conductivity type on said semiconductor substrate, said first and

second storage unit and said intermediate storage unit each comprise direct coupled collector to base double diffused multiemitter transistors formed in said epitaxial layer said gate means comprises an emitter electrode of each of said multiemitter transistors in said second and intermediate storage units and is coupled to the collector electrode of a multiemitter transistor in a preceding storage unit.

6. An information transfer system comprising: a first storage unit containing binary information, a second storage unit, a variable energizing source, transfer means including an intermediate storage unit responsive to said variable energizing source for transferring binary information from said first storage unit to said second storage unit, said transfer means including gate means responsive to one condition of said variable energizing source for transferring said binary information from said first storage unit to said intermediate storage unit, while blocking the transfer of binary information into said second storage unit and responsive to a different condition of said energizing source for transferring said binary information from said intermediate storage unit into said second storage unit while blocking the transfer of binary information from said first storage unit into said intermediate storage unit and nonresponsive to said energizing source when it is changing from said one condition to said different condition and wherein said first storage unit comprises first and second transistors, the collector of said first transistor being directly connected to the base of said second transistor, the collector of said second transistor being directly connected to the base of said first transistor, the emitters of said first and second transistor being connected together, said intermediate storage unit comprising third and fourth multiemitter transistors, the collector of said third transistor being directly connected to the base of said fourth transistor, the collector of said fourth transistor being directly connected to the base of said third transistor, and one of the emitters of said third and fourth transistors being connected to said variable energizing source, said second storage unit comprising fifth and sixth multiemitter transistors, the collector of said sixth transistor being directly connected to the base of said sixth transistor, the collector of said sixth transistor being directly connected to the base of said fifth transistor, and one of the emitters of said fifth and sixth transistors being connected together, said gate means comprising another emitter of said third, fourth, fifth

and sixth transistors and a biasing voltage being connected to the collectors of said transistors.

7. An information transfer system comprising a first storage unit containing binary information, said first storage unit comprising first and second multiemitter transistors, the collector of said first transistor being directly connected to the base of said second transistor, the collector of said second transistor being directly connected to the base of said first transistor and one of the emitters of said first and second transistors being connected together, a second storage unit comprising third and fourth multiemitter transistors, the collector of said third transistor being directly connected to the base of said fourth transistor, the collector of said fourth transistor being directly connected to the base of said third transistor, and one of the emitters of said third and fourth transistors being connected together, a variable energizing source, transfer means including an intermediate storage unit responsive to said variable energizing source for transferring binary information from said first storage unit to said second storage unit said transfer means including gate means responsive to one condition of said variable energizing source for transferring said binary information from said first storage unit to said intermediate storage unit while blocking the transfer of binary information into said second storage unit and responsive to a different condition of said energizing source for transferring said binary information from said intermediate storage unit into said second storage unit while blocking the transfer of binary information from said first storage unit into said intermediate storage unit and nonresponsive to said energizing source when it is changing from said one condition to said different condition, said intermediate storage unit comprising fifth and sixth multiemitter transistors, the collector of said fifth transistor being directly connected to the base of said sixth transistor, the collector of said sixth transistor being directly connected to the base of said fifth transistor and one of the emitters of said fifth and sixth transistors being connected to said variable energizing source and wherein said gate means comprises another emitter of said third transistor coupled to the collector of said first transistor another emitter of said fourth transistor coupled to the collector of said second transistor another emitter of said fifth transistor connected to the collector of said third transistor and another emitter of said sixth transistor connected to the collector of said fourth transistor.

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