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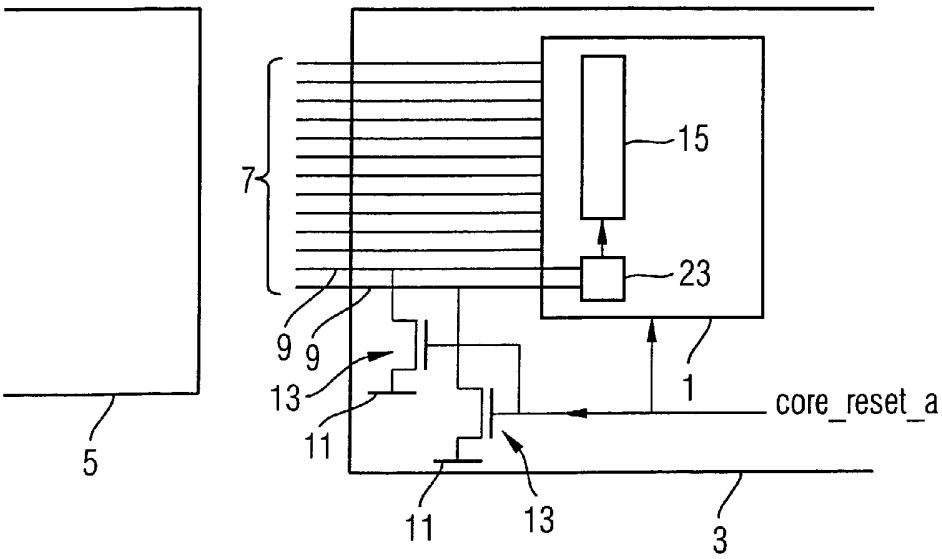
(54) Title: COMMUNICATING DATA IN A SELECTED ONE OF MULTIPLE PROTOCOLS



(57) Abstract: An Ethernet communication interface (1) (for use in equipment (3) such as an (5) Ethernet switch) has a set of interface pins (7) and an internal control logic which assigns respective functions to the interface pins (7) which are consistent with a selected protocol. In other words, the same set of interface pins (7) is used in different ways in the different protocols. This means that any number of protocols may be supported using only a number of interface pins which is as low as the highest number of interface pins required by any single one of the standards. The interface (1) is initialised using initialisation pins (9) among the interface pins (7) which, during an initialisation phase, receive signals indicating which protocol to use. The equipment (3) can ensure that the interface (1) functions in the desired protocol by supplying the corresponding signals to the initialisation pins during the initialisation phase. During the communication phase the input pins (9) are "pin-strapped", to perform the role of output pins.

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Communicating data in a selected one of multiple protocols

Field of the invention

The present invention relates to methods and integrated circuits for transmitting data in a selected one of multiple protocols.

Background of the Invention

A variety of Ethernet MAC interface protocols are known, such as GMII (gigabit medium independent interface), MII (medium independent interface), RGMII (reduced GMII), TBI (ten bit interface), and SMII (serial MII). It would be advantageous if an Ethernet device (such as a switch) were capable of operating according to more than one of these standards, according to which device(s) it is connected to.

The number of pins required by each of these standards is as follows: GMII, 182 pins; MII interface 128 pins; RGMII interface 96; TBI interface, 192 pins, SMII interface 160 pins. Thus, to provide a single data interface with the sets of pins required for multiple respective standards conventionally requires that the total number of pins in the interface is very high, increasing both the size and the area of the interface.

Summary of the invention

The present invention proposes in general terms that, an Ethernet communication interface (for example, an Ethernet switch) having a set of interface pins should include an internal control logic which, according to an interface protocol selected from a predetermined set of interface protocols, assigns respective functions to the interface pins which are consistent with the selected protocol. In other words, the same set of interface pins is used in

different ways in the different protocols. This means that any number of protocols may be supported using only a number of interface pins which is as low as the highest number of interface pins required by any single one of the standards.

Preferably, the interface includes one or more initialisation pins which, during an initialisation phase, receive signals which indicate to the interface which of the protocols is selected. The interface registers the selection, and assigns the functions of the interface pins accordingly. This means that an interface design can be used in a variety of different kinds of equipment which are required to communicate in different respective protocols. The equipment can ensure that the interface functions in the desired protocol simply by supplying the corresponding signals to the initialisation pins during the initialisation phase.

The initialisation pins are preferably comprised among the interface pins. That is, during the initialisation phase the initialisation pins receive the signal indicating the selected format, and subsequently during the communication phase functions are assigned to those pins which enable them to contribute to the communication in the selected format. This means that the total number of pins required by the device is not increased compared to the minimum number required to operate all the predetermined communication protocols. Note that in the second phase the initialisation pins may in certain of the communication protocols be required to be output pins, rather than input pins. The use of pins having input and output roles at different times is known as "pin-strapping".

Note that although this text refers to "pins", no limitation is thereby implied on the physical construction of the pins. For example, the "pins" need not be elongate conductors, but may be any element which permits an electrical connection to be made to a corresponding element of another device.

Brief description of the figures

A non-limiting embodiment of the invention will now be described for the sake of example only with reference to the following drawings in which:

Fig. 1 is a schematic view of the use of an embodiment of the present invention;

Fig. 2 is a schematic view of the pinstrapping operation of the embodiment of Fig. 1; and

Fig. 3 is a view of the control arrangement for assigning functions to the interface pins of the embodiment of Fig. 1.

Detailed Description Of The Embodiments

Referring to Fig. 1 an interface device 1 according to the invention is shown within an item of equipment 3 which is required to communicate with a second item of equipment 5 in a certain communication protocol.

The interface device has a number of interface pins 7 including a plurality (e.g. two) initialisation pins 9. The initialisation pins 9 are connected to respective voltage sources 11 via transistors 13 which conduct only during an initialisation phase indicated by a reset signal ("core_reset_a"), which is transmitted also the interface device 1, becoming high (logic 1) (in other embodiments, a logic 0 value could be the signal for a reset). When the signal core_reset_a is high, a latch 23 reads and stores inputs from the initialisation pins 9 and sends control signals to a control logic 15 of the interface device 1 which sets the communication protocol accordingly. In other words, the equipment 1 can control which communication protocol its interface device 3 uses merely by setting the values of the voltage sources 11 correspondingly. This means that a single design of interface device 3 can be used in multiple kinds of equipment 3 which are required to operate in different respective

communication protocols. Note that the voltage sources 11 may optionally be set to a static value, but more preferably may generate a multibit input to the initialisation pins 9 (e.g. a sequence of highs and lows). One advantage of this is that the number of protocols between which a selection is made need not be limited by the number of initialisation pins.

When the core_reset_a signal becomes logic 0, the communication phase begins. The transistors 13 cease to conduct, cutting the initialisation pins 9 off from the voltage sources 11. The control logic 15 then connect the interface pins 7 to network layer devices (e.g. MAC and GMAC) of the equipment 3 (which may be on the same integrated circuit as the interface 3) with a connectivity determined by the selected protocol. Note that the initialisation pins 9 are used in this phase as if they were normal interface pins 7, so that their signal input role is replaced by a signal output role. Thus, the functions performed by the initialisation pins 9 change ("pinstrapping").

This change of roles is indicated in Fig. 2 which shows how, for a single initialisation pin 9, when the signal core_reset_a becomes logic high it turns on a switch 21 and also makes a latch 23 receptive to receiving a signal. An amplifier 25 ensures that during the initialisation phase the signal received at the initialisation pin 9 does not pass into other portions of the interface device. When the signal core_reset_a becomes logic low (i.e. the communication phase begins), the switch 21 turns off, and the interface pin 9 becomes an output pin having an output gtx_o[9;7]. The latch 23 stores the value it received during the initialisation phase, and continues to outputs two corresponding signals core_is_ge_mode and gmode_sel[1;0] (where "[1;0]" means "[1]" for one of the initialisation pins and "[0]" for the other), which are used to select the protocol used in the communication phase. The output core_is_ge_mode is generated based on the multibit inputs from voltage sources 11.

The communication protocol thus selected is shown in Table 1.

Protocol selected	core_is_ge_mode	gmode_sel[1]	gmode_sel[0]
GMII	1	0	1
MII	1	0	0
RGMII	1	1	0
TBI	1	1	1
SMII	0	Don't care	Don't care

Table 1

Fig. 3 shows an example of the control circuit which determines the correspondence coupling between the inferface pins 7 (marked as PAD – the physical layer) and the network layer signal emitting /receiving interfaces MAC, GMAC of the equipment 3. The correspondence is controlled by a number of selectors 31 which are controlled by the signals output by the latch 23. Note that the precise design of the circuitry shown in Fig. 3 will be straightforward to an expert in the field, given a predetermined set of communication protocols which he wishes to enable. The correspondences between the interface pins and the internal interfaces MAC and GMAC for the GMII, SMII, TBI, and MII protocols are given in Appendix 1.

Although only a single embodiment of the invention has been described here, many variations are possible within the scope of the invention as will be clear to an expert.

Appendix 1

Dir.	Pin name	SMII/GMII/TBI/RGMII/MII interface
Dir.	Pin name	SMII interface
O	gfp_pad_tx_clk	smii_tx_clk=gfp_pad_tx_clk
O	gfp_pad_tx[9:0]	smii_tx_data[7:0]= gfp_pad_tx_code_group[7:0] smii_tx_sync= gfp_pad_tx_code_group[8]
I	pad_gfp_rx_clka	smii_rx_clk=pad_gfp_rx_clka
I	pad_gfp_rx_clkb	
I	pad_gfp_rx_code_group[9:0]	smii_rx_data[7:0]= pad_gfp_rx_code_group[7:0] smii_rx_sync=pad_gfp_rx_code_group[8]
I	pad_gfp_col	
I	pad_gfp_crs	

Dir.	Pin name	GMII interface
O	gfp_pad_tx_clk	gtx_clk= gfp_pad_tx_clk
O	gfp_pad_tx[9:0]	gtx_data[7:0]=gfp_pad_tx_code_group[7:0] gtx_en=gfp_pad_tx_code_group[8] gtx_er=gfp_pad_tx_code_group[9]
I	pad_gfp_rx_clka	
I	pad_gfp_rx_clkb	grx_clk=pad_gfp_rx_clkb
I	pad_gfp_rx_code_group[9:0]	grx_data[7:0]=pad_gfp_rx_code_group[7:0] grx_dv=pad_gfp_rx_code_group[8] grx_er=pad_gfp_rx_code_group[9]
I	pad_gfp_col	gmii_col= pad_gfp_col
I	pad_gfp_crs	gmii_crs= pad_gfp_crs

Dir	Pin name	TBI interface

Dir.	Pin name	SMII/GMII/TBI/RGMII/MII interface
O	gfp_pad_tx_clk	pma_tx_clk=gfp_pad_tx_clk
O	gfp_pad_tx[9:0]	pma_tx_code_group[9:0]= gfp_pad_tx_code_group[9:0]
I	pad_gfp_rx_clka	pma_rx_clka=pad_gfp_rx_clka
I	pad_gfp_rx_clkb	pma_rx_clkb=pad_gfp_rx_clkb
I	pad_gfp_rx_code_group[9:0]	pma_rx_code_group[9:0]=pad_gfp_rx_code_group[9:0]
I	pad_gfp_col	pma_signal_detect=pad_gfp_col
I	pad_gfp_crs	

Dir.	Pin name	RGMII interface
Dir.	**Pin name**	**RGMII interface**
O	gfp_pad_tx_clk	rgmii_tx_clk= gfp_pad_tx_clk
O	gfp_pad_tx[9:0]	rgmii_tx_data[3:0]=gfp_pad_tx_code_group[3:0] rgmii_tx_ctl= gfp_pad_tx_code_group[8]
I	pad_gfp_rx_clka	
I	pad_gfp_rx_clkb	rgmii_rx_clk=pad_gfp_rx_clkb
I	pad_gfp_rx_code_group[9:0]	rgmii_rx_data[3:0]=pad_gfp_rx_code_group[3:0] rgmii_rx_ctl=pad_gfp_rx_code_group[8]
I	pad_gfp_col	
I	pad_gfp_crs	

Dir.	**Pin name**	**MII interface**
O	gfp_pad_tx_clk	
O	gfp_pad_tx[9:0]	mii_tx_data[3:0]=gfp_pad_tx_code_group[3:0] mii_tx_en=gfp_pad_tx_code_group[8] mii_tx_er=gfp_pad_tx_code_group[9]
I	pad_gfp_rx_clka	mii_tx_clk= pad_gfp_rx_clka
I	pad_gfp_rx_clkb	mii_rx_clk=pad_gfp_rx_clkb
I	pad_gfp_rx_code_group[9:0]	mii_rx_data[3:0]= pad-gfp_rx_code_group[3:0] mii_rx_dv=pad_gfp_rx_code_group[8] mii_rx_er=pad_gfp_rx_code_group[9]
I	pad_gfp_col	mii_col=pad_gfp_col
I	pad_gfp_crs	mii_crs=pad_gfp_crs

Claims

1. An Ethernet communication interface comprising:

a set of interface pins; and

a control logic which, according to interface protocol selected from a predetermined set of interface protocols, assigns respective functions to the interface pins which are consistent with the selected protocol.

2. An interface device according to claim 1 including one or more initialisation pins which, during an initialisation phase, receive initialisation signals which indicate to the interface which of the protocols is selected, and a latch for storing the received initialisation signals, the outputs of the latch controlling the control logic.

3. An interface device according to claim 2 in which the initialisation pins are included in the set of interface pins.

4. An apparatus having an interface device according to claim 2 or claim 3 and means for determining the inputs to the initialisation pins during the initialisation phase.

5. A communication method comprising the steps of:

(i) during an initialisation phase supplying signals to an interface device having a plurality of interface pins, the signals indicating a selection of a desired one of a predetermined set of protocols, the interface device registering the selection; and

(ii) during a communication phase communicating using the interface device, the interface device operating using the selected protocol.

6. A method according to claim 5 in which the signals are input to the interface device using initialisation pins which are comprised in the set of interface pins and which during the communication phase are used for the communication.

7. A method according to claim 6 in which the initialisation pins are used as output pins during the communication.

FIG 1

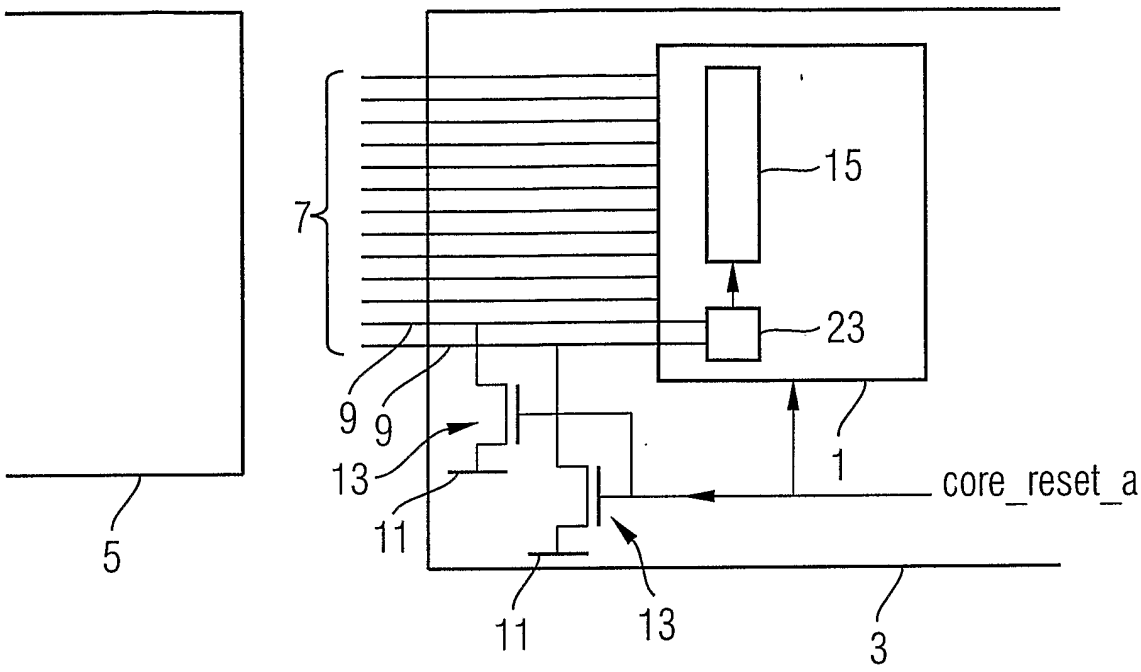

7
15
23
9
9
13
11
1
core_reset_a
5
11
13
3

FIG 2

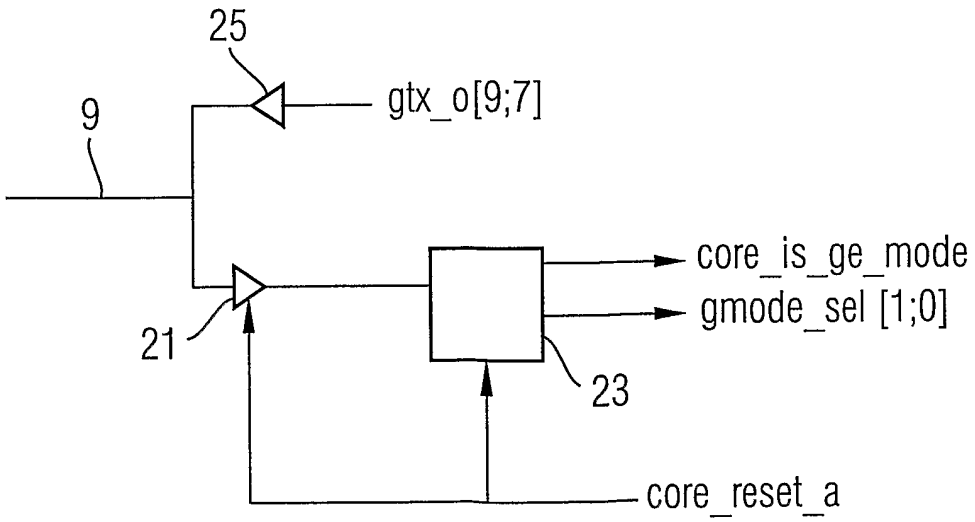
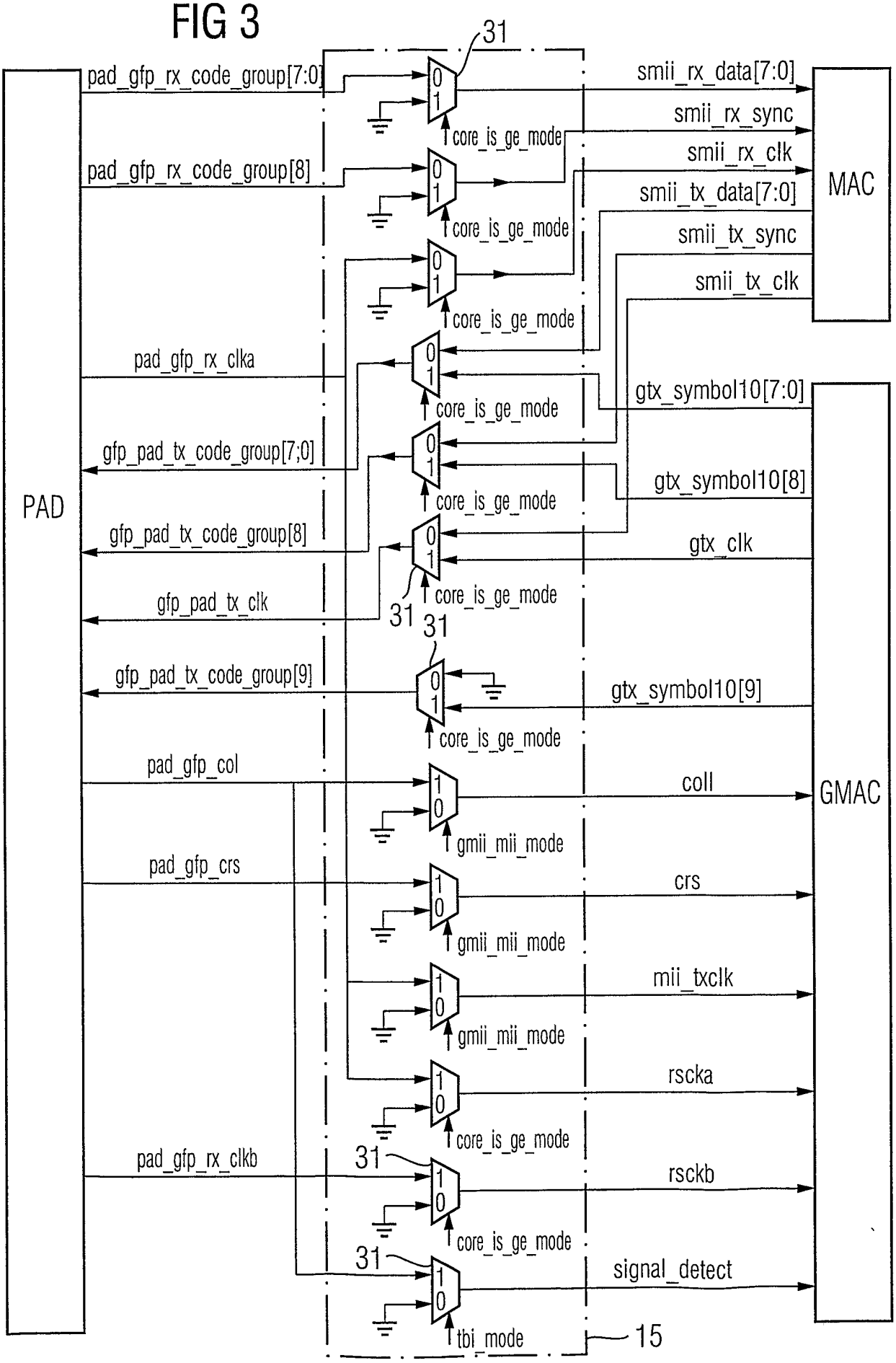

25
gtx_o[9;7]
9
core_is_ge_mode
gmode_sel [1;0]
21
23
core_reset_a

FIG 3


31
pad_gfp_rx_code_group[7:0]
smii_rx_data[7:0]
smii_rx_sync
smii_rx_clk
pad_gfp_rx_code_group[8]
smii_tx_data[7:0]
MAC
smii_tx_sync
smii_tx_clk
core_is_ge_mode
pad_gfp_rx_clka
gtx_symbol10[7:0]
gfp_pad_tx_code_group[7;0]
gtx_symbol10[8]
PAD
gfp_pad_tx_code_group[8]
gtx_clk
gfp_pad_tx_clk
31
gfp_pad_tx_code_group[9]
gtx_symbol10[9]
pad_gfp_col
coll
GMAC
gmii_mii_mode
pad_gfp_crs
crs
mii_txclk
rscka
core_is_ge_mode
pad_gfp_rx_clkb
rsckb
signal_detect
tbi_mode
15

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 02/00175

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L29/06 H01R13/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 577 435 A (DIGITAL EQUIPMENT CORP) 5 January 1994 (1994-01-05) page 3, line 2 -page 7, line 13	1-7
X	EP 0 915 599 A (BOSCH GMBH ROBERT) 12 May 1999 (1999-05-12) the whole document	1-7
A	US 5 305 317 A (SZCZEPANEK ANDRE) 19 April 1994 (1994-04-19) the whole document	1-7

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
25 April 2003	08/05/2003

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/SG 02/00175

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