(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 February 2021 (18.02.2021)

WIPO | PCT

(10) International Publication Number
WO 2021/029825 A1

(51) International Patent Classification:
G01M 3/40 (2006.01) *G01N 27/04* (2006.01)
G01N 27/22 (2006.01)

(21) International Application Number:
PCT/SG2020/050460

(22) International Filing Date:
06 August 2020 (06.08.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10201907526X 15 August 2019 (15.08.2019) SG

(71) Applicant: **NATIONAL UNIVERSITY OF SINGAPORE** [SG/SG]; 21 Lower Kent Ridge Road, Singapore 119077 (SG).

(72) Inventors: **PAN, Jieming**; c/o National University of Singapore, Faculty of Engineering, Department of Electrical and Computer Engineering, 21 Lower Kent Ridge Road, Singapore 119077 (SG). **SALILA VIJAYALAL MOHAN, Hari Krishna**; c/o National University of Singapore, Faculty of Engineering, Department of Electrical and Computer Engineering, 21 Lower Kent Ridge Road, Singapore 119077 (SG). **LI, Yida**; c/o National University of Singapore, Faculty of Engineering, Department of Electrical and Computer Engineering, 21 Lower Kent Ridge Road, Singapore 119077 (SG). **THAM, Chen Khong**; c/o National University of Singapore, Faculty of Engineering, Department of Electrical and Computer Engineering, 21 Lower Kent Ridge Road, Singapore 119077 (SG). **THEAN, Voon Yew Aaron**; c/o National University of Singapore, Faculty of Engineering, Department of Electrical and Computer En-

(54) Title: METHOD AND SYSTEM FOR INTEGRITY TESTING OF PACKAGES

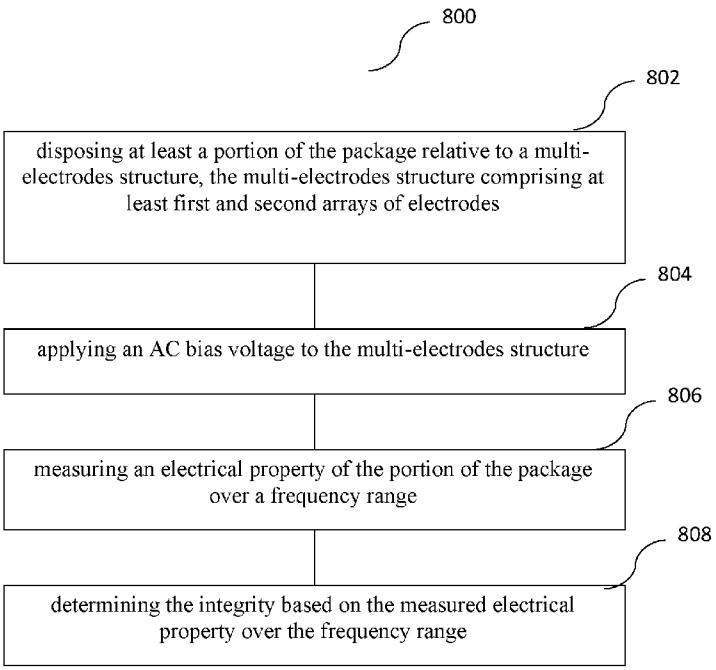

Figure 8

(57) Abstract: A method and system for integrity testing of packages. The method comprises the steps of disposing at least a portion of the package relative to a multi-electrodes structure, the multi-electrodes structure comprising at least first and second arrays of electrodes; applying an AC bias voltage to the multi-electrodes structure; measuring an electrical property of the portion of the package over a frequency range; and determining the integrity based on the measured electrical property over the frequency range; wherein disposing the portion of the package relative to a multi-electrodes structure comprises disposing the portion of the package between the first and second arrays of electrodes; and wherein measuring the electrical property of the portion of the package comprises using a plurality of electrodes of at least one of the first and second arrays of electrodes and at least one of the electrodes of the other one of the first and second arrays of electrodes, or at least three of the electrodes of one of the first and second arrays of electrodes; for

[Continued on next page]

WO 2021/029825 A1

gineering, 21 Lower Kent Ridge Road, Singapore 119077 (SG).

(74) **Agent: VIERING, JENTSCHURA & PARTNER LLP**; P.O. Box 1088, Rochor Post Office, Rochor Road, Singapore 911833 (SG).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *in black and white; the international application as filed contained color or greyscale and is available for download from PATENTSCOPE*

METHOD AND SYSTEM FOR INTEGRITY TESTING OF PACKAGES

FIELD OF INVENTION

The present invention relates broadly to a method and system for integrity testing of packages, in particular to the non-destructive inspection of the integrity of package sealing, quality of the package body and packaged content, e.g. for pharmaceutical, medical supplies, food & beverage packaging.

BACKGROUND

Any mention and/or discussion of prior art throughout the specification should not be considered, in any way, as an admission that this prior art is well known or forms part of common general knowledge in the field.

Safety, quality and quantity of produced drugs and medicine in pharmaceutical industries and food & beverage in consumables industries highly dependent on the efficiency and efficacy of packing as well as quality assurance. Any deviation from maintaining stringent quality standards in the products puts the consumers' life at risk. In particular, over-the-counter (OTC) drugs, medicines, various forms of food products and beverages, which are mass-produced and packaged at a very high speed, may suffer from defective packaging and accidental incorporation of impurities and unwanted substances. In addition, unintentional incorporation of impurities or/and product into the seal can lead to potential leak/breach before the stipulated expiry date.

Both pharmaceutical/medical equipment and food & beverage industries use various packaging which requires the sealing of ends. In a fully integrated fast production line, it is extremely challenging to check every package. Poor or tampered sealing increases the risk of exposure to external environmental factors such as microbes, gas, light and temperature, which could degrade product quality and prove fatal for consumers. Recognizing defects, leaks, and/or potential compromises in such packaging without compromising on the throughput is a challenge.

Popular approaches in pharmaceutical/medical equipment and food & beverage industries for package integrity testing include vacuum leak test, internal pressure method, water tank test, trace gas detection method and visual inspection. Most existing test methods for form filled packages require offline analysis, use of expensive equipment, have low throughput and high processing time, and generate large rejects and waste, which affects the production/packaging cost and time. In addition, these tests are limited to only identifying confirmed leaky or defective seals, whereas weak seal integrity, which can be compromised before reaching the customers, are overlooked.

Embodiments of the present invention seek to address at least one of the above problems.

SUMMARY

In accordance with a first aspect of the present invention, there is provided a method for integrity testing of packages, the method comprising the steps of disposing least a portion of the package relative to a multi-electrodes structure, the multi-electrodes structure comprising at least first and second arrays of electrodes; applying an AC bias voltage to the multi-electrodes structure; measuring an electrical property of the portion of the package is measured over a frequency range; and determining the integrity based on the measured electrical property over the frequency range; wherein disposing the portion of the package relative to a multi-electrodes structure comprises disposing the portion of the package between the first and second arrays of electrodes; and wherein measuring the electrical property of the portion of the package comprises using

- a plurality of electrodes of at least one of the first and second arrays of electrodes and at least one of the electrodes of the other one of the first and second arrays of electrodes, or

- at least three of the electrodes of one of the first and second arrays of electrodes;

for location resolved integrity testing of the package.

In accordance with a second aspect of the present invention, there is provided a system for integrity testing of packages, the system comprising a multi-electrodes structure configured to be disposed relative to least a portion of the package, the multi-electrodes structure comprising at least first and second arrays of electrodes; a source configured to apply an AC bias voltage to the multi-electrodes structure; a measurement unit configured to measure an electrical property of the portion of the package over a frequency range; and a processing unit configured to determine the integrity based on the measured electrical property over the frequency range; wherein multi-electrodes structure is configured to dispose the portion of the package between the first and second arrays of electrodes; and wherein the measurement unit is configured to use

- a plurality of electrodes of at least one of the first and second arrays of electrodes and at least one of the electrodes of the other one of the first and second arrays of electrodes, or

- at least three of the electrodes of one of the first and second arrays of electrodes;

for location resolved integrity testing of the package.

The electrical property may comprise one or more of a group consisting of capacitance, resistance, phase and impedance.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 A shows a schematic drawing of a good package with content.

Figure 1 B shows a schematic drawing of a defective seal package, i.e. tampered/partial seal and body.

Figure 1 C shows a schematic drawing of a defective package, i.e. defective package body and unwanted substance/impurities in package.

Figure 1 D shows a schematic drawing of a defective package, i.e. unwanted substance/impurities incorporated in seal.

Figure 2 A shows a schematic drawing of a perfectly sealed seal area without any defects/leaks/impurities.

Figure 2 B shows a schematic drawing of a tampered/partial seal damage, i.e. with hole/air gaps in seal area.

Figure 2 C shows a schematic drawing of a seal area incorporating impurities/unwanted substances.

Figure 2 D shows a schematic drawing of a cross section view of a whole package with impurities/unwanted substances in package 210 and damaged package body.

Figure 3 A shows a schematic drawing of a multi-electrodes structure comprising first (e.g. top) and second (e.g. bottom) arrays of electrodes connected to a multiplexer, a frequency response analyzer and a data acquisition system (DAQ), according to an example embodiment.

Figure 3 B shows a schematic drawing of a seal area with holes/leaks and impurities incorporated under test between the top and bottom electrode arrays of Figure 3 A.

Figure 3 C shows a schematic drawing of an entire package with holes/leaks and impurities (inside the package) present under test between the top and bottom electrode arrays of Figure 3A.

Figure 3 D shows a schematic drawing of the seal area with holes/leaks and impurities incorporated under test between the top and bottom electrode arrays of Figure 3 A with the top array of electrodes shown in flipped orientation on the right side.

Figure 4 A shows plots of Capacitance (F) vs frequency (Hz), for the different experiment cases using one set of electrodes on opposing sides, according to an example embodiment.

Figure 4 B shows a schematic side view of different possible scanning patterns using pairs of a plurality of electrodes of at least one of the first (e.g. top) and second (e.g. bottom) arrays of electrodes and at least one of the electrodes of the other one of the first and second arrays of electrodes, according to example embodiments, for location resolved integrity testing of the package.

Figure 4 C shows a schematic top view of different possible scanning patterns using pairs of at least three of the electrodes of one of the first and second arrays of electrodes, according to example embodiments, for location resolved integrity testing of the package.

Figure 5 A shows plots of Capacitance (F) vs respective pairs of electrodes at different locations of a package, according to example embodiments.

Figure 5 B is a schematic drawing illustrating the locations of the electrodes for the measurements in Figure 5 A.

Figure 5 C shows a photograph of the package with an illustration of one of the arrays of electrodes for the measurements in Figure 5 A.

Figure 6 shows some examples of electrode distributions according to different example embodiments.

Figure 7 shows schematic diagrams of different electrode configuration which may be used according to various embodiments.

Figure 8 shows a flow chart illustrating a method for integrity testing of packages, according to an example embodiment.

Figure 9 shows a schematic diagram illustrating a system for integrity testing of packages, according to an example embodiment.

DETAILED DESCRIPTION

Embodiments of the present invention provide a non-destructive system and method for location resolved integrity testing of a package for identifying compromised and potentially compromised units in package seals, which can advantageously be integrated fully with the production line. Hence, embodiments of the present invention preferably allow for cheap and fast online analysis for every package output to reduce wastage without affecting the yield.

The detection scheme employed according to example embodiments uses an array of electrodes on opposing sides of the package seal, preferably covering the entire seal/package for location resolved integrity testing of the seal/package. The captured electrical impedance profile is used to identify leaks/defects and potential compromises of the seal/package area. Such a multi-electrode detection setup is connected to a multiplexer and then a frequency response analyzer, which generates an excitation signal creating an electric field of varying

frequencies as the input to the system, according to an example embodiment. The output response is analyzed in the form of an electrical quantity, for example, capacitance and/or inductance. The presence of a defect, for example, torn seal, leads to air gap/lack of packaging material, which generates a distinctive capacitance reading when compared to a well-sealed package. Similarly, incorporation of unwanted impurities in the seal region will cause variation in either or both of the time and frequency domain of the capacitive impedance measured, hence indicating potential seal compromise. With differing layout, arrangement and scanning pattern of the sensor array according to various embodiments, this approach gathers spatial distribution of unwanted impurities for location resolved integrity testing of the package, which can be used for further seal integrity analysis. For example, any deviation from the expected overall capacitance between any scanning patterns in the array will alert the packaging line and divert the defective samples for replacement or re-sealing according to an example embodiment. By altering the size and shape of the electrodes in various embodiments, this technique can be used to analyse packages, their seals and contents of various shape, size and materials.

Preferably, a conventional multiplexer data acquisition system can be used for fast data sampling according to an example embodiment.

Preferably, sensor arrays are designed with different dimension to have the appropriate number of electrode pairs for sufficient electrical profiling resolution, according to example embodiments.

Preferably, an electrical profile image is generated for noise invariant and more accurate artificial intelligence integration, according to an example embodiment.

Preferably, a material capacitance signature database is collected according to an example embodiment.

As mentioned in the background section, package sealing at high speed could suffer from defects such as incomplete seal, tampered seal, seal that incorporates defects, and accidentally sealing impurities and unwanted substances. As such, quality and quantity packing is greatly compromised and hence the need for quality assurance. Any deviation from maintaining stringent quality standards in the products of pharmaceutical and medical supply and food and beverage industries puts the consumers' life at risk. Both pharmaceutical/medical equipment, and food & beverage industries use various packaging approaches that requires the sealing of ends. In a fully integrated fast production line, it is extremely challenging to check on every package. Poor or tampered sealing increases the risk of exposure to external environmental factors such as microbes, gas, light and temperature, which could degrade product quality and prove fatal for the consumers. Recognizing defects/leaks/potential compromises in such packaging without compromising on the throughput is a challenge.

Figure 1 shows a schematic representation of a package seal without and with possible example defects. A) Good package 100 with content 102 in there. B) Defective seal package

104, i.e. tampered/partial seal e.g. 106 and body 108. C) Defective package 110, i.e. defective package body 112 and unwanted substance/impurities e.g. 114 in package 110. D) Defective package 116, i.e. unwanted substance/impurities e.g. 117 incorporated in seal e.g. 118.

Figure 2 shows schematic cross section views of package area and seal area without and with possible example defects. A) Perfectly sealed seal area 200 without any defects/leaks/impurities. B) Tampered/partial seal 202 damage, i.e. with hole/air gaps e.g. 204 in seal 202 area. C) Incorporating impurities/unwanted substances e.g. 206 in seal area 208. D) Cross section view of whole package 210 with impurities/unwanted substances e.g. 212 in package 210 and damaged package body 214.

Existing approaches in pharmaceutical/medical equipment and food & beverage industries for package integrity testing include vacuum leak test, internal pressure method, water tank test, trace gas detection method and visual inspection. The majority of such methods require offline analysis, the use of expensive equipment, have low throughput and high processing time, and generate large rejects and waste, which affects the production/packaging cost and time. In addition, these tests are limited to only identifying a confirmed leaky or defective seal, whereas weak seal integrity which can be compromised before reaching the customers are overlooked.

A system focusing on exploring an electrical quantity, which differs with and without proper sealing is provided according to example embodiments for location resolved integrity testing of the seal/package. In accordance with example embodiments, an external entity perturbs the electric field and hence changes the measured complex impedance. An array of electrodes are placed on opposing sides of the package/package seal covering the entire area under test as shown in Figure 3.

Figure 3 shows schematic representations of electrode array and testing scenarios according to example embodiments. Figure 3 A shows a Multi-electrodes structure 300 comprising first (e.g. top) and second (e.g. bottom) arrays 301a, b of electrodes connected to a multiplexer 302, a frequency response analyzer 304 and a data acquisition system (DAQ) 306. Figures 3 B shows a seal area 308 with holes/leaks 310 and impurities 312 incorporated under test between the top and bottom electrode arrays 301 a, b. Figure 3 C shows an entire package 314 with holes/leaks 316 and impurities 318 (inside the package) present under test between the top and bottom electrode arrays 301 a, b. In the embodiment shown in Figure 3, the arrays 301a, b have the same lay-out (top array 301a shown in flipped orientation on the right side of Figure 3 D for comparison with array 301b shown in Figure 3A. However, the first and second arrays may have different respective lay-outs in different embodiments. Also, the specific lay-out shown in Figure 3 is by way of example only, not limitation.

The multi-electrodes structure 300 is connected to the multiplexer 302 and then the frequency response analyzer 304, which generates an excitation signal creating an electric field of varying frequencies as the input to the multiplexer 302/electrode array 300 system. The output response is analyzed in the form of an electrical quantity, for example, capacitance. A torn seal leads to air gap/lack of packaging material (compare 310) which alters the

capacitance reading captured. Similarly, incorporation of unwanted impurities in the seal region (compare 312) will also cause variations in either or both of the time and frequency domain of the capacitance measured. By varying the pairs of excited electrodes, the presence of a defect or leak can be identified at its location. With differing layout, arrangement and scanning pattern of the sensor array according to various embodiments, this approach gathers spatial distribution of unwanted impurities/defects which can be used for further seal integrity analysis. For example, any deviation from the expected overall capacitance between any scanning patterns in the array will alert the packaging line and divert the defective samples away from the main production line. In addition, by altering the size and shape of the electrodes, changing the arrangement of array and/or signal enhancement using software techniques, embodiments of the present invention can be used to analyses the entire package beyond just the seal area with high precision and accuracy with potentially predictive capability.

Monitoring, for example, the capacitance change can advantageously enable classification of good and defective samples in real-time with high throughput to match the sealing/packaging process throughput, according to example embodiments. Furthermore, capacitance fingerprints can be created to quantify the defect based on the extent of the damage, according to an example embodiment.

Experimental setup according to an example embodiment

Conductive material is used for the construction of metal electrodes of the arrays 301a, b. The array 301a, b of plate electrodes e.g. 320 is placed out uniformly on respective base substrates 322a, 322b that are designed to cover the testing area, as shown for example in Figure 3B. Different package 314 materials are used in an example test as will be described in more detail below, and sealing is completed using heat. The testing was done over a frequency (f) range from 100 Hz to 1 MHz at an AC bias voltage of 1 V to get impedance, capacitance and Phase using a E4980AL LCR meter.

The experiments were done using the multi-electrodes structure 300 for the following cases listed below (see Figure 4):

I. Baseline – to obtain the electrical signature without any package under test

II. Plastic_Ref - well sealed plastic package is under test

III. AR_Ref - well sealed aluminium package is under test

IV. MR_Ref - well sealed metallic package is under test

For each of cases II-IV, different amounts of impurities/liquid were incorporated in the seal area as follows:

_10mg - 10mg of impurities/liquid is incorporated in seal area

_20mg - 20mg of impurities/liquid is incorporated in seal area

_20mg - 20mg of impurities/liquid is incorporated in seal area

Figure 4 A shows plots of Capacitance (F) vs frequency (Hz), for the different experiment cases mentioned above using one set of electrodes on opposing sides. In the experiments, there are a total of 14 electrode pads in top array and 14 electrode pads in the bottom array, according to an example embodiment. Each capacitance vs frequency line plot in Figure 4A is the measurement between one of the top to one of the bottom electrode pads, perpendicular to each other, when different materials are between them. The bias voltage is applied only on the targeted pair of electrode pads, and the rest of the electrode pads are grounded. Capacitance measurement of other combinations of electrode pairs can be collected sequentially for location resolved measurements according to example embodiments. It is noted that the pair of electrode pads can include electrodes only from the top array or only from the bottom array.

Figures 4 B and C show schematic side and top views of different possible scanning patterns using a plurality of electrodes of at least one e.g. 400a of the first (e.g. top) and second (e.g. bottom) arrays 400a, b of electrodes and at least one of the electrodes of the other one e.g. 400b of the first and second arrays 400a, b of electrodes, for example respective measurements of electrode pairs (401-402), (401-403), (401-404), (401-405), and (401-406), for location resolved integrity testing of the package, by way of example, not limitation. Also shown are possible scanning patterns using at least three of the electrodes of one e.g. 400a of the first and second arrays400a, b of electrodes, for example respective measurements of electrode pairs (407-401), (407-408), (407-409), and (407, 409), for location resolved integrity testing of the package, by way of example, not limitation. It is noted that instead of sequential measurements, one-to-many electrodes measurements may be performed simultaneously in different embodiments.

As can be seen in Figure 4 A, the frequency response scans for capacitance are readily distinguishable between the different materials and different amount of defects incorporated using the multi-electrodes structure 300, i.e. a single pair of electrodes of the arrays 301a, b of electrodes. In general, as the dielectric material in the region increases, the capacitance captured increases as well. Discrepancies from this trend are due to variation in test seal area and in proper sealing, which can be identified with increasing the number of tests and data collected. As such, the presence of seal, material of seal, quality of seal can advantageously be identified and classified. In addition, using different scanning patterns of the electrode pairs of the arrays of electrodes, an electrical signature of the package/package seal can be recorded as shown in Figure 5.

Figure 5 A shows plots of Capacitance (F) vs respective pairs of electrodes at different locations, as illustrated in the image in Figure 5 B. Testing using a good plastic package and plastic package with different amounts of impurities/liquid incorporated, as well as a baseline (Air) are shown.

In Figure 5 A, major change in capacitance occurs in regions of 3c, 4d, 10j and 11k when a package is introduced, where the number e.g. 3c refers to the pair of top and bottom electrodes at the location as illustrated in Figure 5 B. This is because the folding 500 of the sealed package 502 is located at that area, as can be seen in Figure 5 C. In addition, the overall capacitance increases as more impurities/liquid are incorporated in the package.

As described above, embodiments of the present invention can provide an electrical quantity measuring system using a multi-electrodes structure with first (e.g. top) and second (e.g. bottom) arrays of electrodes which allows for classification of package material, package profile, and various defect conditions. The above described experiment and data collected shows the effectiveness of such systems according to example embodiments. Development of an electrical signature database can preferably allow for machine learning implementation which enhances the sensing capability of such systems according to example embodiments.

Modifications according to different example embodiments

The use of above described multi-electrodes structure allows defect identification on both the package seal and package itself. It does not require contact with the package and it is non-destructive. To fit different package type and testing requirements, the multi-electrodes structures can be arranged in various lay-outs/distributions to ensure high accuracy, sensitivity and precision of detection. Furthermore, collected data from various scanning patterns, e.g. between opposing side (e.g. top and bottom) electrode arrays can be used to create a model of the package/package seal profile which helps with implementing machine learning and other classification algorithms. Figure 6 shows some examples of electrode distributions according to different example embodiments, by way of example, not limitation.

Similarly, the electrode design in each array can help to focus the electric field differently in different example embodiments and hence can be used for different sensing situations. For example, Figure 7 shows a range of designs ranging from simple single plate to complex circular interdigitated design which produces a highly concentrated electric field which will drastically increase the sensitivity of the detection, by way of example, not limitation. Different structures such as pyramidal, and saw tooth textured electrodes can be used to identify specific defects in hard to reach areas or uncommon package shape and designs.

Specifically, Figure 7 shows schematic diagrams of: plate electrode, interdigitated ring electrodes, different meandering electrodes, circular interdigitated, different pyramids-textured electrodes, saw tooth-textured electrodes, and pores-type electrodes which may be used according to various embodiments.

Figure 8 shows a flow chart 800 illustrating a method for integrity testing of packages, according to an example embodiment. At step 802, at least a portion of the package is disposed relative to a multi-electrodes structure, the multi-electrodes structure comprising at least first and second arrays of electrodes. At step 804, an AC bias voltage is applied to the

multi-electrodes structure. At step 806, an electrical property of the portion of the package over a frequency range is measured. At step 808, the integrity is determined based on the measured electrical property over the frequency range, wherein disposing the portion of the package relative to a multi-electrodes structure comprises disposing the portion of the package between the first and second arrays of electrodes; and wherein measuring the electrical property of the portion of the package comprises using

- a plurality of electrodes of at least one of the first and second arrays of electrodes and at least one of the electrodes of the other one of the first and second arrays of electrodes, or

- at least three of the electrodes of one of the first and second arrays of electrodes;

for location resolved integrity testing of the package.

The electrical property may comprise one or more of a group consisting of capacitance, resistance, phase and impedance.

The portion of the package may comprise a seal portion and the integrity is determined based on identifying trapped particles or holes in the seal portion based on the measured electrical property of the seal portion over the frequency range.

The portion of the package may comprise a body portion and the integrity is determined based on identifying trapped particles or holes in the body portion based on the measured electrical property of the body portion over the frequency range.

The multi-electrodes structure may be operated within a frequency range of about 100 Hz to 1 MHz.

Determining the integrity may comprise applying a machine learning approach.

Applying the AC bias voltage to the multi-electrodes structure may comprise multiplexing an excitation signal for creating an electric field of varying frequencies and applying the excitation signal to pairs of the plurality of electrodes of the at least one of the arrays of electrodes and the at least one of the electrodes of the other one of the first and second arrays of electrodes, or to pairs of the at least three of the electrodes of one of the first and second arrays of electrodes. The AC bias voltage may be applied to the pairs of electrodes sequentially or in a one-to-many measurement configuration.

Measuring the electrical property may comprise measuring the electrical property, during scanning of the excitation signal, across the respective pairs of the plurality of electrodes of the at least one of the arrays of electrodes and the at least one of the electrodes of the other one of the first and second arrays of electrodes, or across the respective pairs of the at least three of the electrodes of one of the first and second arrays of electrodes.

Remaining electrodes of the first and second arrays that are not amongst a target pair of electrodes for measurement may be grounded during applying the measuring of the electrical property.

A number and/or distribution of the electrodes in the first and/or second arrays of electrodes may be chosen to achieve a desired testing area and/or profile.

Figure 9 shows a schematic diagram illustrating a system 900 for integrity testing of packages, according to an example embodiment. The system comprises a multi-electrodes structure 902 configured to be disposed relative to least a portion of the package 904, the multi-electrodes structure 902 comprising at least first and second arrays 906, 908 of electrodes; a source 910 configured to apply an AC bias voltage to the multi-electrodes structure 902; a measurement unit 912 configured to measure an electrical property of the portion of the package 904 over a frequency range; and a processing unit 914 configured to determine the integrity based on the measured electrical property over the frequency range; wherein multi-electrodes structure 902 is configured to dispose the portion of the package 904 between the first and second arrays 906, 908 of electrodes; and wherein the measurement unit 912 is configured to use

- a plurality of electrodes of at least one of the first and second arrays 906, 908 of electrodes and at least one of the electrodes of the other one of the first and second arrays 906, 908 of electrodes, or

- at least three of the electrodes of one of the first and second arrays 906, 908of electrodes;

for location resolved integrity testing of the package.

The electrical property may comprise one or more of a group consisting of capacitance, resistance, phase and impedance.

The portion of the package 904 may comprise a seal portion and the integrity is determined based on identifying trapped particles or holes in the seal portion based on the measured electrical property of the seal portion over the frequency range.

The portion of the package 904 may comprise a body portion and the integrity may be determined based on identifying trapped particles or holes in the body portion based on the measured electrical property of the body portion over the frequency range.

The source 910 and the multi-electrodes structure 902 may be configured to be operated within a frequency range of about 100 Hz to 1 MHz.

The processing unit 914 may be configured to apply a machine learning approach for determining the integrity.

The system may comprises a multiplexing unit 916 configured to multiplex an excitation signal for creating an electric field of varying frequencies from the source 910 for applying

the excitation signal to pairs of the plurality of electrodes of the at least one of the arrays 906, 908 of electrodes and the at least one of the electrodes of the other one of the first and second arrays 906, 908 of electrodes, or to pairs of the at least three of the electrodes of one of the first and second arrays 906, 908 of electrodes. The multiplexing unit 916 may be configured to apply the AC bias voltage to the pairs of electrodes sequentially or in a one-to-many measurement configuration.

The measurement unit 912 may be configured for measuring the electrical property, during scanning of the excitation signal, across the respective pairs of the plurality of electrodes of the at least one of the arrays 906, 908 of electrodes and the at least one of the electrodes of the other one of the first and second arrays 906, 908 of electrodes, or across the respective pairs of the at least three of the electrodes of one of the first and second arrays 906, 908 of electrodes.

The system 900 may be configured such that remaining electrodes of the first and second arrays that are not amongst a target pair of electrodes for measurement are grounded during the measuring of the electrical property.

A number and/or distribution of the electrodes in the first and/or second arrays 906, 908 of electrodes is chosen to achieve a desired testing area and/or profile.

As described above, methods and systems according to example embodiments can identify the type of defects (no seal, seal torn, no product, contaminated etc.), defect location and quantify defects (size of holes/gaps, amount of product, etc.) by comparing against control standards (well-sealed packages). As mentioned above, such a method and system according to example embodiments can generate large dataset due to multipoint scanning/multiple electrodes possibilities. These electrical fingerprints can serve as input patterns for machine learning systems to quantitatively and qualitatively identify and classify defects, according to example embodiments.

Embodiments of the present invention can have one or more of the following features and associated benefits/advantages:

Feature	Benefit/Advantage
Identify potential leak/breach through area profiling	Existing methods are limited to identify a confirmed leaky or defective seal, weak seal integrity which can be compromised before reaching the customers are overlooked. By varying the fineness/layout/structure of the sensor array, example embodiments are able to capture seal profile which enable seal integrity checking to even identify potential leaks/breaches.
Ability to integrate with modeling algorithm and machine learning to enhance	By exciting different pairs of electrodes according to example embodiments, a comprehensive dataset of

seal checking capability	impedance distribution between various scanning patterns are collected. This dataset is advantageous for accurate modeling of the seal profile which allows machine learning algorithm to identify any potential leak/breach/defects.
High throughput for rapid in-line inspection	Capacitance/impedance/phase based screening is highly sensitive to leaks and can screen defects instantly. Example embodiments can provide a real-time package integrity inspection that allows processing/packaging issues to be resolved in production/packaging line at the speed of the machine throughput.
Nondestructive and low cost	Example embodiments use a non-destructive approach with low cost and simple portable circuitry and allows re-packaging of defective units without generating wastage unlike the large reject packets from current leak test methods.
Electrical mode of inspection	Example embodiments can provide instantaneous results and eliminate the need for off-line sampling, which minimizes waste (time, work-backs, materials and labor) compared to the existing methods requiring complex analysis, labor and off-line sampling.

Industrial applications of embodiments of the present invention include, but are not limited to, during pharmaceutical drug manufacturers, medical equipment suppliers and food & beverage manufacturers seal packages production at high speed. During this process, there is a high probability for improper sealing, lack of product filling, torn seal, accidental incorporation of impurities and other particles in seal etc., which leads to poor sample quality and hygiene issues.

Existing methods for leak/breach/particle incorporation testing for such packages are highly dependent on the material and the nature of the product. The majority of the existing methods suffer from low throughput, are destructive to both package and product and are unable to detect if impurities are incorporated into the seal which may lead to potential leak/breach. Due to low throughput and slow test time, manufacturers have to adopt random sampling test process which is limiting and generates huge financial loss in terms of package reject and waste disposal when a defective product is found.

The electrical screening approach according to example embodiments of the present invention can preferably solve the above issues:

- detect tampered/poor seals for different type/quantity of product as well as cavity/seal material.

- identify unwanted particles or/and materials incorporated in the seal itself which introduces potential leaks/breaches.

- identify and locate defective seals at a rapid rate in-line, thereby increasing the throughput during packaging and reducing wastage.

- recognize poorly sealed contents non-destructively, thus allowing re-packaging and no product wastage.

Aspects of the systems and methods described herein, such as devices and methods for the application of the bias signal, devices and methods for measurement of the electrical property, and devices and method for machine learning processing may be implemented as functionality programmed into any of a variety of circuitry, including programmable logic devices (PLDs), such as field programmable gate arrays (FPGAs), programmable array logic (PAL) devices, electrically programmable logic and memory devices and standard cell-based devices, as well as application specific integrated circuits (ASICs). Some other possibilities for implementing aspects of the system include: microcontrollers with memory (such as electronically erasable programmable read only memory (EEPROM)), embedded microprocessors, firmware, software, etc. Furthermore, aspects of the system may be embodied in microprocessors having software-based circuit emulation, discrete logic (sequential and combinatorial), custom devices, fuzzy (neural) logic, quantum devices, and hybrids of any of the above device types. Of course the underlying device technologies may be provided in a variety of component types, e.g., metal-oxide semiconductor field-effect transistor (MOSFET) technologies like complementary metal-oxide semiconductor (CMOS), bipolar technologies like emitter-coupled logic (ECL), polymer technologies (e.g., silicon-conjugated polymer and metal-conjugated polymer-metal structures), mixed analog and digital, etc.

The above description of illustrated embodiments of the systems and methods is not intended to be exhaustive or to limit the systems and methods to the precise forms disclosed. While specific embodiments of, and examples for, the systems components and methods are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the systems, components and methods, as those skilled in the relevant art will recognize. The teachings of the systems and methods provided herein can be applied to other processing systems and methods, not only for the systems and methods described above.

The elements and acts of the various embodiments described above can be combined to provide further embodiments. These and other changes can be made to the systems and methods in light of the above detailed description.

In general, in the following claims, the terms used should not be construed to limit the systems and methods to the specific embodiments disclosed in the specification and the claims, but should be construed to include all processing systems that operate under the claims. Accordingly, the systems and methods are not limited by the disclosure, but instead the scope of the systems and methods is to be determined entirely by the claims.

Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in a sense of "including, but not limited to." Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words "herein," "hereunder," "above," "below," and words of similar import refer to this application as a whole and not to any particular portions of this application. When the word "or" is used in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

CLAIMS

1. A method for integrity testing of packages, the method comprising the steps of:

disposing at least a portion of the package relative to a multi-electrodes structure, the multi-electrodes structure comprising at least first and second arrays of electrodes;

applying an AC bias voltage to the multi-electrodes structure;

measuring an electrical property of the portion of the package over a frequency range; and

determining the integrity based on the measured electrical property over the frequency range;

wherein disposing the portion of the package relative to a multi-electrodes structure comprises disposing the portion of the package between the first and second arrays of electrodes; and

wherein measuring the electrical property of the portion of the package comprises using

- a plurality of electrodes of at least one of the first and second arrays of electrodes and at least one of the electrodes of the other one of the first and second arrays of electrodes, or

- at least three of the electrodes of one of the first and second arrays of electrodes;

for location resolved integrity testing of the package.

2. The method of claim 1, wherein the electrical property comprises one or more of a group consisting of capacitance, resistance, phase and impedance.

3. The method of claims 1 or 2, wherein the portion of the package comprises a seal portion and the integrity is determined based on identifying trapped particles or holes in the seal portion based on the measured electrical property of the seal portion over the frequency range.

4. The method of any one of the preceding claims, wherein the portion of the package comprises a body portion and the integrity is determined based on identifying trapped particles or holes in the body portion based on the measured electrical property of the body portion over the frequency range.

5. The method of any one of the preceding claims, wherein the multi-electrodes structure is operated within a frequency range of about 100 Hz to 1 MHz.

6. The method of any one of the preceding claims, wherein determining the integrity comprises applying a machine learning approach.

7. The method of any one of the preceding claims, wherein applying the AC bias voltage to the multi-electrodes structure comprises multiplexing an excitation signal for creating an electric field of varying frequencies and applying the excitation signal to pairs of the plurality

of electrodes of the at least one of the arrays of electrodes and the at least one of the electrodes of the other one of the first and second arrays of electrodes, or to pairs of the at least three of the electrodes of one of the first and second arrays of electrodes.

8. The method of claim 7, wherein the AC bias voltage is applied to the pairs of electrodes sequentially or in a one-to-many measurement configuration.

9. The method of claims 7 or 8, wherein measuring the electrical property comprises measuring the electrical property, during scanning of the excitation signal, across the respective pairs of the plurality of electrodes of the at least one of the arrays of electrodes and the at least one of the electrodes of the other one of the first and second arrays of electrodes, or across the respective pairs of the at least three of the electrodes of one of the first and second arrays of electrodes.

10. The method of claims 7 or 8, wherein remaining electrodes of the first and second arrays that are not amongst a target pair of electrodes for measurement are grounded during applying the measuring of the electrical property.

11. The method of any one of the preceding claims, wherein a number and/or distribution of the electrodes in the first and/or second arrays of electrodes is chosen to achieve a desired testing area and/or profile.

12. A system for integrity testing of packages, the system comprising:

a multi-electrodes structure configured to be disposed relative to least a portion of the package, the multi-electrodes structure comprising at least first and second arrays of electrodes;

a source configured to apply an AC bias voltage to the multi-electrodes structure;

a measurement unit configured to measure an electrical property of the portion of the package over a frequency range; and

a processing unit configured to determine the integrity based on the measured electrical property over the frequency range;

wherein multi-electrodes structure is configured to dispose the portion of the package between the first and second arrays of electrodes; and

wherein the measurement unit is configured to use

- a plurality of electrodes of at least one of the first and second arrays of electrodes and at least one of the electrodes of the other one of the first and second arrays of electrodes, or

- at least three of the electrodes of one of the first and second arrays of electrodes;

for location resolved integrity testing of the package.

13. The system of claim 12, wherein the electrical property comprises one or more of a group consisting of capacitance, resistance, phase and impedance.

14. The system of claims 12 or 13, wherein the portion of the package comprises a seal portion and the integrity is determined based on identifying trapped particles or holes in the seal portion based on the measured electrical property of the seal portion over the frequency range.

15. The system of any one of claims 12 to 14, wherein the portion of the package comprises a body portion and the integrity may be determined based on identifying trapped particles or holes in the body portion based on the measured electrical property of the body portion over the frequency range.

16. The system of any one of claims 12 to 15, wherein the source and the multi-electrodes structure are configured to be operated within a frequency range of about 100 Hz to 1 MHz.

17. The system of any one of claims 12 to 16, wherein the processing unit is configured to apply a machine learning approach for determining the integrity.

18. The system of any one of claims 12 to 17, wherein the system comprises a multiplexing unit configured to multiplex an excitation signal for creating an electric field of varying frequencies from the source for applying the excitation signal to pairs of the plurality of electrodes of the at least one of the arrays of electrodes and the at least one of the electrodes of the other one of the first and second arrays of electrodes, or to pairs of the at least three of the electrodes of one of the first and second arrays of electrodes.

19. The system of claim 18, wherein the multiplexing unit is configured to apply the AC bias voltage to the pairs of electrodes sequentially or in a one-to-many measurement configuration.

20. The system of claims 18 or 19, wherein the measurement unit is configured for measuring the electrical property, during scanning of the excitation signal, across the respective pairs of the plurality of electrodes of the at least one of the arrays of electrodes and the at least one of the electrodes of the other one of the first and second arrays of electrodes, or across the respective pairs of the at least three of the electrodes of one of the first and second arrays of electrodes.

21. The system of any one of claims 18 to 20, wherein the system is configured such that remaining electrodes of the first and second arrays that are not amongst a target pair of electrodes for measurement are grounded during the measuring of the electrical property.

22. The system of any one of the preceding claims, wherein a number and/or distribution of the electrodes in the first and/or second arrays of electrodes is chosen to achieve a desired testing area and/or profile.

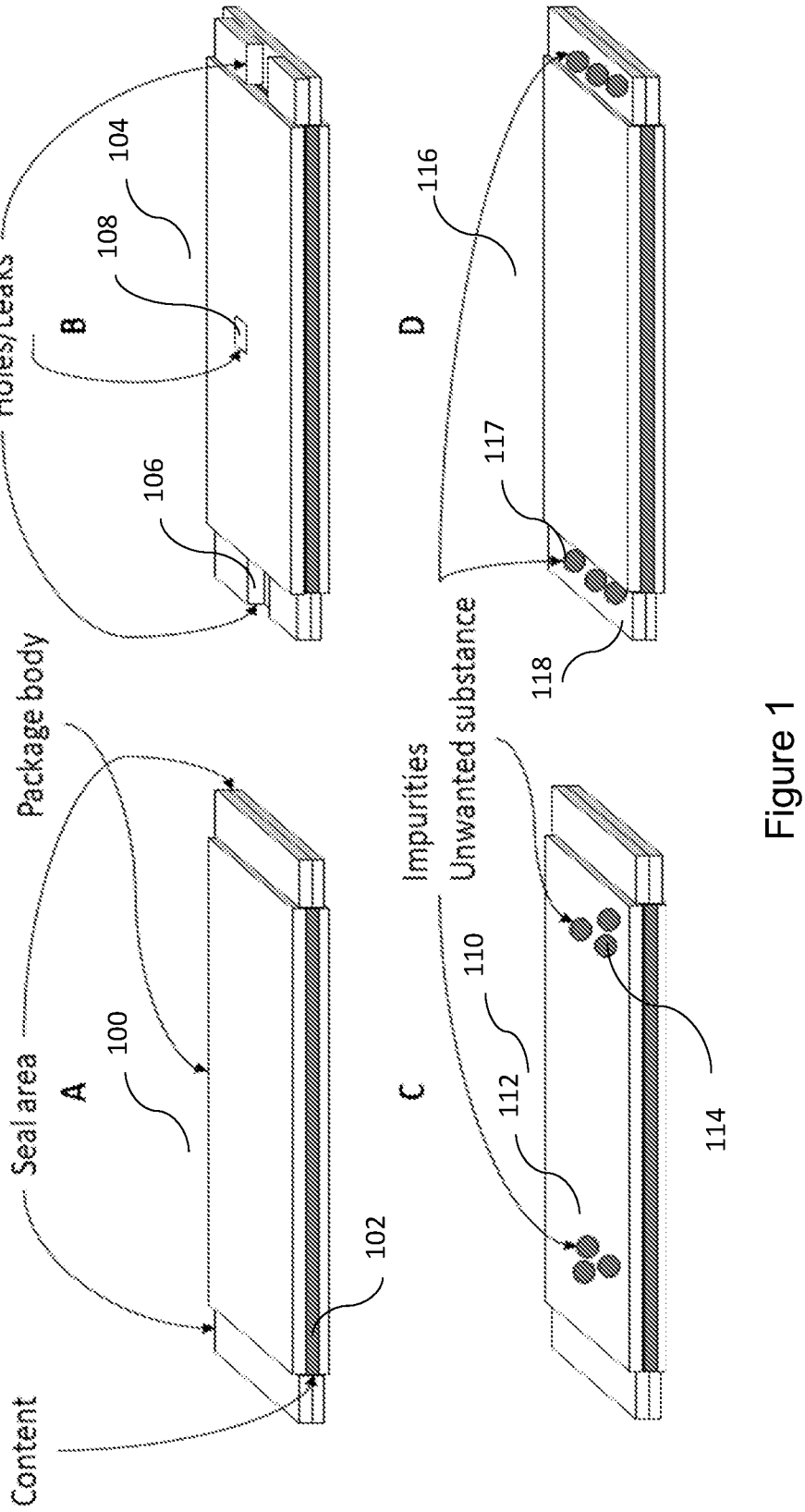
Holes/Leaks
B
104
108
106
Package body
Seal area
A
100
Content
102
D
116
117
118
Impurities
Unwanted substance
C
110
112
114

Figure 1

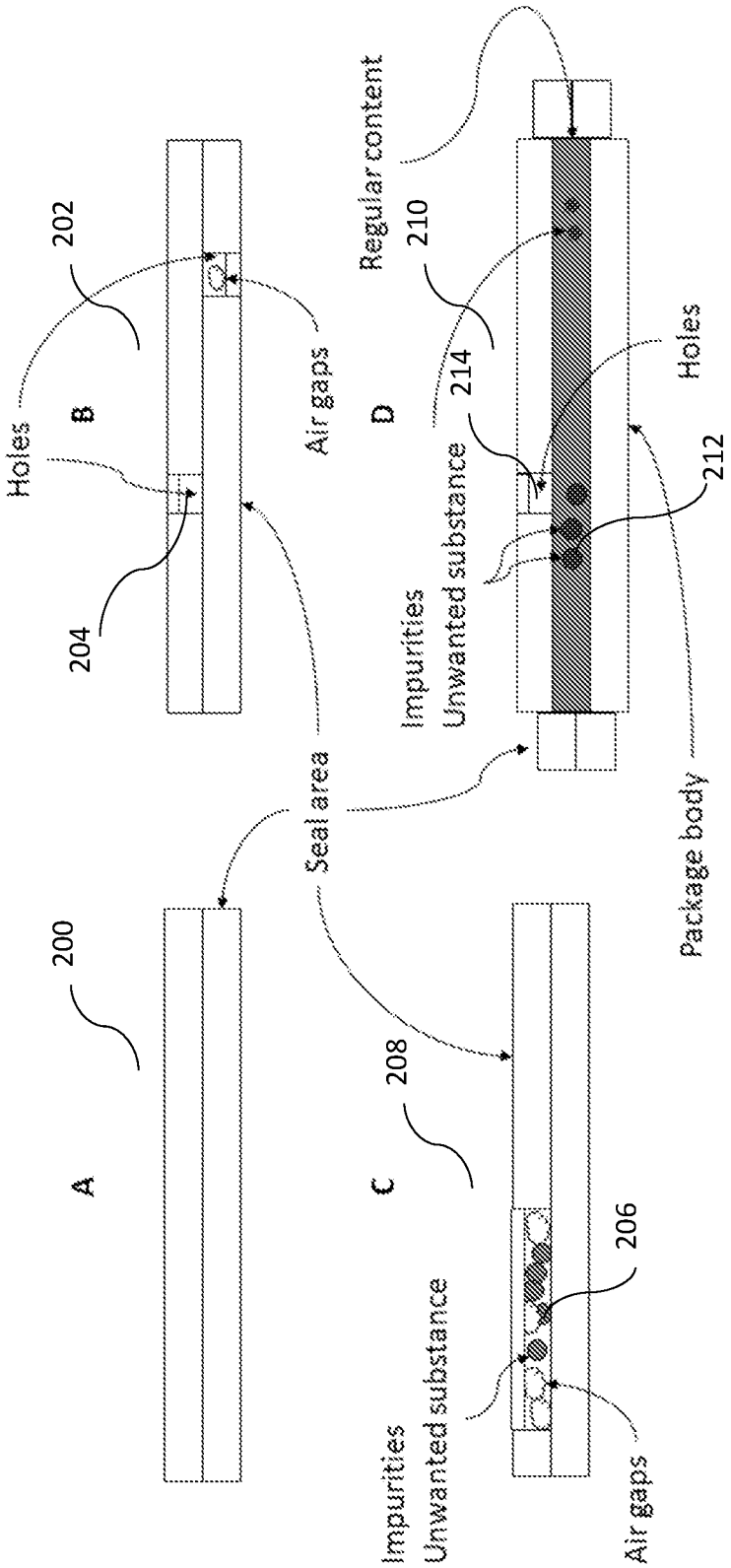
A
200
B
202
Holes
204
Air gaps
C
208
Impurities
Unwanted substance
206
Air gaps
D
Regular content
210
Holes
214
Impurities
Unwanted substance
212
Package body
Seal area

Figure 2

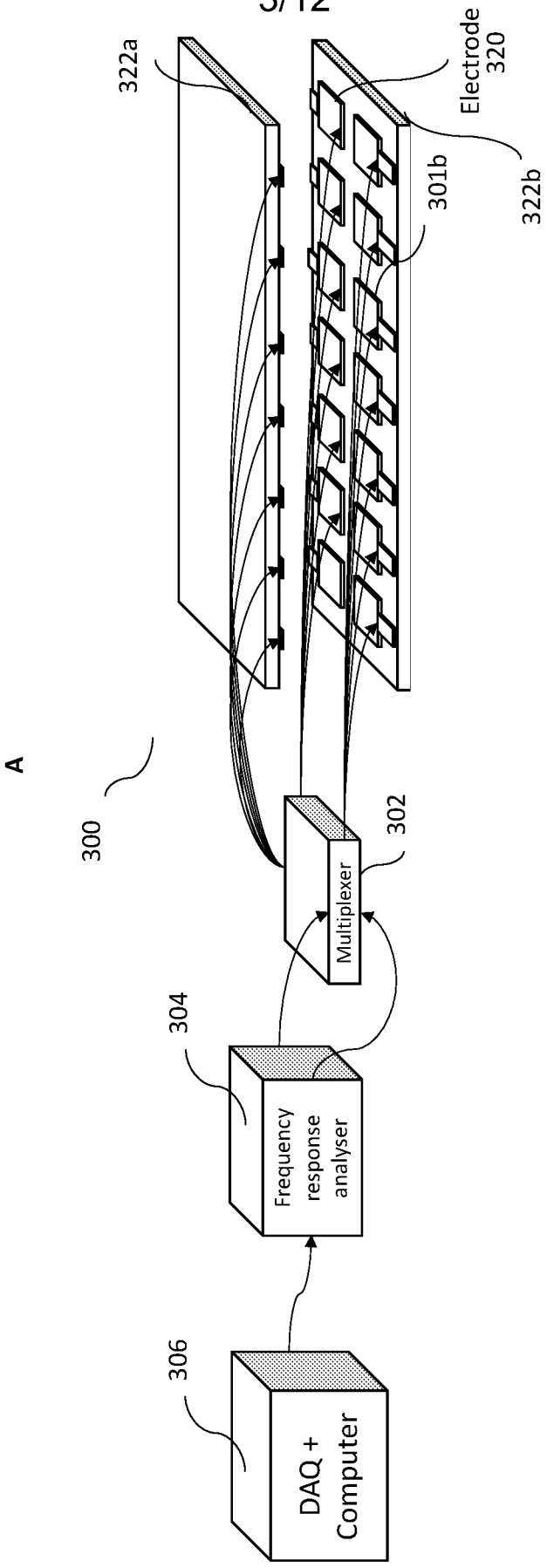
322a
Electrode
320
322b
301b
A
300
302
Multiplexer
304
Frequency
response
analyser
306
DAQ +
Computer

Figure 3

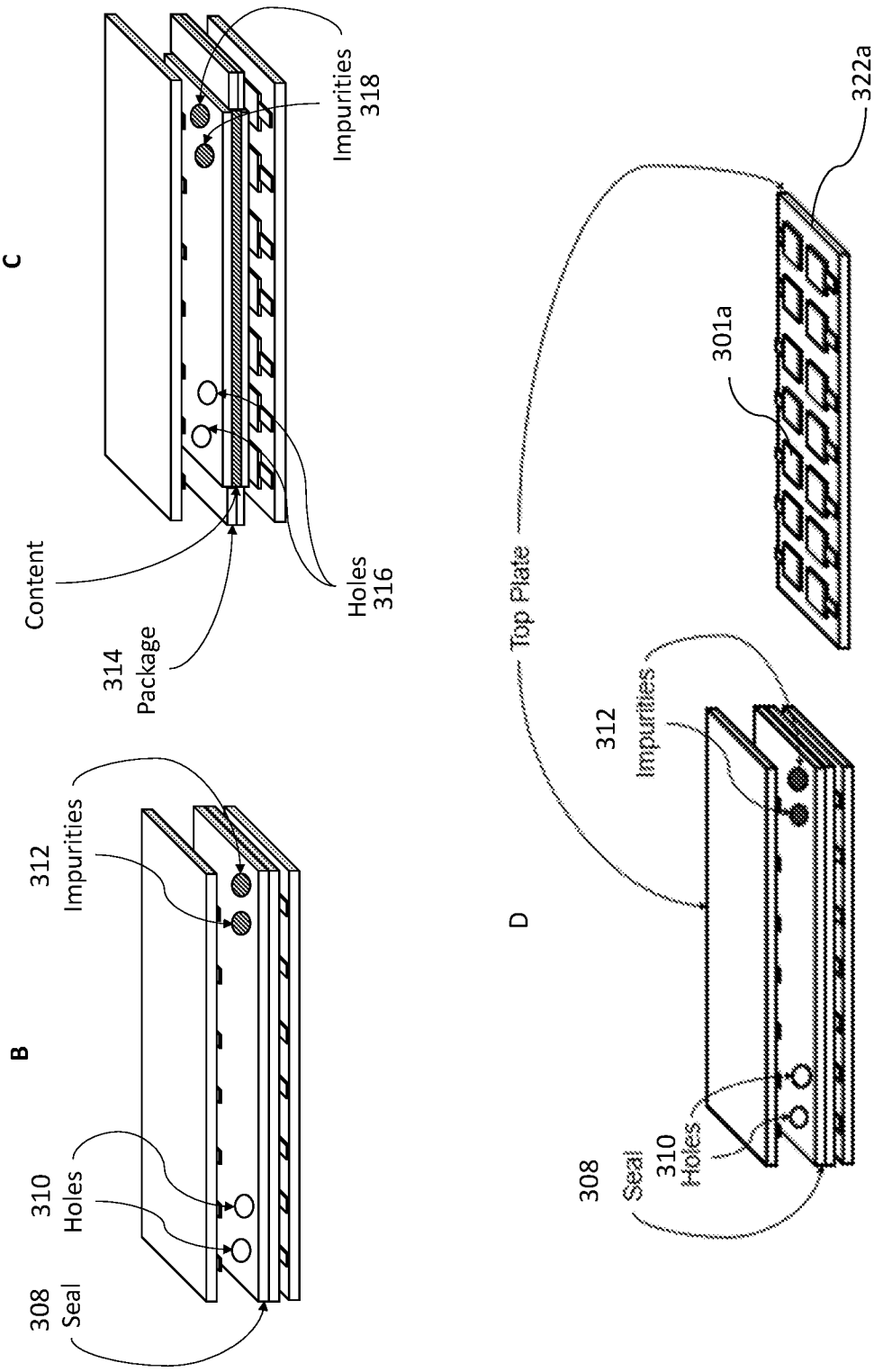

Figure 3 (continued)

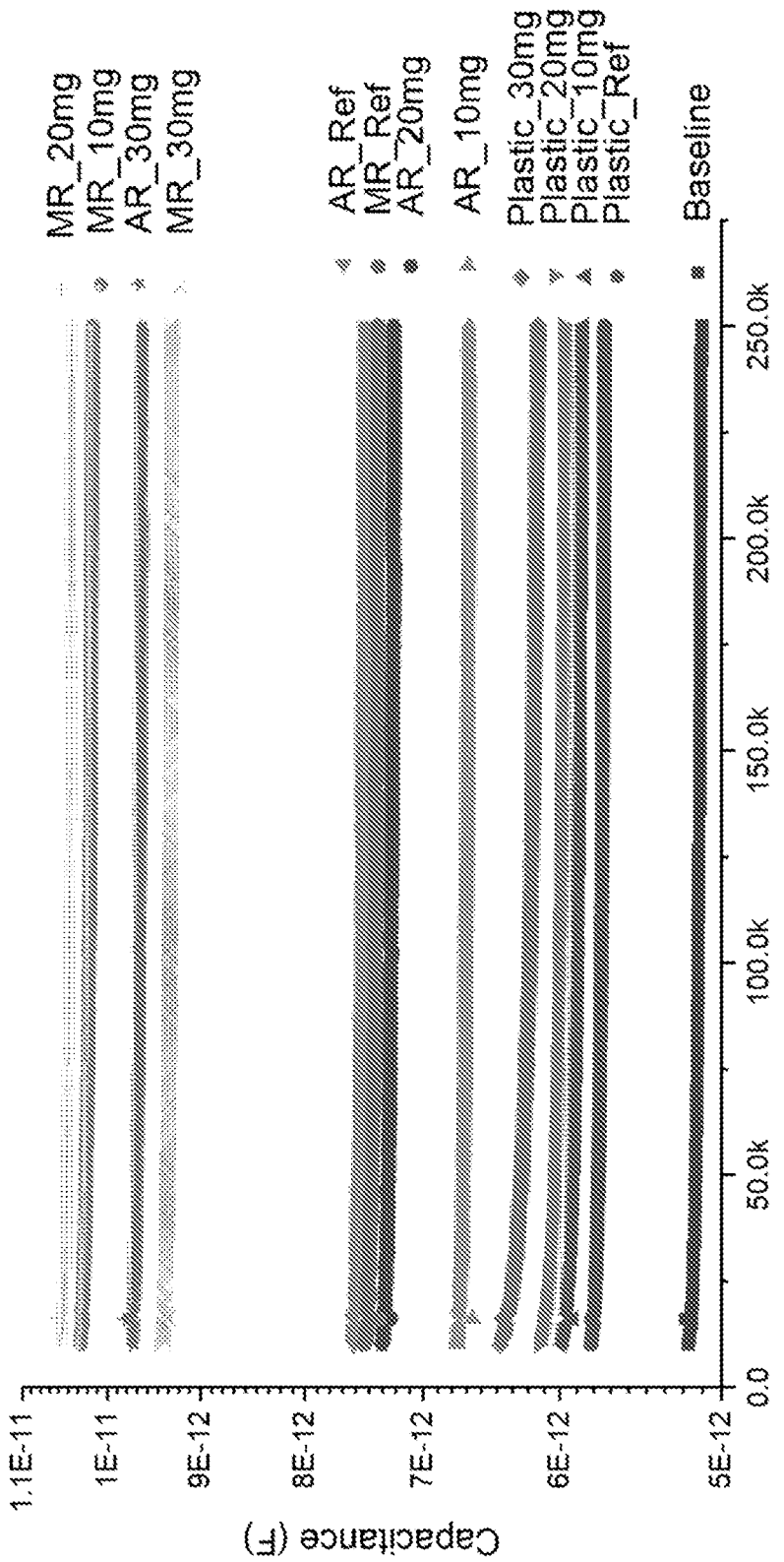
MR_20mg
MR_10mg
AR_30mg
MR_30mg
AR_Ref
MR_Ref
AR_20mg
AR_10mg
Plastic_30mg
Plastic_20mg
Plastic_10mg
Plastic_Ref
Baseline
Capacitance (F)
1.1E-11
1E-11
9E-12
8E-12
7E-12
6E-12
5E-12
0.0
50.0k
100.0k
150.0k
200.0k
250.0k
FREQ (Hz)

Figure 4A

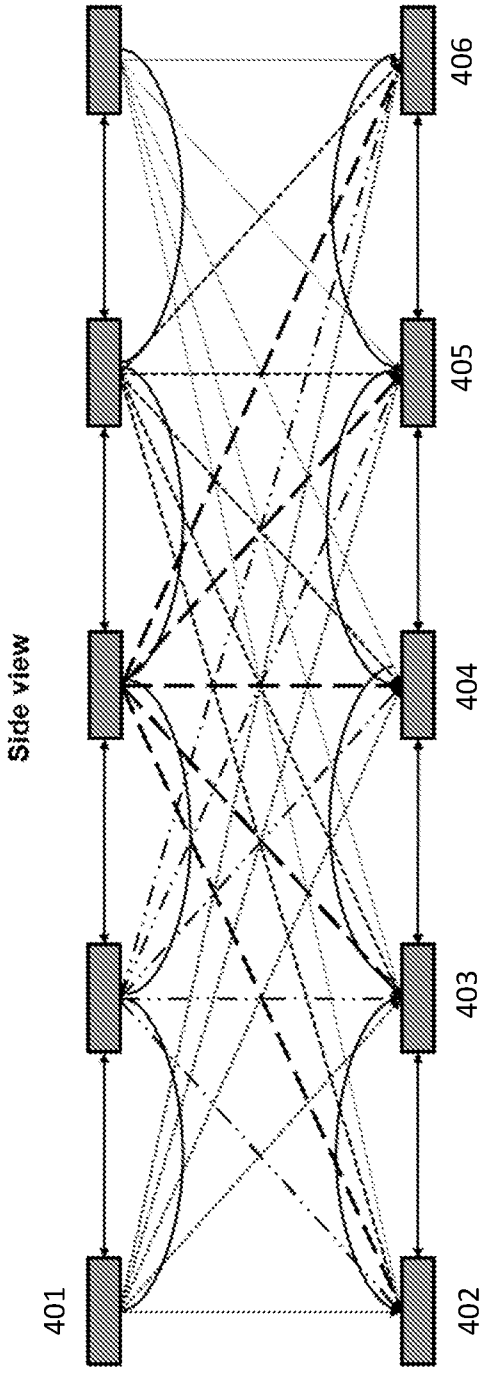

Figure 4B

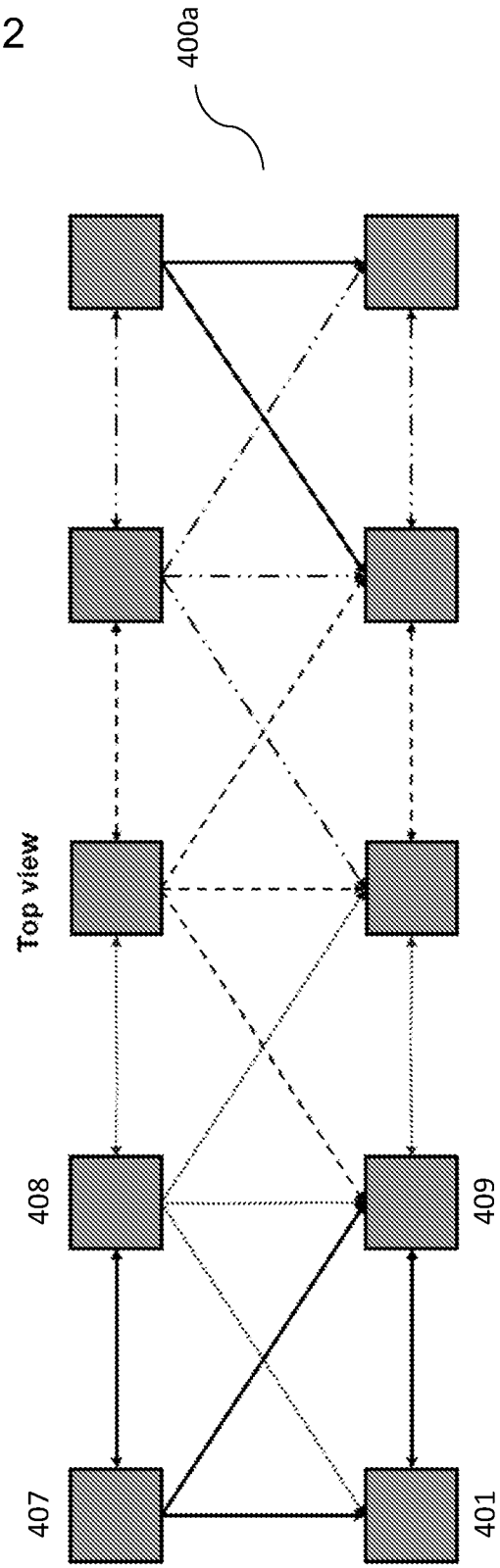

Figure 4C

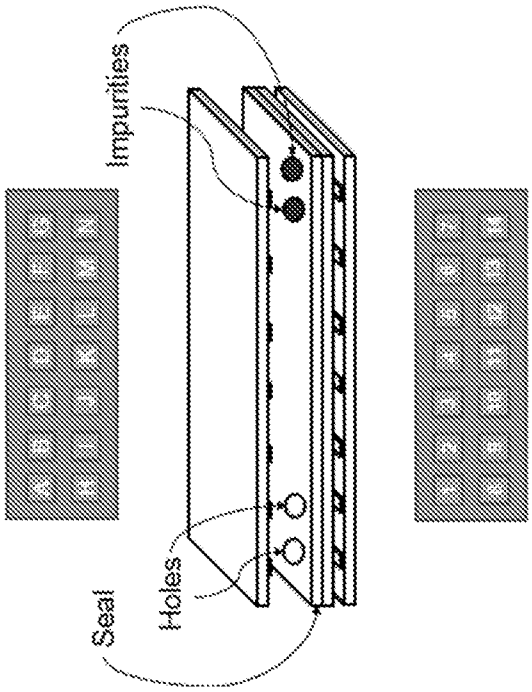

Figure 5B

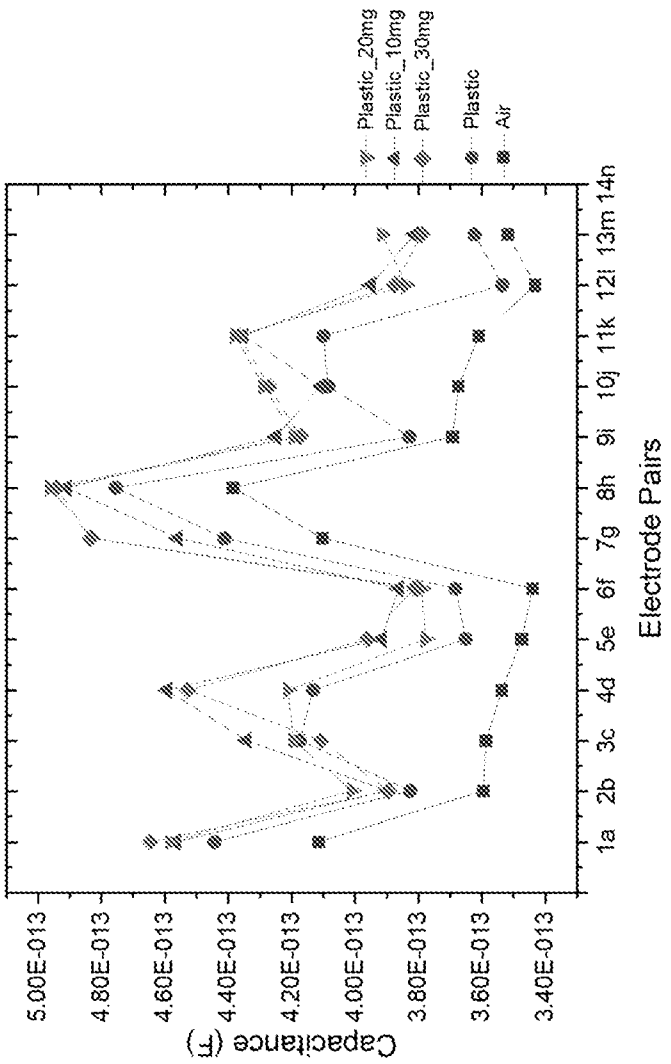

Figure 5A

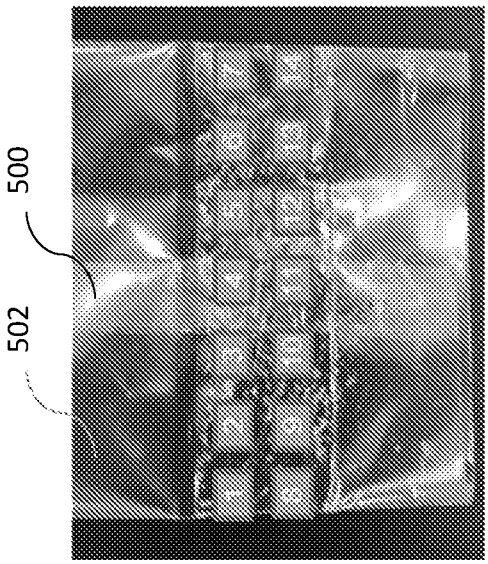

Figure 5C

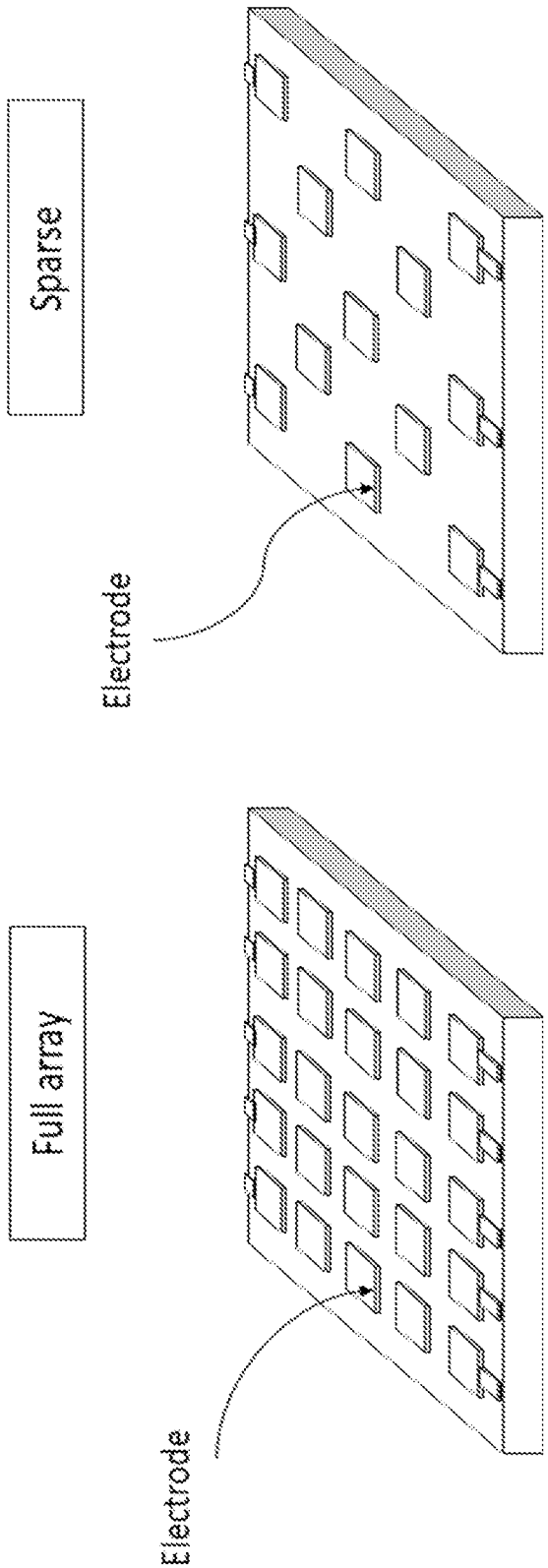

Figure 6

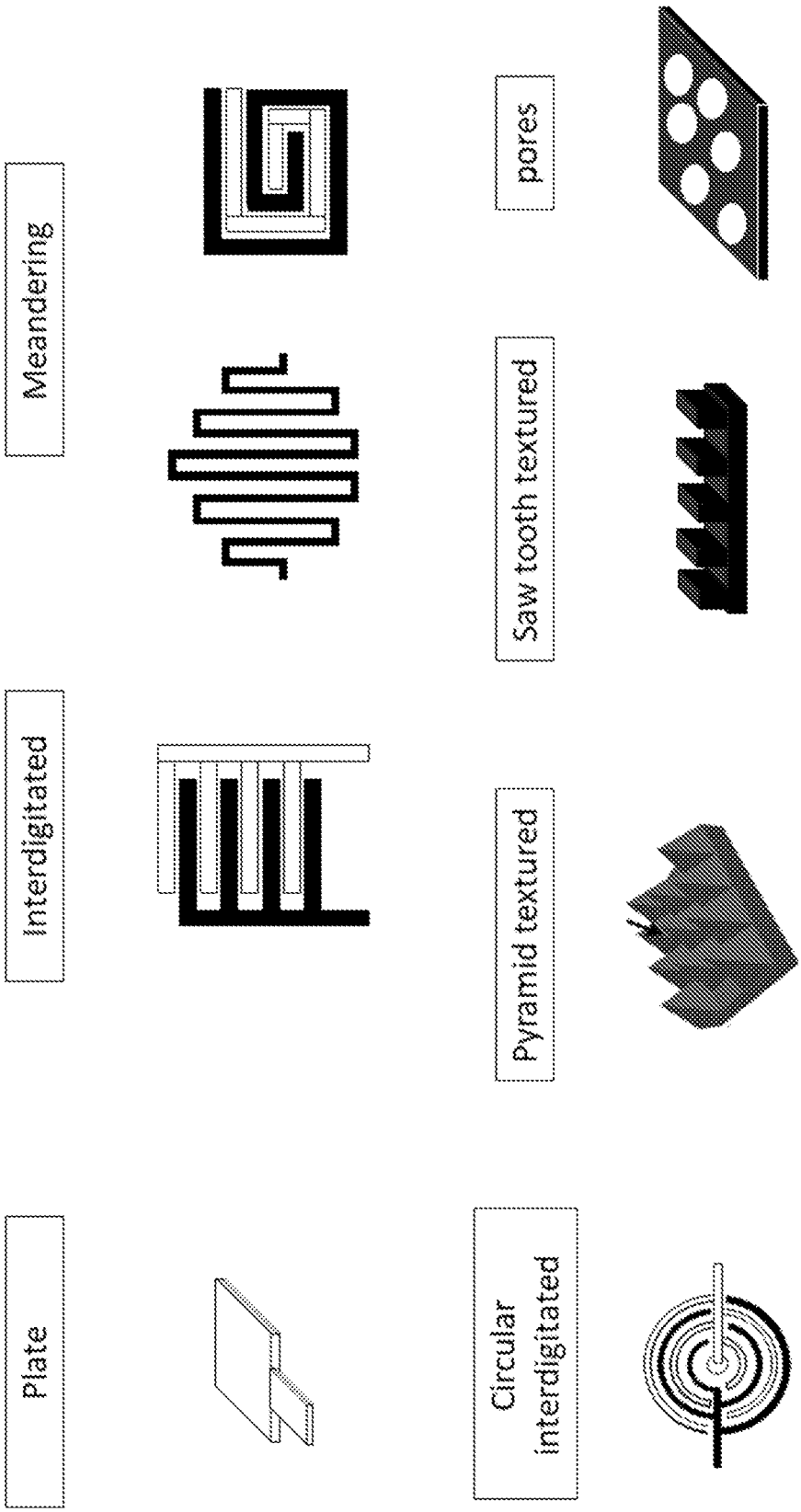
Meandering
pores
Interdigitated
Saw tooth textured
Plate
Pyramid textured
Circular interdigitated

Figure 7

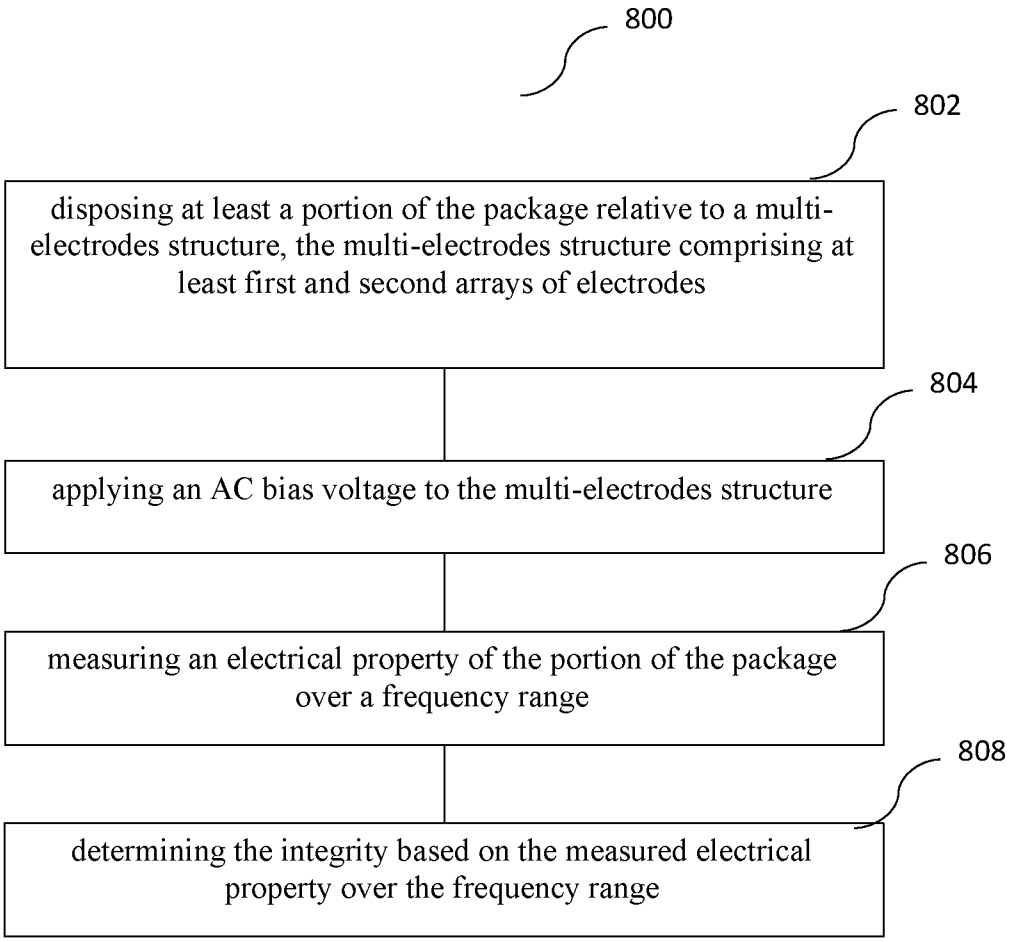
800
802
disposing at least a portion of the package relative to a multi-electrodes structure, the multi-electrodes structure comprising at least first and second arrays of electrodes
804
applying an AC bias voltage to the multi-electrodes structure
806
measuring an electrical property of the portion of the package over a frequency range
808
determining the integrity based on the measured electrical property over the frequency range

Figure 8

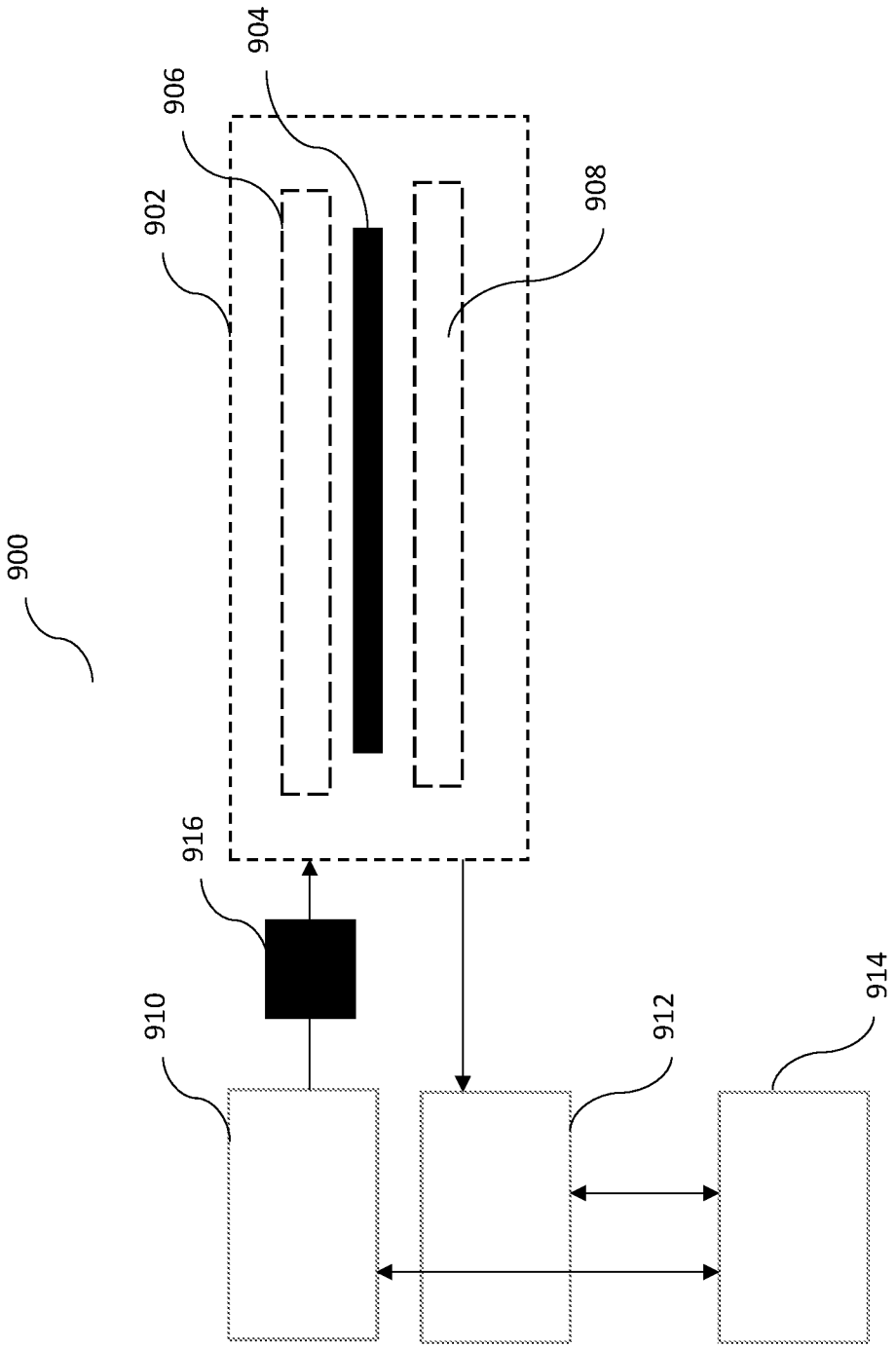

Figure 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2020/050460

A. CLASSIFICATION OF SUBJECT MATTER

G01M 3/40 (2006.01) ***G01N 27/22 (2006.01)*** ***G01N 27/04 (2006.01)***

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01M, G01N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT: Seal, hermetic, integrity, tight, leak, defect, hole, pinhole, flaw, perforation, food, beverage, pharmaceutical, medical, container, package, bag, electrode, pole, assembly, array, alternative current, frequency, capacitance, impedance, resistance, phase, multiplexer, 完整, 密封, 封口, 封, 气密, 密, 漏, 泄漏, 缺陷, 空, 孔, 洞, 缝, 饮料, 食品, 药物, 药品, 杯, 盒, 包, 容器, 容具, 袋, 电极, 极, 端, 电板, 阵列, 组, 阵, 排列, 多, 复, 交流, 偏压, 偏置, 频率, 电容, 阻抗, 电阻, 相位, 相, 多路器 and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/0151529 A1 (ISHIDA T.) 14 July 2005 Figs. 5, 9 and 10, para. [0041], [0056], [0084], [0093]-[0094], [0096], [0098]	1-22
Y	WO 2007/148361 A1 (FEDERIGHU DEDERIGO ET AL.) 27 December 2007 Pg. 3, ll. 10-30	1-22
A	US 4922181 A (PULLAN B. R.) 1 May 1990 Fig. 2, col. 3, ll. 34-39	

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

*Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13/11/2020 *(day/month/year)*	*23/11/2020* *(day/month/year)*

Name and mailing address of the ISA/SG

IPOS INTELLECTUAL PROPERTY OFFICE OF SINGAPORE

Intellectual Property Office of Singapore
1 Paya Lebar Link, #11-03
PLQ 1, Paya Lebar Quarter
Singapore 408533

Email: pct@ipos.gov.sg

Authorized officer

Chen Jiahe (Dr)

IPOS Customer Service Tel. No.: (+65) 6339 8616

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2020/050460

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4243932 A (KAKUMOTO M. ET AL.) 6 January 1981 Fig. 3, col. 3, ll. 21-52	
A	JP 2003-254941 A (NISSHIN DENSHI KOGYO KK) 10 September 2003 Whole document of the machine translation	

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/SG2020/050460

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005/0151529 A1	14/07/2005	JP 2003194663 A CN 1623083 A WO 03058189 A1 KR 20040069203 A AU 2002360010 A1 EP 1460405 A1	09/07/2003 01/06/2005 17/07/2003 04/08/2004 24/07/2003 22/09/2004
WO 2007/148361 A1	27/12/2007	IT RM20060326 A1	22/12/2007
US 4922181 A	01/05/1990	CA 1296769 C EP 0302727 A2 JP H0196569 A AU 2040588 A	03/03/1992 08/02/1989 14/04/1989 09/02/1989
US 4243932 A	06/01/1981	JP S5476284 A DE 2814064 A1 GB 1601797 A	18/06/1979 07/06/1979 04/11/1981
JP 2003-254941 A	10/09/2003	NONE	