

[54] ACCOUNTING MACHINE PROCESSOR

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[58] Field of Search.....235/60, 60.4, 60 C; 340/172.5

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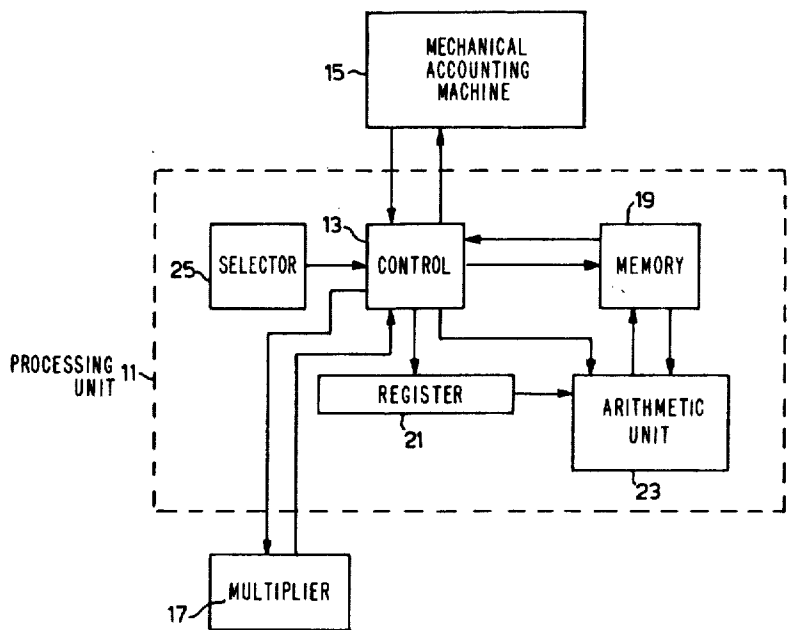
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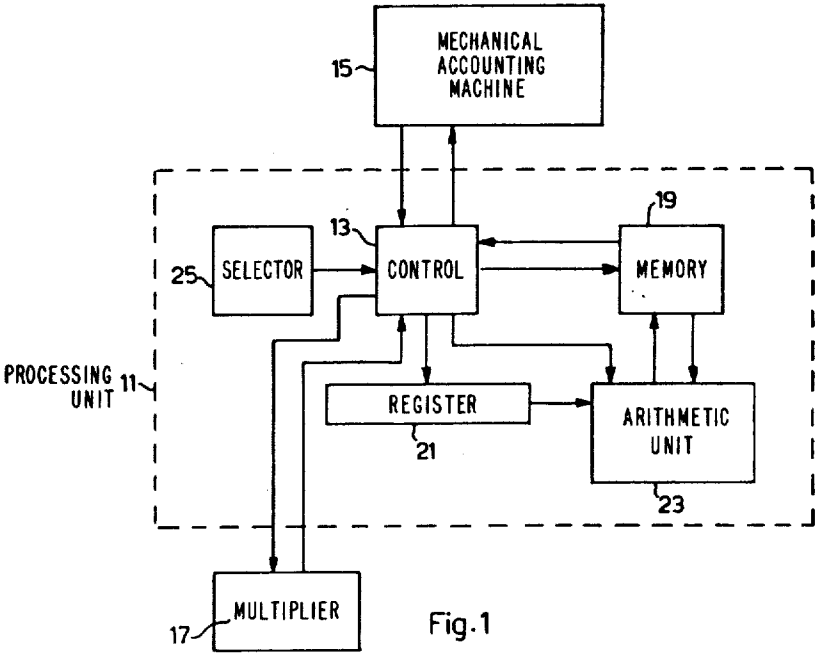
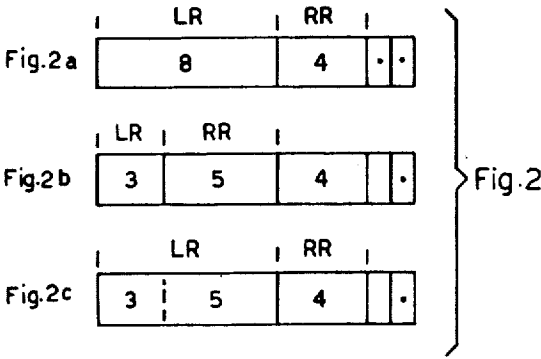
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[57] ABSTRACT

An electronic processing unit for mechanical billing and accounting machines comprising a multiregister memory and an arithmetic unit for operating on data received from the mechanical unit in conjunction with the data stored in an addressed memory register and for storing the result of the operation in the addressed register. A control unit controls the operation of the processing unit in accordance with instructions received from the connected mechanical unit and is responsive to reference codes received from the mechanical unit for overriding the address associated with the following instruction and to the designation of a register for preventing any modification of the data stored in the designated register.

2 Claims, 4 Drawing Figures





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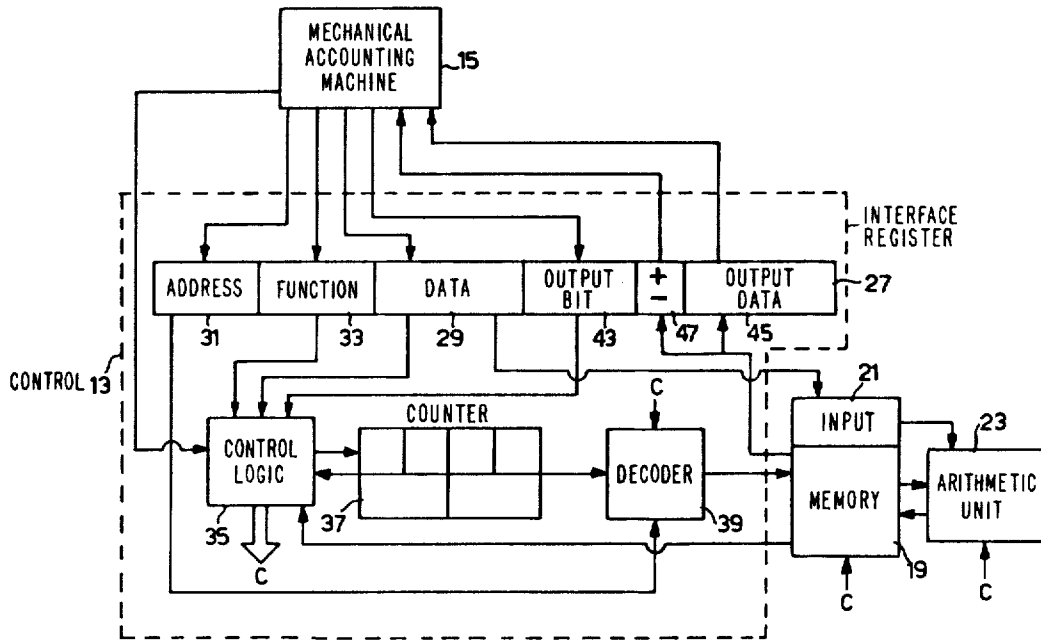


Fig.3

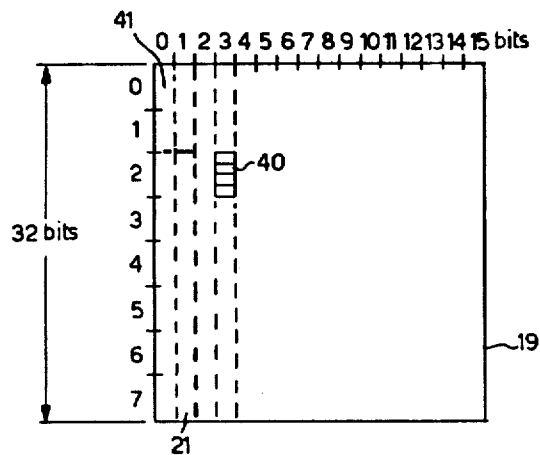


Fig.4

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ACCOUNTING MACHINE PROCESSOR

CROSS REFERENCE TO RELATED APPLICATION

Applicant claims priority from corresponding Italian patent application Ser. No. 51763-A/69, filed May 9, 1969.

BACKGROUND OF THE INVENTION:

1. Field of the Invention

This invention relates to improvements in processors for extending the data handling and processing capacity of mechanical billing and accounting machines.

2. Description of the Prior Art:

Mechanical accounting machines have been very widely used in business offices for many years and still offer substantial cost savings over electronic accounting machines of a similar capacity. Many applications however, require a larger number of accumulators and a greater processing capability than can be practically included in a totally mechanical machine because it would become too complex and slow. The problem of complexity and speed has also prevented the extension of the capabilities of practical mechanical accounting machines to those of a billing machine by the addition of a multiplier.

In order to increase the capabilities of a mechanical accounting machine without decreasing the processing speed, it has been proposed in the past to couple an electronic processing unit to the basic mechanical system in order to provide more accumulators. This processing unit also acted as an intermediary between the mechanical accounting machine and an electronic multiplier unit which gave the system the capabilities of a billing machine.

Although this processing unit greatly increased the capacity of the mechanical machine, some serious problems still existed. It is desirable in some applications to have a read-only memory included in the electronic processor for storing a number of constants, which number depends on the particular operation. It may also be desirable in some applications to have a dynamic memory capability in the processor whereby new data written into a memory location overwrites previous data rather than being accumulated with it. The particular features which are needed vary from application to application so that even a single user often needs one set of capabilities in running one job and another set for another job. These capabilities have not been available in any practical processing unit in the past however, because the cost of providing them would make the unit much too expensive.

Another difficulty with mechanical accounting machines, even when coupled to previously available electronic processing units is that the programming of the machine is rather rigid and there was no way of allowing operator intervention by means of the keyboard to make decisions during the running of a program on how information is to be handled by the machine. All addressing of the memory registers must be set up in the program and is carried out by the machine automatically during the execution of the program. This difficulty severely limits the range of applications for which the machine is suited.

SUMMARY OF THE INVENTION

These and other deficiencies in the prior art are overcome by the improved electronic processing unit according to this invention which comprises a multiregister memory including means for designating selected registers as accumulators or dynamic memories or as read-only memories and an arithmetic unit for operating on data received from the mechanical unit in conjunction with the data stored in an addressed memory register and for storing the result of the operation in the addressed register. Also included is a control unit for controlling the operation of the processing unit in accordance with instructions received from the connected mechanical unit and responsive to reference codes received from the mechanical unit for overriding the address associated with the following instruction and to the designation of a register as a read-only memory for preventing any modification of the data stored in the designated register.

Various other advantages and features of the invention will become apparent from the following specification with its appended claims and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an embodiment of an electronic processing unit according to the invention;

FIG. 2 shows the division of the memory registers when being used to store constants;

FIG. 3 is a more detailed block diagram of an electronic processing unit according to the invention;

FIG. 4 shows a possible configuration of the processing unit memory.

DETAILED DESCRIPTION OF THE INVENTION

The invention can best be understood from the following detailed description of the illustrated embodiment.

General Description

Referring to FIG. 1 of the drawings, electronic processing unit 11 includes the control unit 13 which controls the flow of information between the mechanical accounting machine 15, the other portions of the processing unit 11 and the multiplier unit 17. The mechanical accounting machine 15 may be similar to that described in U.S. Pat. No. 3,006,540 which is assigned to the assignee of the present invention.

The mechanical unit 15 and the electronic unit 11 in the illustrated embodiment of the invention operate on data with a binary-decimal format in which each decimal digit is made up of 4 binary bits. Communication between the mechanical unit 15 and the control unit 13 is on a parallel by bit, serial by digit fashion whereas the operation of the electronic unit 11 in the preferred embodiment of the invention is completely serial. This serial mode of operation allows a substantial saving in hardware and, since the electronic processing speed is very much higher than the speed of the mechanical unit, the still higher speed obtainable by parallel operation of the electronic unit 11 is not needed.

Instructions and data to be operated on in accordance with the instructions which are received by

the control unit 13 from the mechanical unit 15. The control unit 13 transfers the data number in a serial fashion to the input register 21, causes it to be operated on in accordance with the associated instruction in the arithmetic unit 23 and transfers the result to a selected register in the memory 19.

If an instruction for recalling a data word from a selected portion of the memory 19 is received by the control unit 13, it reads the addressed word in a serial fashion from the memory 19 and transfers it to the mechanical unit 15 in a parallel by bit, serial by digit fashion.

The memory 19 may consist of a magnetic core memory and includes eight registers each being capable of storing a 12 digit number and a sign bit. Associated with each register are two tag bits which are used to designate how the register is to be used in the carrying out of a particular problem. Each memory register may be used either as an accumulator or a dynamic memory or as a read only memory for storing either two or three constants. The memory 19 also includes a service area for storing item or reference codes and miscellaneous control bits.

The five position, manually settable selector 25 may be set by operator in one of the first three positions when it is desired to run a program or in the fourth or fifth positions for entering constants into registers which are to be used as read-only memories. As illustrated in FIG. 2 of the drawings, a memory register may be used to store either 2 constants of 4 and 8 bits, respectively, or 3 constants of 4, 5 and 3 bits, respectively. If the first case both tag bits are recorded as illustrated in FIG. 2A of the drawings and in the case of 3 constants only 1 tag bit is recorded, as illustrated in FIGS. 2B and 2C.

In entering constants into a register a 12 digit number is entered with the digits and zeros in the proper places so that the desired constants appear in the various portions of the register. When the selector 25 is set to 4, the number entered into a register is interpreted as consisting of 3 constants and a single tag bit is recorded in order to mark the register as containing 3 constants during the later processing. A 12 digit number entered into a register while the selector 25 is set at 5 is interpreted as 2 constants and 2 tag bits are recorded to mark the register in later processing.

By way of example, if it is desired to record the constants 31, 45351 and 25 in a register, the selector 25 is set to position 4 and the 12 digit number 031453510025 is entered into the selected register from the keyboard of the mechanical unit 15. The entering of the number in the register while the selector 25 is set at 4 automatically sets 1 tag bit in the register. In order to run a program the selector 25 is reset to one of the first three positions and the operation is begun. The contents of a register having 1 or 2 tag bits recorded therein may be read but cannot be erased or changed while the selector 25 is set to one of the first three states. Each time the control unit 13 receives an instruction for inserting data into a selected memory register, it checks the associated tag bits and if one is recorded, the control unit 13 does not carry out the instruction but only enters the data into the input register 21.

In the preferred embodiment of the invention, a constant stored in register 8 is always interpreted as a 12 digit constant whether it was entered in state 4 or 5. This feature is very useful when the multiplier unit 17 is connected in the system and it is desired to divide numbers by a constant. The reciprocal of the constant is stored in the eighth register and the divisions is carried out by multiplication by the reciprocal.

One difficulty which in the past has limited the amount by which an electronic processing unit can expand the capabilities of a mechanical accounting machine is the fact that the number of different instruction codes in the repertoire of the mechanical unit is relatively small. Thus only a relatively few instruction codes are available for controlling the operation of the electronic unit so that the number of functions which it can perform are therefore limited.

This problem is solved in the present invention by defining a plurality of statuses of the mechanical machine 15 and providing logic in the control unit 13 for interpreting an instruction code differently depending on which status the machine 15 is in. Thus an instruction code may have one meaning if the machine 15 is in one status and another meaning if the machine 15 is in another status.

There are two instructions used to recall a constant from a constant storing register to the mechanical unit 15. These are a left side recall instruction (LR) and a right side recall instruction (RR). In cases where 2 constants are stored in a register, i.e., where both tag bits are recorded, the left and right recall instruction addresses the 8 and 4 digit constants stored on the left and right sides, respectively, of the addressed register, as illustrated in FIG. 2A of the drawings. The operation in this case is independent of the status in which the machine 15 is in.

When 3 constants are stored in a register, the interpretation by the control unit 13 of the left and right recall instructions depend on which status the machine 15 is in. Normally the left and right recall instructions are interpreted in the same manner as described above in the case of 2 constants as illustrated in FIG. 2C. This, however, allows only the right hand 4 digit constant to be recalled separately. In order to recall the 5 and 3 digit constants, the machine 15 must be in a particular status, here designated C2. When the machine 15 is in this status the control unit 13 interprets the left and right recall instructions for recalling the 3 and the 5 digit constants, respectively, as shown in FIG. 2B of the drawings.

When no tag bits are recorded in a register it may be used either as an accumulator or as a dynamic memory. Normally the untagged registers act as accumulators with the new data words being added to or subtracted from the previous contents and the result being stored in the addressed register. When the machine is in status C2, however, the registers act as dynamic memory and each new data entry erases the previous one.

Referring now to FIG. 3 of the drawings, the control unit 13 of the illustrated embodiment of the invention includes an input-output interface register 27 for providing a data and instruction interface with the mechanical unit 15. When the mechanical unit 15 wants to send data to the processing unit 11 for entry into the memory 19 it first sends a 4 bit processing unit

select signal to the data portion 29 of the register 27, the 3 bit address of the desired memory register to the address portion 31 and the sign of the data to the 1 bit function portion 33. The reception of the select signal causes the control logic 35 to transfer the data characters which follow to the input register 21 which, in the preferred embodiment of the invention, is physically a part of the memory 19.

The addressing of the memory is performed by means of the address portion 31 of the register 27 and a counter system 37 whose outputs are decoded by decoder 39. The address portion 31 selects one of the memory registers. The counter system 37 includes a 4 bit counter for addressing the digits of the selected register and the 2 bit counter for addressing one of the 4 bits which make up a digit.

Referring to FIG. 4 of the drawings, the memory 19 may, in the preferred embodiment of the invention, be made up of a commercially available 32×16 bit magnetic core memory. The 32 bit side of the memory may be divided into eight groups of four rows of bits, numbered 0 through 7, for making up the eight registers. Since each register has a 12 digit capacity only 12 columns, numbered 4 through 15, of the 16 bit side of the memory 19 are used for the register. The 13th column, numbered 3, contains eight groups 40 of 4 bits, each of which is associated with the register whose rows it falls in. Two of the 4 bits may be used as tag bits and a third for indicating the sign of the number stored in the register. The input register 21 may be made up of two columns, numbered 0 and 1, of six groups of four rows of bits, numbered 2 through 7. The service area 41 may be constituted by the other two groups of four rows of bits numbered, 0 and 1, in the 0 and 1 columns.

The 4 bit counter of counter system 37 is also used for addressing the digits of the input register 21. The 3 most significant bits of the counter indicate which of the eight registers is being addressed and the least significant bit indicates whether column 0 or 1 is being addressed. When addressing the input register 21, the control logic 35 causes the decoder 39 to interpret the output of the 4 bit counter in this manner. The overflow from the two bit counter acts to increment the 4 bit counter.

The data which accompanies an input instruction is received one digit at a time from the mechanical unit 15. When entering this data into the input register 21, the control logic 35 initially enters a binary 2 into the 4 bit counter. The control logic 35 then initiates a memory cycle for transferring the least significant bit of the digit in the data portion 29 of the register 27 to the least significant bit of the input registers, which are both addressed by the 2 bit counter which is initially set to zero.

The processing unit uses the memory cycle as a clock and thus has clock pulses generated only when the memory 19 is operating. Each memory cycle increments the 2 bit counter which causes the control logic 35 to initiate the next cycle. This process continues until all 4 bits of the digit are read into the least significant digit place of the input register 21. The overflow from the 2 bit counter increments the 4 bit counter to 3 and stops the operation of the control logic 35. The processing unit 11 then waits until the next digit from the mechanical unit 15 is inserted into the data portion

29 which insertion initiates another entry operation for entering the digit into the next digit place of the input register 21. This process continues until all the digits are entered into input register 21.

The meaning of the bit stored in the function portion 33 of the register 27 depends on whether an output signal is sent by the mechanical unit 15 to the portion 43 of the register 27 and whether the register addressed is a constant storing register. If there is no output signal, i.e., if the instruction is for the input of data, the function bit 33 indicates whether the accompanying data word is to be algebraically added to or subtracted from the contents of the addressed register.

If there is an output signal stored in portion 43 and a tag bit is present in the addressed register, the function bit 33 indicates either the right or left recall instruction. If no tag bit is present in the addressed register the function bit 33 indicates whether the data word in the addressed register is to be recalled as a total or as a subtotal, that is, recall with or without erasure of the contents of the register.

When data is being entered into an untagged register which is being used as an accumulator, i.e., when the machine is not in status C2, the control logic 35, after entering the data into the input register 21, senses the function bit 33 of the instruction and the sign of the number in the addressed register of the memory 19 in order to decide whether an addition or a subtraction operation is to be performed.

In order to simplify the logic of the arithmetic unit 23 and the control logic 35, the arithmetic operation between the contents of the input register 21 and the addressed register of the memory 19 is performed twice. The first time the result is not entered into the memory 19 but the original contents are restored. The second time the result is entered.

The operation is performed in this manner since a different algorithm must be used in subtraction operations depending on whether the minuend or subtrahend is larger. Therefore the logic may be greatly simplified if the smaller number is always subtracted from the larger or vice-versa.

The first time the subtraction is performed it is done merely to find out which number is larger. The second time through the smaller number is always subtracted from the larger and the result is entered into the addressed register of the memory 19. The proper sign of the result is determined by the control unit 13 and entered into the memory 19.

It is not necessary to know which operand is larger in the case of an addition operation but the addition is also performed twice in the same manner as the subtraction in order to simplify the logic.

The arithmetic operations are performed in a completely serial manner. The corresponding bits, starting from the least significant bit of the least significant digit, are read under the control of the control logic 35 from the input register 21 and the addressed register of the memory 19 by the arithmetic unit 23, operated upon and the result bit is written into the addressed memory register in place of the bit which was operated upon. As stated above, the first time the operation is performed the result bit is not written into the memory 19.

In addressing the memory 19 each successive value of the 4 bit counter is used both to address a digit of the addressed register and the corresponding digit of the input register 21. The 2 bit counter addresses the corresponding bits in both registers. Before commencing the arithmetic operation the control logic 35 enters a binary 2 into the 4 bit counter. The overflow of the 4 bit counter indicates the end of the operation.

The arithmetic unit 23 may be similar to that described in U.S. Pat. No. 3,304,418 which issued on Feb. 2, 1967 and which is assigned to the assignee of the present invention.

The operation of the arithmetic unit 23 could clearly be made much faster by including more logic for allowing additions and subtractions to be performed in a single cycle of the data through the unit 23 and by providing for more parallel handling of the data. This extra speed would yield no advantages in the present case, however, since the electronic unit 11 is already much faster than the mechanical unit 15.

When a register is being used as a dynamic memory i.e., when the machine is in status C2, the reading of the contents of the addressed register by the arithmetic unit 23 is inhibited during the arithmetic operation so that the contents of the input register 21 are, in effect, added to zero and entered into the addressed memory register.

When the mechanical unit wishes to recall data from the processing unit 11 it sends the 4 bit processing unit select signal to the data portion 29 of the register 27, sets the output bit 43 and inserts the address of the desired memory register to the address portion 31. If it wishes to recall the contents of the input register the mechanical unit 15 sends only the output bit and the select code.

In carrying out the recall, the control logic 35 first enters a binary 2 in the 4 bit counter and causes the decoder 39 to begin the recall starting from the most significant digit.

The control logic 35 then transfers the bits of the digit to the 4 bit output data portion 45 of the register 27 and resets the output bit 43. After doing this the processing unit 11 waits until the mechanical unit 15 again sets the output bit 43 which initiates another sending cycle. This process continues until all 12 digits in the addressed register are recalled.

The overflow of the 4 bit counter indicates that the 12th digit has been sent and that the sign bit is to be sent next. When the mechanical unit 15 next sets the output bit 43, the control logic 35 causes the sign bit which is preferably stored in the least significant bit place of the corresponding 4 bit group 40 in column number 13, to be sent to the sign bit portion 47 of register 27.

If the register being recalled is storing constants the recall instruction can also set the function bit 33. When the control logic senses a tag bit associated with the register addressed by a recall instruction the function bit 33 determines whether it is a left or right recall instruction. The counter system 37 counts through the entire register in the same manner as described above but the control logic enables the memory 19 to send only those digits to the data portion 45 of register 27 which are specified by the function bit 33, the tag bits and the status of the mechanical unit 15.

Instead of using the address sent with an input or output instruction, it is also possible to address a memory register means of an item or reference code. This item or reference code may be entered by the operator manually from the keyboard or may be generated by the mechanical machine 15. It may have the significance of a code number or model number for a particular item which identifies the item both to the operator and to the machine or it may have another significance chosen by the programmer.

The mechanical unit 15 sends the item code to the service area 41 of the memory 19 by first transmitting a special selection code to the data portion 29 of register 27, the address of a predetermined portion of the service area 41 to the address portion 31 and a code bit to the function portion 33 for indicating whether the least significant or next more significant digit of the item or reference code is to be used entered into the service area 41. This is followed by the data block of the item or reference code sent in the ordinary digit by digit manner. The control logic, however, in response to the special selection code, enters only the first or second digit received into the service area 41, depending on whether or not the function bit 33 is set. The other digits of the data block are ignored.

If the selected digit has the value of 0 it indicates that the register address which accompanies the following instruction should be used as the address. If it has a value between 1 and 8, it signifies that it is to be substituted in the address portion 31 in place of the address which accompanies the next instructions received from the mechanical unit 15. If it has the value 9, it indicates that the next instruction should not be executed by the processing unit 11. In this case only the mechanical unit 15 executes the instruction.

Each time the register 27 receives an instruction from the mechanical unit 15, the control logic 35 checks the predetermined location in the service area 41 of the memory 19 to see if it contains a digit. If it does, the digit is used in the manner stated in the preceding paragraph. After a digit in the service area 41 is used by an instruction it is automatically erased from the service area 41 so that the next instruction uses the address which accompanies it unless a new item or reference code is received.

As stated above, the first three settings of the selector 25 are used for the normal operation of the system. When the selector 25 is set at the one position all the instructions of the repertoire may be executed. When the selector 25 is set in positions two or three selected ones of the instructions of the repertoire are not executed by the processing unit 11. This is a useful feature when it is desired to execute some instructions in the mechanical unit 11 but not in the processing unit 15.

The multiplier unit 17 may be connected into the system to extend the capabilities of the system to that of a billing machine. The data and instructions for the multiplier unit 17 are sent to the multiplier 17 from the mechanical unit 15 through the control unit 13. Some instructions are executed both in the processing unit 11 as an addition or subtraction and in the multiplier as a multiplication. In this case the control unit 13 causes the accompanying data word to be sent both to the multiplier 7 and to the input register 21.

Other instructions are executed only in one unit or the other. In this case the control unit either sends the instruction and the accompanying data to the multiplier 17 or executes it in the processing unit 11.

In the illustrated embodiment of the invention data stored in the memory 19, in order to be sent to the multiplier 17 must first be sent to the mechanical unit 15 and then transferred to the multiplier.

I claim:

1. An electronic processing unit for a mechanical accounting or billing machine, said processing unit receiving address containing instructions from the mechanical machine for entering data therein and recalling data therefrom comprising:

a. a memory including

1. a plurality of registers, and

2. settable means associated with said registers for indicating the storage of different numbers of constants in the associated memory registers and for designating selected ones of said registers as read-only memories, said settable means causing tag bits to be placed into said selected registers, said tag bits causing said selected registers to be treated as read-only memories,

b. an arithmetic unit coupled to said memory for operating on data received from the mechanical machine in conjunction with data stored in a register of said plurality of registers in said memory designated by the address contained in the instruction and for storing the result of the operation in the addressed designated register, and

c. controlling means coupled to said mechanical

machine and said settable means of said memory for controlling the storage of data in said memory, said controlling means being responsive to an instruction from said mechanical machine and to said settable means for recalling a selected one of the constants stored in a selected designated register of said plurality of memory registers to said mechanical machine and responsive to the designation of one of said plurality of memory registers by said settable means as a read-only memory for preventing any modification of the contents of the designated register, and responsive to a reference code received from the mechanical machine for substituting an address contained in said reference code for the address associated with the next instructions received from the mechanical machine.

2. The processing unit of claim 1 wherein said controlling means includes:

a. control logic, and

b. an interface register for receiving instructions from said mechanical machine and data for transfer between said mechanical machine and said memory, said memory including an input register for receiving from said interface register, under the control of said control logic, the data being sent by said mechanical machine, said control logic including means for transferring the data inserted into said input register to said arithmetic unit for processing in accordance with the accompanying instruction.

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