(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 June 2014 (19.06.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/093651 A1

(51) **International Patent Classification**:
H01L 27/115 (2006.01)

(21) **International Application Number**:
PCT/US2013/074724

(22) **International Filing Date**:
12 December 2013 (12.12.2013)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
13/715,185 14 December 2012 (14.12.2012) US

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: CHARGE TRAPPING SPLIT GATE DEVICE AND METHOD OF FABRICATING SAME

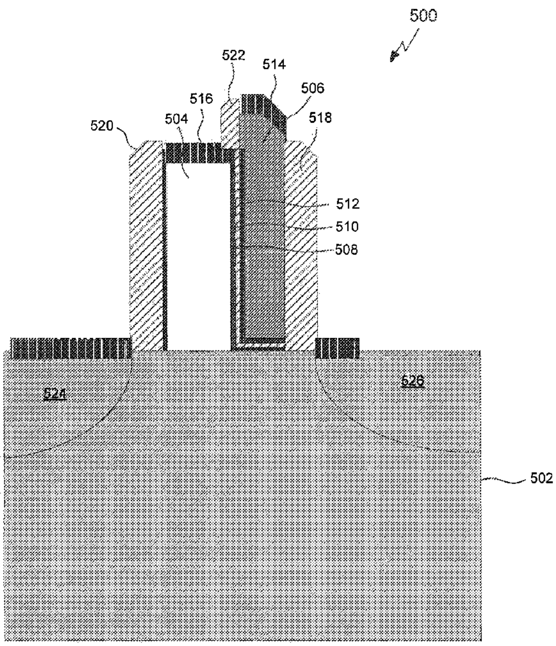

FIG. 5

(57) Abstract: Embodiments provide a split gate device, methods for fabricating a split gate device, and integrated methods for fabricating a split gate device and a periphery device. In an embodiment, the split gate device is a charge trapping split gate device, which includes a charge trapping layer. In another embodiment, the split gate device is a non-volatile memory cell, which can be formed according to embodiments as standalone or embedded with a periphery device.

WO 2014/093651 A1

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

CHARGE TRAPPING SPLIT GATE DEVICE AND METHOD OF FABRICATING SAME

BACKGROUND

Field of the Invention

[0001] The present disclosure relates generally to nonvolatile memory.

Background Art

[0002] There is a growing demand to provide advanced logic components (e.g., microcontrollers) with support memory, commonly implemented using non-volatile memory (e.g., Flash). Generally, two approaches exist for providing the support memory. One approach includes fabricating the advanced logic components and the memory components on separate semiconductor chips and interfacing the separate chips via a communication interface, resulting in a non-monolithic design. Another approach includes integrating the advanced logic and the memory components on the same semiconductor chip, in what is known as an embedded memory design.

[0003] Generally, an embedded memory design is favored over a non-monolithic design for speed, security, and power consumption considerations, but requires an integration process for fabricating the advanced logic components and the memory components on the same semiconductor chip.

BRIEF SUMMARY

[0004] Embodiments provide a split gate device, methods for fabricating a split gate device, and integrated methods for fabricating a split gate device and a periphery device. In an embodiment, the split gate device is a charge trapping split gate device, which includes a charge trapping layer. In another embodiment, the split gate device is a non-volatile memory cell, which can be formed according to embodiments as standalone or embedded with a periphery device.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0005] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate the present disclosure and, together with the description, further serve to explain the principles of the disclosure and to enable a person skilled in the pertinent art to make and use the disclosure.

[0006] FIG. 1 illustrates an example split-gate non-volatile memory cell.

[0007] FIG. 2 illustrates an example circuit diagram of the memory cell illustrated in FIG. 1.

[0008] FIG. 3 illustrates an example semiconductor device that includes both memory and peripheral circuitry embedded in the same substrate.

[0009] FIGs. 4A-J are cross sectional views illustrating various example steps in a method of fabricating a split gate device according to an embodiment.

[0010] FIG. 5 is a cross sectional view of an example split gate device according to an embodiment.

[0011] The present disclosure will be described with reference to the accompanying drawings. Generally, the drawing in which an element first appears is typically indicated by the leftmost digit(s) in the corresponding reference number.

DETAILED DESCRIPTION OF EMBODIMENTS

[0012] This specification discloses one or more embodiments that incorporate the features of this invention. The disclosed embodiment(s) merely exemplify the present invention. The scope of the present invention is not limited to the disclosed embodiment(s). The present invention is defined by the claims appended hereto.

[0013] The embodiment(s) described, and references in the specification to "one embodiment," "an embodiment," "an example embodiment," etc., indicate that the embodiment(s) described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is understood that it is within the knowledge of one skilled in the art to effect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0014] FIG. 1 illustrates an example split-gate non-volatile memory cell 100 according to an embodiment. Memory cell 100 is formed on a substrate 102, such as silicon. Substrate 102 is commonly p-type or a p-type well while a first doped source/drain region 104 and a second doped source/drain region 106 are n-type. However, it is also possible for substrate 102 to be n-type while regions 104 and 106 are p-type.

[0015] Memory cell 100 includes two gates, a select gate 108 and a memory gate 110. Each gate may be a doped polycrystalline silicon (poly) layer formed by well known, for example, deposit and etch techniques to define the gate structure. Select gate 108 is disposed over a dielectric layer 112. Memory gate 110 is disposed over a charge trapping dielectric 114 consisting of one or more dielectric layers. In one example, charge trapping dielectric 114 includes a silicon nitride layer sandwiched between two silicon dioxide layers to create a three-layer stack collectively and commonly referred to as "ONO." Other charge trapping dielectric may include a silicon-rich nitride film, or any film that includes, but not limited to, silicon, oxygen, and nitrogen in various stoichiometries.

[0016] A vertical dielectric 116 is also disposed between select gate 108 and memory gate 110 for electrical isolation between the two gates. In some examples, vertical dielectric 116 and charge trapping dielectric 114 are the same dielectric, while in other examples one dielectric is formed before the other (i.e., they can have different dielectric properties). As such, vertical dielectric 116 need not include the same film structure as charge trapping dielectric 114.

[0017] Regions 104 and 106 are created by implanting dopants using, for example, an ion implantation technique. Regions 104 and 106 form the source or drain of a split-gate transistor depending on the voltages applied to each. In split gate transistors, for convenience, region 104 is commonly referred to as the drain, while region 106 is commonly referred to as the source, independent of the relative biases. It is to be understood that this description is meant to provide a general overview of a common split-gate architecture and that, in actual practice, many more detailed steps and layers are provided to form the final memory cell 100.

[0018] An example write, read, and erase operation will now be described as it relates to memory cell 100. In order to write a bit in memory cell 100, a positive voltage on the order of 5 volts, for example, is applied to region 106 while region 104 and substrate 102 are grounded. A low positive voltage on the order of 1.5 volts, for example, is applied to select gate 108 while a higher positive voltage on the order of 8 volts, for example, is applied to memory gate 110. As electrons are accelerated within a channel region between the source and drain, some of the electrons will acquire sufficient energy to be injected upwards and get trapped inside the charge trapping dielectric 114. This is known as hot electron injection. In one example of charge trapping dielectric 114, the electrons are trapped within the nitride layer of charge trapping dielectric 114. This nitride layer is also commonly referred to as the charge trapping layer. The trapped charge within charge trapping dielectric 114 store the "high" bit within memory cell 100, even after the various supply voltages are removed.

[0019] In order to "erase" the stored charge within memory cell 100 and return the state of memory cell 100 to a "low" bit, a positive voltage on the order of 5 volts, for example, is applied to region 106 while region 104 is floated or placed at certain bias, and select gate 108 and substrate 102 are typically grounded. A high negative voltage on the order of -8 volts, for example, is applied to memory gate 110. The bias conditions between memory gate 110 and region 106 generate holes through band to band tunneling. The generated holes are sufficiently energized by the strong electric field under memory gate 110 and are injected upwards into charge trapping dielectric 114. The injected holes effectively erase the memory cell 100 to the "low" bit state.

[0020] In order to "read" the stored bit of memory cell 100, a low voltage in the range between zero and 3 volts, for example, is applied to each of select gate 108, memory gate 110, and region 104, while region 106 and substrate 102 are typically grounded. The low voltage applied to memory gate 110 is chosen so that it lies substantially equidistant between the threshold voltage necessary to turn on the transistor when storing a "high" bit and the threshold voltage necessary to turn on the transistor when storing a "low" bit in order to clearly distinguish between the two states. For example, if the application of the low voltage during the "read" operation causes substantial current to flow between regions 104 and 106, then memory cell 100 holds a "low" bit and if the application of the low voltage during the "read" operation does not cause substantial current to flow between regions 104 and 106, then memory cell 100 holds a "high" bit.

[0021] FIG. 2 illustrates an example circuit diagram 200 of memory cell 100 including connections to various metal layers in a semiconductor device. Only a single memory cell 100 is illustrated, however, as evidenced by the ellipses in both the X and Y direction, an array of memory cells may be connected by the various lines running in both the X and Y directions. In this way, one or more memory cells 100 may be selected for reading, writing, and erasing bits based on the bit line (BL) and source line (SL) used.

[0022] An example source line (SL) runs along the X direction and is formed in a first metal layer (M1). The source line (SL) may be used to make electrical connection with doped region 106 of each memory cell 100 along a row extending in the X direction.

[0023] An example bit line (BL) runs along the Y direction and is formed in a second metal layer (M2). Bit line (BL) may be used to make electrical connection with doped region 104 of each memory cell 100 along a column extending in the Y direction.

[0024] It is to be understood that the circuit connections shown in FIG. 2 are only exemplary and that the various connections could be made in different metal layers than those illustrated. Furthermore, although not depicted, memory cells 100 may be arrayed in the Z direction as well formed within multiple stacked layers.

[0025] There is commonly a need to provide advanced logic components (e.g., microcontrollers) with support memory components, typically implemented using memory cells, such as memory cells 100. Generally, two approaches exist for providing the memory components. One approach includes fabricating the advanced logic components and the memory components on separate semiconductor chips and interfacing the separate chips via a communication interface, resulting in a non-monolithic design. Another approach includes integrating the advanced logic and the memory components on the same semiconductor chip, in what is known as an embedded memory design. Generally, an embedded memory design is favored over a non-monolithic design for speed and power consumption considerations, but requires an integration process for fabricating the advanced logic components and the memory components on the same semiconductor chip.

[0026] FIG. 3 illustrates an example semiconductor device 300 that includes memory and peripheral circuitry embedded in the same substrate. The peripheral circuitry may include advanced logic components as described above. Device 300 is commonly known as a system-on-chip (SOC). In this example, substrate 102 includes a core region 302 and a periphery region 304. Core region 302 includes a plurality of memory cells 100 that may operate similarly to those previously described. It should be understood that the cross-section of FIG. 3 is only exemplary, and that core region 302 and periphery region 304 may be located in any area of substrate 102. Furthermore, core region 302 and periphery region 304 may exist in the same general area of substrate 102.

[0027] Periphery region 304 may include integrated circuit components such as resistors, capacitors, inductors, etc., as well as transistors. In the illustrated embodiment, periphery region 304 includes a plurality of high-voltage transistors 306 and low-voltage transistors 308. High-voltage transistors 306 are capable of handling voltages up to 20 volts, for example, while low-voltage transistors 308 operate at a faster speed, but cannot operate at the same high voltages as high-voltage transistors 306. In an embodiment, low voltage transistors 308 are designed to have a shorter gate length than high voltage transistors 306. High-voltage transistors 306 are commonly characterized as having a thicker gate dielectric 310 than the gate dielectric of low-voltage transistors 308.

[0028] An existing process for integrating a split gate device (e.g., memory cell 100) with a periphery device (e.g., transistor 306 or 308) includes forming simultaneously the select gate (e.g., select gate 108) of the split gate device in a core region of a substrate (e.g., core region 302) and the gate of the periphery device in a periphery region (e.g., periphery region 304) of the substrate; forming a bottom oxide layer, a charge trapping layer, and a blocking dielectric layer over both the core region and the periphery region; forming the memory gate (e.g., memory gate 110) of the split gate device; and then stripping the blocking dielectric layer and the charge trapping layer in the periphery region of the substrate.

[0029] Because the gate of the periphery device is formed at the same time as the select gate of the split gate device, the periphery device gate is exposed to the deposition/growth process steps of the bottom oxide layer, the charge trapping layer, and the blocking dielectric layer as well as to the subsequent removal steps of the blocking dielectric layer and the charge trapping layer. This exposure typically causes narrowing (the length) of the periphery device gate, resulting in significant performance degradation of the resulting periphery device (particularly for short gate devices) as well as undesired process variations across devices.

[0030] Embodiments as further described below provide methods for fabricating a split gate device as well as an integrated method for fabricating a split gate device and a periphery device. In an embodiment, the split gate device is a charge trapping split gate device. Embodiments do not suffer from the above described problems of the existing integration process. FIGs. 4A-J are cross sectional views illustrating various exemplary steps of a fabrication method according to an embodiment.

[0031] A description of the fabrication method begins with reference to FIG. 4A, which shows a substrate 402 (e.g., silicon substrate) having device isolation trench (e.g., shallow trench isolation (STI)) formations 408 created in substrate 402, a pad oxide layer

404 disposed over substrate 402, and a silicon nitride layer 406 disposed over pad oxide layer 406.

[0032] Commonly, the cross section illustrated in FIG. 4A is obtained by first disposing a pad oxide layer 404 over substrate layer 402, followed by silicon nitride layer 406. Pad oxide layer 404, silicon nitride layer 406, and substrate 402 are then patterned and etched to form trenches, which are then filled with an oxide (e.g., STI oxide) to form trench formations 408. Subsequently, in steps not shown in FIG. 4A, silicon nitride layer 406 and pad oxide layer 404 are removed (e.g. wet etched), and a gate oxide layer (thin and/or thick) is grown from substrate 402.

[0033] In some cases, the removal step of pad oxide layer 404 also causes degradation of the trench formations 408 (which typically are oxide also) at the regions illustrated by the numeral 440 in FIG. 4A. As a result, when the gate oxide layer is subsequently grown from substrate 402, the gate oxide layer will be thinner near the regions 440 than in other regions of the substrate. This variation in gate oxide thickness is particularly problematic when a thick gate oxide is grown from substrate 402, and can result in the gate of a subsequently formed device to break down at regions 440 under high voltage conditions.

[0034] In an embodiment, to remedy this problem, trench formations 408 are formed after the gate oxide layer (thin and/or thick) is grown from substrate 402. As such, in this embodiment, a thick gate oxide layer (and optionally a thin gate oxide layer) is grown from a respective region of substrate 402 before silicon nitride layer 406 is disposed over substrate 404. Silicon nitride layer 406, the gate oxide layer (where grown), and substrate 402 are then patterned and etched to form trenches, which are then filled with an oxide (e.g., STI oxide) to form trench formations 408. Silicon nitride layer 406 is then removed.

[0035] Referring now to FIG. 4B, a thin gate oxide layer 410 and a thick oxide layer 412 are disposed over respective regions of substrate 402. As described above, in an embodiment, thin gate oxide layer 410 and thick gate oxide layer 412 are created before forming trench formations 408. In an embodiment, to create thin gate oxide layer 410 and thick gate oxide layer 412, a gate oxide layer having a thickness appropriate for desired high voltage applications is first grown from substrate 402, then the gate oxide layer is etched to form thin gate oxide layer 410 and thick gate oxide layer 412 where desired over substrate 402.

[0036] Subsequently, a first conductor (e.g., poly) layer 414 is disposed (e.g., deposited) over substrate 402, and a hardmask layer 416 is disposed (e.g., deposited) over first conductor layer 414. In an embodiment, hardmask layer 416 includes a first layer 418 and a second layer 420. First layer 418 and second layer 420 can be any combination of oxide, nitride, or silicon, for example.

[0037] Subsequently, as illustrated in FIG. 4C, a photo resist mask (not shown in FIG. 4C) is selectively created (e.g., using standard lithography steps) over a first region 442 and a second region 444 of substrate 402. In an embodiment, first region 442 corresponds to a core region (e.g., core region 302) where split gate devices are ultimately formed, and second region 444 corresponds to a periphery region (e.g., periphery region 304) where periphery devices are ultimately formed. For simplification purposes, trench formations 408 are not shown in first region 442 in FIG. 4C.

[0038] Hardmask layer 416 (only) is then etched (e.g., dry etched) according to the photo resist mask to form a first hardmask gate pattern over first region 442 and a second hardmask gate pattern over second region 444 of substrate 402. The photo resist mask is then stripped and a wet clean is performed, before another photo resist mask 422 is created to cover second region 444 (or a portion thereof) as shown in FIG. 4C.

[0039] Then, as illustrated in FIG. 4D, first conductor layer 414 is etched (e.g., dry etched) according to the first hardmask gate pattern over first region 442 to form one or more first gates 446 of split gate devices. In an embodiment, the first gates 446 correspond to select gates of the split gate devices. It is noted that no photo resist mask over first region 442 is needed to perform the etching of first conductor layer 414 because the first hardmask gate pattern provides a mask equivalent in this case. As a result, however, some of hardmask layer 416 is eroded in first region 442. For example, as shown in FIG. 4D, second layer 420 of hardmask layer 416 may be completely eliminated and only some of first layer 418 of hardmask layer 416 may remain after the etching of first conductor layer 414 over first gates 446. In contrast, because second region 444 is protected by photo resist mask 422 as shown in FIG. 4C, hardmask layer 416 is unaffected in second region 444 by the etching of first conductor layer 414. Photo resist mask 422 is then stripped and a wet clean is performed.

[0040] Subsequently, as illustrated in FIG. 4E, a dielectric is formed over the entire substrate 402. Specifically, the dielectric is formed over first gates 446 formed on first region 442 and the second hardmask gate pattern in second region 444. In an embodiment, the dielectric includes one or more dielectric layers. For example, the dielectric may include a silicon nitride layer sandwiched between two silicon dioxide layers to create a three-layer stack collectively and commonly referred to as "ONO." In an embodiment, the silicon nitride layer is used as a charge trapping layer in a charge trapping split gate device. Other charge trapping dielectric may also be used including a silicon-rich nitride film, or any film that includes, but is not limited to, silicon, oxygen, and nitrogen in various stoichiometries.

[0041] In an embodiment, as shown in FIG. 4E, the dielectric includes a bottom oxide layer 424, a nitride layer 426, and a top oxide layer 428. To form the dielectric, bottom oxide layer 424 is grown over the entire substrate 402. In an embodiment, as shown in FIG. 4E, bottom oxide layer 424 may grow minimally or may not grow over regions of substrate 402 topped by hardmask material. Then, nitride layer 426 is formed (e.g., deposited) over bottom oxide layer 424, and top oxide layer 428 is formed (e.g., grown or deposited) over nitride layer 426.

[0042] Then, as illustrated in FIG. 4F, a second conductor (e.g., poly) layer is disposed (e.g., deposited) over the dielectric over the entire substrate 402. A photo resist mask 432 is then created to cover second region 444, and the second conductor layer is etched (e.g., anisotropically dry etched) at region 442 as shown in FIG. 4F. In an embodiment, the second conductor layer is etched until top oxide layer 428 of the dielectric is exposed. As such, the etching of the second conductor layer results in first and second formations 430 of the second conductor layer on first and second sidewalls respectively of each first gate 446. Photo resist mask 432 is then stripped and a wet clean is performed.

[0043] Then, as illustrated in FIG. 4G, a photo resist mask 434 is created such that one or the other of first and second formations 430 around each first gate 446 is covered by photo resist mask 434. The second conductor layer is then etched (e.g., dry etched) over the entire substrate 402. The etching of the second conductor layer removes the non-covered formation 430 of each first gate 446. The remaining formation 430 of each first gate 446 corresponds to a second gate (e.g., memory gate) of the split gate device (hereinafter referred to as second gate 430). The etching of the second conductor layer also removes the second conductor layer from second region 444 to re-expose the dielectric.

[0044] Then, as illustrated in FIG. 4H, photo resist mask 434 is stripped, and top oxide layer 428 and nitride layer 426 are removed (e.g., wet etched) from the top surface over the entire substrate 402. Specifically, top oxide layer 428 and nitride layer 426 are removed over a top surface of each first gate 446 to expose any remaining hardmask layer (e.g., remainder of first layer 418 of the hardmask layer) over the top surface of first gate 446. In another embodiment, no hardmask layer remains over the top surface of first gate 446 at this step and first conductor layer 414 of first gate 446 is exposed. Over second region 444, the removal of top oxide layer 428 and nitride layer 426 exposes the hardmask layer 416 with its first layer 418 and second layer 420.

[0045] At this point in the process, the split gate device has been formed, with a first gate 446 (provided by first conductor layer 414) and a second gate 430 (provided by second conductor layer formation 430), and with a dielectric provided by bottom oxide layer 424, nitride layer 426, and top oxide layer 428 to separate the inner facing sidewalls of the first and second gates. However, the periphery device has not yet been formed, with only the second hardmask gate pattern having been formed over second region 444 and first conductor layer 414 still unpatterned.

[0046] Then, as illustrated in FIG. 4I, a photo resist mask 436 is formed to cover first region 442. In an embodiment, photo resist mask 436 extends slightly onto second region 444 as shown in FIG. 4I. First conductor layer 414 is then etched according to the second hardmask gate pattern over second region 444 to form periphery device gates 448. It is noted that no photo resist mask over second region 444 is needed to perform the etching of first conductor layer 414 because the second hardmask gate pattern provides a mask equivalent in this case. As a result, however, some of hardmask layer 416 is eroded in second region 444. For example, as shown in FIG. 4I, second layer 420 of hardmask layer 416 may be completely eliminated and only some of first layer 418 of hardmask layer 416 may remain after the etching of first conductor layer 414 over periphery device gates 448.

[0047] Then, as illustrated in FIG. 4J, photo resist mask 436 is stripped and a wet clean is performed, before a spacer layer is formed (e.g., disposed) over the entire substrate 402. The spacer layer may include an oxide layer and/or a nitride layer. The spacer layer is then etched (e.g., anisotropically dry etched) to form first and second spacers 438 on respective sidewalls of the split gate device. A third spacer 450 is also formed over first gate 446 by the etching of the spacer layer. Third spacer 450 covers a portion of the inner sidewall of second gate 430 that extends above the top surface of the first gate.

[0048] Finally, a silicide layer 440 is formed. In an embodiment, silicide layer 440 is formed by depositing a metal over the entire substrate 402 and then exposing the wafer to temperatures that promote a chemical reaction between the metal and any exposed silicon to form a silicide. Silicide layer 440 thus forms on top of first gate 446, second gate 430, and over exposed regions of substrate 402 as shown in FIG. 4J. In an embodiment, silicide layer 440 is configured to lower the resistance of first gate 446 and second gate 430, making them faster to read, write, or erase.

[0049] As described above, the FIGs. 4A-J represent only exemplary steps of an integrated method for fabricating a split gate device and a periphery device according to an embodiment. These exemplary steps are provided for the purpose of illustration and are not limiting of embodiments. As would be understood by a person of skill in the art based on the teachings herein, a method according to embodiments may include fewer or more steps than described above and any of the steps described above can be performed in a variety of other ways as would be apparent to a person of skill in the art.

[0050] FIG. 5 is a cross sectional view of an example split gate device 500 according to an embodiment. Example split gate device 500 is provided for the purpose of illustration and is not limiting of embodiments. Example split gate device 500 can be realized using the process described above in FIGs. 4A-4J, whereby a periphery device is also formed together with example split gate device 500. Alternatively, example split gate device 500 can be realized using a process that results in a standalone split gate device.

[0051] As shown in FIG. 5, example split gate device 500 is formed over a substrate 502 having first and second doped regions 524 and 526. Split gate device 500 includes a first gate 504 (e.g., select gate); a second gate 506 (e.g., memory gate); and a dielectric (made of three layers 508, 510, and 512) having a first portion disposed between second gate 506 and substrate 502 and a second portion disposed along an inner sidewall of first gate 504 to separate select gate 504 from memory gate 506.

[0052] In an embodiment, first gate 504 and second gate 506 are made from first and second poly materials, which may or may not be the same. The dielectric may include one or more dielectric layers. For example, the dielectric may be of the ONO type, which includes a silicon nitride layer sandwiched between two silicon dioxide layers. In an embodiment, the silicon nitride layer is used as a charge trapping layer resulting in split gate device 500 being a charge trapping split gate device. Other charge trapping dielectric may also be used including a silicon-rich nitride film, or any film that includes, but is not limited to, silicon, oxygen, and nitrogen in various stoichiometries.

[0053] Split gate device 500 also includes first and second silicide layers 516 and 514 disposed over first gate 504 and second gate 506 respectively; first and second spacers 520 and 518 disposed along the outer sidewalls of first gate 504 and second gate 506 respectively; and a third spacer 522 formed over first gate 504 along the inner sidewall of second gate 506. Third spacer 522 covers a portion of the inner sidewall of second gate 506 that extends above a top surface of first gate 504. According to embodiments, third spacer 522 can be formed due to the fact that second gate 506 is greater in height than first gate 504 and that first gate 504 has a flat surface (rather a sloped surface like second gate 506). Third spacer 522 prevents silicide layers 514 and 516 from coming in contact with each other when formed (which can result in first gate 504 and second gate 506 forming a short-circuit).

[0054] Embodiments have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0055] The foregoing description of the specific embodiments will so fully reveal the general nature of the disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0056] The breadth and scope of embodiments of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method of fabricating a split gate device, comprising:

disposing a first conductor layer over a substrate;

disposing a hardmask layer over the first conductor layer;

etching the hardmask layer to form a first hardmask gate pattern over a first region of the substrate and a second hardmask gate pattern over a second region of the substrate;

etching the first conductor layer according to the first hardmask gate pattern to form a first gate of the split gate device;

forming a dielectric over the first gate and the second hardmask gate pattern;

disposing a second conductor layer over the dielectric; and

etching the second conductor layer to form a second gate of the split gate device.

2. The method of claim 1, further comprising:

etching the first conductor layer according to the second hardmask gate pattern to form a gate of a periphery device.

3. The method of claim 2, wherein the etching of the first conductor layer according to the first hardmask gate pattern and the etching of the first conductor layer according to the second hardmask gate pattern are performed at different times.

4. The method of claim 2, wherein the etching of the first conductor layer according to the first hardmask gate pattern is performed before the etching of the first conductor layer according to the second hardmask gate pattern.

5. The method of claim 2, wherein etching the first conductor layer according to the first hardmask gate pattern to form the firstgate of the split gate device comprises:

forming a photo resist mask over the second region only of the substrate

6. The method of claim 2, wherein etching the first conductor layer according to the second hardmask gate pattern to form the gate of the periphery device comprises:

forming a photo resist mask over the first region only of the substrate.

7. The method of claim 2, wherein the first gate and the second gate of the split gate device are formed before the gate of the periphery device.

8. The method of claim 1, wherein etching the first conductor layer according to the first hardmask gate pattern to form the first gate of the split gate device comprises:

forming a photo resist mask over the second region only of the substrate.

9. The method of claim 1, further comprising:

growing a thick oxide layer over the substrate;

forming a device isolation trench in the substrate after growing the thick oxide layer over the substrate; and

forming a high voltage periphery device using the thick oxide layer as a gate oxide of the high voltage periphery device.

10. The method of claim 1, wherein etching the second conductor layer to form the second gate of the split gate device comprises:

etching the second conductor layer to create first and second formations of the second conductor layer on first and second sidewalls respectively of the first gate;

forming a photo resist mask over the first formation; and

etching the conductor layer to remove the second formation,

wherein the first formation corresponds to the second gate of the split gate device.

11. The method of claim 1, further comprising:

forming a spacer over the first gate, the spacer covering a portion of an inner sidewall of the second gate that extends above a top surface of the first gate.

12. The method of claim 1, wherein forming the dielectric comprises:

forming a bottom oxide layer over the first gate, an exposed region of the substrate, and the second hardmask pattern;

forming a nitride layer over the bottom oxide layer; and

forming a top oxide layer over the nitride layer.

13. The method of claim 12, further comprising:

removing the top oxide layer and the nitride layer from a top surface of the first gate of the split gate device.

14. The method of claim 1, further comprising:

forming first and second spacers on first and second sidewalls on the split gate device.

15. The method of claim 1, further comprising:

forming a silicide layer over the first gate and the second gate.

16. An integrated method for fabricating a split gate device and a periphery device, comprising:

etching a hardmask layer to form a first hardmask gate pattern over a first region of a substrate and a second hardmask gate pattern over a second region of the substrate;

etching a first conductor layer according to the first hardmask gate pattern to form a first gate of the split gate device;

forming a dielectric over the first gate and an exposed region of the substrate;

forming a second conductor layer over the dielectric;

etching the second conductor layer to form a second gate of the split gate device; and

etching the first conductor layer according to the second hardmask gate pattern to form a gate of the periphery device.

17. The method of claim 16, further comprising:

disposing the first conductor layer over the substrate; and

disposing the hardmask layer over the first conductor layer.

18. The method of claim 16, wherein the etching of the first conductor layer according to the first hardmask gate pattern and the etching of the first conductor layer according to the second hardmask gate pattern are performed at different times..

19. The method of claim 16, wherein the etching of the first conductor layer according to the first hardmask gate pattern is performed before the etching of the first conductor layer according to the second hardmask gate pattern.

20. A split gate device, comprising:

first and second doped regions formed in a substrate;

a select gate disposed over the substrate;

a memory gate disposed over the substrate;

a dielectric having a first portion disposed between the memory gate and the substrate and a second portion disposed along a sidewall of the select gate to separate the select gate from the memory gate;

first and second silicide layers disposed over the select gate and the memory gate respectively; and

a spacer formed over the select gate along a sidewall of the memory gate, the spacer covering a portion of the sidewall of the memory gate that extends above a top surface of the select gate.

21. The split gate device of claim 20, wherein a height of the memory gate is greater than a height of the select gate.

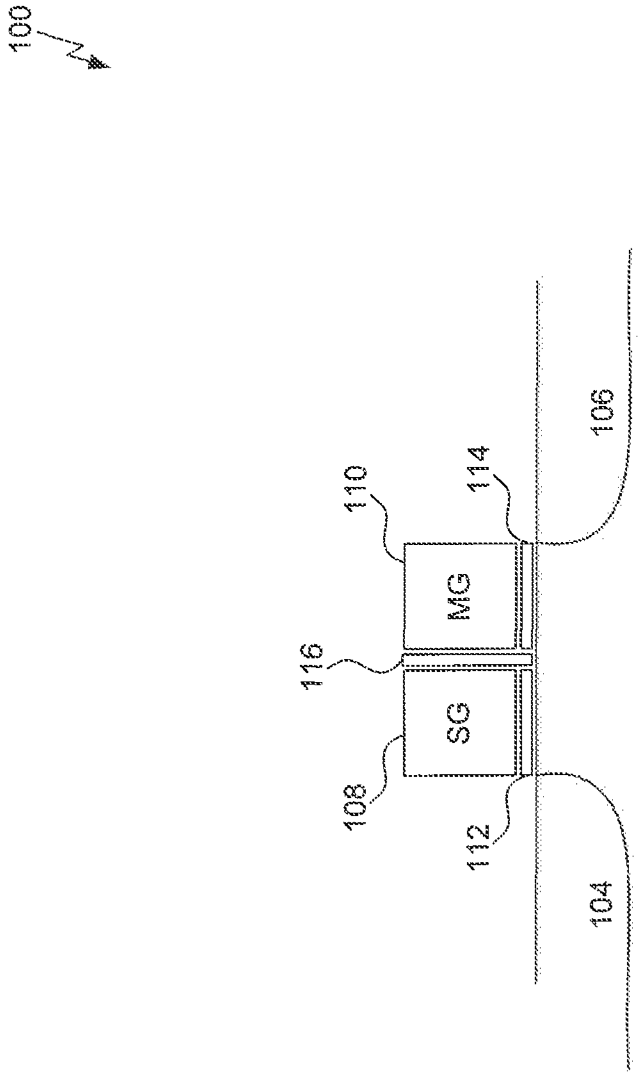

FIG. 1

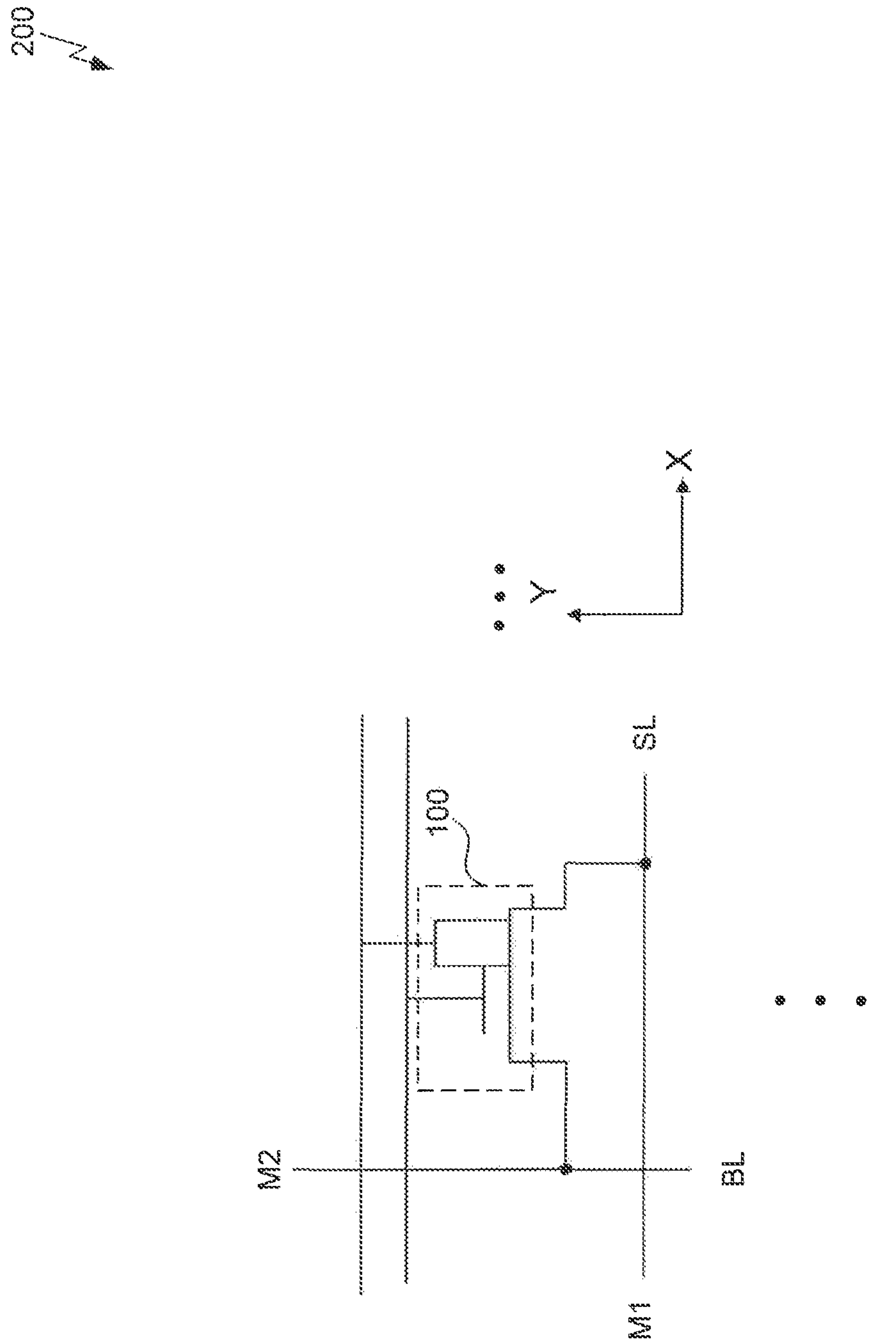

FIG. 2

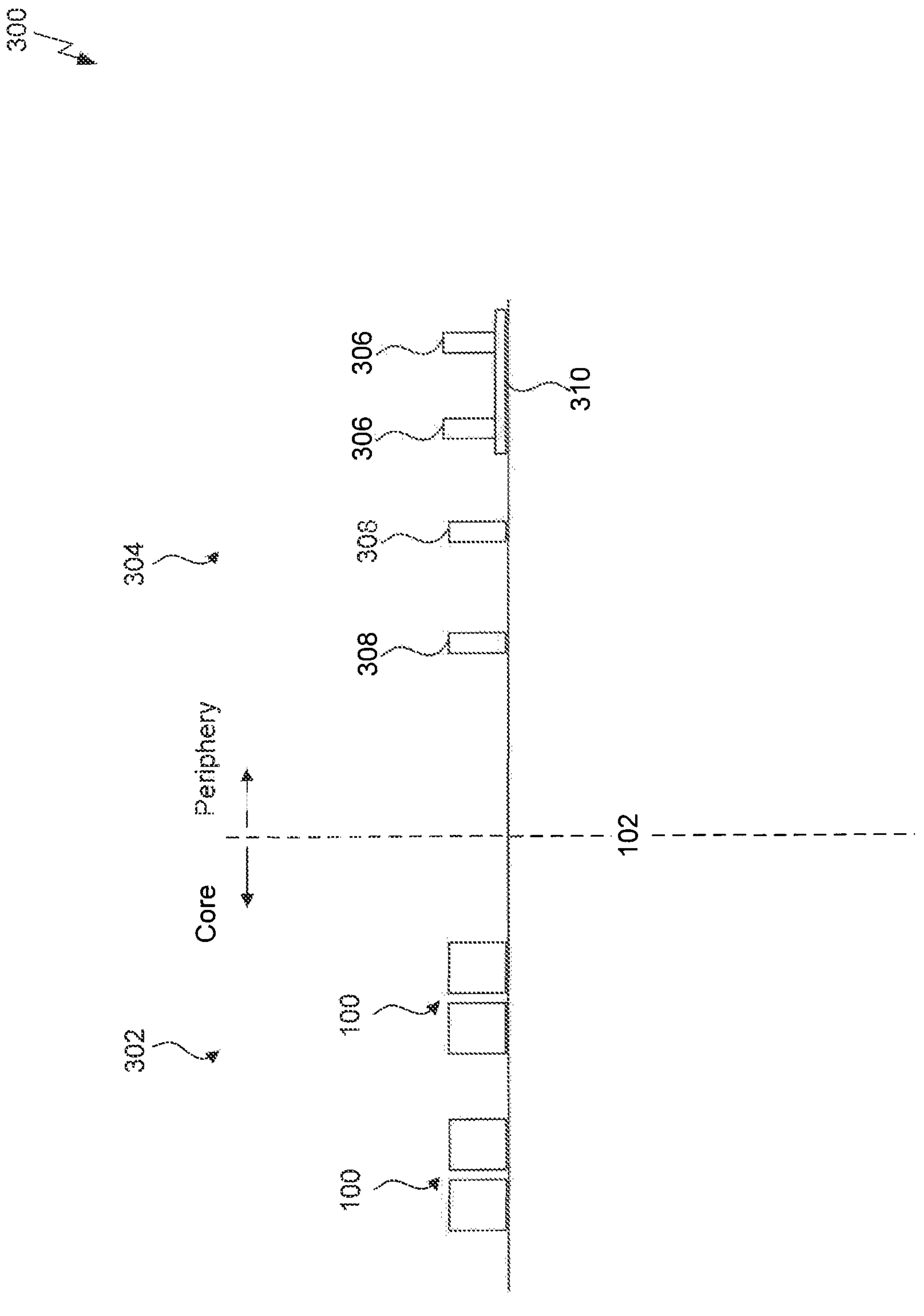

FIG. 3

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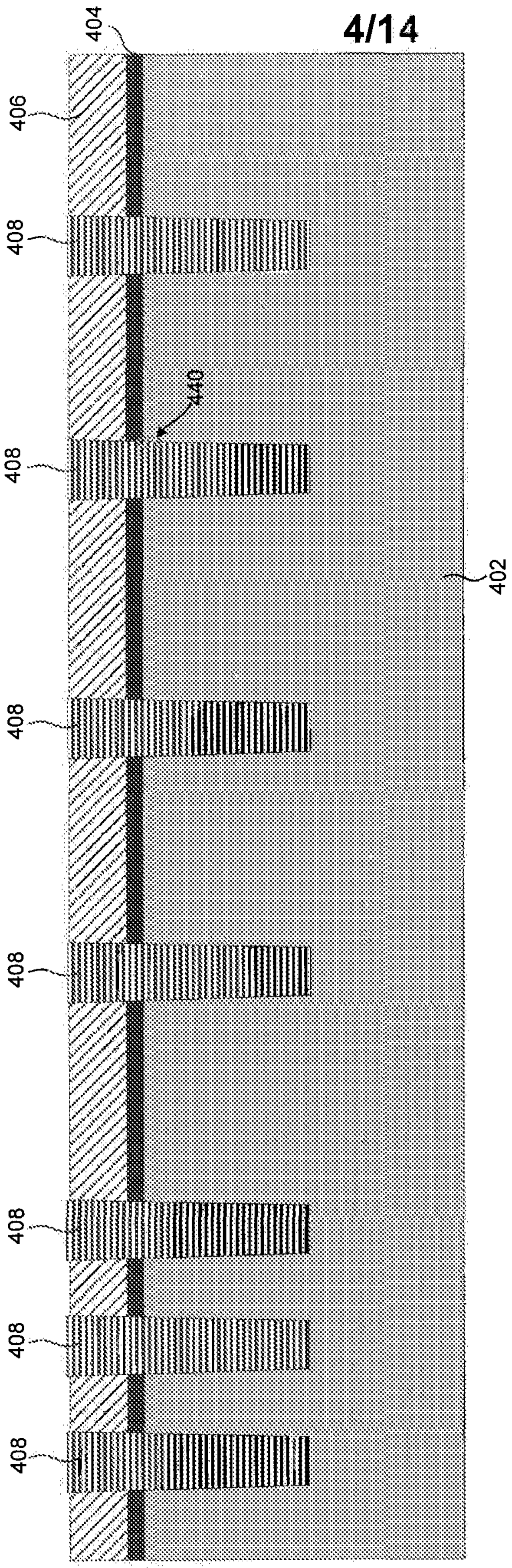

FIG. 4A

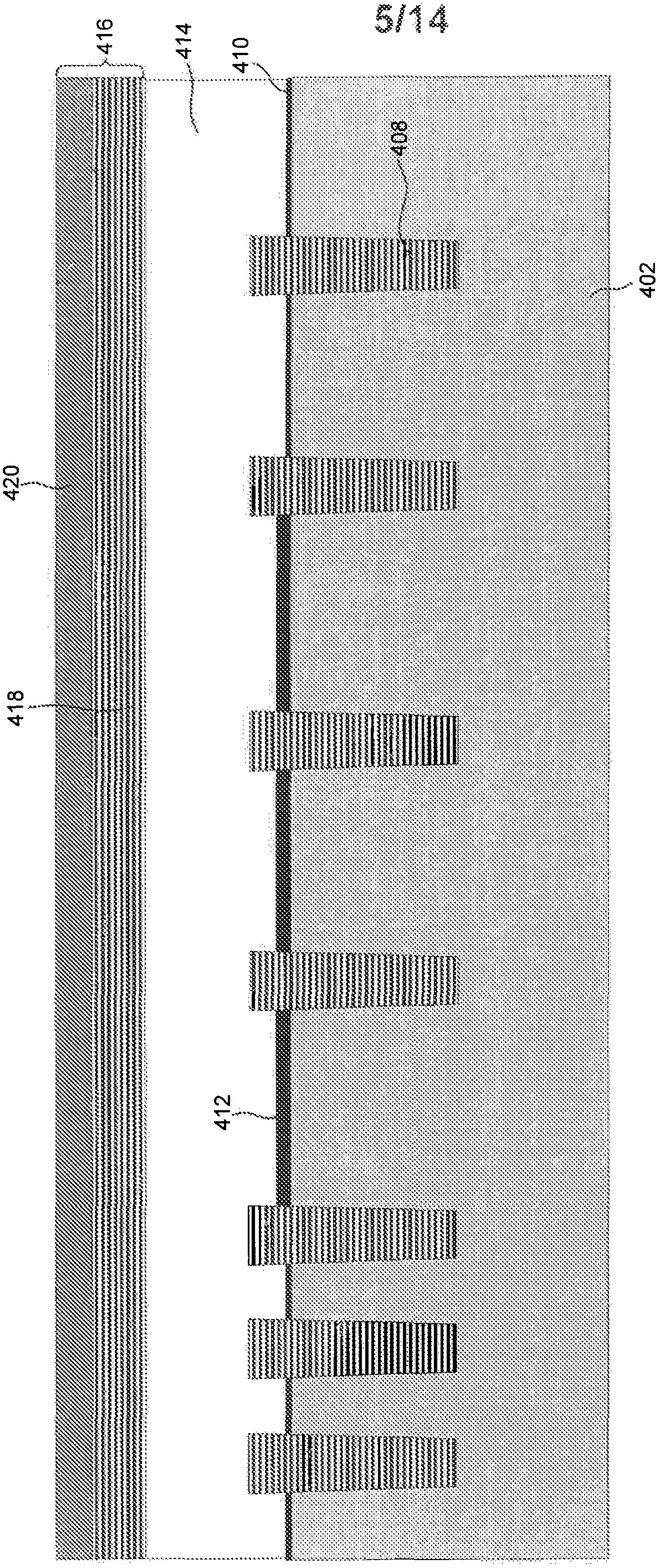

FIG. 4B

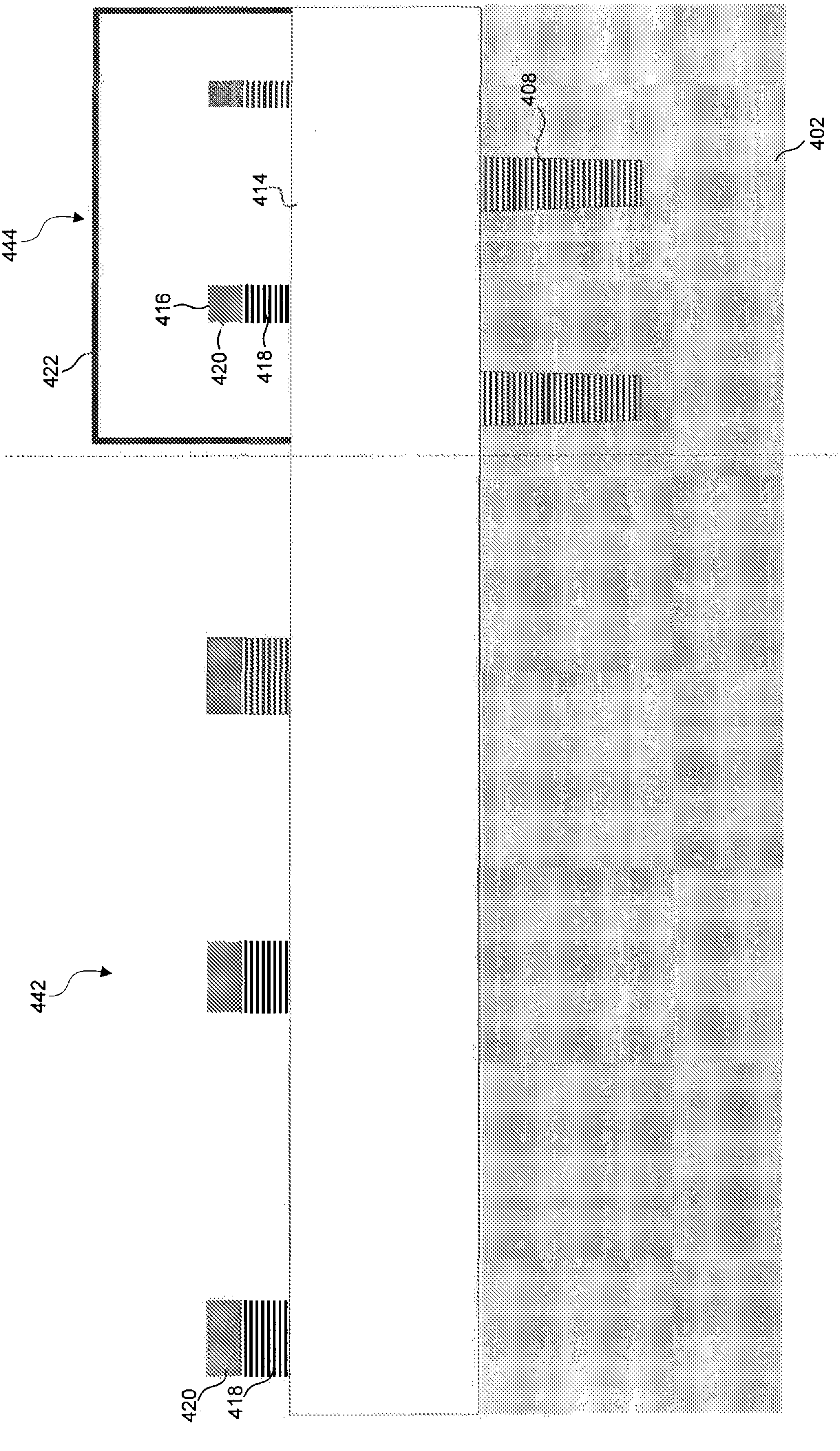

FIG. 4C

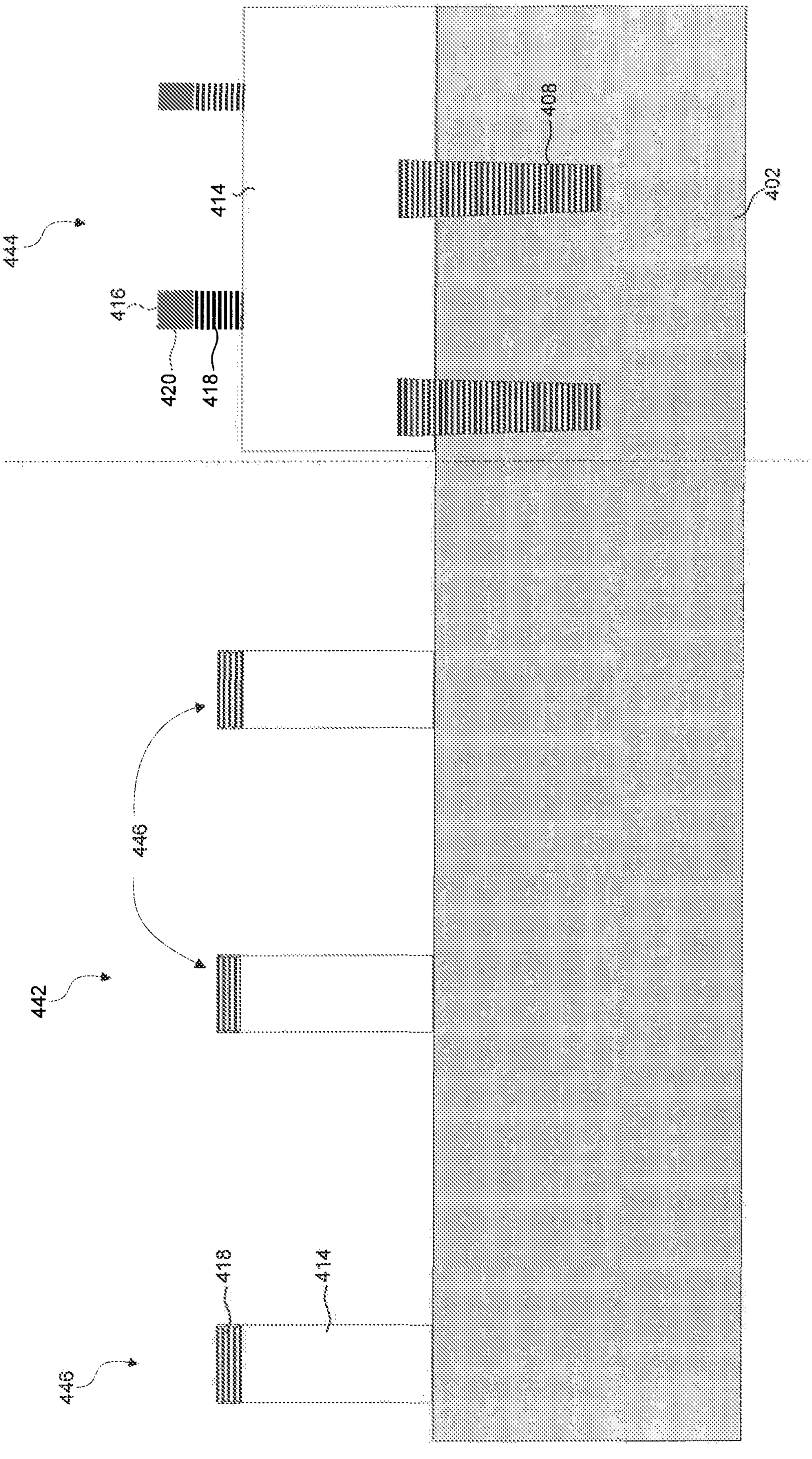

FIG. 4D

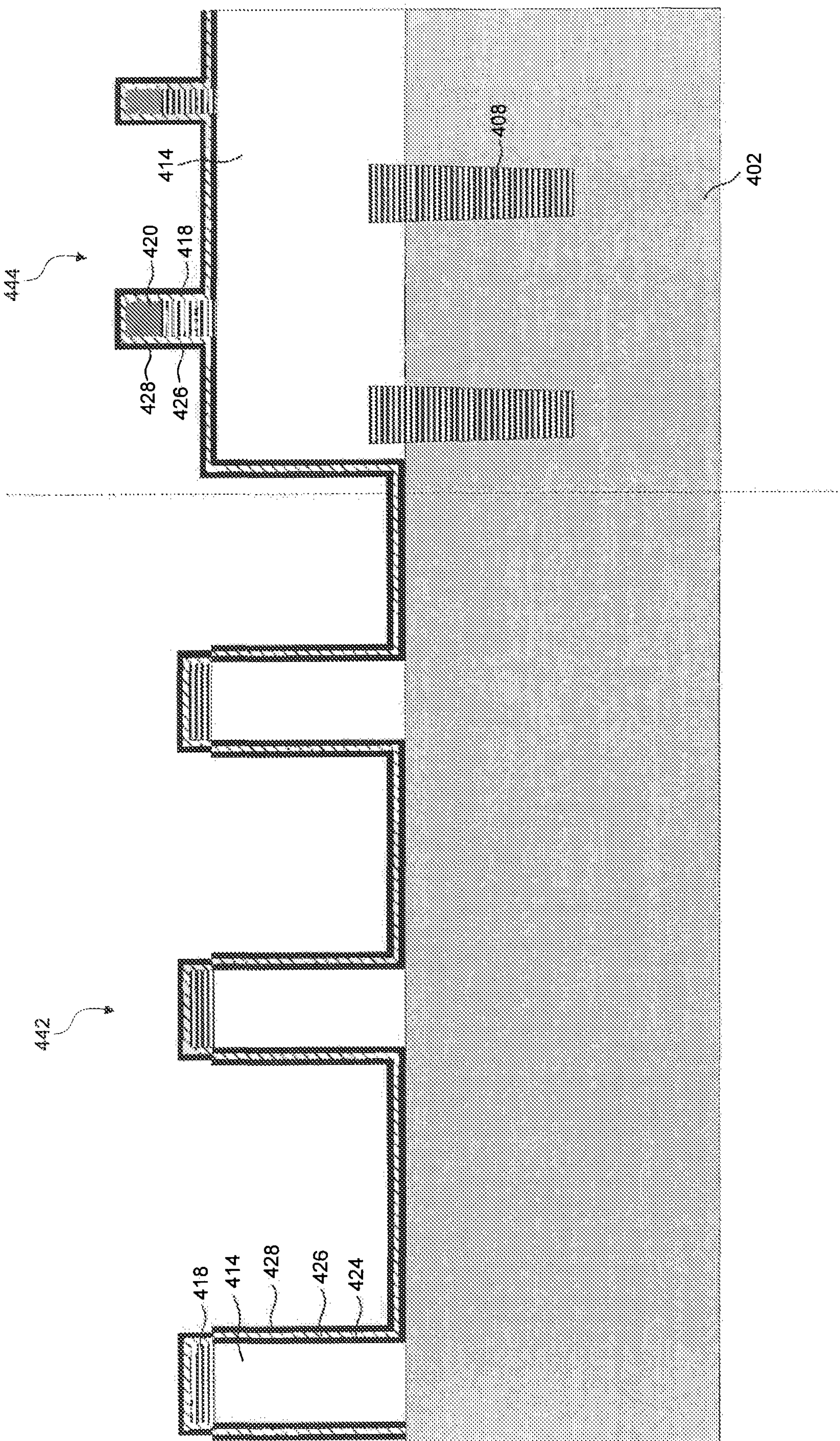

FIG. 4E

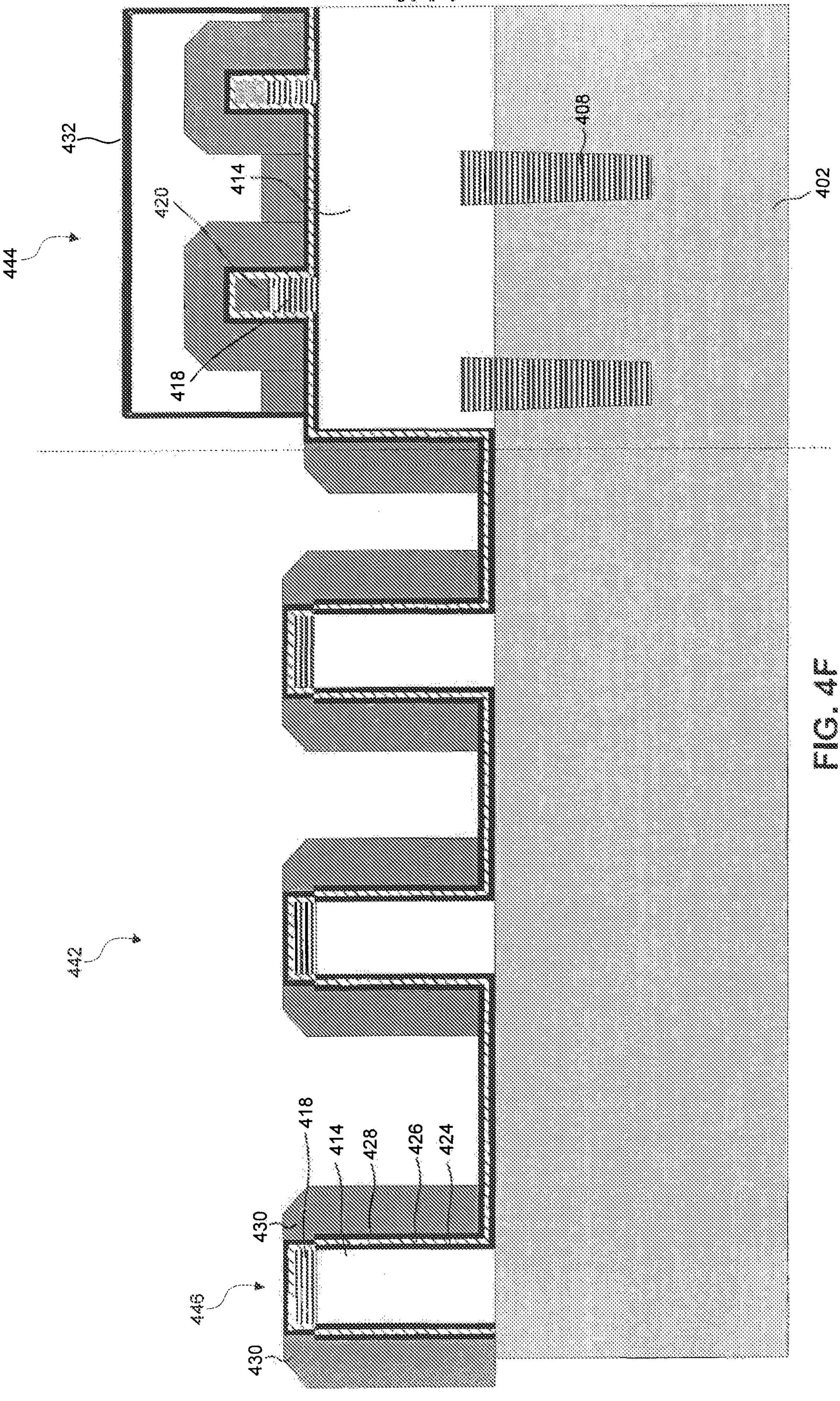

FIG. 4F

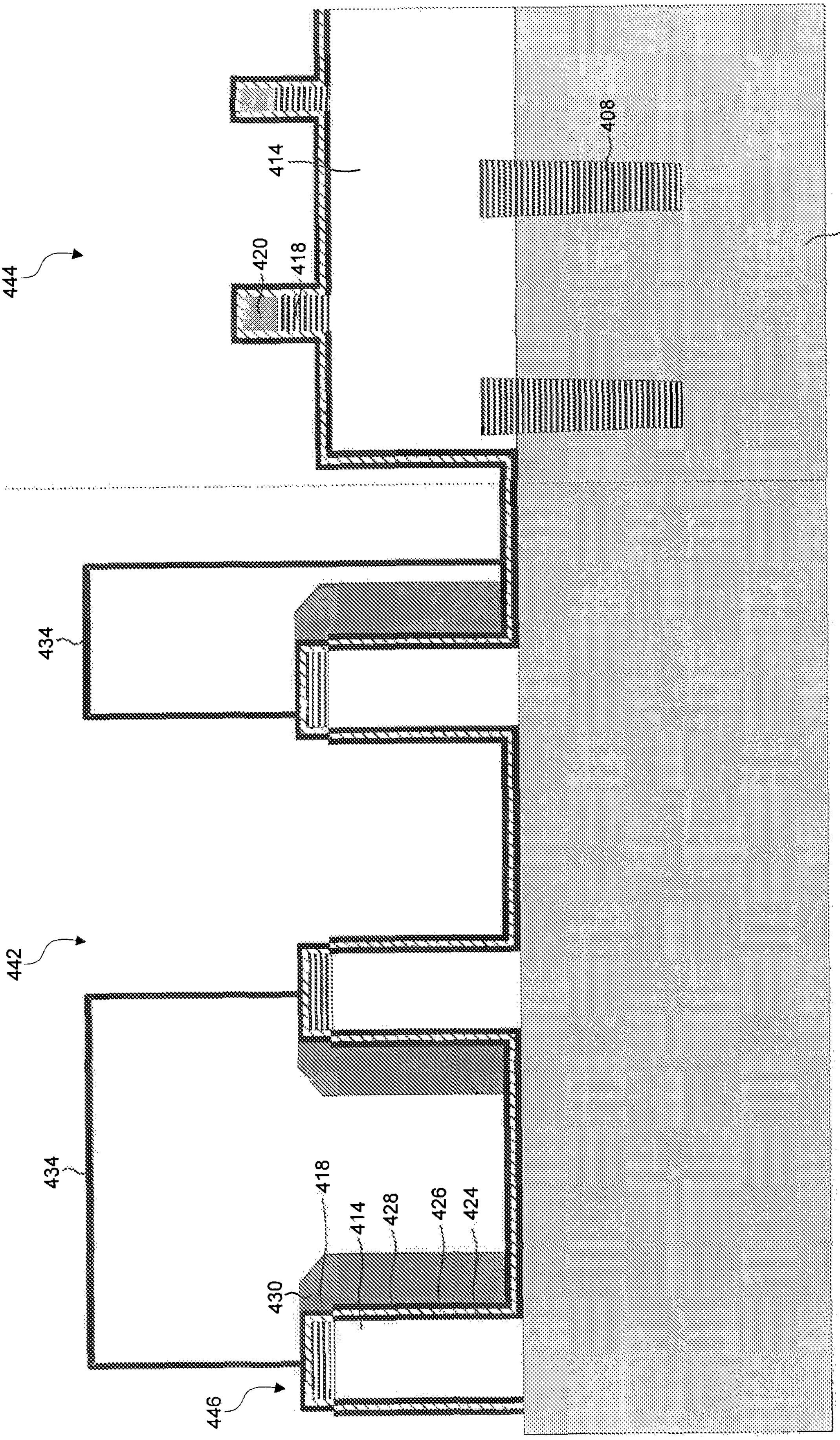

FIG. 4G

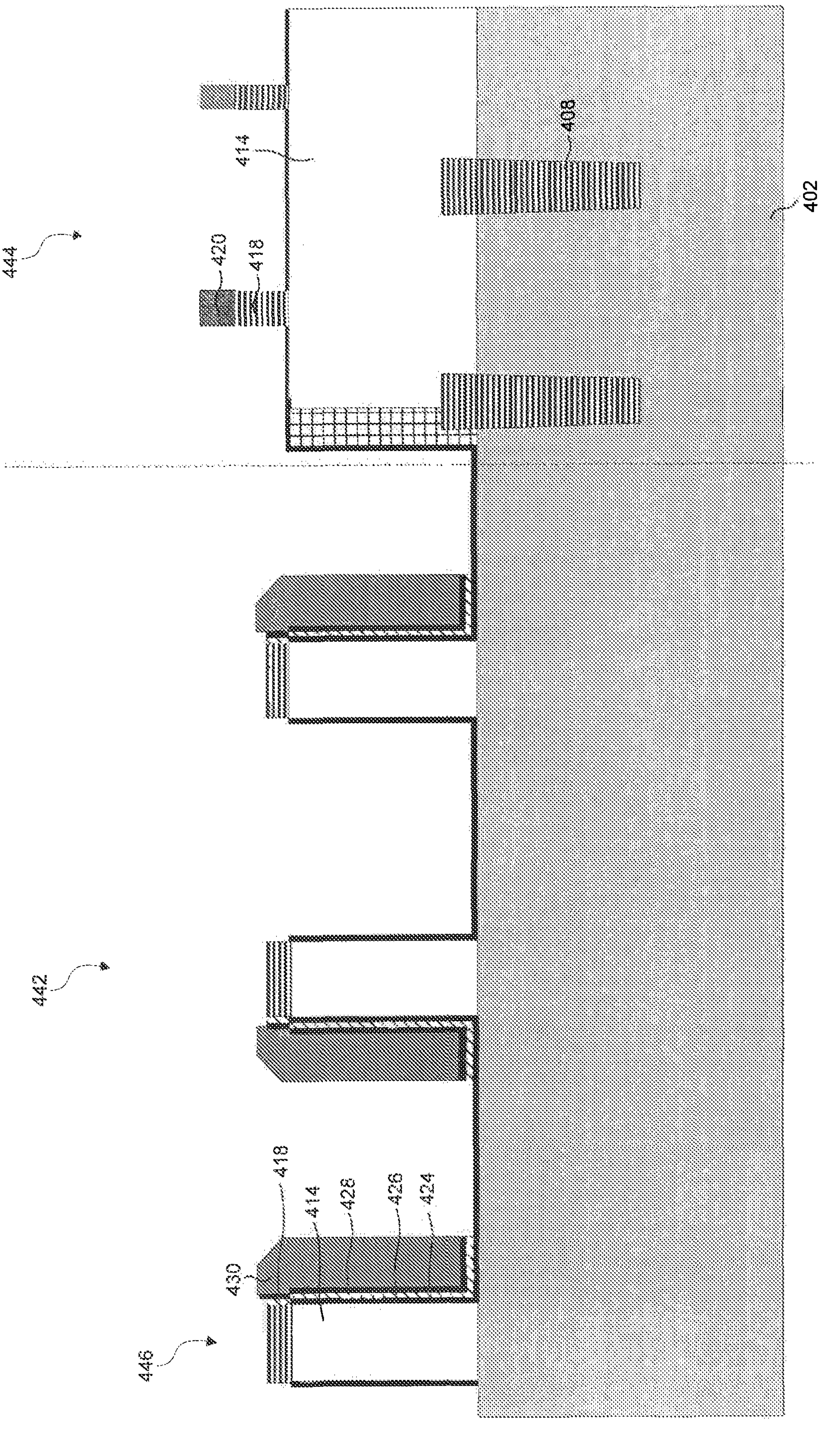

FIG. 4H

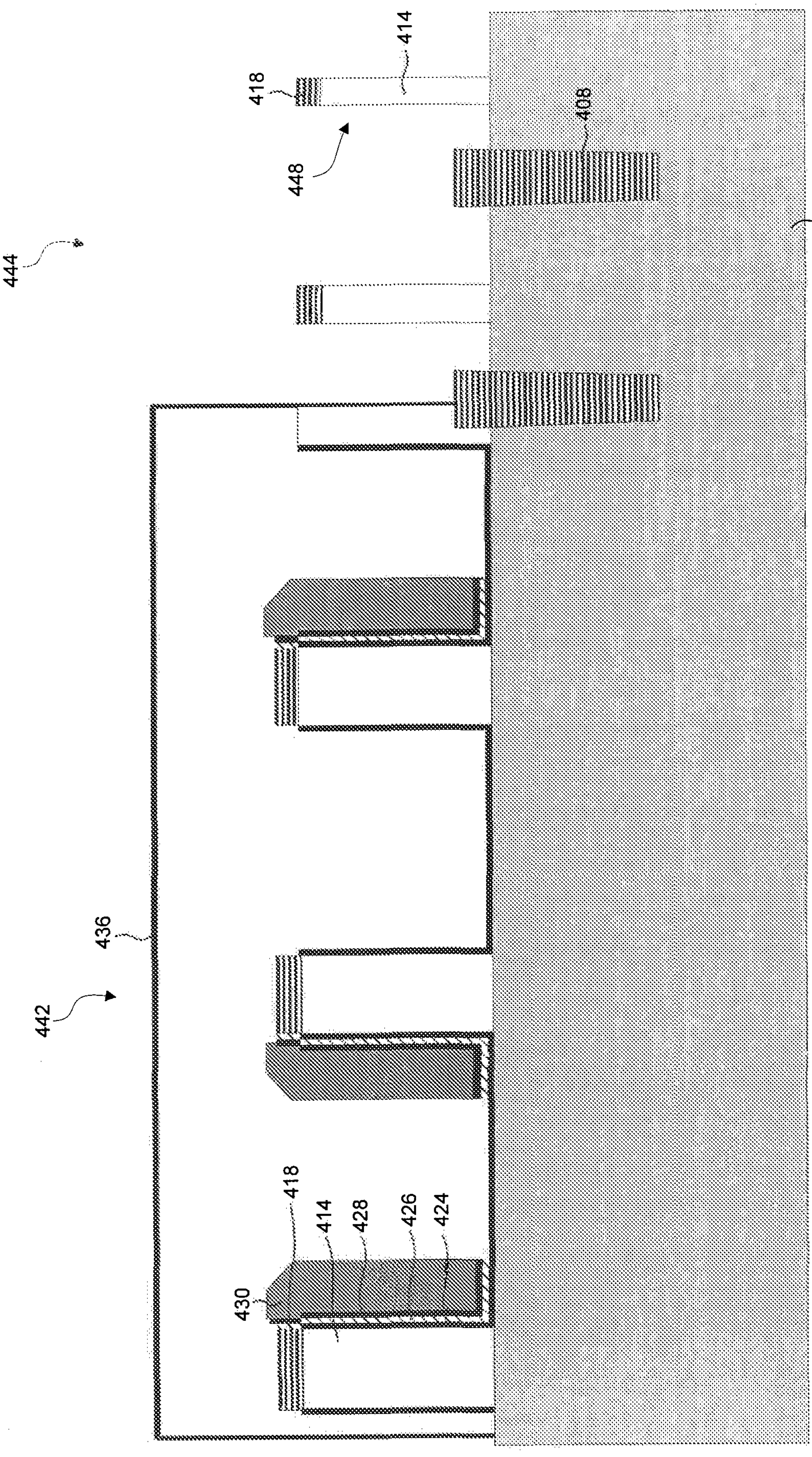

FIG. 4I

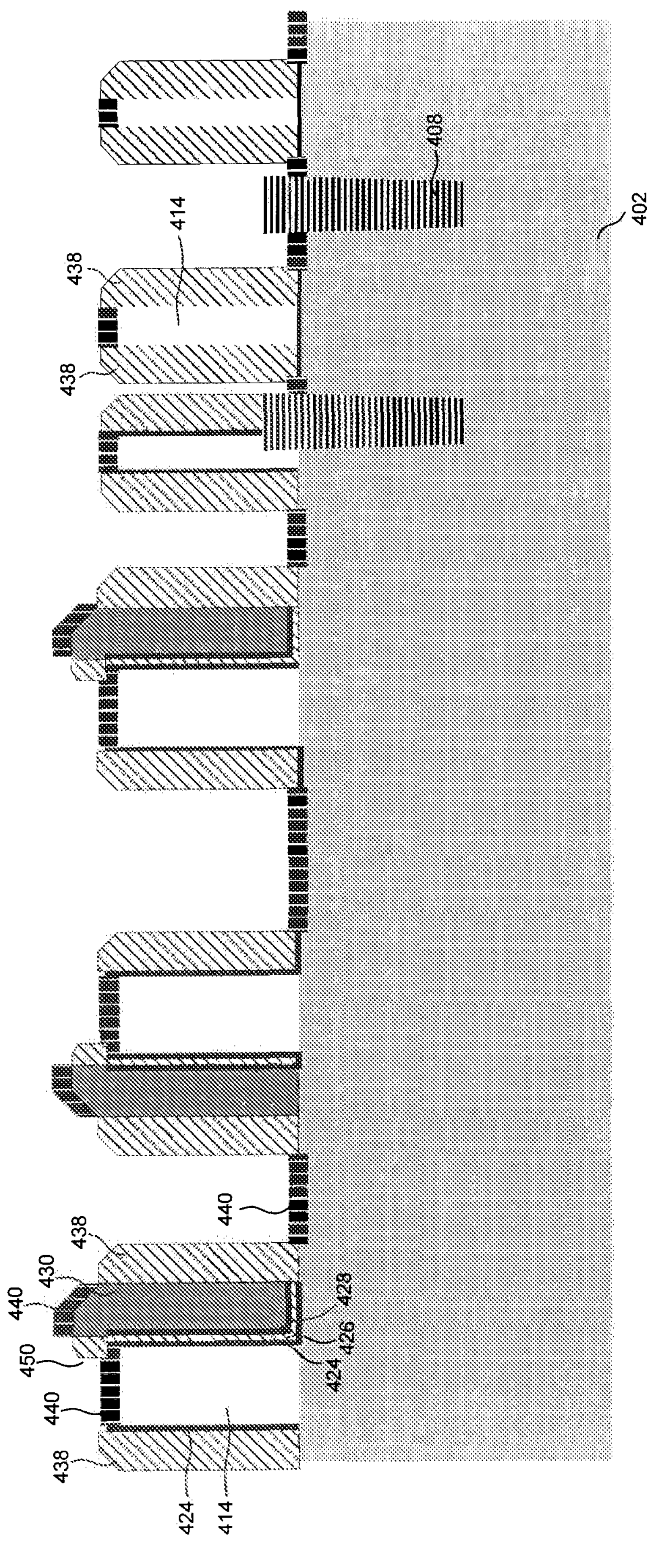
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FIG. 4J

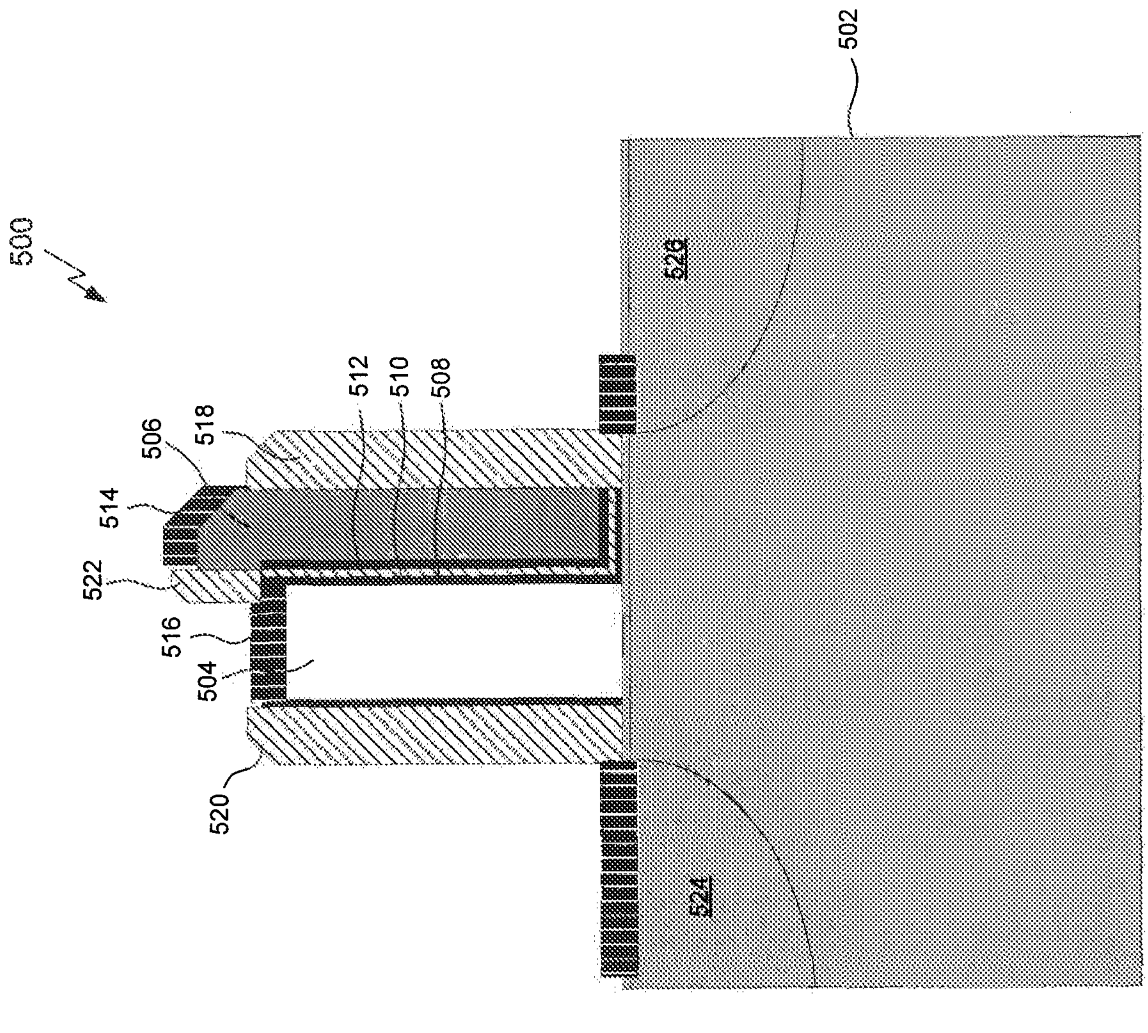

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/074724

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/115; H01L 21/336; H01L 29/94; H01L 29/76; H01L 21/8247; H01L 29/788

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: gate, select, memory, split, mask, dielectric

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2011-0095348 A1 (HIRAKU CHAKIHARA et al.) 28 April 2011 See abstract, paragraphs [0183], [0230]-[0259] and figures 8-23.	1-10,12-19 11
X Y	US 2007-0218633 A1 (ERWIN PRINZ et al.) 20 September 2007 See abstract, paragraphs [0028]-[0032], [0034], [0038]-[0040], [0052] and figures 1-5, 7, 9-11.	20-21 11
A	US 2007-0145455 A1 (KAN YASUI et al.) 28 June 2007 See abstract, paragraphs [0058]-[0067] and figures 13-22.	1-21
A	US 2009-0108325 A1 (SUNG-TAEG KANG et al.) 30 April 2009 See abstract, paragraphs [0009]-[0020] and figures 1-11.	1-21
A	KR 10-2010-0080226 A (DONGBU HITEK CO., LTD.) 08 July 2010 See abstract, paragraphs [0035]-[0075] and figures 1a-9.	1-21

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 April 2014 (24.04.2014)	**24 April 2014 (24.04.2014)**

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INTERNATIONAL SEARCH REPORT
Information on patent family members

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