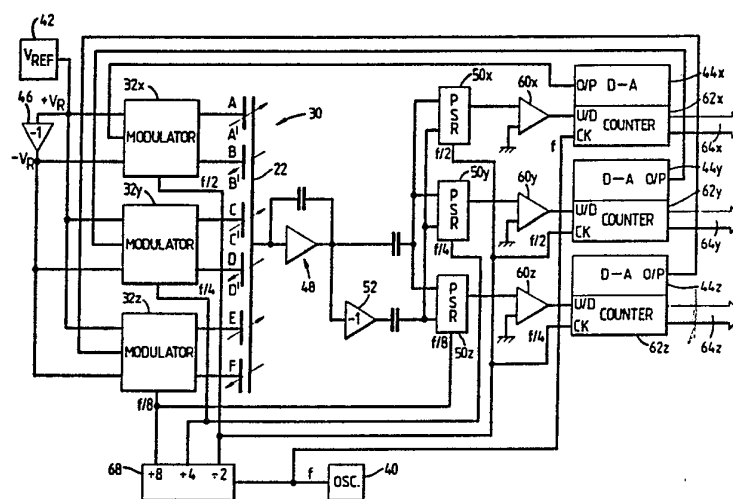




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(54) Title: CAPACITIVE TRANSDUCERS



(57) Abstract

A signal conditioning circuit for multiple channel capacitive displacement transducers. The transducer (30) comprises three differential capacitive transducers, driven by respective square waves from modulators (32x, 32y, 32z). The modulators are driven at different frequencies which are even multiples of each other, derived from a divider (68). The signals from each differential capacitance pair of the transducer (30) are received by a common charge amplifier (48). They are then demodulated by respective phase sensitive rectifiers (50x, 50y, 50z), each of which is driven at the same frequency as the corresponding modulator. The outputs of the phase sensitive rectifiers are integrated, e.g. by circuits (60, 62, 44) for one of the channels, and the resulting voltage signal is fed back to the corresponding modulator so as to tend to null the input to the charge amplifier (48). The use of modulating frequencies which are even multiples of each other enables the signals to be multiplexed through a single charge amplifier (48). The mechanical construction of the multi-channel transducer (30) is also described.

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**CAPACITIVE TRANSDUCERS**

This invention relates to capacitive transducers, for  
5 example for use in displacement-responsive devices.

Capacitive displacement transducers are known for use in  
displacement-responsive devices such as measurement probes  
and joysticks, where a stylus or lever is movable in the  
10 directions of two or more orthogonal axes. Normally there  
would be one or more separate capacitive transducers for  
each axis of movement. Each such transducer comprises at  
least a pair of capacitor plates which are relatively  
movable. In some known devices, e.g. as shown in  
15 EP 0239337 A, there are three or more capacitor plates in  
each transducer, so that the transducer comprises a  
differential pair of capacitors. Such an arrangement has  
improved performance.

20 In conventional displacement-responsive devices with  
capacitive transducers, the transducer associated with  
each axis has a separate signal processing circuit which  
determines the capacitance of the transducer as the same  
varies with displacement. Such a signal processing  
25 circuit is known from British Patent No. GB 1 366 284, in  
which phase and antiphase AC input signals are applied to  
a differential capacitive transducer, and subsequently  
demodulated synchronously by a phase sensitive rectifier,  
and then integrated. The resulting DC signal is used to  
30 control the differential AC inputs to the transducer so as  
to produce a null output from the transducer, and the size  
of the DC control signal required to do this provides an  
output proportional to displacement. British Patent No.  
GB 2 036 982 B describes similar circuits, and  
35 additionally suggests that differential transducers in  
three channels may be multiplexed together in a  
time-sharing arrangement, so that the demodulation and

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control circuitry may be shared between the three channels. However, such a time-sharing arrangement does not provide a continuous output for each channel.

5 A first aspect of the present invention provides a circuit for providing outputs from at least two capacitive transducers, the circuit comprising:

respective means for each transducer for feeding an alternating input signal thereto;

10 common means for receiving the signals thereby produced from the transducers; and

respective means for each transducer for receiving the output signal from said common means and demodulating the received signal synchronously with the frequency of the

15 respective input signal to that transducer;

wherein the frequencies of said input signals are even harmonics or sub-harmonics of each other.

As noted above, a known capacitive displacement transducer  
20 may comprise three or more plates, arranged as a differential pair of capacitors. Thus, a two axis device normally requires six capacitor plates, and because of the requirements for relative movement of the plates on two separate axes, it follows that each of the six plates  
25 forms a separate sub-assembly of the device. In the case of a three axis device, the situation is even worse because nine capacitor plates are required, each forming an individual sub-assembly. Construction of the device is therefore complicated and relatively expensive.

30

A second aspect of the present invention provides a device which is responsive to displacement in at least two axes, the device comprising a capacitive displacement transducer for each said axis, each transducer including at least two  
35 opposed capacitor electrodes, one electrode of each transducer being common with an electrode of the or each other transducer.

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Preferably the capacitor electrodes of the transducers which are not common are provided on a common printed circuit board. Preferably there are two such printed circuit boards, on opposing sides of the common electrode, giving each transducer a differential arrangement in which the common central electrode is relatively movable between the two outer electrodes on the printed circuit boards.

Examples which incorporate both aspects of the invention will now be described, with reference to the accompanying drawings, wherein:

Fig. 1 is a vertical section through a joystick incorporating capacitance transducers,

Figs. 2 and 3 are sections on the lines II-II and III-III respectively in Fig. 1,

Fig. 4 is a diagrammatic isometric view of the arrangement of electrodes in Figs. 1 to 3,

Fig. 4A is a view corresponding to Fig. 4, but showing an alternative electrode arrangement,

Fig. 5 is a circuit diagram of a signal conditioning system for the transducers for a single axis of movement of the joystick,

Fig. 6 is a circuit diagram of a signal conditioning system for the transducers for three axes of movement,

Fig. 7 is a partial circuit diagram showing a modification of Fig. 5 or Fig. 6, and

Figs 8,9,10 and 11 are circuit diagrams of alternative signal conditioning systems.

Referring firstly to Figs. 1 to 4, the joystick comprises a housing 10 from which projects a control lever 12. The control lever 12 is supported by a spring diaphragm 14 so as to be manually tiltable about axes x and y and translatable along an axis z. The diaphragm 14 exerts a restoring force on the control lever to return it to a null position when no external force is applied. The diaphragm is clamped between clamp rings 16,18 which form

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part of the housing 10.

The control lever 12 may be provided with a conventional knob or hand grip so that it can be manipulated manually.

5 Alternatively, the device may be constructed as a measuring probe rather than as a joystick, in which case the lever 12 functions as a stylus and would have a conventional stylus tip for contacting a workpiece.

10 Within the housing 10, a metal disc-shaped plate 22 is fastened to the bottom end of the control lever 12, via an insulating block 24. The plate 22 is therefore tiltable in the x and y directions and translatable along the z axis by means of the control lever 12.

15

The device comprises two printed circuit boards 26,28, one on each side of the plate 22 and generally parallel with it. The circuit boards 26,28 are spaced apart by and secured to a spacer ring 20, which forms part of the housing 10 and is clamped to the clamp rings 16,18. As shown in the drawings, both printed circuit boards are annular, though it is only necessary for the upper circuit board 26 to be annular (in order to accommodate the control lever 12). Printed on the circuit boards 26,28 are electrode patterns which form variable capacitors, in cooperation with the plate 22. Simplified versions of these patterns are shown in Figs. 2 and 3 (and the layout is shown diagrammatically in Fig. 4) though in practice the pattern etched onto the printed circuit boards also incorporates connections to the various electrodes, and guard rings around some or all of them which are connected to earth or another constant potential. Such details are conventional and have been omitted for simplicity of description.

35

The lower circuit board 28 has an outer annular electrode E as part of its printed pattern, and the upper circuit

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board 26 has a corresponding, identical electrode F. These two electrodes E,F cooperate with the central plate 22 to form a differential capacitor, varying as the control lever 12 is moved in the  $\pm z$  directions.

5

Inside the electrode E, the lower circuit board 28 has four quadrant-shaped electrodes A,B,C,D. The upper circuit board 26 similarly has four quadrant-shaped electrodes A',B',C',D', each of which is diametrically  
10 opposed to the respective electrode A,B,C,D. The two circuit boards are interconnected (by means not shown) such that the electrode A is electrically connected to the electrode A'. Similarly the electrodes B,C,D are respectively connected to the electrodes B',C',D'. The  
15 connected electrode pair A,A' and the connected pair B,B' form a differential capacitor with the centre plate 22, which varies as the control lever 12 tilts about the x axis. Likewise, the electrode pair C,C' and the electrode pair D,D' form another differential capacitor with the  
20 central electrode 22, which varies as the control lever 12 is tilted about the y axis.

The arrangement of electrodes just described provides a three axis capacitive transducer which needs only three  
25 electrode assemblies, namely the two circuit boards 26,28 and the central electrode plate 22. Since the central plate 22 has just one electrode, it is easily fabricated from sheet metal. All the complicated electrode shapes are provided on just the two circuit boards 26,28, and  
30 since these can be easily fabricated as conventional printed circuits they are very cheap. Furthermore, the signal conditioning circuitry (described below) can if desired be provided on an extension of one of the two circuit boards, further reducing the overall cost of the  
35 device.

If desired, the second set of quadrant-shaped electrodes A',B',C',D', may be omitted. However, the performance of

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the device will suffer slightly, and since little additional cost is involved in providing these electrodes, their omission is not preferred.

5 In Fig. 4A, there is shown an alternative electrode arrangement. Electrodes which correspond electrically to the electrodes A,A',B,B' etc. of Fig. 4 have been labelled AA,AA',BB,BB' etc. As can be seen, the arrangement is the inverse of that shown in Fig. 4, with the electrode EE  
10 being surrounded by an annulus divided up into the electrodes AA,BB,CC,DD, and with the electrode FF being surrounded by an annulus divided up into the electrodes AA',BB',CC',DD'. The electrical connections into differential capacitors are analogous to those previously  
15 described.

The signal conditioning system for the joystick will now be described. For purposes of explanation, Fig. 5 shows a single channel signal conditioning system, useful for  
20 processing signals from the transducers on a single axis. Fig. 6 shows how such a single axis circuit can be expanded to three channels for a three axis device.

Referring to Fig. 5, reference numeral 30 generally  
25 indicates a single channel transducer, consisting of the electrodes A,A', B,B' and 22, forming the differential capacitor which reacts to tilting about the x axis. Two square wave drives are applied to the fixed plates A,A' and B,B' respectively of the differential capacitor.  
30 These two square wave drives are derived from a modulator 32 which comprises two pairs of electronic switches, 34A,34B and 36A,36B. The switch pairs are driven by phase and antiphase signals derived by a bistable 38 from a clock oscillator 40. The amplitude of the square wave  
35 applied to the electrodes A,A' by the switch pair 34A,34B is set at a reference voltage  $+V_R$  generated by a reference source 42, and by a feedback voltage  $V_F$  which is derived



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from a digital to analogue converter 44 as discussed below. In a similar fashion, the amplitude of the square wave applied to the electrodes B,B' is determined by the feedback voltage  $V_F$  and by a reference voltage  $-V_R$ ,  
5 produced by an inverter 46 which inverts the output of the reference source 42.

The resulting signal produced on the central electrode 22 is received by a charge amplifier 48, which detects and  
10 amplifies any imbalance in current between the two capacitances of the differential capacitor 30. The output of the charge amplifier 48 is taken to one input of a phase sensitive rectifier (PSR) 50, which acts as a synchronous demodulator. Another input of the PSR 50  
15 receives an inverted version of the output of the charge amplifier 48, produced by an inverter 52.

The PSR 50 comprises two pairs of electronic switches 54A,54B and 56A,56B, which are driven by the same phase  
20 and antiphase signals as the modulator 32, derived from the bistable 38. The PSR 50 produces an output on a line 58, the net DC value of which is indicative of any current imbalance between the two capacitances of the transducer  
30.

25

A current comparator 60 receives this output on line 58, and controls the up/down input of an up/down counter 62 according to whether the current on line 58 is positive or  
negative. The counter 62 is clocked by the output of the  
30 clock oscillator 40, and will count up or down one count on each clock pulse (that is on each half cycle of the square waves driving the modulator 32 and PSR 50).

The counter 62 produces a digital output 64, which is used  
35 as the output of the signal conditioning system, and which also feeds the digital to analogue converter 44 to produce the feedback voltage  $V_F$ . Thus, the feedback voltage  $V_F$

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reacts to any current imbalance in the differential capacitor 30 in the sense which tends to reduce that imbalance to zero. It follows that the digital output 64 is then an indication of the position of the centre electrode 22 relative to the two fixed electrode pairs A,A' and B,B'. It will be seen that, in effect, the comparator 60 and counter 62 act to integrate the output of the PSR 50.

10 To be more exact, the digital output is proportional to  $(C1-C2)/(C1+C2)$ , where C1 and C2 are the capacitances of the two halves of the differential capacitor. This ratio is linearly proportional to the displacement of the electrode 22.

15

To give ratiometric operation, the digital to analogue converter 44 has its reference input supplied by a line 66 from the voltage reference source 42.

20 If desired, the signal  $V_F$  can be used as an alternative, analogue output in place of or as well as the digital output 64.

In the multi-channel system of Fig. 6, use is made of the property of phase sensitive rectifiers that they have no net DC output from signals which are even harmonics or even sub-harmonics of the carrier. This allows a system to be built in which the signals of the three separate channels are in effect multiplexed through a single charge amplifier 48 from the single centre electrode 22 of the transducer. The advantages of this are firstly that it allows the use of a simple metal plate for the central electrode 22, and secondly that it requires only the one charge amplifier 48. The significance of the latter point lies in the fact that such a charge amplifier is often an expensive component, so that expense is once again reduced.

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Referring to Fig. 6, the same reference numbers and letters have been used as previously, with the addition of suffixes x,y or z where appropriate to denote components which are duplicated in each of the x,y and z channels.

5 Thus, each channel has its own modulator 32x,32y,32z, its own PSR 50x,50y,50z, its own comparator 60x,60y,60z, its own counter 62x,62y,62z producing respective digital outputs 64x,64y,64z and its own digital to analogue converter 44x,44y,44z. Each of these components is

10 constructed in an identical manner to Fig. 5. Additionally, the circuit has a charge amplifier 48, voltage reference source 42, corresponding inverters 52,46, and clock oscillator 40, which are common to all three channels. For simplicity, the reference line 66 to

15 the digital to analogue converters has not been shown.

The clock oscillator 40 produces an output frequency  $f$  and this is fed to a divider 68 producing outputs of  $f/2$ ,  $f/4$  and  $f/8$ . These are respectively used as carrier signals

20 by the modulators and PSRs of the x,y and z channels respectively. The outputs of the divider 68 are each in phase and antiphase form, as previously, but for simplicity only one of each signal  $f/2$ ,  $f/4$ ,  $f/8$  has been shown leading to the modulators and PSRs. The counters

25 62x,62y,62z are respectively clocked by the signals  $f$ ,  $f/2$  and  $f/4$ . That is, as previously, they are clocked at twice the rate of the corresponding carrier frequency for the channel concerned. This is the maximum useful clock frequency, there being no advantage to higher frequencies.

30 However, the counters will perform their integrating function if clocked at any frequency, subject to the proviso that if a counter's clock frequency is too low, it will have a very slow response. Accordingly, if desired, all three counters 62x,62y,62z may be clocked at the same

35 frequency, say  $f/4$  or at a slower frequency. This has the advantage of simplification, and also ensures that all the channels respond at the same update rate.

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Each channel works in the same way as the single axis system of Fig. 5, and is independent of the other channels because the PSRs produce no net DC output from (i.e. they reject) the carriers of the other two channels. This is  
5 because the carriers are even harmonics or sub-harmonics of each other. It will be seen that each output is produced continuously: multiplexing of the amplifier 48 is achieved without time-sharing, which would give discontinuous outputs.

10

Unlike the single axis version the outputs of the PSRs 50x,50y,50z may need some low pass filtering to remove the AC content generated by the other two carriers. Suitable low pass filters can be inserted before the inputs of the  
15 comparators 60x,60y and 60z.

In the systems shown, taking the single axis system of Fig. 5 as an example, a simple comparator 60 is used to control the up/down input of the counter 62. This means  
20 that once the system is in balance, the digital output will oscillate by one count. If it is desired to remove this oscillation, the comparator 60 may be replaced by a window comparator, which has a dead band of one or more counts and two output signals to the counter 62, namely a  
25 count enable and an up/down signal. Once within the dead band, the counter would be disabled, so as not to change state every clock pulse. Similarly, window comparators may replace the comparators 60x,60y and 60z in Fig. 6.

30 The circuit of Fig. 5, or each channel for Fig. 6, could be modified as shown in Fig. 7. Whereas Figs. 5 and 6 form Class 1 servo loops, Fig. 7 shows how to modify the circuit to give a Class 2 servo loop, in which the rate of change of the feedback signal  $V_F$  depends on the size of  
35 the error detected by the PSR 50.

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As shown in Fig. 7, the output of the PSR 50 is buffered by an amplifier 70, to give a voltage signal. This is rectified by a rectifier 72, giving a positive voltage whose magnitude represents the error detected by the PSR.

5 This positive voltage controls a voltage controlled oscillator 74, which produces clock pulses for the counter 62. Thus, the counter is clocked at a rate which depends of the size of the error. The direction of counting (up or down) is governed as previously by a comparator 60,

10 which receives the output of the amplifier 70 and determines whether it is positive or negative. The output of the counter 62 is used as previously to generate the feedback signal  $V_F$  via a digital-to-analogue converter 44 (not shown in Fig. 7), and to provide the digital output

15 64 of the system.

Fig 8 shows an alternative to the circuit of Fig 6. It is intended for use with single ended capacitive transducers, as opposed to the differential capacitive transducers of

20 Fig 6. The circuit effectively compares the capacitance of a capacitive transducer  $CV_1$  with a fixed reference capacitance  $CR_1$ . Similarly, it compares a variable capacitive transducer  $CV_2$  with a fixed reference capacitance  $CR_2$ . Thus, as shown, the circuit of Fig 8 has

25 two channels, but it will be appreciated that the circuit can be readily expanded to three or more channels.

In Fig 8, the transducer  $CV_1$  is fed with a square wave from a modulator comprising a pair of electronic switches

30 134A,134B. These are driven in phase and anti-phase so as to chop a reference voltage from a reference source 42. Similarly, the transducer  $CV_2$  is supplied with a square wave from a modulator consisting of a pair of electronic switches 234A,234B. The switches 234A,234B are switched

35 at a drive frequency which is at half the drive frequency of the switches 134A,134B, in exactly the same manner as shown in Fig 6. Alternatively, of course, the chosen

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drive frequencies may be a different even multiple or sub-multiple of each other, rather than one half.

As previously, the resulting signals from the transducers  
5  $CV_1$ ,  $CV_2$  are received by a common charge amplifier 48.  
The output of the amplifier 48 is taken in parallel to two  
sets of signal conditioning electronic circuits 150,250,  
one for each channel. The circuits 150,250 also receive  
an inverted version of the output of the amplifier 48 via  
10 an inverting amplifier 52. The circuits 150,250 each  
include a phase sensitive rectifier 50, a comparator 60,  
an up/down counter 62 and a digital-to-analogue converter  
44, as described in Figs 5 and 6 (not shown in Fig 8), and  
each produces a digital output as previously. The phase  
15 sensitive rectifier 50 in each of the circuits 150,250 is  
driven at the appropriate frequency corresponding to the  
modulator for the respective channel. That is, the phase  
sensitive rectifier in the circuit 150 is driven at the  
same frequency as the electronic switch pair 134A,134B,  
20 while that in the circuit 250 is driven at the same  
frequency as the electronic switch pair 234A,234B. In  
this way, the common output of the charge amplifier 48 is  
demodulated to produce a separate feedback voltage  $VF_1$ ,  
 $VF_2$  for each of the respective transducers  $CV_1$ ,  $CV_2$ .

25  
The feedback voltage  $VF_1$  is chopped by a pair of  
electronic switches 136A,136B at the same frequency as the  
switches 134A,134B. The resulting square wave is fed back  
through the fixed reference capacitance  $CR_1$  to the input  
30 of the charge amplifier 48. In exactly the same manner as  
Figs 5 and 6, the circuit 150 reacts to any change in the  
capacitance of the transducer  $CV_1$  by changing the feedback  
voltage  $VF_1$  in such a a manner as to tend to null the  
change. This gives the effective comparison between the  
35 capacitance of the transducer  $CV_1$  and the fixed reference  
capacitance  $CR_1$  as mentioned above. The output of the  
circuit 150 is given by  $VF_1/VR = CV_1/CR_1$ , where VR is the

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voltage of the reference source 42.

Likewise, the feedback voltage  $VF_2$  from the circuit 250 is chopped by a pair of electronic switches 236A,236B at the same frequency as the electronic switch pair 234A,234B. The resulting square wave is fed through the reference capacitor  $CR_2$  to the input of the charge amplifier 48. The result is that the output of circuit 250 is given by  $VF_2/VR = CV_2/CR_2$ .

10:

Of course, the digital outputs (not shown) of the circuits 150,250 mirror the analogue feedback voltages  $VF_1, VF_2$ .

Fig 9 shows a circuit which is similar to Fig 8. Similar circuit components have been given the same reference numerals, and need not be described further. However, in Fig 9, a single reference capacitor CR replaces the two separate reference capacitors  $CR_1, CR_2$  of Fig 8. In order that the respective chopped output voltages  $VF_1, VF_2$  can both be fed back to the input of the amplifier 48 via this single reference capacitance, the voltage outputs of the electronic switch pairs 136A,136B and 236A,236B are added together by a transformer T1. The advantage of the Fig 9 circuit is that the matching of the outputs of the two channels does not depend upon the matching of the two reference capacitances. Instead, it depends upon the matching of the primary coils of the transformer T1, which is more easily achieved.

The transformer T1 merely serves as a convenient voltage addition means, it being easy to ensure that the signals are accurately added together by such a device.

The above examples have used square wave drives for the modulators and demodulators. However, it should be appreciated that the invention is not limited to square wave drives, and may for example use drive waveforms of

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any other shape, such as sinusoidal or triangular. To illustrate this, Figs 10 and 11 show circuits with sinusoidal drives. For each of these figures, only one channel will be described in detail, since the further  
5 channels are similar.

Fig 10 is intended for use with a differential capacitance transducer 30, having a common plate 22 and input plates A and B, as in Figs 5 and 6. However, in place of the  
10 modulator 32, there is provided a transformer T2. The primary of the transformer T2 is driven by a sinusoidal AC oscillator 142, the output of which has an amplitude at a reference voltage. The secondary of the transformer T2 is  
15 centre-tapped, and has its two ends connected to the plates A and B of the differential transducer 30, which are thus fed with phase and anti-phase sinusoidal signals. A charge amplifier 48 receives the common output from the  
20 plate 22 of the transducer 30, summing the differential signals received from the two sides of the transducer.

The output of the charge amplifier 48 is taken to a circuit 300 which is analagous to the circuits 50,60,62 and 44 of Figs 5 and 6, but which is designed for the sinusoidal signals of the present circuit. Thus, the  
25 circuit 300 includes a phase sensitive detector in the form of a multiplier 350 which receives the output of the charge amplifier 48 and is driven by the reference sinusoidal signal from the oscillator 142. The output of the multiplier 350 is a voltage which is positive or  
30 negative, depending on the phase of the output of the amplifier 48 relative to the reference. A comparator 360 detects whether this output is positive or negative, and sets the up/down control input of an up/down counter 362 accordingly. The counter 362 is clocked at the same  
35 frequency as the reference oscillator 142, by a comparator 380 which serves to square the sinusoidal oscillation.



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In the present case, the output of the counter 362 is signed, giving a digital output 364 which can be either positive or negative. This is taken to a four quadrant multiplying digital-to-analogue converter 344. This  
5 converter 344 has a reference input which receives the sinusoidal reference signal from the oscillator 142. The output of the converter 344 is a voltage signal  $V_F$ , which is the result of multiplying the sinusoidal reference signal by the positive or negative digital output of the  
10 counter 362. The resulting feedback signal  $V_F$  is a sinusoidal signal having an amplitude depending on the digital output 364 of the counter 362, which is in phase with the reference signal if the digital output is positive, and in anti-phase if the digital output is  
15 negative. This signal  $V_F$  is taken to the centre tap of the transformer T2, with the same result as in the previous circuits, namely that the circuit 300 acts to tend to null the input to the charge amplifier 48, so that the digital output 364 reflects the setting of the  
20 differential capacitance 30 which is to be measured. The output 364 is proportional to  $(C_1 - C_2) / (C_1 + C_2)$ , where  $C_1$  and  $C_2$  are the respective capacitances of the two halves of the differential capacitance transducer 30.

25 Thus far, only one channel of the circuit of Fig 10 has been described. However, the circuit has the ability to multiplex the signal conditioning from several transducers 30 through a common charge amplifier 48. As shown in Fig 10, a circuit block 130 consists of the differential  
30 transducer 30 and transformer T2 just described, and is repeated in further channels as a circuit block 230. The input to the circuit 230 is a sinusoidal reference signal derived from the oscillator 142 via a frequency doubler 168. Thus, the reference signal in the second channel is  
35 twice that of the first channel. The output from the common plate of the differential transducer in the circuit 230 is taken to the common input of the charge amplifier

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48. The second channel has a circuit 400, identical to the circuit 300 of the first channel, which receives the output of the amplifier 48 and demodulates it using the reference signal from the frequency doubler 168. Thus, the second channel works in exactly the same manner as the first, but with a reference signal which is double the frequency of the first.

Likewise, if further channels are required, they can be added in identical fashion, for example using a further frequency doubler 268.

Fig 11 shows an example which is analagous to Fig 8, but using a sinusoidal reference signal as in Fig 10. The circuit 130 of Fig 10 is replaced by a circuit 330, comprising a variable capacitance transducer  $CV_1$  and a fixed reference capacitance  $CR_1$ , similar to those of Fig 8. A reference oscillator 142, similar to that of Fig 10, provides a sinusoidal signal having a reference amplitude voltage, which passes through the transducer  $CV_1$  to the input of a common charge amplifier 48. The output of the amplifier 48 is processed by a circuit 500. The circuit 500 contains a multiplier 550 and comparators 560 and 580, which function in exactly the same manner as Fig 10 and will not be described further. However, the counter 562 of the circuit 500, while corresponding to the counter 362, does not have a signed digital output, but instead has a digital output 564 which is always positive. This is multiplied by the sinusoidal reference signal in a multiplying digital-to-analogue converter 544. The converter 544 corresponds to the converter 344, but need only be a two quadrant multiplier rather than the previous four quadrant multiplier, because the digital input 564 is always positive. The resulting sinusoidal output signal  $V_F$  is fed back to the charge amplifier 48 via the reference capacitance  $CR_1$ , so as to act in a similar manner to the circuit of Fig 8. The output 564 is

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proportional to  $CV_1/CR_1$ , as in Figs 8 and 9.

The circuits 330 and 500 are of course duplicated for other channels, which are driven at even multiples of the  
5 frequency of the reference oscillator 142 via frequency doublers, exactly as in Fig 10.

In the single ended circuits described (Figs 8,9 and 11) the accuracy can be improved by fabricating the reference  
10 capacitances in the same manner as the variable transducer capacitances. This ensures that such factors as variances in the dielectric constant, manufacturing tolerances, etc, affect both the variable capacitances and the reference capacitances equally, and therefore cancel out.

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The above examples of the invention have related to joysticks. However, the electrode arrangements and signal conditioning circuits described can each also be used in measuring probes, separately or together. Moreover, they  
20 are not limited to use in devices for detecting displacement, and may be used in any other sensors in which such transducers are used, e.g. pressure sensors.

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**CLAIMS**

1. A circuit for providing outputs from at least two  
5 capacitive transducers, the circuit comprising:  
    respective means for each transducer for feeding an  
alternating input signal thereto;  
    common means for receiving the signals thereby  
10 produced from the transducers; and  
    respective means for each transducer for receiving  
the output signal from said common means and demodulating  
the received signal synchronously with the frequency of  
the respective input signal to that transducer;  
    wherein the frequencies of said input signals are  
15 even harmonics or sub-harmonics of each other.
2. A circuit according to claim 1, wherein each  
receiving and demodulating means provides a feedback  
signal, which is fed back to said common means via a  
20 reference capacitance, the feedback signal acting so as to  
tend to cancel the signal received by said common means  
from the respective transducer, whereby the magnitude of  
the feedback signal indicates the output of the respective  
transducer.
- 25
3. A circuit according to claim 1, wherein each  
transducer comprises a differential pair of capacitances.
4. A circuit according to claim 3, wherein each  
30 receiving and demodulating means provides a feedback  
signal, which is fed back to the respective transducer,  
the feedback signal acting so as to tend to cancel the  
signal received by said common means from the respective  
transducer, whereby the magnitude of the feedback signal  
35 indicates the output of the respective transducer.

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5. A circuit according to any one of the preceding claims, wherein each said receiving and demodulating means includes means for integrating the demodulated signal.
- 5 6. A circuit according to claim 5, wherein the integrating means includes a counter which provides a digital output which indicates the output of the respective transducer.
- 10 7. A circuit according to any one of the preceding claims, in combination with a device which is responsive to displacement in at least two axes, the device comprising a respective said capacitive transducer responsive to displacement in each said axis, said circuit  
15 being connected to said transducers in order to provide outputs indicating the displacements in said axes.
8. A device which is responsive to displacement in at least two axes, the device comprising a capacitive  
20 displacement transducer for each said axis, each transducer including at least two opposed capacitor electrodes, one electrode of each transducer being common with an electrode of the or each other transducer.
- 25 9. A device according to claim 8, wherein the capacitor electrodes of the transducers which are not common are provided on a common printed circuit board.
- 30 10. A device according to claim 9, wherein there are two said printed circuit boards, on opposing sides of the common electrode, giving each transducer a differential arrangement in which the common central electrode is relatively movable between the two outer electrodes on the printed circuit boards.

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11. A device according to claim 8, claim 9 or claim 10,  
wherein at least one said transducer has two said  
capacitor electrodes which are not common to another said  
transducer, said two electrodes being electrically  
5 connected to each other in a pair so as to form parts of a  
composite electrode.

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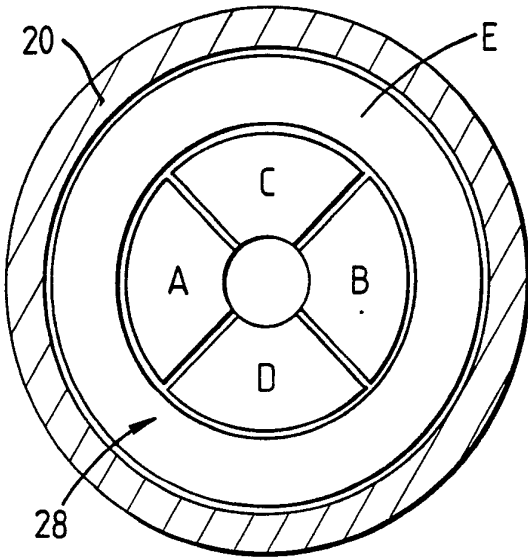
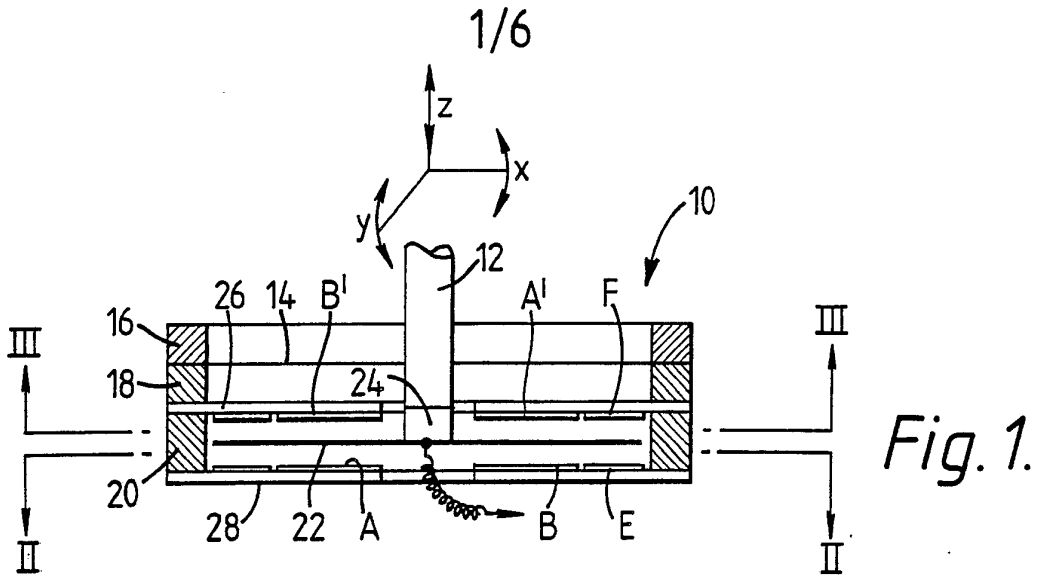
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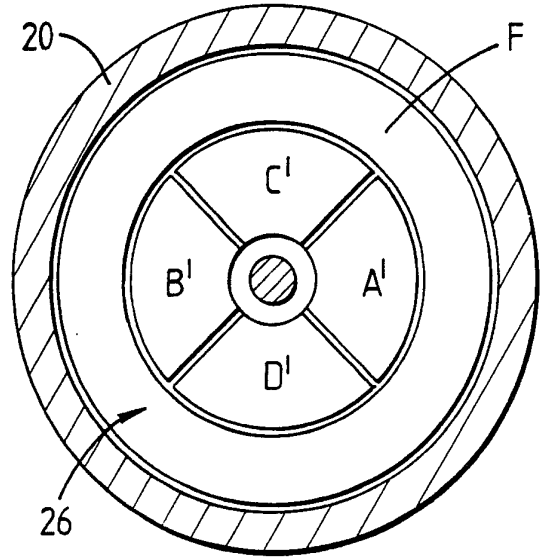
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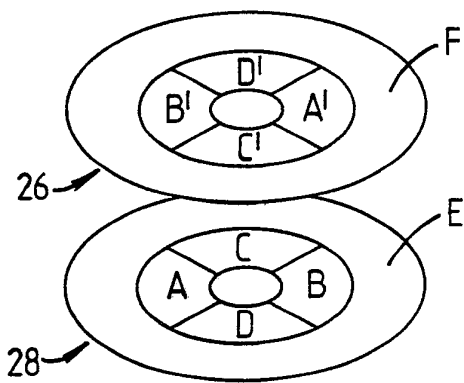
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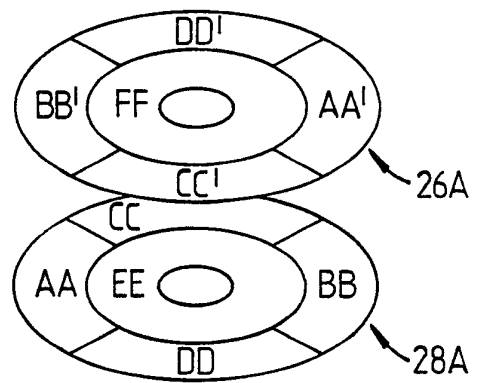
*Fig. 2.*



*Fig. 3.*



*Fig. 4.*



*Fig. 4A*

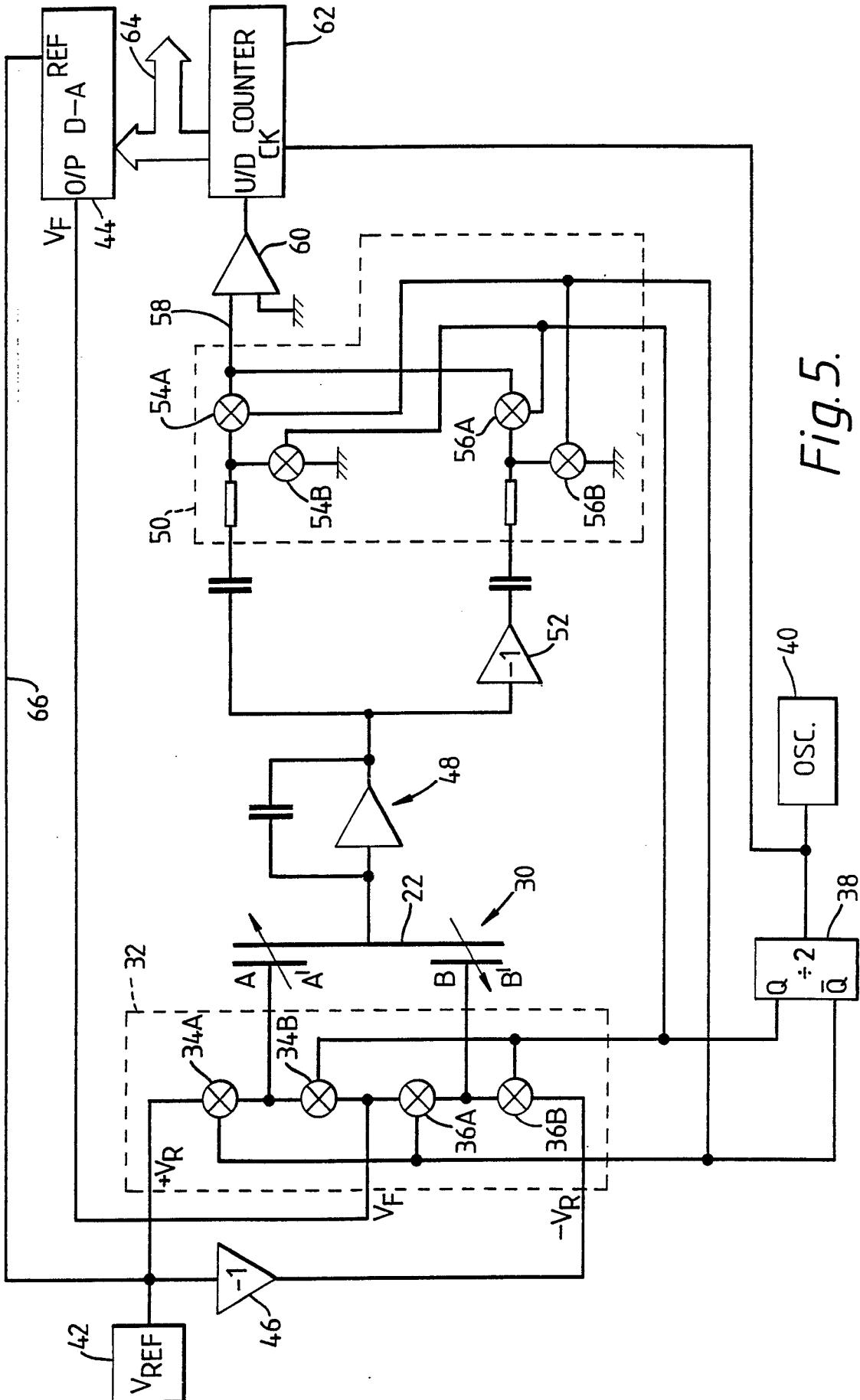


Fig. 5.



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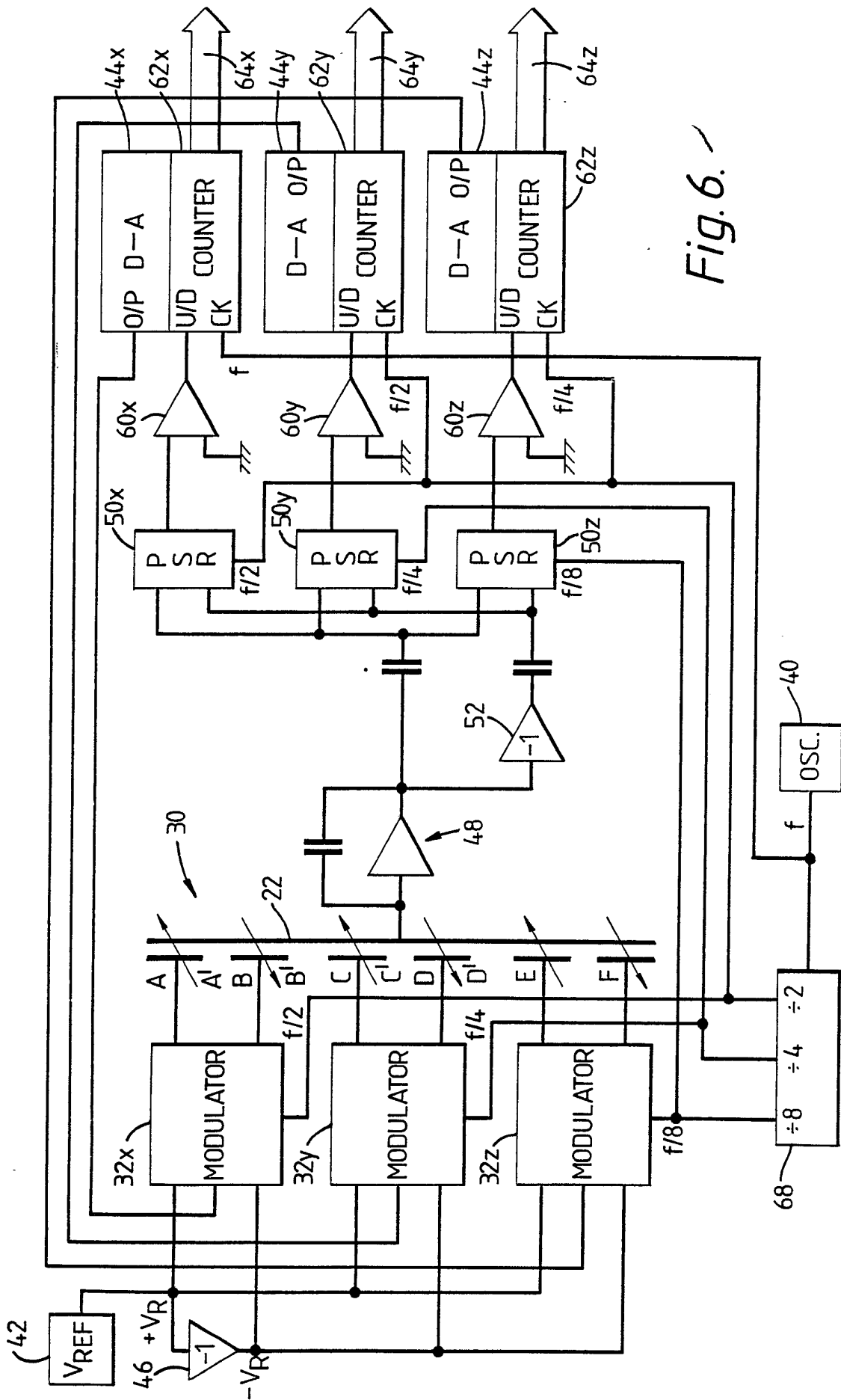


Fig. 6.

Fig. 7.

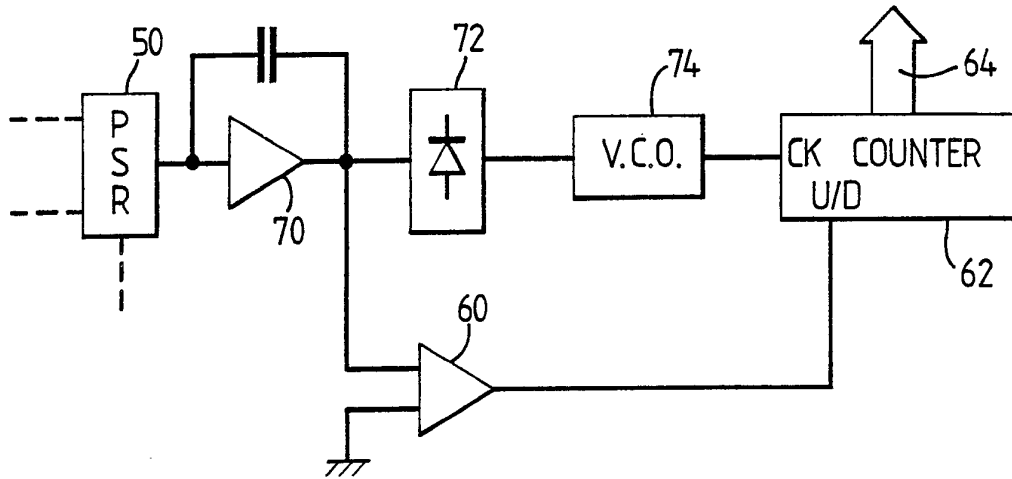
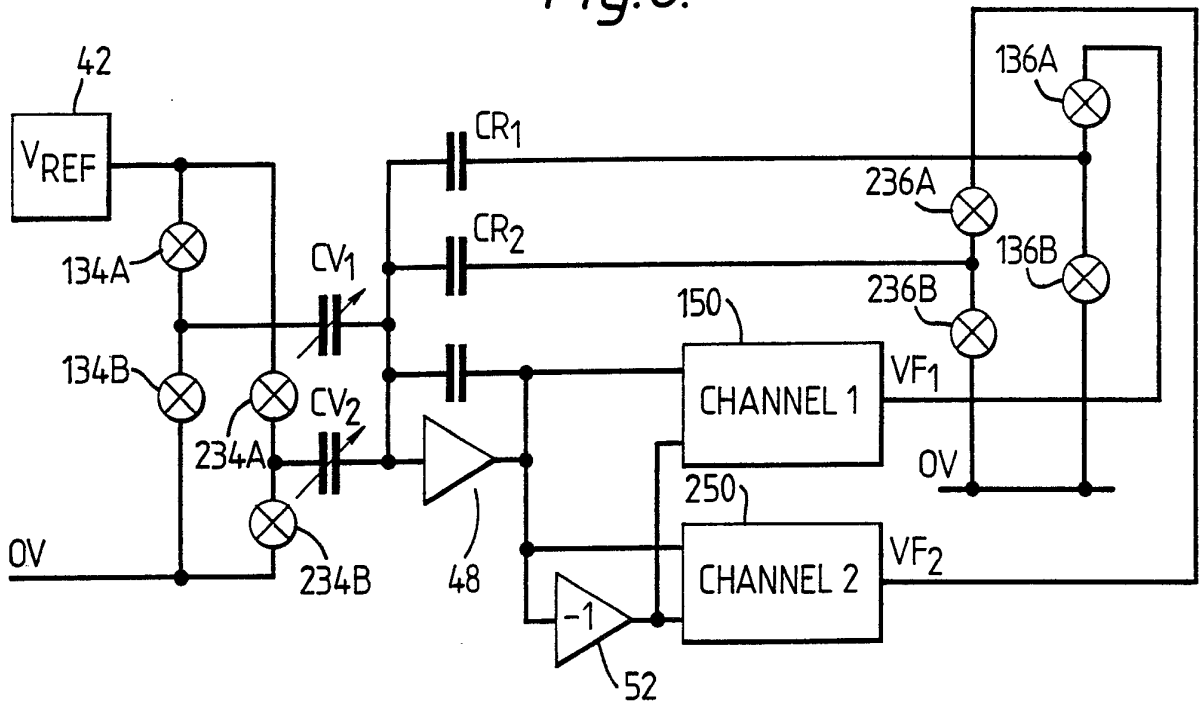


Fig. 8.



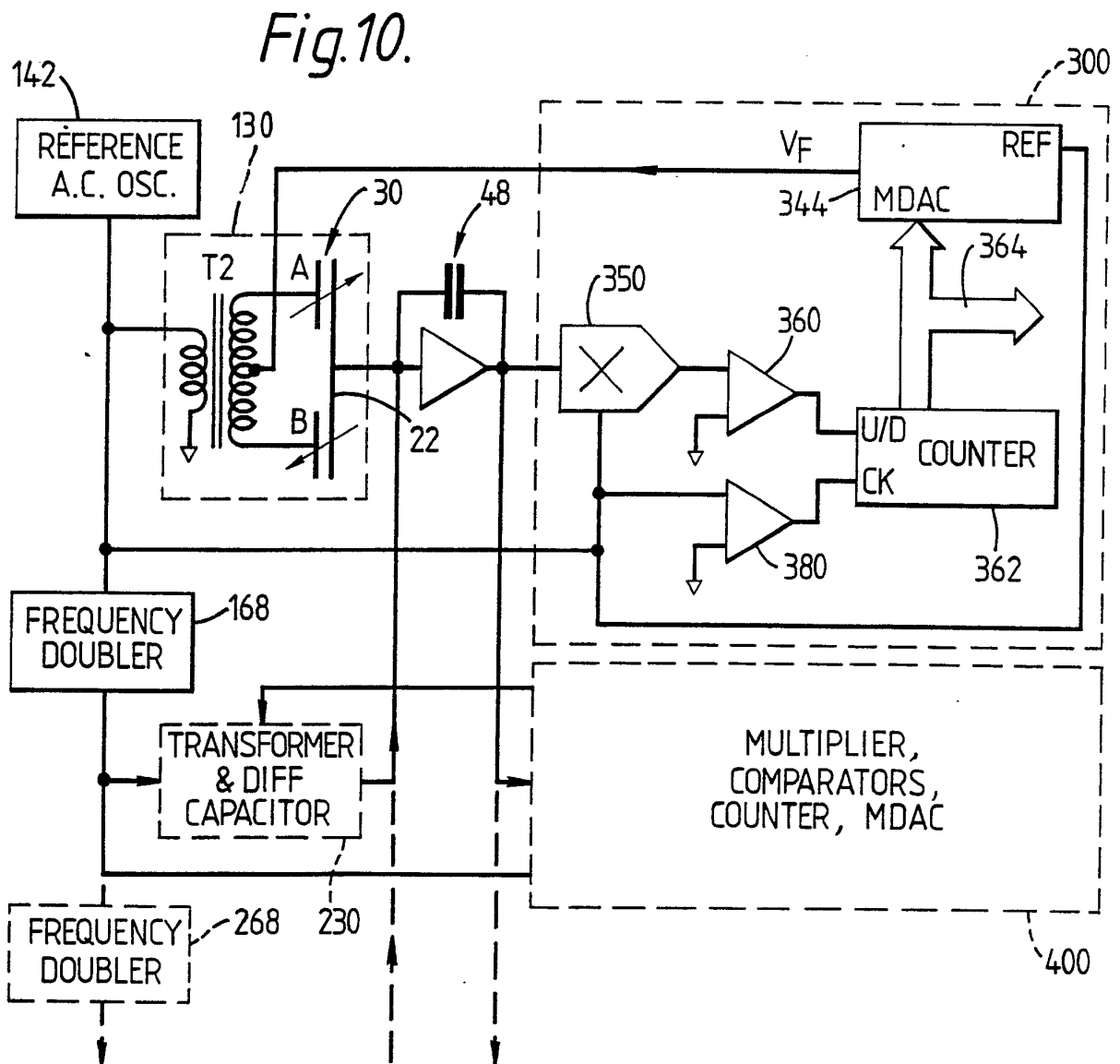
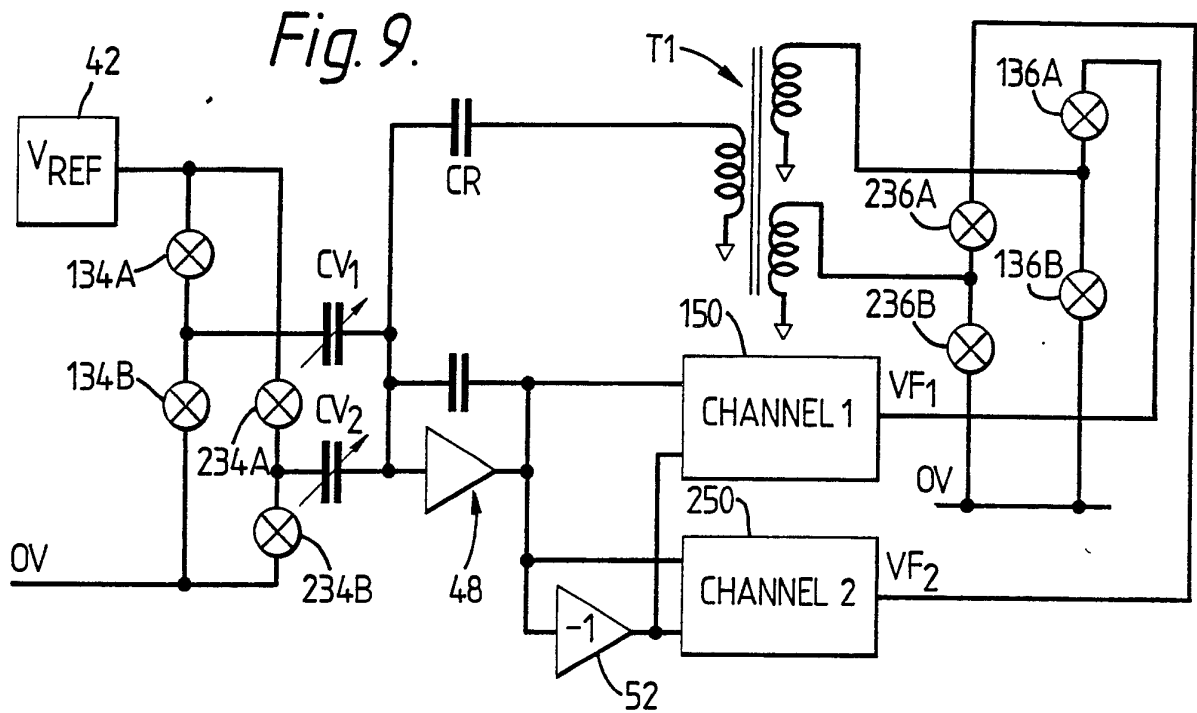
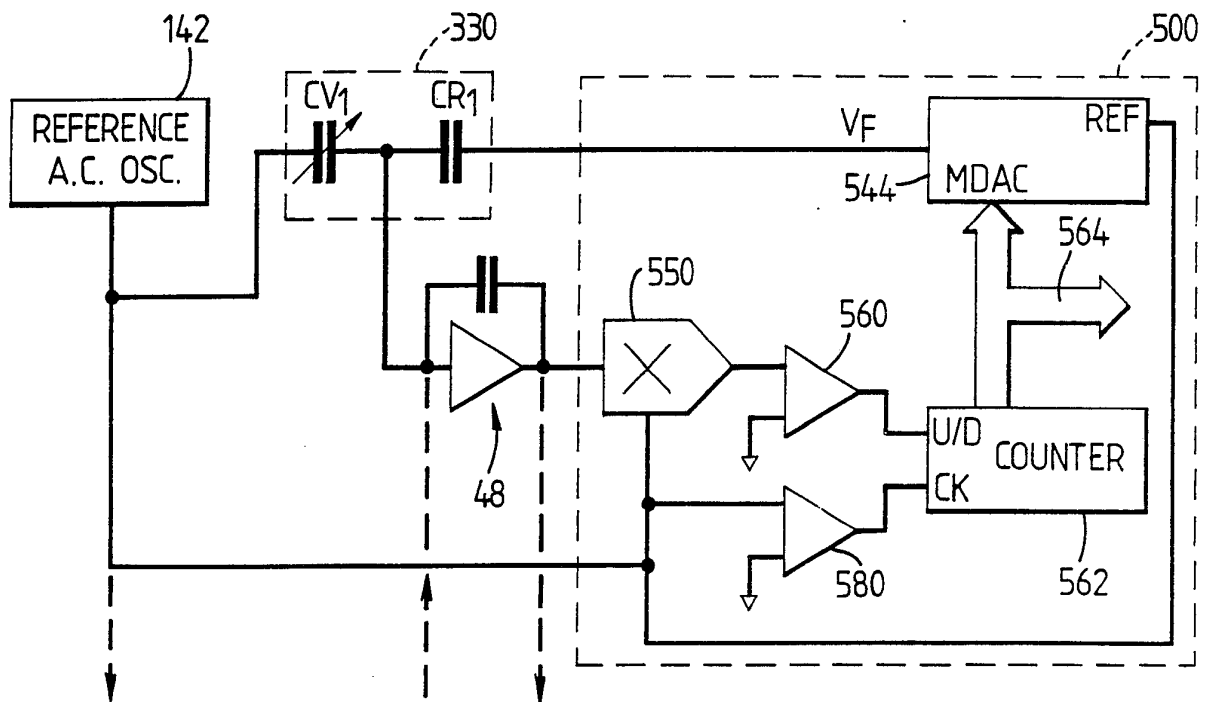
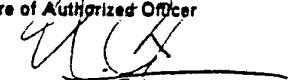


Fig. 11.



# INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 89/00389

<b>I. CLASSIFICATION OF SUBJECT MATTER</b> (if several classification symbols apply, indicate all) <sup>6</sup>		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC <sup>4</sup> : G 01 D 5/24, G 01 B 7/00		
<b>II. FIELDS SEARCHED</b>		
Minimum Documentation Searched <sup>7</sup>		
Classification System	Classification Symbols	
IPC <sup>4</sup>	G 01 B, G 01 D, G 01 R	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched <sup>8</sup>		
<b>III. DOCUMENTS CONSIDERED TO BE RELEVANT <sup>9</sup></b>		
Category <sup>9</sup>	Citation of Document, <sup>11</sup> with indication, where appropriate, of the relevant passages <sup>12</sup>	Relevant to Claim No. <sup>13</sup>
X	US, A, 4719538 (COX) 12 January 1988 see the whole document	8,9,11
A	---	1-7
A	IBM Technical Disclosure Bulletin, vol. 25, no. 3B, August 1982, (New York, US), E. Courtens: "Ultrafine displacement detector and balance", pages 1645-1646 see the whole article	10
A	---	1-7
A	US, A, 4098000 (EGGER) 4 July 1978 see abstract; figure 4	1-7
A	---	1-4
A	US, A, 3857092 (MEYER) 24 December 1974 see abstract; figure 1 cited in the application -----	1-4
<p><sup>10</sup> Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&amp;" document member of the same patent family</p>		
<b>IV. CERTIFICATION</b>		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
22nd August 1989	22. 09. 89	
International Searching Authority	Signature of Authorized Officer	
EUROPEAN PATENT OFFICE	 L. ROSSI	

**ANNEX TO THE INTERNATIONAL SEARCH REPORT  
ON INTERNATIONAL PATENT APPLICATION NO.**

GB 8900389

SA 28133

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 15/09/89. The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4719538	12-01-88	None	
US-A- 4098000	04-07-78	None	
US-A- 3857092	24-12-74	CH-A- 539837 DE-A, B, C 2218824 FR-A, B 2176724 GB-A- 1366284 JP-A- 49008266 NL-A- 7303858	14-09-73 04-10-73 02-11-73 11-09-74 24-01-74 25-09-73