# United States Patent [19]

**Marinkovich et al.**

[11] **3,796,156**

[45] **Mar. 12, 1974**


## [54] LINE PRINTER WITH RECIRCULATING LINE STORE AND LINE PRINT MEMORIES


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[52] **U.S. Cl.** ..... **101/93 C,** 340/172.5

[51] **Int. Cl.** ..... **B41j 5/00,** G06f 1/00

[58] **Field of Search**...101/93 C; 340/172.5; 197/20



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*Attorney, Agent, or Firm*—Coffee and Sweeney



[57] **ABSTRACT**

A printer for simultaneously printing an entire line of characters in accordance with information received in the form of binary coded characters includes a plurality of discs respectively located at a plurality of aligned print locations. Each disc has a plurality of type characters embossed around its peripheral surface, and is rotated to successively present its type characters at the print location. The received characters are stored and provided with addresses corresponding to the print locations. Each type character, as it is presented, is successively compared with all of the stored characters, and the disc at each location which corresponds to the address of a stored character that compares with the presented type character is stopped from further rotation to maintain the corresponding presented type character thereon at the print location. After all the discs have been stopped, all of the selected type characters at the aligned print locations are simultaneously impacted with a print receiving surface to transfer the entire line of print thereto.


**26 Claims, 8 Drawing Figures**

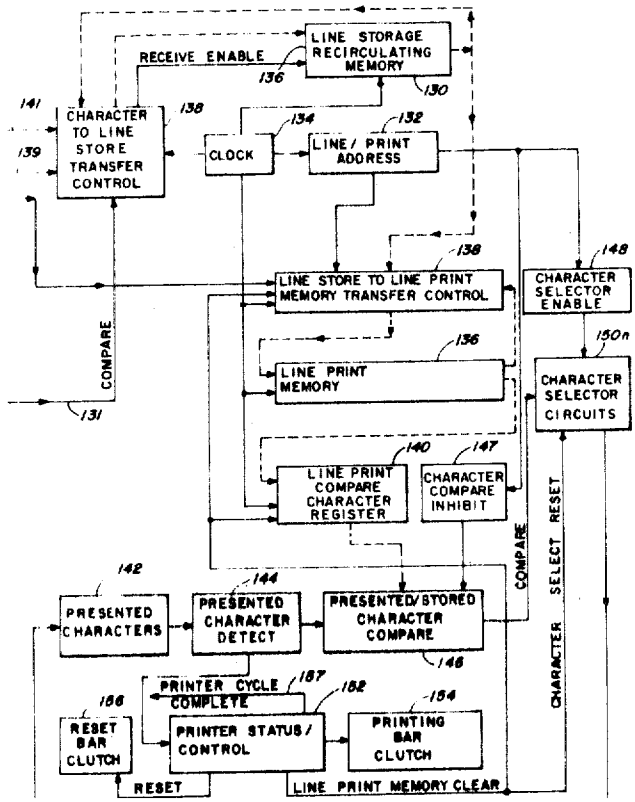
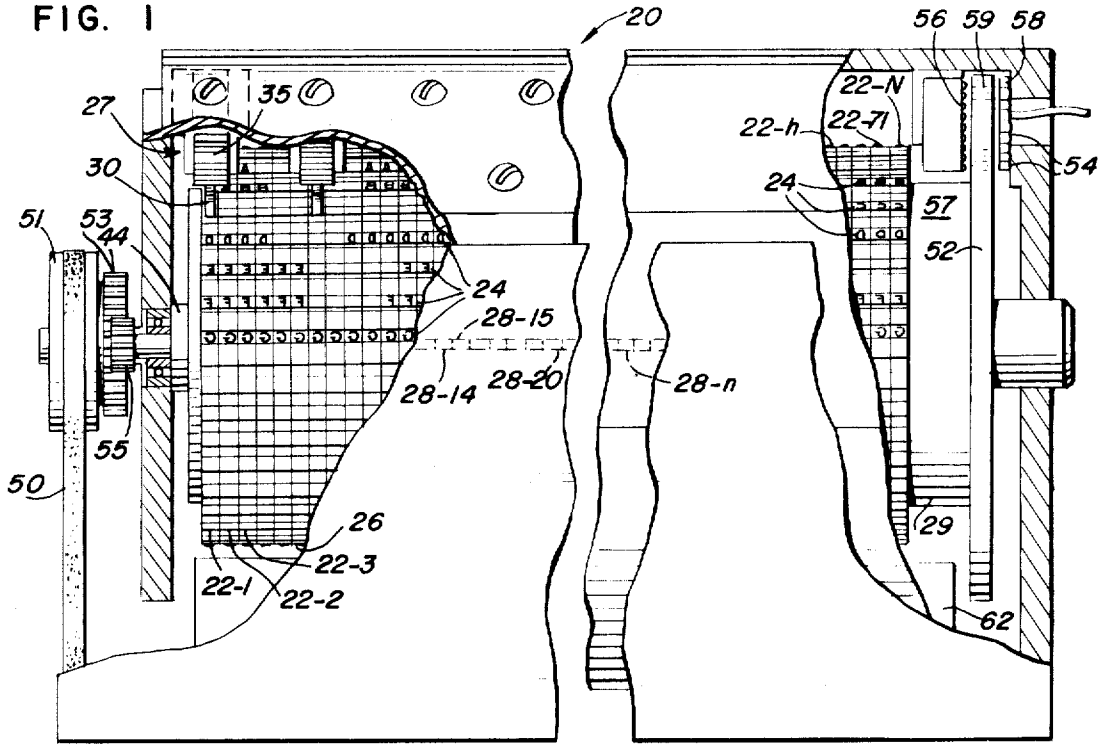


FIG. 1



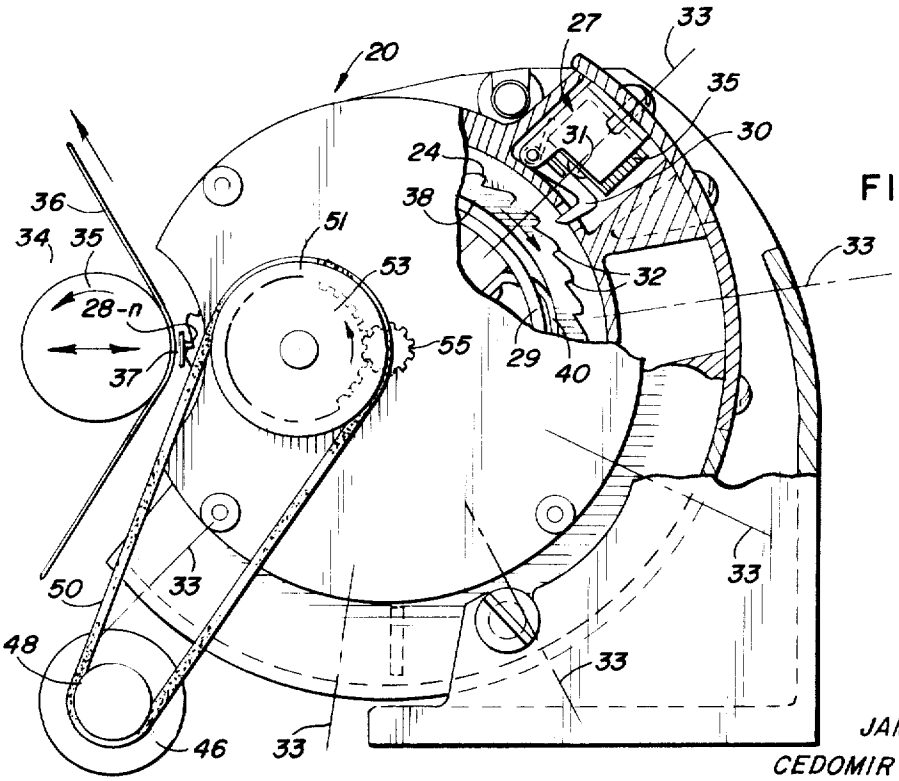




FIG. 2

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ATTORNEYS

FIG. 5a

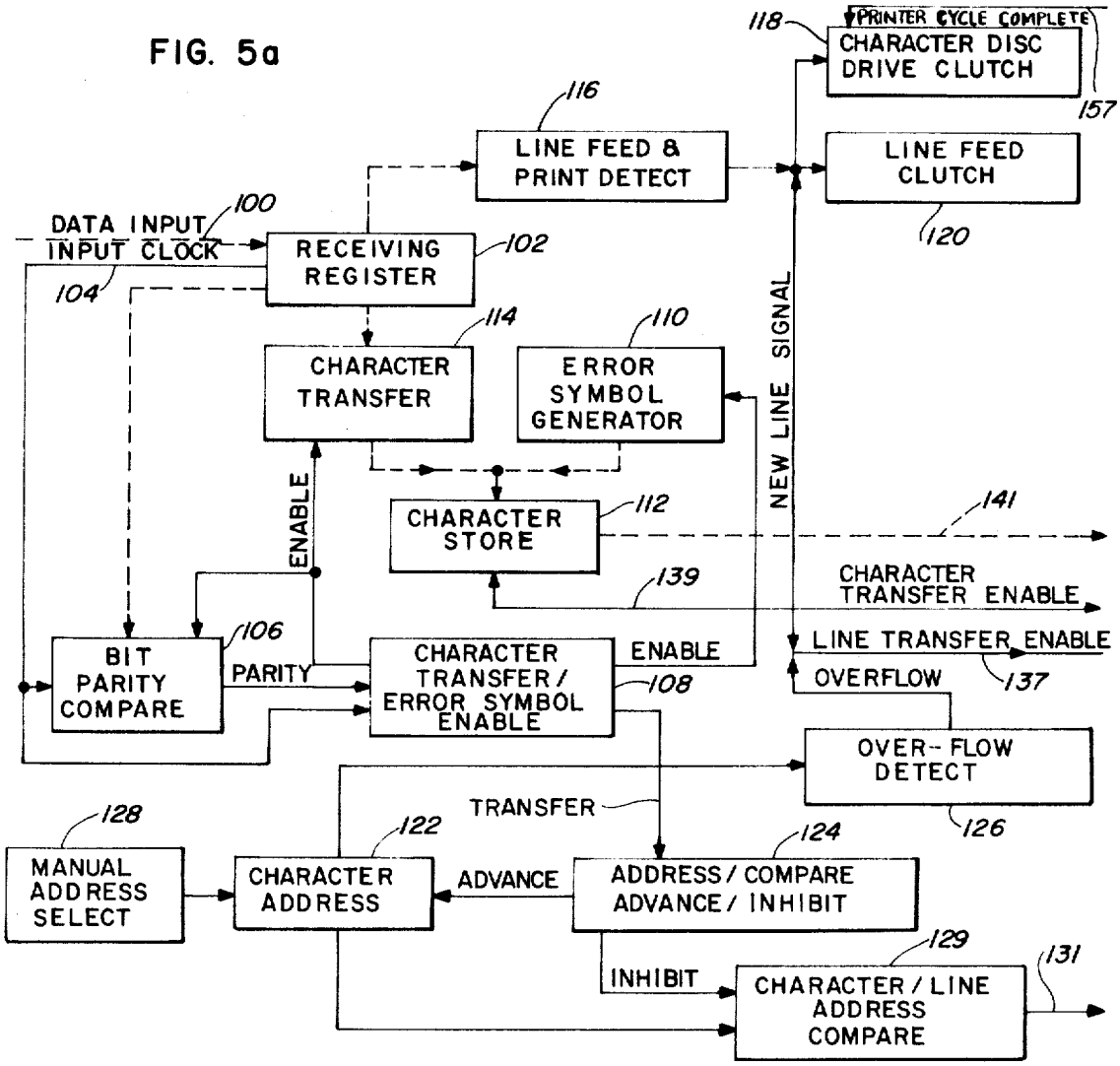



FIG. 4

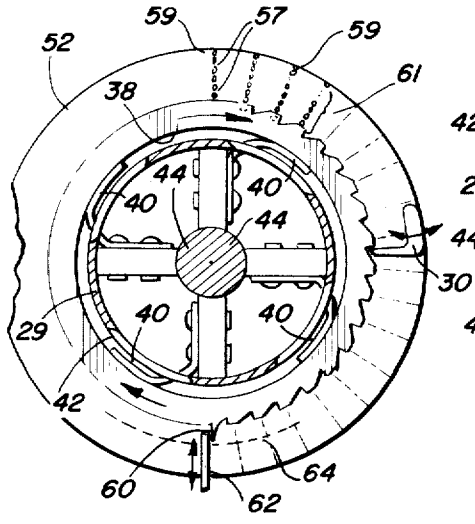



FIG. 3

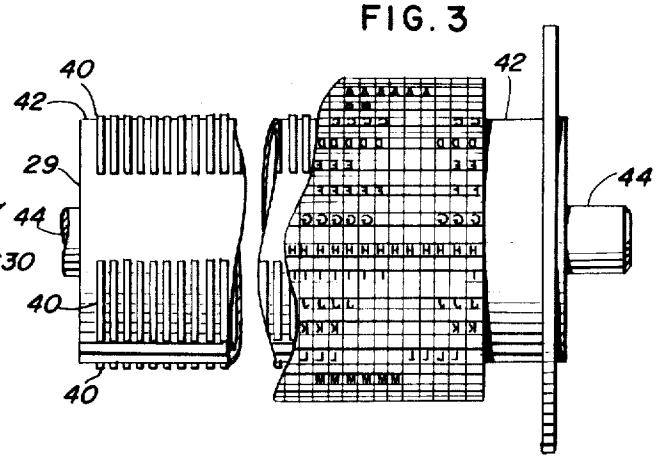
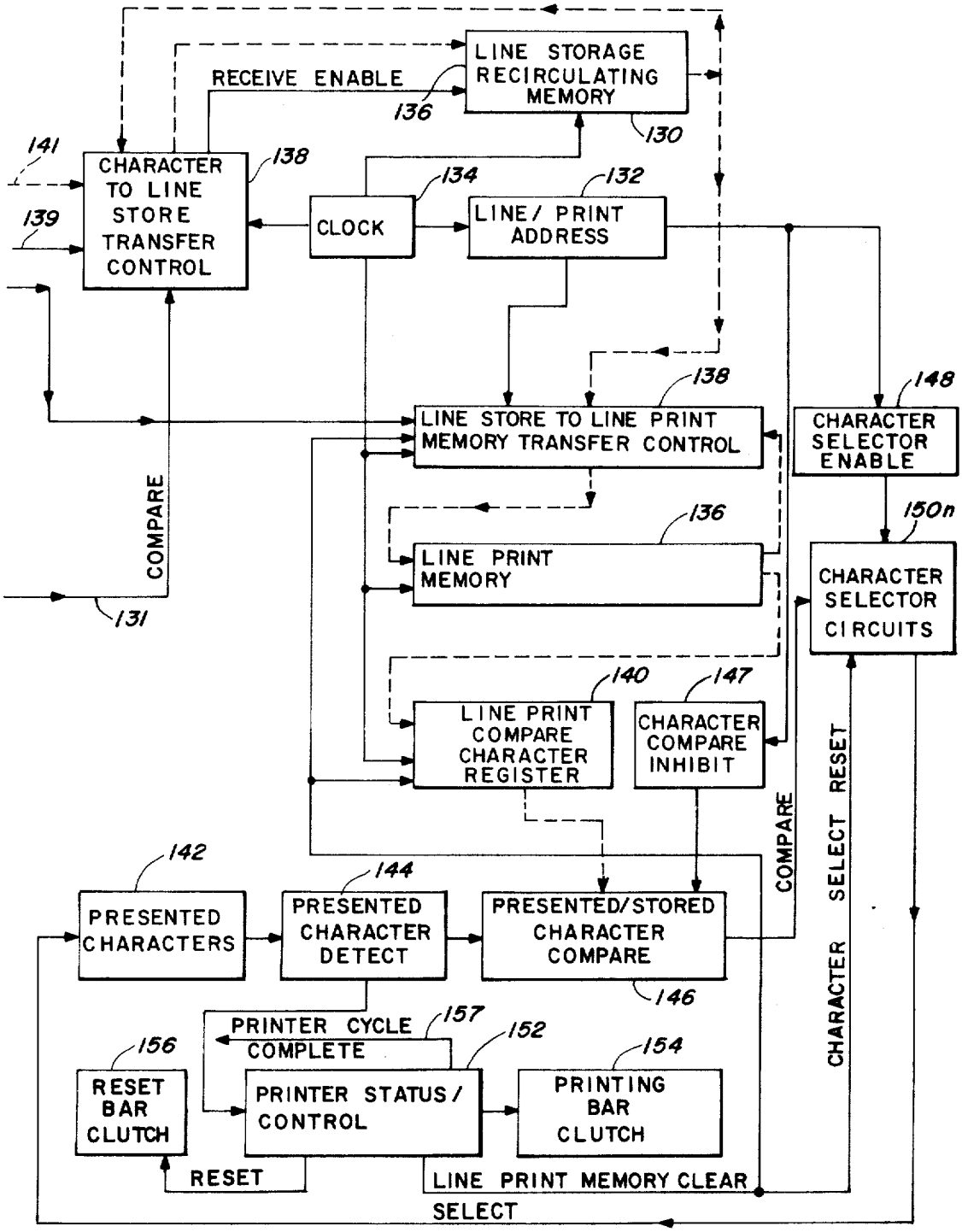


FIG. 5b


LINE STORAGE RECIRCULATING MEMORY
130
RECEIVE ENABLE
136
141
139
CHARACTER TO LINE STORE TRANSFER CONTROL
138
CLOCK
134
LINE/ PRINT ADDRESS
132
138
LINE STORE TO LINE PRINT MEMORY TRANSFER CONTROL
148
CHARACTER SELECTOR ENABLE
150n
136
LINE PRINT MEMORY
CHARACTER SELECTOR CIRCUITS
COMPARE
131
140
147
LINE PRINT COMPARE CHARACTER REGISTER
CHARACTER COMPARE INHIBIT
142
144
PRESENTED CHARACTERS
PRESENTED CHARACTER DETECT
PRESENTED/STORED CHARACTER COMPARE
146
COMPARE
CHARACTER SELECT RESET
PRINTER CYCLE COMPLETE
157
152
156
154
RESET BAR CLUTCH
PRINTER STATUS/ CONTROL
PRINTING BAR CLUTCH
RESET
LINE PRINT MEMORY CLEAR
SELECT

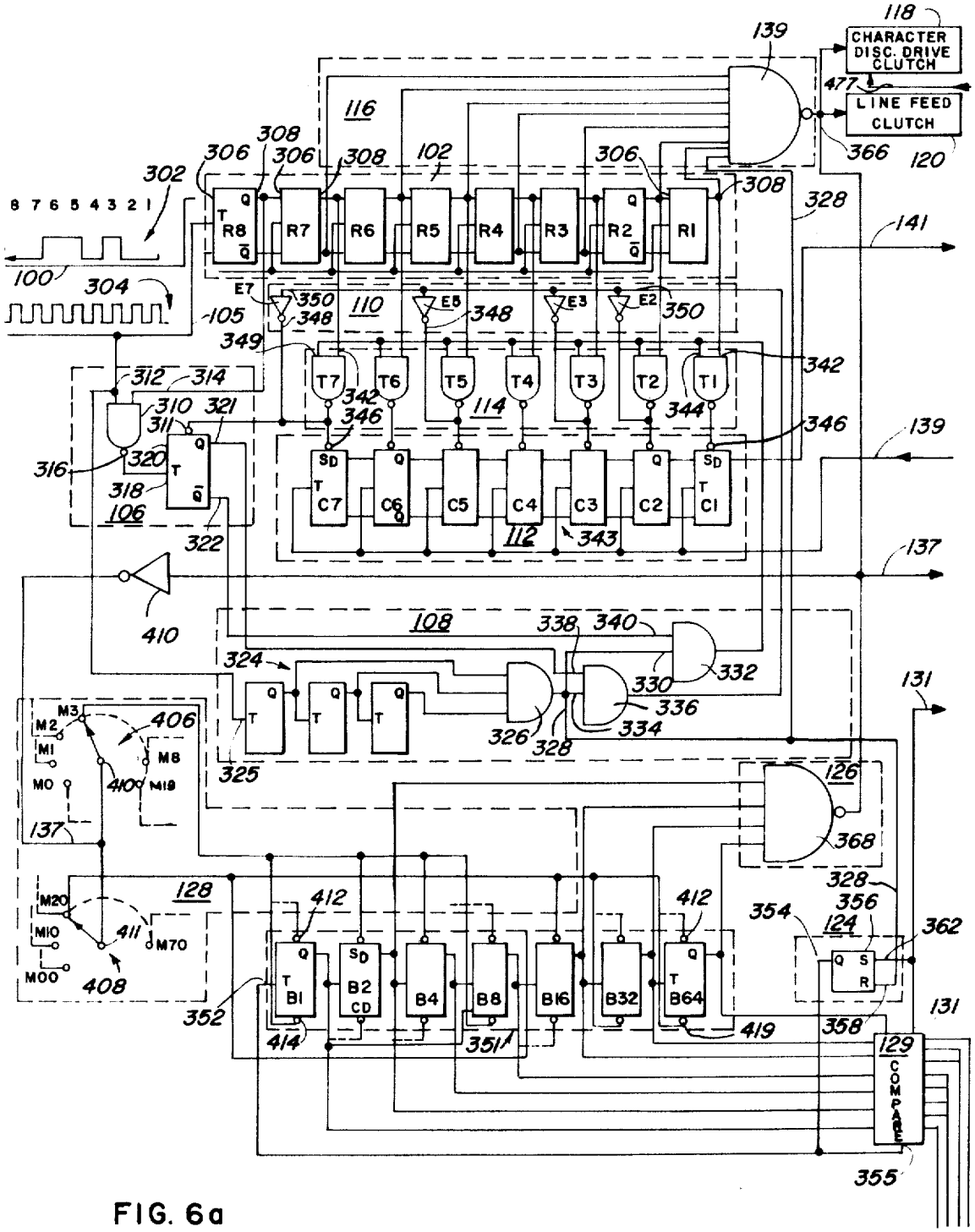
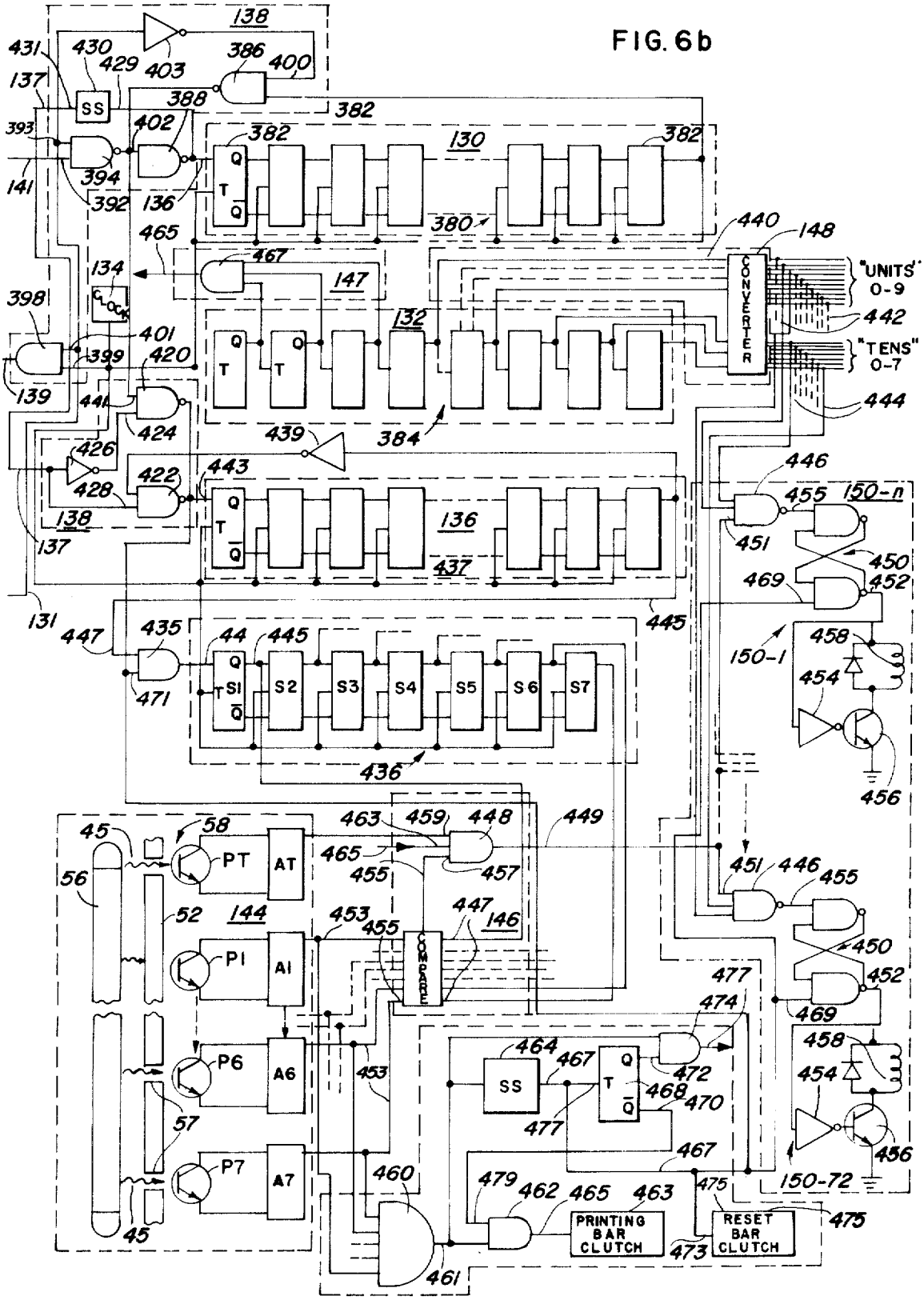

CHARACTER DISC. DRIVE CLUTCH
LINE FEED CLUTCH
COMPARE
8 7 6 5 4 3 2 1
R8
R7
R6
R5
R4
R3
R2
R1
T7
T6
T5
T4
T3
T2
T1
C7
C6
C5
C4
C3
C2
C1
B1
B2
B4
B8
B16
B32
B64
M3
M2
M1
M0
M8
M16
M20
M10
M00
M70
116
102
110
114
112
106
108
128
126
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129
118
120
139
141
137
131
100
302
304
105
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406
408
410
411
412
414
419
477

FIG. 6a

FIG. 6b


138
431
430
429
403
386
400
137
SS
388
382
393
402
382
130
382
141
394
392
136
380
465
440
148
467
134
147
"UNITS" 0-9
398
132
442
401
399
420
CONVERTER
"TENS" 0-7
139
441
424
444
439
384
426
446
422
443
455
150-n
428
138
136
451
450
137
437
469
452
131
445
447
435
44
445
458
150-1
471
S1
S2
S3
S4
S5
S6
S7
454
436
456
45
58
463
459
448
449
PT
AT
465
455
457
56
451
446
455
52
144
453
455
447
146
PI
AI
450
452
477
474
469
458
464
467
472
P6
A6
SS
468
454
453
470
57
477
456
467
460
479
462
465
463
475
150-72
P7
A7
PRINTING BAR CLUTCH
RESET BAR CLUTCH
475
45
473
461

# LINE PRINTER WITH RECIRCULATING LINE STORE AND LINE PRINT MEMORIES

## BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to devices for converting electrical signals into a readable format and, in particular, to an impact printer for simultaneously printing a line of printed characters in accordance with information received in the form of digital electrical signals.

2. Description of the Prior Art

Due to the rapidly increasing use of computers in recent years, a great need has developed for a printer capable of economically transforming electrical signals, such as from digital computers, into a readable printed format. Economy in this area can best be realized by maximizing the rate at which the printer can operate and by reducing equipment cost. The factor which imposes the greatest limitation on the efficient use of computers is the long readout time, the time it takes for the computed information to be put into a readable form, relative to the computation time. Similarly, the cost of data transmission, over telephone lines for instance, is directly proportional to the time that the lines are in use which, in turn, is directly proportional to the time it takes to receive and print the transmitted information. Thus, there is a great demand for a cheap, reliable and fast printer. Unfortunately, up until now, this demand has not been met. Presently, printers are either slow, unreliable or prohibitively expensive for most applications.

One of the first attempts at reducing readout time consisted of modifying the standard teletypewriter, which prints one character at a time, so that it would operate at faster speeds. These attempts have met with only minor success due to the inherent time limitations imposed by successively impacting one character at a time against the print receiving material. This duplication of impacting motion reduces the efficiency of the printing mechanism, inherently makes the printer noisy, causes excessive wear to severely limit the operating life and reliability of the printer and, as stated, limits the maximum operating speed at which the printer can operate.

In an attempt to resolve these problems, a variety of so-called electromechanical "line printers" have been developed which simultaneously print a plurality (but less than a full line) of characters. One known printer of this type comprises a rotating drum having a matrix of type characters embossed around its cylindrical surface. As the drum rotates, identical characters are successively presented at each of a plurality of print locations. A print hammer adjacent each of the print locations impacts the print receiving material such as paper, against selected ones of the characters as they are presented. For example, as the letter "A" is presented at all the print locations, selected ones of the printer hammers, such as the first and thirteenth print hammer, are actuated to impact the paper against the presented type letter "A." The same action occurs as the letter "B" is presented, and so on until the drum has made a complete revolution and all of the characters are printed.

Using this approach, the operating speed may be increased somewhat, but the aforementioned problems with regard to single-character printing remain, and



some new problems are created. First, the mechanism is made much more complex and, thus, more prone to failure, by the provision of a plurality of independently actuated print hammers for each of the print locations. The duplication of impacting motion is not reduced by this approach, but rather, is simply distributed over a plurality of print hammers. Finally, due to the fact that the print hammers impact the type characters "on the run," precision timing is essential. The coil dynamics of the print hammers are critical to obtaining a uniform and readable line of print, for the print hammer must impact the selected character on the character drum the instant that the character is precisely aligned with the theoretical base line for each line of print. Furthermore, these critical timing requirements require highly sophisticated control circuits which make the printer unduly expensive.

Another approach of solving the operating speed requirement has been to make the "printer" action entirely, or almost entirely, electrical. One known approach along this line has been to use a television picture tube to display the characters. A rapid operating speed is easily achieved, but the displayed data is, of course, not very portable, multiple copies cannot be provided and, again, the required use of sophisticated control circuits make such a display unit inherently expensive.

Another known printer uses the basic approach as in a television picture tube display by spraying ink, rather than electrons, through controlled deflection magnets onto the paper. The deflection magnets deflect the ink particles to form the desired characters, but due to the excessive power and critical timing requirements, only one character can be sprayed onto the paper at a time for all practical purposes. One of the major drawbacks in such an ink spraying approach is that carbon copies of the printed material cannot be made. Also, such a unit has stringent specification requirements with regard to timing, power, ink temperature, etc., which make it prone to failure and, again, inherently expensive.

## SUMMARY OF THE INVENTION

The improved printer of the present invention overcomes the disadvantages of the prior printers noted above in a novel and simple manner. In the present printer, a plurality of identical discs, each of which carries an ordered sequence of type characters around its peripheral surface, are simultaneously rotated to successively present the type characters thereon at aligned print locations. A printer control receives information in the form of electrically coded characters, stores a plurality of received characters corresponding to a line of print, and provides an address corresponding to a print location for each of the stored characters. After a complete line of characters is stored, they are compared with eacy type character as it is presented at the print location, and the character discs at the locations corresponding to the addresses of each stored character which compares with the presented type character is stopped to maintain the type character thereon at the print location. After all of the discs have been stopped with their respective selected type characters at the print location, the print receiving material is simultaneously impacted against the selected type characters at the print locations to transpose the entire line of print thereto. After the line has been printed, the discs

are again rotated and selectively stopped until the characters on each of the discs are in a preselected alignment. During the time that the line of characters is being selected a new line of coded characters may be received and stored, so that after all the discs have been positioned into their preselected alignment, selection of a new line of characters may commence immediately.

Thus, a principal feature of the printer is that an entire line of selected type characters are first maintained at respective print locations and then simultaneously impacted with a print receiving material, so that the aforementioned problems due to critical timing and wear requirements are either entirely eliminated or substantially reduced.

Another important feature of the unique printer of this invention is that the provision for first selecting and then simultaneously printing all the characters of a line of print allows for a much simpler and, thus, much more reliable printer control circuit and printer mechanism.

Yet another feature of the improved printer of this invention is the provision of simultaneously printing an entire line of characters substantially reduces the printer operating noise.

Still another feature of the printer is the provision of means for detecting reception of an erroneous character and for storing and printing an error character in its place.

A further feature of the invention is the provision of a code disc synchronized with the rotation of the character discs, and means for detecting the code thereon for indicating to the printer control which type character is being presented.

Still a further feature of the invention is a means for detecting a control function character representing the end of a line of print, and means for selecting the appropriate type characters and actuating the printer to print the selected type characters in response thereto.

Yet a further feature of the printer is the provision of a means for automatically actuating the printer to select the appropriate type characters and print the selected type characters when the maximum storage capability of the printer control has been exhausted so that subsequently received characters will not be lost.

Still another important feature of the printer is the provision of a recirculating memory for storing an entire line of received characters.

Yet another important feature of the invention is the provision of a means for indicating to the printer control when all of the selected characters are at their respective print locations.

A further important feature of the invention is the provision of a means for indicating when all of the discs have been positioned with the type characters thereon in a preselected alignment so that selection of a new line of characters may commence.

Still another feature of the invention is that the discs are disengaged from their rotary driving means when all of the characters are in the preselected alignment and a new line of characters to be selected is not being stored.

One more feature of the invention is that the code disc and character disc may be easily changed to allow the printer to receive information in different codes and to print different characters.

## BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the invention will be apparent from the following description taken in connection with the accompanying drawings, in which:

FIG. **1** is a front view, partially in section, of a preferred embodiment of the printer mechanism showing the arrangement of the character discs and the code disc;

FIG. **2** is a view, partially in section, of the left side of FIG. **1**, showing the character discs, the disc selector mechanism, the print locations and the impact printing bar;

FIG. **3** is a front view of the clutch drum with several character discs mounted thereto;

FIG. **4** is a side view of FIG. **3** showing the location of the reset and character selection mechanisms and the character code disc;

FIG. **5***a* is a block diagram of a portion of a preferred embodiment of a control circuit for the printer mechanism of FIGS. **1–4**;

FIG. **5***b* is a block diagram of the remaining portion of the control circuit for the printer mechanism of FIGS. **1–4**, the first portion of which is shown in FIG. **5***a*;

FIG. **6***a* is a circuit logic diagram of the portion of the printer control circuit shown in block form in FIG. **5***a*; and

FIG. **6***b* is a circuit logic diagram of the portion of the printer control circuit shown in block form in FIG. **5***b*.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

As previously explained, the line printer of this invention comprises a printer mechanism which performs the actual printing function and a printer control which control the printer mechanism in accordance with received information. Exemplary embodiments of the printer mechanism and the printer control are respectively shown in FIGS. **1–4** and FIGS. **5–6** and will be described in that order.

Referring first to FIGS. **1** and **2**, the printer mechanism or printer **20** includes a plurality of type character carrying members or annular character discs **22**-n (*n* equals 1 through N, N being the total number of character column locations in a full line of print, such as 72) respectively located adjacent a plurality of aligned print locations **28**-n. Each character disc **22**-n carries a plurality of print or type characters **24** embossed around its outer peripheral surface which are successively presented at the print location **28**-n of that disc as it is rotated about its major axis.

In the preferred embodiment, the character carrying members **22**-n comprise annular discs, but it should be understood that any shaped members capable of carrying and presenting a plurality of embossed characters could be used. For example, the characters could be embossed on the surface of a closed loop which is driven past the print locations. Also, typically, all of character discs **22**-n are identical, each disc carrying the same characters in the same order around its peripheral surface, but, for purposes of receiving cryptographic messages for example, each of the discs might be different.

The print characters **24** for most applications are the standard characters found in most typewriters, such as all of the upper and lower case letters of the alphabet,

numerals 0 through 9, all of the punctuation marks and a character space. However, any symbols could be used. For example, the printer might be used to transmit weather maps or the like, in which case the characters would comprise weather symbols.

A cylindrical clutch drum **29**, extending through the annular opening **38** of each of character discs **22**-n and frictionally engaged therewith, provides the rotary drive for discs **22**-n which rotate therewith. As shown in FIGS. **3** and **4**, a set of four clutch fingers **40**, mounted to clutch drum **29** and extending in a substantially tangential relationship to cylindrical surface **42**, resiliently and frictionally engages the inner surface of the annular opening **38** of each of character disc **22**-n. Axial shaft **44** of clutch drum **29** is axially coupled to gear **55** (FIG. **2**), which is driven in rotation by motor **46** through gear **53**, pulley wheel **51**, drive belt **50** and disc drive clutch **48** in an obvious manner whenever drive clutch **48** is engaged by the printer control. During intervals when the printer control does not have a complete line stored, the printer control disengages disc drive clutch **48** to allow motor **46** to idle, to conserve power.

However, upon reception of a complete line of characters, disc drive clutch **48** is engaged to initiate presentation of type characters **24**. Also, upon reception of a complete line of characters, a line feed clutch (not shown) or any like suitable mechanism is engaged to rotate printing bar or printing roll **34** in a direction indicated by curved arrow **35** to advance the print receiving material on paper **36** to a new line.

A character code disc **52** axially mounted to clutch drum **29**, and extending between light source or lamp **56** and photodetectors **54**, is provided to detect and indicate to the printer control which of print characters **24** is being presented at print locations **28**-n. As shown in FIG. **4**, character code disc **52** carries a plurality of circumferentially located character codes **61** in the form of code holes **57** at preselected ones of a plurality of radial locations. Code disc **52** rotates with clutch arm **29** so that as each print character **24**, which is not on a character disc **22**-n that has been stopped, is presented at its print location **28**-n, the character code **61** corresponding to that presented character **24** is positioned between lamp **56** and photodetectors **54** and detected thereby. Those photodetectors **54**, which are adjacent a location at which a code hole **57** is present, are energized by the light from lamp **56** passing therethrough and those adjacent a location at which a code hole **57** is not present are not energized. A unique combination of code holes is provided for each presented character, and, thus, the collective state of photodetectors **54**, which are electrically coupled to the printer control, give a unique indication to the printer control of the character being presented. Code disc **52** also carries a clock code hole **59** which is presented to a clock pulse photodetector **58** during presentation of each of the character codes **61**. Clock photodetector **58** generates a clock pulse which enables the printer to make a selection which will be explained in more detail hereinafter.

A character selector mechanism **27** mounted adjacent each of character discs **22**-n at various circumferential locations **33** is provided to stop character discs **22**-n as the type characters **24** thereon corresponding to the received characters are presented. Selector mechanisms **27** comprise a solenoid selector coil **35** coiled around a push member **31** in mechanical engagement with a pivotal mounted character stop member or pawl **30**. During presentation of each type character **24**, as indicated by photodetectors **54**, it is compared with an entire line of received characters stored in the printer control. If the presented character as indicated and the stored character at any location compare, the selector coil **35** at that location is energized and kept energized until all of the other selector coils have been similarly energized and the line has been printed. Upon energization of selector coil **35**, push member **31** is pushed against pawl **30** which pivots into engagement with one of a plurality of ratchet gear teeth or stop surfaces **32** of character disc **22**-n. Upon engagement of pawl **30** with any of stop surfaces **32**, the frictional coupling forces between the disc character **22**-n and clutch drum **29** are overcome and the character disc **22**-n stops rotating with the selected presented character maintained at its print location **28**-n. The position of pawl member **30** relative to stop surface **32** before and after energization of coil **35** is respectively shown in FIGS. **2** and **4**.

Upon one complete revolution of clutch drum **29**, all of character discs **22**-n have been stopped with their selected type characters at print locations **22**-n. This condition is detected by the printer control which, in response thereto, energizes a printing bar clutch (not shown) or other suitable mechanisms to impact printing bar **34** and, thus, paper **36** and inked ribbon **37** or the like against the line of presented type characters **24** at print locations **28**-n, thus, simultaneously imprinting the entire line of characters onto paper **36**.

As may already be understood from the foregoing, prior to selective stopping of any of character discs **22**-n, they must all be positioned relative to one another and code disc **52**, with the characters on each of discs **22**-n in a preselected alignment in order for the detected character code to accurately represent a known set of presented characters of which some may be selected. In most applications, the set of presented characters comprises the same presented characters **24** at each print location **22**-n, as illustrated in FIGS. **1** and **3**, with all of the type characters **24**, "A," "B," "C," etc., in alignment. If such a preselected alignment is used, detection of a character code **61** corresponding to a letter of the alphabet would indicate to the printer control that that letter of the alphabet was being presented at all of the print locations **28**-n and could be selected.

After the line of characters **24** has been printed, all of the selector coils **30** are deenergized to release character discs **22**-n to, once again, rotate with clutch drum **29**. At that point, type characters **24** are no longer in the preselected alignment and, thus, the detected character codes **16** are not representative of the predetermined sets of presented characters. Thus, a reset mechanism, as shown in FIG. **4**, is provided to reposition character disc **22**-n with the characters on each of the discs in the preselected alignment. The reset mechanism selectively stops character discs **22**-n until type characters **24** are again in the preselected alignment desired. Each of character discs **22**-n carries a reset stop surface **60** on its outer peripheral surface which extends outwardly from the center of the disc beyond print characters **24**, as shown in FIG. **4**. After all of the characters have been printed and pawl members **30** have been moved out of engagement with character

stop surfaces **32** to release character discs **22-n** with clutch drum **29**, the printer control engages a reset bar clutch or other suitable device, to move a reset bar **62** into the path of engagement **64** of stop surfaces **60** of all character discs **22-n**. Upon engagement with reset bar **62**, the frictional coupling forces between clutch drum **29** and character discs **22-n** are overcome and each of discs **22-n** stops rotating. Upon completion of one revolution, all of the reset stop surfaces **60** are in engagement with reset bar **62** and character discs **22-n** are positioned with type characters **24** in the desired preselected alignment. At this point, the character code being detected corresponds to the predetermined set of characters at print locations **28-n**, and the reset bar clutch is disengaged to move reset bar **62** out of engagement with the stop surfaces **60** to allow selection of another line of print.

In summary, during operation, the printer control receives electrical digital signals in the form of binary coded characters corresponding to print characters **24**, stores a plurality of these characters corresponding to a complete line of print and compares the stored characters with the set of presented characters as indicated by the photodetectors **54** and selectively stops character discs **22-n** in accordance with that comparison. When a line of print is stored, disc drive clutch **48** is engaged by the printer control to rotate clutch drum **29**. As clutch drum **29** rotates, character discs **22-n** are selectively stopped until a complete revolution of clutch drum **29** has been made and a full line of print characters **24** corresponding to the line of stored characters is present at the aligned print locations **28-n**. The printer control then actuates a print bar clutch (not shown) to impact the printing bar **34** and, thus, paper **36** against the line of selected print characters **24** at the print locations **28-n**. The printer control then deenergizes or resets all of the selector coils **35** to release all of the character discs **22-n** and engages a reset clutch (not shown) to move the reset bar **62** into the path of engagement **64** of stop surfaces **60**. Upon the next complete revolution of clutch drum **29**, all of the character discs **22-n** are reset, reset bar **62** is moved out of the path of engagement **64** and a new line of print may be selected. If another line of stored characters is not present, the printer control disengages character disc drive clutch **48** to allow motor **46** to idle until a new line of characters is received. If another line of stored characters is present, the process is repeated.

Referring now to FIGS. **5***a* and **5***b*, a preferred embodiment of the printer control is shown in block form in which the flow of data is shown in dashed lines and control signals are indicated by solid lines. The data in the form of binary coded characters (a binary 1-state represented by a high voltage and a binary 0-state represented by a low voltage) appears on data input lead **100** and enters receiving register **102** in a serial-by-character fashion with the characters entering in either a parallel-by-bit or serial-by-bit fashion. If the printer control is operated in a synchronous system, a data input clock signal transmitted with the data appears on data input clock lead **104**, In a synchronous system, this clock signal is provided to enable the receiver to distinguish between the various bits and characters. For purposes of illustration only, the printer control will be described as operating in such a synchronous system.

Two checks are performed on the incoming data as it is received. The first check is a receive parity check to verify the accuracy of transmission and reception of data. It is performed by a bit parity compare circuit block **106**. Error detection by parity check involves transmitting each character with either an odd or even number of 1-state bits and then checking the received character to determine whether it also has the odd or even number of 1-state bits as transmitted. Each character comprises a plurality of information bits, such as seven, and one parity bit. If the information bits have an even number of 1-state bits, a 1-state is provided in the parity bit, and, if there are an odd number of 1-state information bits, a 0-state is generated in that parity bit, thus maintaining the odd parity of the seven bit information character in the full eight bits of the transmitted character.

If the bit parity compare circuit block **106** detects a character having the wrong parity, it generates a wrong parity signal which is coupled to a character transfer/error symbol enable block **108** which generates an error symbol enable signal at the end of each erroneous character in response thereto. The error symbol enable signal is coupled to an error symbol generator block **110** which, in turn, transfers the code of an error symbol, such as an asterisk, to a character store block **112** in place of the erroneous character. This error symbol will eventually appear in the printed line at the location of the erroneous character and will indicate to the reader that an erroneous character was received. This feature is particularly important where an erroneous character could not be easily detected from the context of the other printed matter, as where the message comprises all numerals.

If the parity is proper, the character transfer/error symbol enable block **108**, upon completion of reception of the character by receiving register **102**, generates a character transfer enable signal to enable character transfer block **114** which, in response thereto transfers the complete character in receiving register **102** to the character store block **112** in a parallel-by-bit fashion. The character is stored in character store block **112** on a temporary basis until it can be transferred to another memory, as will be explained hereinafter.

The other aforementioned check performed on the received characters is provided by a line feed and print detect block **116**. Typically, a nonprinting control function character is transmitted at the end of each line of print to indicate to the printer control that a line of characters has been received, a new line should be started and that the printing cycle may commence. The line feed and print detect block **116**, upon detecting reception of this control character, generates a new line signal which activates a character disc drive clutch circuit block **118** to engage character disc drive clutch **48** to initiate presentation and selection of the print characters, as previously explained. The new line signal also activates a line feed clutch circuit block **120** to engage the line feed clutch (not shown) associated with printing roll **34** to advance the paper to a new line and, further, enables transfer of the stored characters from one memory to another as will be explained in more detail hereinafter.

Each character which is transferred from either receiving register block **102** or error symbol generator **110** to character store block **112** is provided with a character address by character address circuit block

122. Character transfer/error symbol enable block 108 generates a transfer signal to address advance/compare inhibit block 124 which, in turn, generates an advance signal to character address block 122 to provide a new address.

An overflow detect circuit block 126 monitors the character address and, if the address reaches a preselected count, such as 72, corresponding to a full line of print, it generates an overflow signal which activates the print disc drive clutch block 118 and line feed/-clutch block 120. The overflow detect signal also enabes transfer of the stored characters in the same manner as the new line signal, and either of these signals may be considered to comprise a line transfer enable signal. Detection of an overflow condition is done to prevent loss of data which would otherwise occur if an overfilled line condition was presented by virtue of transmission of a number of characters between control function characters which exceeds the maximum number corresponding to a full line of print, as may happen where inadvertently a control character is not transmitted at the end of the line.

In either case, upon detection of the control character or upon occurrence of an overflow condition, character address block 122 is reset to a preselected starting address. A manual address select block 128 is provided to allow manual selection of the address to which the character block 122 is reset, thus enabling manual selection of the left margin. This feature is quite useful where printed paper formats are being used which require a fixed left hand margin and results in a saving of transmission time by eliminating the requirement for "spacing over" each time a new line is started.

As each character is stored in character store block 112, its address, as provided by a character address block 122, is compared by a character/line address compare block 129 with the address of a storage location in line storage recirculating memory block 130 (FIG. 5*b*), as provided by line/print address block 132. Any one of several types of memories would be suitable, but for purposes of illustration the line storage block 130 will be described as comprising a recirculating memory which recirculates at a rate determined by clock 134. Line/print address block 132 comprises a counter which assumes a unique count, or line storage character address, as each corresponding character storage location in line storage memory block 130 is presented at data input access point 136.

Clock 134 operates at a much greater rate than the data input clock so that access to each storage location, ao indicated by the line address, is provided before the next transmitting character can be received. When the character address and the line address compare, address compare block 129 generates a compare signal on output 131 to character to line store transfer control block 138. Transfer control block 138, in response to the compare signal, generates a transfer enable signal on output 139 which enables character store block 112 to transfer the character stored therein to data input access point 136 through character output 141. Transfer control block 138 also generates a transfer enable signal to enable line storage memory 130 to receive and store the character.

Once the character is entered into the line storage memory, character advance/compare inhibit block 124 gives an inhibit command to compare block 129 to prevent resampling of the contents of the character storage block 112 during subsequent periods of access to that location. When the next character is entered in the character storage block 112, the character address block is updated by one count and compare block 129 is again enabled so that during input access to the corresponding storage location indicated by line address circuit block 132, a new character may be entered into the storage location immediately following the one previously entered.

The outputs of both the line feed and print detect block 116 and the overflow detect block 126 are coupled together at output 137 which is connected to line store to line print memory transfer control block 138. As stated, when either the new line signal or overflow signal is generated, which indicates that a line of print has been received and entered into the line store memory, it appears on output 137 as a line transfer enable signal which enables the transfer control block 138 to transfer the line of characters to line print memory 138. The line storage and line print memories recirculate and the line print address block 132 advance, all at the same rate as determined by clock 134. Thus, the count of address block 132 simultaneously represents corresponding storage locations of both line print memory 136 and line storage memory 130, and an address compare to enable transfer between these memories need not be provided.

After all of the coded characters previously stored in line storage memory 130 are transferred to line print memory 136, the actual printing cycle begins. The characters in line print memory 136 successively appear at line print character compare register block 140 and are compared with the presented characters 142, as indicated by character code disc or presented character detect block 144, by presented/stored character compare block 146. To avoid false comparison while the characters are being entered into the compare character register 140, a character compare inhibit block 147 inhibits character compare block 146 except when a full character has been entered.

A character selector circuit 150 is provided for each of selector coils 35 and, as each stored compared character appears at character compare register 140, a character select enable block 148 detects its address and enables an appropriate character selector circuit 150-n. If the store character in register 140 compares with the character presented, a compare signal is generated which is coupled to all of the selector circuits 150-n. The enabled character selector circuit 150-n, in response to the compare signal, energizes the selector coil 35 to select the presented character 142 at the point location corresponding to the address of the stored character being compared.

During presentation of each print character 24, all of the stored characters are successively entered into register 140 and compared therewith and the presented print character at the locations corresponding to the addresses of the stored characters which compare therewith are selective. For example, if the coded character "A" was stored in print address No. 1 and print address No. 70, print character "A," as it is presented at all print locations, is selected at print locations 28-n and 28-70. The next character is then presented and selected at the appropriate print locations and so on, until all of the print characters 24 corresponding to the stored characters in the line print memory 136 have been selected.

After the full line of print characters has been selected, as indicated by presented character detect block **144** detecting a disc cycle complete character after all of the characters have been presented, a printer status and control circuit block **152** activates a printing bar clutch block **154** to engage the printing bar clutch (not shown) to simultaneously impact the print receiving material with the selected print characters. After the line is printed, printer status control circuit block **152** generates a signal to clear line print memory **136,** generates a reset signal to eset all the character selector circuits **150-n** and activates reset bar clutch block **156** to engage the reset bar clutch (not shown) which repositions the character discs, as previously explained.

After the character discs are repositioned, printer status control circuit block **152** provides a printer cycle complete signal on output **157** to print disc drive clutch circuit **118** to disengage print disc drive clutch **48** until generation of the next line transfer enable signal. During the entire printing cycle, a new line of characters may be received and stored in line storage recirculating memory **130** and, upon generation of a line transfer signal, the printing cycle for the new line is repeated.

Referring to FIGS. **6***a* and **6***b*, a particular printer control circuit is shown with illustrative logic circuits corresponding to the circuit blocks of FIGS. **5***a* and **5***b* indicated by the same reference numerals. The printer control circuit is designed to receive data synchronously in a nonreturn-to-bias coding system, but could operate asynchronously or could receive data in any of the many digital formats by making only slight alterations therein.

The received characters appearing on data input lead **100,** as previously explained, comprise binary coded characters as illustrated by a wave form **302** of one such character. For purposes of illustration, the format of the received characters will be presumed to comprise seven information bits **303,** numbered one through seven, and one parity bit, bit number eight. A binary 1 or 1-state is represented by a high voltage as shown in bit numbers three, five and six, and a binary 0 or 0-state is represented by a low voltage, as shown in bit numbers one, two, four, seven, eight of wave form **302.** Each character is represented by a unique combination of 1-state and 0-state bits. For example, the character represented by wave form **302** might be the letter "Z." A "space" might be represented by a character code of all seven bits in the 0-state. The period of each bit is defined by the period of an input clock signal as illustrated by wave form **304,** with each time period between successive clock pulses defining successive bits. In an odd parity system, as will be described herein the parity bit, bit number **8,** is in the 1-state, if and only if, there are an even number of 1-state information bits and in the 0-state, if and only if, there are an odd number of 1-state information bits. Thus, if the full 8-bit character is not erroneous, it has an odd number of 1-state bits.

Receiving register **102** comprises a shift register having eight stages **R1** through **R8,** one stage being provided for each of the bits in a character. The voltage appearing on input **306** of each of the stages enters that stage and appears at its output **308** in response to a negative transition (i.e., a transition from a 1-state to a 0-state) of the data input clock signal **304** on clock input lead **104.** The input **306** of each stage is connected to the output **308** of the next stage, so that the state present in each stage shifts to the next stage on each negative clock transition. Thus, the state of bit number one first enters register stage **R8,** then register state **R7,** etc., and, as bit number one enters stage **R7,** bit number two enters stage **R-8,** etc. After eight clock pulses, a full eight bit character is entered into receiving register **102** with bit number one in shift register stage **R1** and the parity bit, bit number eight in shift register stage **R8.** Although the characters are received in a serial-by-bit fashion, they could be entered in a parallel-by-bit fashion by providing an entire register for each bit.

The bit parity compare circuit **106,** which performs the parity check on the received characters, comprises a NAND gate **310** having an input **312** coupled to the clock input lead **105,** an input **314** coupled to output **308** of the parity bit storing shift register stage **R8,** and an output **316** coupled to toggle input **318** of monostable multivibrator or flip-flop **320.** The output of a NAND gate assumes a 0-state if, and only if, all of its inputs are in a 1-state, and, thus, each time a 1-state is entered into shift register stage **R8,** output **316** makes a negative transition from a 1-state to a 0-state. This transistion toggles flip-flop **320** (i.e., causes its outputs, normal or Q output **320** and inverting or $\overline{Q}$ output **322,** to exchange states). Flip-flop **320,** prior to reception, is in a 0-state with its Q output in the 0-state, and its $\overline{Q}$ output in the 1-state. Thus, upon the entering of a full character, it will be in the 1-state, if the character has an odd parity, and in a 0-state, if the character has an even bit parity.

Normal output **321** and inverting output **322** are coupled to character transfer/error symbol enable block circuit **108** which determines when a full character has entered into receiving register **102** to enable character transfer circuit **114,** if the character has the proper, odd bit parity, or to enable error symbol generator **110,** if the character has an improper, even bit parity, as indicated by the normal and inverting outputs **321** and **322** of flip-flop **320.**

Transfer/enable circuit **108** includes a three-stage binary counter **324** which has its toggle input **325** coupled to clock input lead **104** to count the clock pulses thereon and a three-input AND gate **326,** which has an input coupled to the normal output of each of the stages of counter **324** to detect, and generate a 1-state pulse on its output **328** during, every eighth clock pulse. Output **328** is coupled to input **330** of AND gate **332** and to input **334** of AND gate **336** and comprises one of three outputs of transfer/error enable circuit **108.** Normal output **321** is coupled to input **338** of AND gate **336** and inverting output **322,** which carries a signal in the opposite state of normal output **320,** and to input **340** of AND gate **332.**

The output of an AND gate assumes a 1-state if, and only if, all of its inputs are also in the 1-state. As explained, if the received character has odd parity, input **338** is in the 1-state when output **328** switches to the 1-state on the eighth input clock pulse, and, thus, AND gate **336** generates a 1-state transfer pulse to enable character transfer circuit **114.** The transfer enable pulse is also coupled to a clear direct input **311** of flip-flop **320,** which is cleared in response thereto so that normal output **321** will be in the 0-state at the beginning of reception of the next character. However, if the received character has an even parity, input **340** is in

the 1-state when output 328 switches to the 1-state, and AND gate 332 generates a 1-state pulse to enable error symbol generator circuit 110. In either case, upon reception of a complete character, AND gate 326 generates a 1-state pulse which comprises the aforementioned line transfer signal for address advance/compare inhibit circuit 124 and an inhibit signal for line feed and print detect circuit 116, as will be explained in more detail hereinafter.

Character transfer circuit 114 comprises a plurality of NAND gates T1 through T7, each having an input 342 coupled to an output 308 of receiving register stages R1 through R7, respectively. Each of NAND gates T1 through T7 also has an input 344 coupled to the output of AND gate 336 which provides the character transfer enable pulse, as explained.

The outputs of NAND gates T1 through T7 are respectively coupled to clear direct inputs 346 of shift register stages C1 through C7 of a shift register 343 which comprises character store circuit 112. A 1-state enters each stage whenever its set direct input 346 assumes a 0-state. While the character is being entered into the receiving register 102, inputs 344 are in a 0-state, and clear direct inputs 346 are in a 1-state, but, upon completion of reception of the character, if the parity is proper, the 1-state, character transfer enable pulse coupled to inputs 344 enables of NAND gates T-1 through T-7, and those transfer NAND gates which have their input 342 coupled to a receiving resister stage having its output 308 in the 1-state, switch to a 0-state to enter a 1-state into the character store shift register state to which they are connected. Thus, if the character represented by wave form 302 was stored in receiving register 102 with shift register stages R-3, R-5 and R-6 in the 1-state and register stages R-1, R-2, R-4, R-7 and R-8 in the 0-state, upon transfer, the coded character would appear in character store 112 with shift register stages C-3, C-5, C-6 in the 1-state and shift register stages C-1, C-2, C-4 and C-7 in the 0-state. The parity bit is not transferred for it is a known quanity and carries no information. After the character is shifted out of character store, shift register 343, shift register stages C-1 through C-7 are again in a 0-state and a new character may be entered.

The error symbol generator circuit 110 comprises a plurality of inverter gates E-2, E-3, E-5 and E-7 having their outputs 348 respectively coupled to set direct inputs 346 of character store, shift register stages C-2, C-3, C-5 and C-7 and having their inputs 350 coupled to the output of AND gate 332 which, as previously explained, provides the error symbol enable pulse. While the character is being entered into receiving register 102, inputs 350 of the error symbol inverter gates E-2, E-3, E-5 and E-7, and inputs 344 of transfer NAND gates T-1 through T-7 are in a 0-state and, thus, set direct inputs 346 are in a 1-state. Upon completion of reception of an erroneous character; i.e., one having an even parity, the error symbol enable pulse is generated, inverted by inverter gates E2, E3, E5 and E7 and appears as a 0-state pulse at the appropriate set direct inputs 346 to enter a 1-state in the character store stages T2, T3, T5 and T7. The remaining character store stages remain in the 0-state, since the character transfer enable pulse is not generated. This code combination of a 0-state in shift register stages T1, T4 and T6 and a 1-state in shift register stages T2, T3, T5 and T7 represents an error symbol which will later appear on the printed line at a location where the erroneous character would appear if correct. It should be appreciated that this code combination is arbitrary and a different error symbol could be obtained by simply coupling the error symbol inverter gates to different shift register stages of shift register 343.

The character address circuit 122 which provides an address for each of the characters stored in character store register 343 comprises a plurality of flip-flops B1, B2, B4, B8, B16, B32 and B64 connected to operate as a binary counter 351 capable of counting up to the maximum number of characters in a line of print, such as 72. The toggle input 352 of the first stage of counter 351, flip-flop B1, is coupled to the normal output 354 of a dynamic S-R flip-flop 356 which comprises the address advance/error inhibit circuit 124 discussed previously. Output 328 of AND gate 326 is coupled to reset input 358, and each time the transfer pulse thereon makes a negative transition from the 1-state to the 0-state after the transfer to the character store register is complete, normal output 354 and, thus, toggle input 352 switch to a 0-state, which advances character address counter 351 by one count.

As previously explained, character/line address compare circuit 129 generates a 1-state, compare pulse on output 360 when the line address corresponds with the character address. This compare pulse enables the character to line store transfer control circuit 138 to transfer the character into line storage recirculating memory 130, as will be explained in more detail hereinafter. Compare circuit 129 is inhibited from generating another compare pulse during the period after the character has been transferred to character store circuit 112 and before a new character has been entered to prevent subsequent entrance into the line storage memory of an all 0-state character in place of the transferred character. An inhibit input 355 of compare circuit 129 is coupled to normal output 354 of flip-flop 356 and, when in the 1-state, inhibits generation of the compare pulse. As explained, normal output 354 switches to the 0-state in response to the negative transition of the transfer pulse, and the compare circuit is enabled. When the character address and line address compare, output 360 switches to the 1-state, remains in the 1-state until the transfer is complete and then returns to the 0-state. This negative transition of the compare pulse is coupled to set input 362 which switches normal output 354 and, thus, inhibit input 355 back to the 1-state to inhibit further comparison. The next transfer pulse resets flip-flop 355 and the compare and inhibit cycle is repeated.

Character to line store transfer control circuit 138 (FIG. 6*b*) comprises a plurality of logic gates which, upon being enabled by the compare pulse from compare circuit 129, couple output 141 of character store circuit 112 with data input access point 136 of line storage memory 130. The line storage recirculating memory comprises a recirculating shift register 380, driven by clock circuit 134, and having a sufficient number of stages 382 to store a full line of print. Clock circuit 134 drives both shift register 380 and character counter 384 which is capable of counting up to the maximum number of characters in a full line of print and comprises line/print address circuit 132. Thus, line/print address counter 384 recycles at the same rate as line storage shift register 380 recirculates, with the counter advancing by one count each time a character storage

location is presented at input data access point **136.** The clock circuit **134,** which may comprise any suitable free running oscillator, operates at a much greater rate than the data input clock so that line storage shift register **380** recirculates through an entire cycle during storage of each character in character store circuit **122.**

During the interval between compare signals the characters recirculate through NAND gates **386** and **388** of transfer control circuit **138,** being twice inverted thereby. Output **141** of character storage circuit **112** (FIG. **6***a*) is coupled to input **392** of NAND gate **394** (FIG. **6***b*) which has its other input **393** coupled to output **131** of character/line address compare circuit **124.** The toggle inputs **396** of the shift register stages of character store shift register **343** are coupled to the character transfer enable output **139** of AND gate **398** which as one input **397** coupled to the clock circuit **134** and the other input **401** coupled to output **131** of compare circuit **129.**

The compare pulse, which indicates that the storage location for the address of the character stored in character storage circuit **112** is at input data access point **136,** enables AND gate **398** to couple the clock pulses from clock circuit **134** to toggle inputs **396** of the character store circuit which, in response thereto, shifts the character stored therein to input **392** of NAND gate **394.** Simultaneously, the 1-state compare pulse is inverted to a 0-state pulse by inverter gate **403** and coupled to input **400** of NAND gate **386** which assumes a **1**-state in response thereto. NAND gate **394** which is enabled by the compare pulse, inverts the voltage states of the character bits appearing at input **392** and again inverts the character bits and applies them to input **402** of NAND gate **388** which shifts them into the line storage shift register **380.** When the entire character has been entered, the compare pulse switches **9**back to a 0-state to enable NAND gate **386** to transfer the recirculating stored characters.

After a complete line of characters has been stored in the line storage shift register **380,** as indicated either by generation of the 0-state line transfer enable pulse on output **137** from line feed and print compare circuit **116** or overflow detector circuit **126,** the line of characters is transferred to line print memory circuit **136,** line storage memory **102** is cleared and character address circuit **122** is reset. Line feed and print compare circuit **116** comprises a NAND gate **364** having seven of its inputs coupled to the appropriate normal or inverting outputs of shift register stages **R1** through **R7** and an eighth input **405** coupled to output **328** of AND gate **326.** After a full character has been entered into the receiving register **102,** output **328** and, thus, input **405** switch to a 1-state and a compare is made. As illustrated in FIG. **6***a*, the other seven inputs of NAND gate **364** are coupled to the normal outputs of stages **R1, R2, R5** and **R6,** and to the inverting outputs of stages **R3, R4** and **R7.** When the control character is entered into receiving register **102,** shift register stages **R1, R2, R5** and **R6** are in the 1-state, and stages **R3, R4** and **R7** are in the 0-state, all of the inputs to NAND gate **364** are in the 1-state and, thus, output **366** of NAND gate **364** and output **137** switch to the 0-state.

As explained, if a control character is not received after reception of a preselected number of characters, overflow detect circuit **126** generates a line transfer enable pulse. Overflow detect circuit **126** comprises a NAND gate **368** having its inputs coupled to the outputs of the appropriate flip-flop stages of character address counter **324** to detect a count corresponding to the maximum number of characters in a full line of print, such as **72.** When the count reaches this preselected number, all of the inputs of NAND gate **368** are in the 1-state and output **370** of NAND gate **368** and output **137** switch to a 0-state.

The line transfer enable pulse on output **137** is coupled to character disc drive clutch circuit **118,** line feed clutch circuit **120,** character to line store transfer control circuit **138** and manual address select circuit **128,** each of which perform their respective functions in response thereto. The line transfer enable pulse activates the print disc drive clutch circuit **118** to engage character disc drive clutch **48** to initiate presentation of the print characters, activates line feed clutch circuit **120** to advance the paper by one line, resets character address counter **351** through manual address select circuit **128,** activates line store to line print memory transfer control circuit **138** to enable transfer of the line of characters in the line storage memory to the line print memory circuit **136** and causes the line store memory to be cleared after the line transfer is complete.

The manual address select circuit **128** comprises a 10 position rotary switch **406** for selecting the "units" position of the left-hand margin and an eight position rotary switch **408** for selecting a "10s" position of the left-hand margin. The position of switches **406** and **408** determines the count to which character address counter is reset at the beginning of each new line and, thus, determines the location of the left-hand margin. For example, with switch **406** in position **M3** and switch **408** in position **M20,** the character address circuit **122** in response to the line transfer enable pulse is reset to counter number **22** and, when the first received character of the new line is received, address counter **351** is advanced by one count to **23,** which is the new location at which it will eventually appear. The counter will advance consecutively by one count as each subsequent character is received until it is again reset to count **22** at the completion of the next line.

The center terminals **410** and **411** of switches **406** and **408** are coupled through inverter gate **410** to line transfer enable output **137** and the switch contacts **M0** through **M9** of "units" switch **406,** and switch contacts **M00** through **M70** of "10s" switch **406,** are coupled to the appropriate set direct inputs **412** and clear direct inputs **414** of the binary counter stages of character address counter **351.** Each flip-flop stage of counter **351** assumes a 1-state in respone to the 1-state pulse applied to its set direct input **412** and a 0- state in response to the 1-state pulse applied to its clear direct input **414.** As illustrated in FIG. **6***b*, contact **M3** is connected to set direct input **112** of binary counter stage **B2** and to clear direct input **114** of counter stage **B1,** while contact **M20** is connected to set direct inputs of counter stages **B4** and **B16** and to clear direct inputs of stages **B8, B32** and **B64.** Hence, when switches **406** and **408** are in the appropriate positions corresponding to a left-hand margin location of **23** the 1-state, inverted line transfer enable pulse from inverter gate **410** pulse is applied through the switch contacts **M20** and **M3** to these set direct and clear direct inputs to reset the counter to a binary count of 22. The remaining switch contacts are similarly connected.

Also in response to the line transfer enable pulse, the line storage/print memory transfer control circuit **138**

transfers an entire line of characters in line storage recirculating memory **130** into line print memory circuit **136**. The line print recirculating memory circuit **136** comprises a recirculating shift register **437** identical to that of the line storage memory and is also driven by clock **134**. Thus, the line storage memory, the line print memory and the line print address circuits operate in synchronism, which allows the line/print address counter to simultaneously provide the address for both memories which eliminates the need for an address compare during address transfer from one to the other, as is required during the transfer from character store circuit **12**.

Line store to line print memory transfer control circuit **138** comprises a NAND gate **420** for transferring the characters from the line store to the line print memory, and a NAND gate **422** for allowing recirculation of the line print memory except during transfer. During the interval between line transfer enable pulses, input **424** of NAND gate **420**, which is coupled to line transfer enable output **137** through inverter gate **426**, is in a 0-state which keeps NAND gate **420** disabled from transferring any characters. Input **428** of NAND gate **422** is directly coupled to line transfer enable output **137** and, thus, during the interval between line transfer enable pulses maintains its output in a 1-state to enable recirculation through inverter gate **439** and NAND gate **422**.

The output of NAND gate **386** which inverts the data recirculating through line store shift register **380** is coupled to input **441** of NAND gate **420**. Upon generation of the line transfer enable pulse, input **424** switches to a 1-state which enables NAND gate **424** to invert the once inverted data at input **441** and apply the twice inverted data signals to data input access point **443** of line print register **437**. The 0-state transfer enable pulse coupled to input **428** also disables NAND gate **422** from recirculating the inverted data signals from inverter gate **439** applied to input **443**. When the line transfer enable pulse terminates, all of the characters are entered into line print register **437**, and inputs **424** and **428** switch states to respectively disable further transfer and enable recirculation.

After a sufficient period of time to transfer all of the characters to the line print memory circuit, the line transfer enable pulse returns to the 1-state. Output **137** is coupled to input **431** of monostable multivibrator or single-shoft **430**, and in response to this positive transition of the line transfer enable pulse, the output **429** of single-shot **430**, which is coupled to data input access point **136** assumes a 0-state for a sufficient length of time to clear line storage shift register **380**; that is, to enter 0-states into all of register stages **382**. After the line store memory is cleared, output **429** returns to the 1-state, and storage of a new line of characters therein may commence.

The data output **445** of line print register **437** is coupled to input **447** of AND gate **439** which has its input coupled to data input access point **441** of line print character compare register **140** and, thus, as the characters recirculate, they are successively shifted into line print compare character register **140**. Compare character register **140** comprises a seven storage shift register **436** having shift register stages S1 through S7 which are driven by clock **134** and are thus in synchronism with line print register **473** and line/print address couner **384**.

As each stored character is entered into compare register **436**, a selector circuit **150-n** corresponding to the address of that character is enabled by a binary coded decimal to decimal converter circuit or character selector circuit **148**. Converter circuit **148** has an input **440** coupled to the output of each of the flip-flop stages of line/print address counter **389** and produces a 1-state pulse on one of its 10 "units" outputs **442** and on one of its eight "10s" outputs **444** to indicate the decimal equivalent of the binary count of the register. For example, when the character having a print address of **52** is entered into compare register **436**, a 1-state pulse will appear on the number **50** "10s" output **444** and on the number two "units" output **442**.

A different pair of outputs from converter circuit **148**, one from "units" outputs **442** and one from "10s" outputs **444**, are coupled to an enabling NAND gate **446** of each of the selector circuits **150-n**. For example, as shown in FIG. **6***b*, enabling gate **446** of selector circuit **150-1** for print location number one has an input coupled to the number one "units" output and the number zero "10s" output. Similarly, enabling NAND gate **446** of selector circuit **150-72** has an input coupled to the number two "units" output and the number 70 "10s" output. Only when the character is stored in character compare register **436**, will the input pair to NAND gate **446** of the selector circuit **150-n** corresponding to the address of that character be in a 1-state and, thus, only during the storage of that character in compare register **436** will the selector circuit **150-n** stop the character disc at the print location corresponding to that address be enabled. All of the remaining selector circuits are disabled.

The outputs **445** of each of compare register stages **S1** through **S7** are respectively coupled to inputs **447** of presented/stored character compare circuit **146** which may comprise any suitable matrix of inhibit gates or the like and need not be shown in detail. All of the characters stored in line print register **437** are successively entered into character compare register **436** and compared with the presented print characters during presentation of each of the characters. phototransistor preamplifiers A1 through A7, respectively, coupled to and responsive to phototransistors P1 through P7 and operating in cooperation with character code disc **52**, provide an indication of which characters are being presented. As previously explained, character code disc **52** rotates with the unselected character discs and presents a unique code combination of code holes **57** between light source **56** and selected ones of photodetectors **54**, phototransistors P1 through P7, during presentation of each of the unselected characters. The preamplifiers which have their phototransistors aligned with a code hole **57** and are, thus, impinged by the light **451** from light source **56**, such as preamplifiers A6 and A7 as illustrated in FIG. **6***b*, generate a 1-state pulse on output **453**, and those preamplifiers, such as A1, whose phototransistors are not impinged by the light **451** because a code hole **59** is not aligned therebetween, maintain a 0-state on each of their outputs **453**.

When the output states of the preamplifiers A1 through A7 respectively correspond to the states of the compare register stages S1 through S7, compare circuit **146** generates a 1-state compare pulse on output **455** which is coupled to an input **457** of AND gate **448**. Another input **459** to AND gate **449** is coupled to a preamplifier AT which generates 1-state clock pulses in

response to a phototransistor PT being impinged by light from light source **56** when clock code holes **59** is in alignment therewith. Clock code hole **59** is presented to phototransistor PT during the trailing edge of each group of character code holes **57** and has a greater resolution than character code holes **57**; i.e., clock code holes **59** are smaller in diameter than the character code holes **57**. The provision of clock code hole **59** insures that a compare pulse will not be generated until all of the character code holes of each character code **61** have aligned with tieir respective phototransistors which, in turn, have had sufficient time to switch on in response thereto.

A third input **463** of AND gate **448** is coupled to output **465** of AND gate **467** of character compare inhibit circuit **147** which generates a 1-state pulse thereon as each complete character is entered into character compare register **436**. Until an entire character has entered into character compare register **436**, output **465** and, thus, input **463** are maintained in a 0-state to inhibit generation of the compare pulse by AND gate **448**. When all of the inputs to AND gate **448** are in the 1-state indicating that a complete character is stored in compare register **436** and that it compares with the presented character, it generates a 1-state compare pulse on output **449**, which is coupled to inputs **451** selector enable AND gates **446**. However, only the AND gate **446** corresponding to the address of the stored character being compared is enabled during this period and, thus, only that selector circuit can respond thereto. The enabled NAND gate **446** generates a 1-state set pulse on output **455** which sets an S-R flip-flop or latch circuit **450** of the enabled selector circuit **150**-n. The normal output **452** of latch circuit **450** assumes a 1-state in response to the set pulse which is inverted by inverter gate **454** and coupled to an NPN transistor **456** which turns on in response thereto to energize the selector coil **458** to stop the character disc with the selector character at the print location.

After all of the stored characters have been compared with the presented character, the appropriate latch circuits **450** set and the corresponding selector coils **458** energized, another character is presented and the process is repeated. After all the characters have been presented and the appropriate ones selected, a disc cycle complete character code is presented by code disc **52** and detected by AND gate **460** of printer status/control circuit **152** which generates a 1-state, disc cycle complete pulse on output **461** in response thereto. The disc cycle complete pulse is coupled to AND gate **462** which generates an identical 1-state pulse on output **463** to activate a printing bar clutch circuit **463** to engage the printing bar clutch, as previously explained. Output **461** of AND gate **460** is also coupled to input **465** of a monostable multivibrator or single-shot **464** which, after a sufficient time for the impact printing action to be completed, generates a 0-state clutch cycle complete pulse on output **467**. The clutch cycle complete pulse on output **467** is coupled to all of the reset inputs **469** of latch circuits **450**, input **471** of AND gate **435** data input access print **443** of line print register **437**, and input **473** of reset bar clutch circuit **475** which, in response thereto, respectively reset all the latch circuits **450**, clear line print register **437** and character compare register **436**, and energize the reset bar clutch circuit **475** to engage the reset bar clutch (not shown). The clutch cycle complete pulse is also coupled to toggle input **477** of a toggle flip-flop **468** which s set in response thereto.

Clutch drum **29** and, thus, character discs **22**-n continue to rotate to reset the character discs until, after a complete revolution, the disc cycle complete character code is again detected by AND gate **460** which generates another 0-state pulse in response thereto. Since flip-flop **468** was set with inverting output **470** and, thus, input **479** in the 0-state, AND gate **462** is disabled and its output **465** remains in the 0-state. However, previously disabled AND gate **474** is enabled by the 1-state of normal output **472** of flip-flop **468** and generates a printer cycle complete pulse in response to the second disc cycle complete pulse on output **477**. The printer cycle complete pulse on output **477** is coupled to print disc drive clutch circuit **118** which disengages the drive clutch **48** in response thereto to allow drive motor **46** to idle until generation of the next line transfer enable pulse. Upon generation of the next line transfer enable pulse, the process is repeated to print another line of characters.

What is claimed is:

**1.** A control for a printer having a plurality of print locations, each of which is successively presented with an ordered sequence of characters, one character at each location being selectable for simultaneous printing, comprising:

means for receiving information in the form of binary coded characters in serial fashion corresponding to said presented characters, each coded character containing a pre-selected number of bits, one of said received coded characters representing a non-printing control function;

character storing means for storing at least one character, said receiving means upon receiving a first character transferring a second character to said character storing means, said character storing means including a line store memory for storing a plurality of characters corresponding to a full line of print at a plurality of line store character storage locations, and means for providing an address for each of said line store storage locations, a line print memory for storing said plurality of characters in a plurality of line print character storage locations, and means for providing an address for each of said line print storage locations;

means for comparing the presented characters with the stored characters;

means for selecting a presented character at each location in accordance with said comparison;

means for actuating said selecting means to initiate selection of said presented characters in response to reception of said control function character; and

means for actuating said printer, after a character has been selected at each of said locations, to print all of said selected characters.

**2.** The printer control of claim **1** wherein said receiving means receives said bits in a serial fashion.

**3.** The printer control of claim **2** including means operably associated with said receiving means for providing an address for each character transferred to said character storing means.

**4.** The printer control of claim **3** wherein said address is a count representing the print location at which the character is to be selected.

**5.** The printer control of claim **3** including means operably associated with said receiving means for manu-

ally preselecting the address of the first character of each group of characters representing a line of print.

6. The printer control of claim 1 wherein said receiving means comprises a serial shift register.

7. The printer control of claim 1 wherein said received characters have a preselected bit parity and said control circuit includes means operatively associated with said receiving means for detecting an improper parity.

8. The printer control of claim 7 including means responsive to detection of an improper parity to store an error character in place of the character having the improper parity.

9. The printer control of claim 1 including means operably associated between said line print memory and said actuating means for actuating said selecting means to initiate selection of said presented characters in response to reception of a preselected number of characters corresponding to a full line of print.

10. The printer control of claim 1 including means operably associated between said receiving means and said character storing means for detecting an erroneous character and means responsive to said detector for transferring an error character to said character storing means in place of the erroneous character.

11. The printer control of claim 1 including means operably associated between said receiving means and said line store memory for transferring each character to a line store storage location having an address corresponding to the character address thereof.

12. The printer control of claim 1 wherein said line memory comprises a recirculating memory.

13. The printer control of claim 1 wherein the address providing means for said line print memory comprises the address providing means for said line store memory.

14. The printer control of claim 1 including means operably associated between said line store memory and said line print memory to transfer the characters from said line storage locations to the corresponding line print memory locations in response to the reception of a control character.

15. The printer control of claim 14 wherein said selecting means selects the presented character, at each print location corresponding to the address of the stored character that compares therewith.

16. The printer control of claim 1 wherein both said line storage memory and said line print memory comprise recirculating memories, both of said recirculating memories recirculating at the same rate.

17. In a printer having a plurality of type carrying members, each of said members carrying a plurality of type characters, drive means operatively connected to said members for moving each of said members to present successive characters on each member at respective aligned print locations, a character selector associated with each member actuatable for maintaining a selected type character on a member at its respective aligned print location, and printing means operatively associated with said members for simultaneously imprinting all of the presented type characters maintained at their respective print locations on a print receiving surface, a printing control system comprising:

a character command receiver for receiving command input information in the form of coded command characters representative of the different characters on the type carrying members, one of said coded command characters representing a nonprinting control function for initiating a character type selection process;

addressing means operatively associated with said receiver for providing each coded command character with an address representative of a print location;

recirculatory storage means operatively associated with said addressing means including a line store memory having a plurality of line store memory positions each corresponding to an address for receiving and storing a plurality of command characters at their corresponding address corresponding to a full line of print, a line print memory having a plurality of line print memory positions each corresponding to an address for receiving the stored command characters from the line store memory and generating a line print command signal representative of the line of print desired to be printed, and means associated between said line store memory and line print memory to transfer the command characters from the line store memory positions to the line print memory positions in response to the reception of the command control character;

a character detector associated with each type carrying member for sensing which character is at the corresponding print location and for generating a character detect signal representative thereof;

comparator means operably associated between said character detector and said line print memory for comparing the line print command signal with each character detect signal, said comparator means generating a character select signal for said comparator means generating a character select signal for each type carrying member whenever said compared signals for that member match signifying that the desired type character on a given type carrying member is at the desired print location;

a character selection actuator operably associated with each selector and said comparator means for actuating each selector in response to its corresponding character select signal and generating a print command signal when all of the selectors have been actuated; and

a print actuator operably associated between said character selection actuator and said printing means for actuating said printing means in response to said print command signal whereby a line of type is imprinted on the print receiving surface.

18. The printing control system of claim 17 wherein said print actuator generates a print complete signal after a line of print has been imprinted, said system including means operatively associated with said print actuator and said selectors responsive to said print complete signal for releasing said selectors to their initial state.

19. The printing control system of claim 17 wherein said information comprises binary coded characters, each character containing a preselected number of bits, wherein said receiver receives said bits in serial fashion.

20. The printing control system of claim 19 wherein said receiver includes a serial shift register.

21. The printing control system of claim 19 wherein said characters have a preselected bit parity, said control system including means operatively associated with said receiver for detecting improper parity and means operatively associated with said detecting means and

said storage means responsive to the detection of an improper parity to store an error character in place of the character having the improper parity.

22. The printing control system of claim 1 wherein said addressing means includes means operably associated with said storage means for manually preselecting the address of the first coded command character of each group of said characters with comprise a line of print.

23. The printing control system of claim 1 wherein said receiver receives a coded command character one at a time and transfers a second character to said storage means, said system including means operatively associated with said receiver for detecting an erroneous coded command character and means operatively associated with said detecting means and said storage means responsive to said erroneous character detector for transferring an error character to said storage means in place of the erroneous coded command character.

24. The printing control system of claim 17 wherein said line print command signal is generated after reception of a preselected number of coded command characters which correspond to a full line of print.

25. The printing control system of claim 17 wherein both said line store memory and said line print memory comprise recirculatory memories which recirculate at the same rate.

26. The printing control system of claim 17 wherein each type carrying member is a disc which carries the type characters in said ordered sequence on its outer peripheral surface, said type characters being presented for selection by rotation of said discs by said drive means, each selector stopping the rotation of its respective disc when the selected character thereon is presented at its print location, said character detector including a coded member mounted for rotation with each disc and means for detecting the code corresponding to the character being presented.

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# UNITED STATES PATENT OFFICE
# CERTIFICATE OF CORRECTION

Patent No. 3,796,156 Dated March 12, 1974

Inventor(s) CEDOMIR MARINKOVICH et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

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Column 6, line 55, "16" should be --61--.
Column 7, lin 62, after "104" the comma should be a period.
Column 9, line 12, "enabes" should be --enables--.
Column 9, line 51, "ao" should be --as--.
Column 11, line 11 "eset" should be --reset--.
Column 13, line 32, "state" should be --stage--.

Column 15, line 36, after "switches" delete --9--.
Column 19, line 2 "holes 59" should be --hole 59--.
Column 19, line 11, "tieir" should be --their--.
Column 20, line 2, delete "s" and substitute --is--.

IN THE CLAIMS

Column 21, line 32, before "memory" insert --store--.

Column 22, lines 33-35, delete "said comparator means generating a character select signal for".

Signed and Sealed this

eighteenth Day of May 1976

[SEAL]

*Attest:*

RUTH C. MASON
*Attesting Officer*

C. MARSHALL DANN
*Commissioner of Patents and Trademarks*