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- (71) Applicant: MICRON TECHNOLOGY, INC. [US/US];
8000 South Federal Way, Boise, Idaho 83716-9632 (US).
- (72) Inventors: PAN, Feng; 3160 Hancock Pl, Fremont, California 94538 (US). PARK, Jaekwan; 22920 Stonebridge, Cupertino, California 95014 (US). GHODSI, Ramin; 2714 Cardinal Lane, San Jose, California 95125 (US).
- (74) Agents: HEGSTROM, Brandon et al.; DORSEY & WHITNEY LLP, 701 5TH Ave, Suite 6100, Seattle, Washington 98104 (US).
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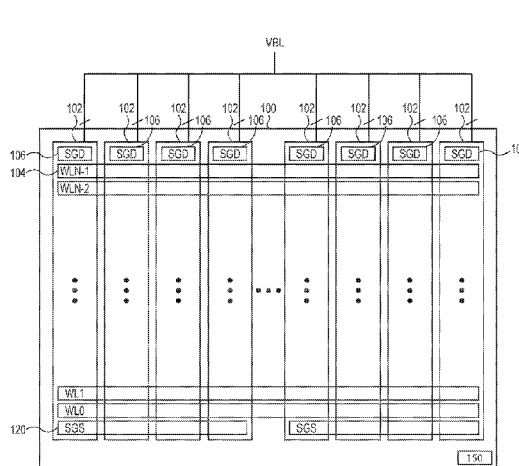


Fig. 1

(57) Abstract: Apparatuses and methods for segmented SGS lines are described. An example apparatus may include first and second pluralities of memory subblocks of a memory block. The apparatus may include a first select gate control line associated with the first plurality of memory subblocks and a second select gate control line associated with the second plurality of memory subblocks. The first select gate control line may be coupled to a first plurality of select gate switches of the first plurality of memory subblocks. The second select gate control line may be coupled to a second plurality of select gate switches of the second plurality of memory subblocks. The first and second pluralities of select gate switches may be coupled to a source. The apparatus may include a plurality of memory access lines associated with each the first and second pluralities of memory subblocks.



APPARATUSES AND METHODS FOR SEGMENTED SGS LINES

CROSS-REFERENCE

[001] This application claims priority to U.S. Non-Provisional Application No. 14/518,807 filed October 20, 2014, which application is incorporated herein by reference, in its entirety, for any purpose.

BACKGROUND

[002] Memory cell density, such as that of non-volatile memory, has been improved significantly in an effort to achieve greater storage capacity, while not significantly increasing cost or memory footprint. One widely adopted solution has been to implement memory cells in three-dimensions, for instance, using vertically oriented NAND strings.

[003] Implementing memories in this manner has presented challenges, however. By way of example, as a result of three-dimensional implementation, block sizes have increased, and as a corollary, capacitive and resistive loads generated during operation have increased as well.

SUMMARY

[004] Example apparatuses are disclosed herein. An example apparatus may include a first plurality of memory subblocks of a memory block, a second plurality of memory subblocks of the memory block, and a first select gate control line associated with the first plurality of memory subblocks. The first select gate control line may be coupled to a first plurality of select gate switches of the first plurality of memory subblocks, and the first plurality of select gate switches may be coupled to a source. The example apparatus may further include a second select gate control line associated with the second plurality of memory subblocks. The second select gate control line may be coupled to a second plurality of select gate switches of the second plurality of memory subblocks, and the second plurality of select gate switches may be coupled to the source. The example apparatus may further include a plurality of memory access lines, each memory access line of the plurality of memory access lines associated with each

memory subblock of the first plurality of memory subblocks and each memory subblock of the second plurality of memory subblocks.

[005] Another example apparatus may include a first select gate source control line associated with a first plurality of memory subblocks and a second select gate source control line associated with a second plurality of memory subblocks. The example apparatus may further include a memory subblock of the first plurality of memory subblocks including a first plurality of select gate source switches. Each select gate source switch of the first plurality of select gate source switches may be coupled to the first select gate source control line and configured to be enabled responsive to receipt of an asserted select gate control signal. The example apparatus may further include a memory subblock of the second plurality of memory subblocks including a second plurality of select gate source switches. Each select gate source switch of the second plurality of select gate source switches may be coupled to the second select gate source control line and configured to be enabled responsive to receipt of the asserted select gate source control signal. The example apparatus may further include a control unit coupled to the first and second select gate source control lines and configured to provide the select gate source control signal to each select gate source switch of the first plurality of select gate source switches using the first select gate source control line responsive to a read operation associated with the memory subblock of the first plurality of memory subblocks, and to provide the select gate source control signal to each select gate source switch of the second plurality of select gate source switches using the second select gate source control line responsive to a read operation associated with the memory subblock of the second plurality of memory subblocks.

[006] Another example apparatus may include a plurality of select gate source control lines. Each select gate source control line of the plurality of select gate source control lines may be associated with a respective plurality of memory subblocks of a block. The another example apparatus may further include a memory access line associated with each memory subblock of the block. The memory access line may be substantially parallel to each select gate source control line of the plurality of select gate source control lines.

[007] Example methods are disclosed herein. An example method may include providing, during a read operation, a first control signal on a first select gate source

control line to enable select gate source switches of a first plurality of memory subblocks of a block. The example method may further include providing, during the read operation, a second control signal on a second select gate source control line to disable select gate source switches of a second plurality of memory subblocks of the block.

[008] Another example method may include selectively providing a respective control signal on each select gate source control line of a plurality of select gate source control lines to enable select gate source switches of a plurality of memory subblocks of a block during a read operation. Each select gate source control line of the plurality of select gate source control lines may be parallel to at least one memory access line of the block.

BRIEF DESCRIPTION OF THE DRAWINGS

[009] Fig. 1 is a schematic block diagram of an apparatus including a memory block according to an embodiment of the present invention.

[010] Fig. 2 is a block diagram of a three-dimensional memory array according to an embodiment of the present invention.

[011] Fig. 3a is a schematic diagram of a NAND string of a selected subblock during a program operation according to an embodiment of the present invention.

[012] Fig. 3b is a schematic diagram of a NAND string of an unselected subblock during a program operation according to an embodiment of the present invention.

[013] Fig. 3c is a schematic diagram of a NAND string of a selected subblock during a read operation according to an embodiment of the present invention.

[014] Fig. 3d is a schematic diagram of a NAND string of an unselected subblock during a read operation according to an embodiment of the present invention.

[015] Fig. 3e is a schematic diagram of a NAND string of an unselected subblock during a read operation according to an embodiment of the present invention.

[016] Fig. 4 is a block diagram of a memory according to an embodiment of the present invention.

DETAILED DESCRIPTION

[017] Apparatuses and methods for segmented SGS lines are described herein. Certain details are set forth below to provide a sufficient understanding of embodiments of the invention. However, it will be clear to one having skill in the art that embodiments of the invention may be practiced without these particular details. Moreover, the particular embodiments of the present invention described herein are provided by way of example and should not be used to limit the scope of the invention to these particular embodiments. In other instances, well-known circuits, control signals, timing protocols, and software operations have not been shown in detail in order to avoid unnecessarily obscuring the invention.

[018] Figure 1 is a block diagram of an apparatus that includes a memory block 100 according to an embodiment of the present invention. As used herein, apparatus may refer to, for example, an integrated circuit, a memory device, a memory system, an electronic device or system, a smart phone, a tablet, a computer, a server, etc. The memory block 100 includes a plurality of memory subblocks 102, a plurality of memory access lines 104, a plurality of select gate drain (SGD) control lines 106, a plurality of select gate source (SGS) control lines 120, and control unit 150. Each of the SGD control lines 106 may be associated with a respective memory subblock 102 and each of the SGS control lines 120 may be associated with a respective plurality of memory subblocks 102.

[019] In some examples, each of the memory subblocks 102 may include a plurality of memory cells, such as non-volatile memory cells (e.g., NAND memory cells) that may be arranged in rows and/or columns. In some examples, each of the memory cells may be a single-level cell (SLC) and/or may be a multi-level cell (MLC). In this manner, each memory cell may be programmed to distinct voltage states, each of which may correspond to a particular representation of binary data (e.g., single bit data 0, 1, multi-bit data 00, 01, 10, 11). Because each plurality of memory cells may include NAND memory cells, each plurality of memory cells may be implemented using one or more NAND strings within each memory subblock 102. Each string may, for instance, include 32 non-volatile memory cells, or may include a greater or lesser number of memory cells, and memory cells of each string may share a common channel. Each memory subblock 102 may include any number of strings.

[020] With reference to Figs. 3a-3e, each string may include a select gate drain (SGD) switch located at a first end of the string and a select gate source (SGS) switch located at a second end of the string opposite the first end. The SGD switch and the SGS switch may be implemented as transistors, as shown in the embodiments of Figs. 3a-3e. The memory cells of the string may be coupled in a series configuration between the SGD switch and the SGS switch. Each of the memory cells of the string may be coupled to a respective memory access line WL that may be used to access the memory cell. Memory access line drivers may provide various voltages to the memory access lines during memory operations, for example, during program operations, read operations, erase operations, as well as other memory operations.

[021] In some examples, an SGD switch may be configured to selectively couple a string to a signal line VBL and an SGS switch may be configured to selectively couple a string to a source (e.g., source line) SRC. By way of example, an SGD switch of a string included in a memory subblock 102 may be coupled to a respective SGD control line 106 associated with the memory subblock 102. Providing (e.g., asserting) a control signal (e.g., active control signal) on the SGD control line 106 may enable the respective SGD switch, thereby coupling the associated string to the signal line VBL. An SGD control line 106 providing a control signal to enable the SGD switch in this manner is described herein as an “active” SGD control line 106. Similarly, an SGS switch of a memory subblock 102 may be coupled to an SGS line 120 associated with the memory subblock 102. Providing a control signal on the SGS line 120 may enable the SGS switch, thereby coupling the respective string to the source. An SGS control line 120 providing a control signal to enable the SGS switch in this manner is described herein as an “active” SGS control line 120. Providing (e.g., deasserting) a control signal (e.g., inactive control signal) on the SGD control line 106 may disable the respective SGD switch, thereby decoupling the associated string from the signal line VBL. An SGD control line 106 providing a control signal to disable the SGD switch in this manner is described herein as an “inactive” SGD control line 106. Similarly, an SGS switch of a memory subblock 102 may be decoupled from an SGS line 120 associated with the memory subblock 102. Providing a control signal on the SGS line 120 may disable the SGS switch, thereby decoupling the respective string to the source.

An SGS control line 120 providing a control signal to disable the SGS switch in this manner is described herein as an “inactive” SGS control line 120.

[022] In some examples, control signals provided on respective SGD control lines 106 and SGS control lines 120, respectively, may be provided by control unit 150. The control unit 150 may be coupled to each of the SGD control lines 106 and the SGS control lines 120 and further may be configured to provide control signals to perform respective memory operations, described herein. The control unit 150 may be implemented in software and/or hardware, and may include any circuitry and/or logic required to perform operations. In some examples, the control unit 150 may be included in the block 100 and in other examples, the control unit 150 may be located outside of the block 100, for instance, in a row decoder, an address decoder, control logic coupled to the block 100 and/or a controller (not shown in Fig. 1). In this manner, one or more portions of the circuitry and/or logic of the control unit 150 may be employed in a distributed configuration.

[023] Each SGD control line 106 may be associated with a respective memory subblock 102 of the block 100, each memory access line 104 may be associated with all memory subblocks 102 of the block 100, and/or each SGS control line 120 may be associated with a respective plurality of memory subblocks 102 of the block 100. Accordingly, each SGD control line 106 may be included, at least in part, in a respective memory subblock 102 and may be coupled to the SGD switch of the corresponding memory subblock 102. In this manner, each active SGD control line 106 may couple the string or strings of a respective memory subblock 102 to a set of signal lines shared, for instance, by each memory subblock 102. A memory access line 104 may be coupled to a memory cell of a string in each memory subblock 102 of the block 100. As a result, a memory access line 104 may span across all memory subblocks 102 of the block 100 and may be coupled to each memory cell of a particular row of memory cells. Each SGS control line 120 may span across an associated plurality of memory subblocks 102 and may be coupled to the SGS switches of the associated memory subblocks 102. In this manner, an active SGS control line 120 may couple strings of the associated plurality of memory subblocks 102 to a source SRC. In some examples, SGD control lines 106 and/or SGS control lines 120 may span memory subblocks 102 in a same direction as memory access lines 104 such that the SGD

control lines 106, memory access lines 104, and/or SGS control lines 120 are substantially parallel. In other examples, SGD control lines 106, and/or SGS control lines 120 may span memory subblocks in an orthogonal direction or other non-parallel directions relative to memory access lines 104. SGD and SGS control lines 106, 120 may, for instance, be substantially parallel to one or more signal lines.

[024] Because each SGS control line 120 may be associated with a respective plurality of memory subblocks 102, SGS switches coupled to an active SGS control line 120 may be enabled while SGS switches coupled to an inactive SGS control line 120 may be disabled. As will be explained in more detail below, by selectively enabling SGS switches in this manner, capacitive loading during one or more memory operations (e.g., read operations) may be reduced.

[025] In some examples, any ratio of SGD control lines 106 to SGS control lines 120 and/or any ratio of memory access lines 104 to SGS control lines 120 may be achieved. By way of example, the block 100 may include 32 memory subblocks 102 and each SGS control line 120 may be coupled to the SGS switches of strings for 4 memory subblocks 102 of the block 100. Accordingly, a 4:1 ratio of SGD control lines 106 to SGS control lines 120 and a 1:8 ratio of memory access lines 104 to SGS control lines 120 may be achieved. In other examples, each SGS control line 120 may be coupled to the SGS switches of strings for 2, 8, 16, 32, 64, or any other number of memory subblocks 102. It will be appreciated that in some examples, each SGS control line 120 may be coupled to the SGS switches of strings for a same number of memory subblocks 102, and that in other examples, SGS control lines 120 may be coupled to the SGS switches of strings for differing numbers of memory subblocks 102. A first SGS control line 120, for instance, may be coupled to the SGS switches of strings for 8 memory subblocks and a second SGS control line 120 may be coupled to the SGS switches of strings for 16 memory subblocks 120.

[026] Generally, memory operations (e.g., read operations, program operations, erase operations) may be performed on one or more selected memory subblocks 102 while all other memory subblocks 102 may be unselected. Performing a memory operation on one or more selected memory subblocks 102 may include selectively enabling SGD switches, SGS switches, and/or memory cells. Description of memory operations is made herein with respect to individual memory subblocks 102. It will be appreciated,

however, that in some examples, one or more described operations may be applied simultaneously to any number of memory subblocks 102. Moreover, reference is made herein to selectively enabling SGD and SGS switches to perform memory operations. As described, SGD and SGS switches may be enabled by providing control signal on SGD control lines 106 or SGS control lines 120, respectively, and control signals provided in this manner may be provided by the control unit 150.

[027] In an erase operation, for example, SGD and SGS switches may be disabled. For each row, a low voltage, such as ground potential (e.g., 0V), may be applied to the memory access line 104 associated with the row, thereby erasing the voltage state of each memory cell. In some examples, erase operations may be implemented at a block level and accordingly one or more memory subblocks 102 may be erased simultaneously. As a result, all SGD lines 106 and all SGS lines 120 may have a low voltage during an erase operation to disable the SGD and SGS switches.

[028] Typically, program operations are performed on erased memory cells, and as a result, only memory cells of a memory subblock 102 intended to be adjusted from an erased voltage state to a different voltage state need be programmed. In an example programming operation, one or more selected rows of a memory subblock 102 may be programmed sequentially. By way of example, for each selected row, signal lines associated with a cell to be programmed may be precharged to a first voltage (e.g., 0-1V) and signal lines associated with a cell not to be programmed may be precharged to a second voltage (2-3V) that may for instance, be higher than the first precharge voltage. A relatively high voltage (e.g., 15V) may be applied to a memory access line 104 corresponding to the row being programmed, while an intermediate voltage (e.g., 8V) may be applied to all other memory access lines 104. A magnitude of the intermediate voltage may be greater than a voltage of the voltage state having a highest magnitude to ensure that all memory cells of the memory subblock 102 are conductive. Thereafter, an SGD control line 106 associated with the selected memory subblock 102 may become active and SGD switches associated with strings to be programmed may be selectively enabled (while SGS switches may remain disabled) to program cells of the row. Because signal lines associated with cells not to be programmed have a higher precharge voltage, SGD switches associated with those signal lines may remain disabled and prevent programming of respective cells. In some examples, the relatively

high voltage applied to the memory access line 104 may be incrementally increased until each selected cell of the target row achieves a desired voltage level. During the programming operation, SGD and SGS switches of unselected memory subblocks 102 may be disabled.

[029] In an example read operation, selected signal lines may be precharged to a voltage (e.g., 0.3V), and both the SGD and SGS switches of a memory subblock 102 may be enabled. Because each SGS control line 120 may be associated with a respective plurality of memory subblocks 102, SGS switches of one or more other memory subblocks 102 associated with the same SGS control line 120 may be enabled as well. Thereafter, a relatively low voltage (e.g., 0-2V) may be applied to a memory access line 104 associated with the row to be read, while an intermediate voltage (e.g., 8V) may be applied to all other memory access lines 104. In some examples, the relatively low voltage may be a voltage having a magnitude between voltage levels of particular voltage states. Further, as described, a magnitude of the intermediate voltage may be greater than a voltage of the voltage state having a highest magnitude to ensure that all memory cells of the memory subblock 102 are conductive. The SGD switches may be disabled (e.g., to electrically isolate selected signal lines), and the voltage of each selected signal line may be used to determine the voltage state of selected memory cells of the row. In some examples, the voltage of each selected signal line may be sensed to determine the voltage state of selected memory cells of the row prior to disabling the SGD switches. During the read operation, SGD switches of unselected memory subblocks 102 may be disabled, and SGS switches of all memory subblocks 102 not associated with the active SGS line 120 of the read operation may be disabled. In this manner, only the respective plurality of memory subblocks 102 associated with an active SGS line 120 may have enabled SGS switches. All other memory subblocks 102 may be associated with an inactive SGS line 120 and accordingly may have disabled SGS switches.

[030] In some examples, the block 100 may be implemented in a three-dimensional arrangement. Fig. 2 is a block diagram of a three-dimensional memory array 200 according to an embodiment of the present invention. The three-dimensional memory array 200 may include any number of blocks 202, one or more of which may be implemented using the block 100 of Fig 1. By way of example, the three-dimensional

memory array 200 may include 32 blocks 202, or may include 64 blocks 202. In some examples, memory cells of each block 202 may be accessed concurrently, simultaneously, and/or in an otherwise overlapping manner such that data may be read from, programmed to, and/or erased from multiple blocks 202 in accordance with one or more memory operations. In other examples, the blocks 202 may be configured to share one or more components, such as signal lines and/or control lines.

[031] Figs. 3a-3b illustrate schematic diagrams of NAND strings 300-310 during a program operation and Figs. 3c-3e illustrate schematic diagrams of NAND strings 320-340 during a read operation. The NAND strings 300-340 may include respective SGD switches 302-342, respective SGS switches 304-344, and respective memory cells 306-346. As described, each SGD switch may be located at a first end of a NAND string and may be configured to selectively couple the NAND string to a signal line VBL responsive to assertion of a control signal provided to an SGD switch. The control signal may be provided, for instance, on an SGD control line coupled to an SGD switch 302, such as an SGD control line 106 of Fig. 1. Similarly, each SGS switch may be located at a second end of the NAND string and may be configured to selectively couple the NAND string to a source SRC responsive to assertion of a control signal provided to an SGS switch. The control signal may be provided, for instance, on an SGS control line coupled to a SGS switch, such as an SGS control line 120 of Fig. 1. Each of the memory cells may be coupled in a series configuration between respective SGD and SGS switches.

[032] Fig. 3a is a schematic diagram of a NAND string 300 of a selected memory subblock during a program operation according to an embodiment of the present invention. As described, during the program operation, the SGD switch 302 may be enabled and the SGS switch 304 may be disabled. As a result, during a program operation, each cell 306 may provide (e.g., generate) a capacitive load between a gate of the cell 306 and the signal line VBL.

[033] Fig. 3b is a schematic diagram of a NAND string 310 of an unselected memory subblock during a program operation according to an embodiment of the present invention. As described, during the program operation, the SGD switch 312 and the SGS switch 314 may be disabled. In this manner, voltage levels of the string may float. As a result, during the program operation, each cell 316 may provide a capacitive load

between a gate of the cell 316 and the source SRC. The capacitive load, however, may be in series with a junction capacitance of the SGS switch 314. Because the capacitive load provided by cells 316 of the NAND string 310 may be in series with junction capacitance of the SGS switch 314, the capacitive load provided by the NAND string 300 may exceed the capacitive load provided by the NAND string 310 during program operations.

[034] Fig. 3c is a schematic diagram of a NAND string 320 of a selected memory subblock during a read operation according to an embodiment of the present invention. As described, during the read operation, both the SGD switch 322 and the SGS switch 324 may be enabled simultaneously. As a result, each of the cells 326 may provide a load between a gate of the cell 326 and the source SRC. The load may include a capacitive load and a resistive load. The resistive load may include a channel resistance of the NAND string 320.

[035] Fig. 3d is a schematic diagram of a NAND string 330 of an unselected memory subblock during a read operation according to an embodiment of the present invention. The NAND string 330, while included in an unselected memory subblock, may, for instance, be associated with a same SGS control line 120 as the NAND string 320 of Fig. 3c. Accordingly, during a read operation, the NAND string 330 may be associated with an active SGS control line 120 and have an enabled SGS switch 334. As a result, during the read operation, each cell 336 may provide a capacitive load between a gate of the cell 306 and the source SRC.

[036] Fig. 3e is a schematic diagram of a NAND string 340 of an unselected memory subblock during a read operation according to an embodiment of the present invention. In contrast to the NAND string 330 of Fig. 3d, the NAND string 340 may not be associated with a same SGS control line as the selected NAND string 320 of Fig. 3c. Accordingly, during the read operation, the NAND string 340 may be associated with an inactive SGS control line 120 and the SGS switch 344 may be disabled. As a result, each cell 316 may provide a capacitive load between a gate of the cell 346 and the source SRC. The capacitive load, however, may be in series with a junction capacitance of the SGS switch 344. Because the capacitive load provided by cells 346 of the NAND string 340 may be in series with junction capacitance of the SGS switch

344, the capacitive load provided by the NAND string 330 may exceed the capacitive load provided by the NAND string 340 during read operations.

[037] With reference to Fig. 1, by reducing the number of memory subblocks 102 having enabled SGS switches during a read operation (e.g., less than all memory subblocks 102 of the block 100), the overall capacitive load of the block 100 may be reduced during the read operation. In this manner, design constraints may be relaxed and/or performance may be improved. By way of example, capacitive loads driven by memory access line drivers (not shown), may be reduced such that a smaller charge pump may be required for operation and/or memory access line voltages transition more quickly during operation.

[038] Fig. 4 illustrates a memory 400 according to an embodiment of the present invention. The memory 400 includes a memory array 430 with a plurality of memory cells. The memory cells may be non-volatile memory cells, such as NAND flash cells, or may generally be any type of memory cells. In some examples, the memory array 430 may include one or more memory blocks, such as a memory block 100 of Fig. 1. Moreover, the memory array 430 may be implemented as a three-dimensional memory array, such as the three-dimensional memory array 200 of Fig. 2.

[039] Command signals, address signals, and write data signals may be provided to the memory 400 as sets of sequential input/output (“I/O”) signals transmitted through an I/O bus 428. Similarly, read data signals may be provided from the memory 400 through the I/O bus 428. The I/O bus 428 is connected to an I/O control unit 420 that routes the signals between the I/O bus 428 and an internal data bus 422, an internal address bus 424, and an internal command bus 426. The memory 400 also includes a control logic unit 410 that receives a number of control signals either externally or through the internal command bus 426 to control the operation of the memory 400.

[040] The internal address bus 424 applies block-row and/or subblock-row address signals to a row decoder 440 and column address signals to a column decoder 450. The row decoder 440 and column decoder 450 may be used to select blocks of memory or memory cells for memory operations, for example, read, program, and erase operations. The column decoder 450 may enable write data signals to be applied to columns of memory corresponding to the column address signals and allow read data signals to be coupled from columns corresponding to the column address signals.

[041] In response to the memory commands decoded by the control logic unit 410, the memory cells in the memory array 430 are read, programmed, and/or erased. Read, program, erase circuits 468 coupled to the memory array 430 receive control signals from the control logic unit 410 and include voltage generators (e.g., charge pumps) for generating various pumped voltages for read, program and erase operations.

[042] After the row address signals have been applied to the internal address bus 424, the I/O control unit 420 routes write data signals to a cache register 470. The write data signals are stored in the cache register 470 in successive sets each having a size corresponding to the width of the I/O bus 428. The cache register 470 sequentially stores the sets of write data signals for an entire row or page of memory cells in the memory array 430. All of the stored write data signals are then used to program a row or page of memory cells in the memory array 430 selected by the block-row address or subblock-row address coupled through the internal address bus 424. In a similar manner, during a read operation, data signals from a row or block of memory cells selected by the block-row address coupled through the internal address bus 424 are stored in a data register 480. Sets of data signals corresponding in size to the width of the I/O bus 428 are then sequentially transferred through the I/O control unit 420 from the data register 480 to the I/O bus 428.

[043] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a first plurality of memory subblocks of a memory block;

a second plurality of memory subblocks of the memory block;

a first select gate control line associated with the first plurality of memory subblocks, the first select gate control line coupled to a first plurality of select gate switches of the first plurality of memory subblocks, the first plurality of select gate switches coupled to a source;

a second select gate control line associated with the second plurality of memory subblocks, the second select gate control line coupled to a second plurality of select gate switches of the second plurality of memory subblocks, the second plurality of select gate switches coupled to the source; and

a plurality of memory access lines, each memory access line of the plurality of memory access lines associated with each memory subblock of the first plurality of memory subblocks and each memory subblock of the second plurality of memory subblocks.

2. The apparatus of claim 1, wherein each memory subblock of the first plurality of memory subblocks includes a plurality of strings, each string of the plurality of strings including a first select gate switch coupled to a signal line and a second select gate switch included in the first plurality of select gate switches.

3. The apparatus of claim 2, further comprising:
a control unit configured to selectively enable the first plurality of select gate switches.
4. The apparatus of claim 1, further comprising:
a plurality of select gate control lines, each select gate control line of the plurality of select gate control lines associated with a respective one of the first plurality of memory subblocks.
5. The apparatus of claim 1, wherein the first select gate control line is configured to be active responsive to a read operation being performed on a memory subblock of the first plurality of memory subblocks and the second gate control line is configured to be inactive responsive to the read operation being performed on the memory subblock of the first plurality of memory subblocks.
6. The apparatus of claim 1, wherein the first plurality of memory subblocks and the second plurality of memory subblocks include a same number of memory subblocks.
7. The apparatus of claim 1, wherein the apparatus is included in a memory.
8. An apparatus, comprising:
a first select gate source control line associated with a first plurality of memory subblocks;
a second select gate source control line associated with a second plurality of memory subblocks;
a memory subblock of the first plurality of memory subblocks including a first plurality of select gate source switches, each select gate source switch of the first plurality of select gate source switches coupled to the first select gate source control

line and configured to be enabled responsive to receipt of an asserted select gate control signal;

a memory subblock of the second plurality of memory subblocks including a second plurality of select gate source switches, each select gate source switch of the second plurality of select gate source switches coupled to the second select gate source control line and configured to be enabled responsive to receipt of the asserted select gate source control signal; and

a control unit coupled to the first and second select gate source control lines and configured to provide the select gate source control signal to each select gate source switch of the first plurality of select gate source switches using the first select gate source control line responsive to a read operation associated with the memory subblock of the first plurality of memory subblocks, and to provide the select gate source control signal to each select gate source switch of the second plurality of select gate source switches using the second select gate source control line responsive to a read operation associated with the memory subblock of the second plurality of memory subblocks.

9. The apparatus of claim 8, wherein the memory subblock of the first plurality of memory subblocks further includes a plurality of select gate drain switches, each select gate drain switch of the plurality of select gate drain switches configured to be enabled responsive to receipt of a select gate drain control signal and wherein the control unit is configured to provide the select gate drain control signal to each select gate drain switch of the plurality of select gate drain switches responsive to the read operation associated with the memory subblock of the first plurality of memory subblocks.

10. The apparatus of claim 8, wherein the memory subblock of the first plurality of memory subblocks is a first memory subblock of the first plurality of memory subblocks, the apparatus further comprising a second memory subblock of the first plurality of memory subblocks, the second memory subblock of the first plurality of memory subblocks including a third plurality of select gate source switches, each select gate source switch of the third plurality of select gate source switches coupled to

the first select gate source control line and configured to be enabled responsive to receipt of the select gate source control signal.

11. The apparatus of claim 8, wherein the memory subblock of the first plurality of memory subblocks is configured to provide a first capacitive load during the read operation associated with the memory subblock of the first plurality of memory subblocks and the memory subblock of the second plurality of memory subblocks is configured to provide a second capacitive load during the read operation associated with the memory subblock of the first plurality of memory subblocks, the first capacitive load greater than the second capacitive load.

12. The apparatus of claim 8, further comprising:

a memory access line coupled to a plurality of memory cells of the memory subblock of the first plurality of memory subblocks and a plurality of memory cells of the memory subblock of the second plurality of memory subblocks.

13. The apparatus of claim 8, wherein the apparatus is included in a three-dimensional memory array.

14. An apparatus, comprising:

a plurality of select gate source control lines, each select gate source control line of the plurality of select gate source control lines associated with a respective plurality of memory subblocks of a block; and

a memory access line associated with each memory subblock of the block, the memory access line substantially parallel to each select gate source control line of the plurality of select gate source control lines.

15. The apparatus of claim 14, further comprising:

a control unit configured to selectively provide a select gate source control signal on each select gate source control line of a plurality of select gate source control lines during a read operation based on a memory subblock of the plurality of memory subblocks associated with the read operation.

16. The apparatus of claim 15, wherein the control unit is further configured to selectively provide a select gate drain control signal on each select gate drain control line of a plurality of select gate drain control lines during the read operation based on the memory subblock of the plurality of memory subblocks associated with the read operation.

17. The apparatus of claim 14, wherein each memory subblock of the block is selectively coupled to a same set of signal lines.

18. A method, comprising:

providing, during a read operation, a first control signal on a first select gate source control line to enable select gate source switches of a first plurality of memory subblocks of a block; and

providing, during the read operation, a second control signal on a second select gate source control line to disable select gate source switches of a second plurality of memory subblocks of the block.

19. The method of claim 18, wherein the control signal is a first control signal, the method further comprising:

providing a third control signal on a first select gate drain control line to enable select gate drain switches of a first memory subblock of the first plurality of memory subblocks; and

providing a fourth control signal on a second select gate drain control line to disable select gate drain switches of a second memory subblock of the first plurality of memory subblocks.

20. The method of claim 18, wherein providing, during a read operation, the first control signal on a first select gate source control line to enable select gate source switches of a first plurality of memory subblocks of a block comprises:

for each memory subblock of the first plurality of memory subblocks of the block, coupling a plurality of strings to a source.

21. The method of claim 18, wherein providing, during the read operation, the second control signal on a second select gate source control line to disable select gate source switches of a second plurality of memory subblocks of the block causes coupling of a capacitive load in series with a junction capacitance of a select gate source switch.

22. The method of claim 18, further comprising:

applying a first voltage to a memory cell of each memory subblock of the first plurality of memory subblocks associated with a row; and

applying a second voltage lower than the first voltage to a plurality of memory cells of each memory subblock of the plurality of memory subblocks not associated with the row.

23. The method of claim 18, wherein providing, during a read operation, the first control signal on a first select gate source control line to enable select gate source switches of a first plurality of memory subblocks of a block comprises:

providing the first control signal using a control unit, the control unit located in the block.

24. The method of claim 18, wherein the first plurality of memory subblocks includes a first number of memory subblocks and the second plurality of memory subblocks includes a second number of memory subblocks greater than the first number of memory subblocks.

25. A method, comprising:

selectively providing a respective control signal on each select gate source control line of a plurality of select gate source control lines to enable select gate source switches of a plurality of memory subblocks of a block during a read operation, each select gate source control line of the plurality of select gate source control lines parallel to at least one memory access line of the block.

26. The method of claim 25, wherein selectively providing a respective control signal on each select gate source control line of a plurality of select gate source control lines to enable select gate source switches of a plurality of memory subblocks of a block during a read operation comprises:

providing the respective control signal on at least one select gate source control line of the plurality of select gate source control lines to disable select gate source switches of memory subblocks of the plurality of memory subblocks associated with the at least one select gate source control line.

27. The method of claim 26, wherein providing the respective control signal on at least one select gate source control line of the plurality of select gate source control lines to disable select gate source switches of memory subblocks of the plurality of memory subblocks associated with the at least one select gate source control line causes coupling of each capacitive load of a plurality of capacitive loads in series with a junction capacitance.

28. The method of claim 25, further comprising:

selectively providing a respective control signal on each select gate drain control line of a plurality of select gate drain control lines to enable select gate drain switches of a plurality of memory subblocks of the block during the read operation, each select gate drain control lines of the plurality of select gate drain control lines parallel to the at least one memory access line of the block.

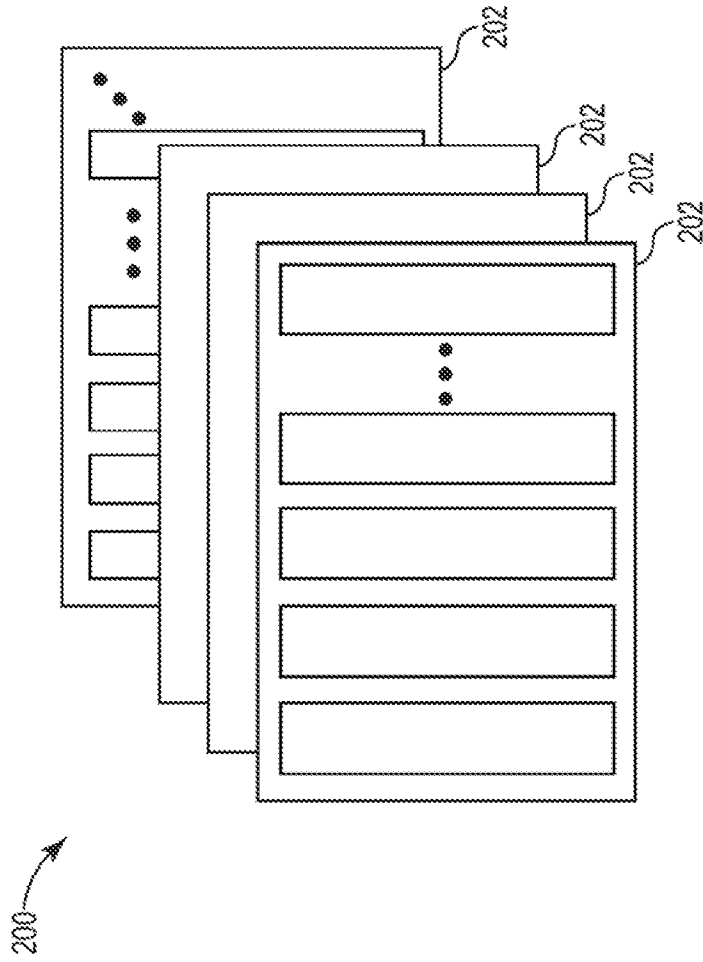


Fig. 2

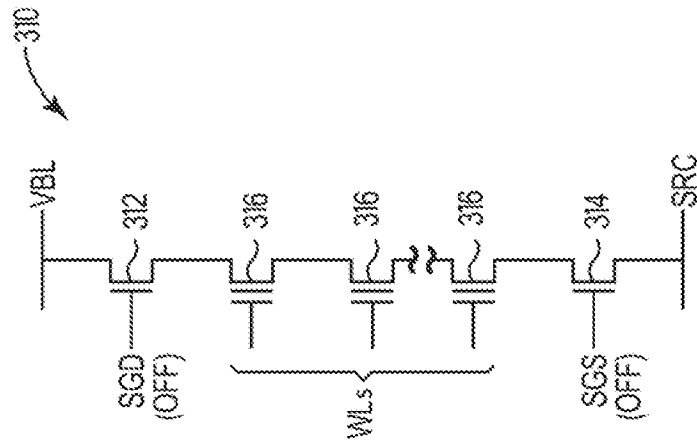


Fig. 3b

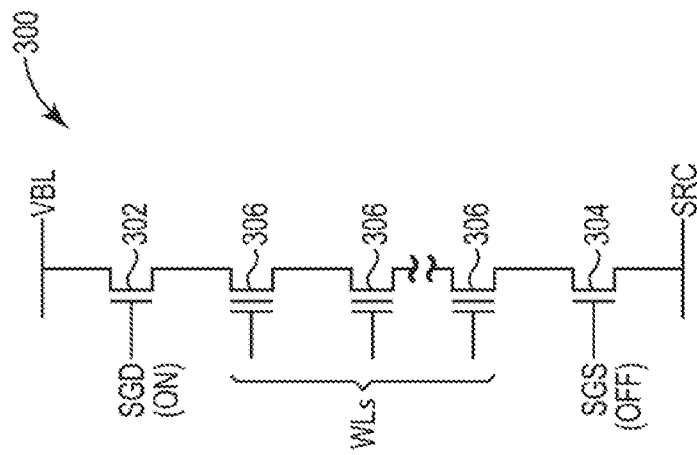


Fig. 3a

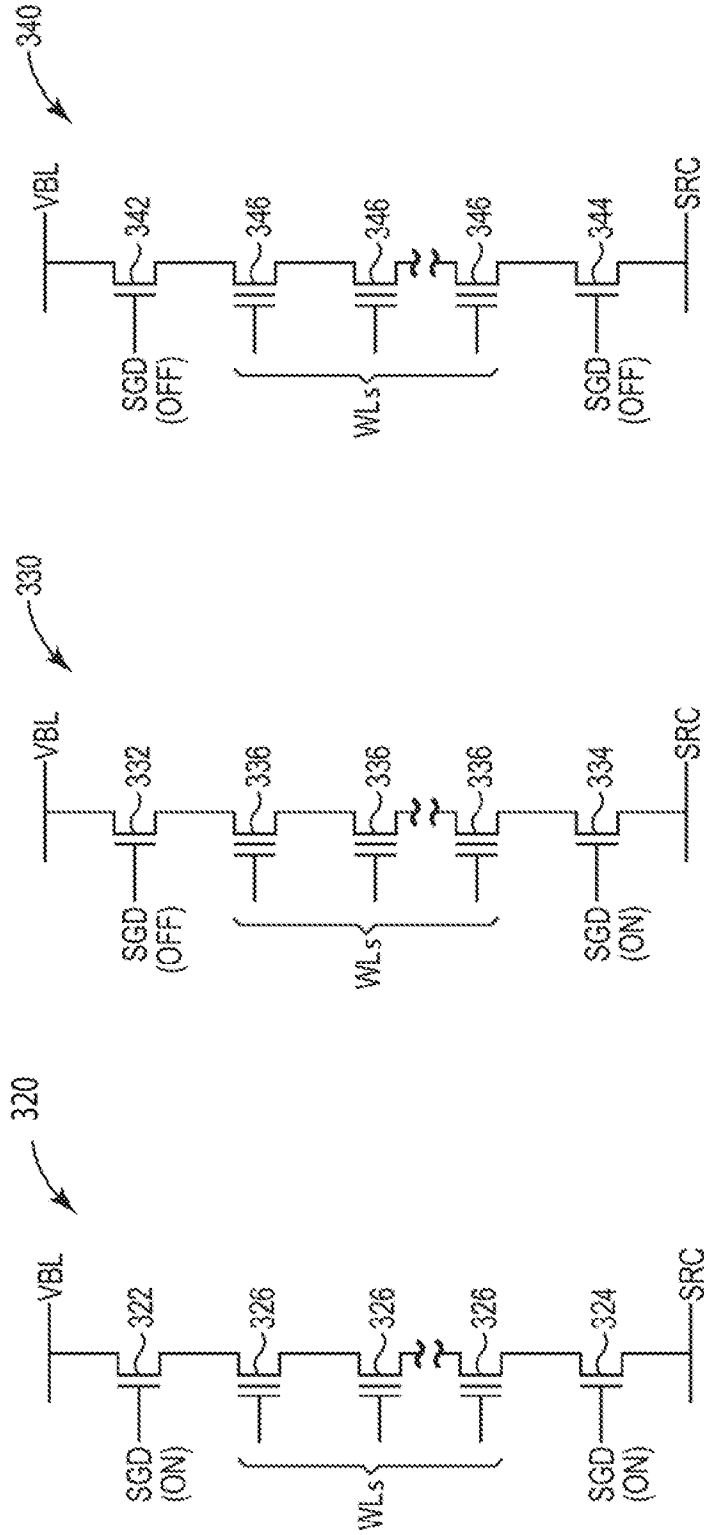


Fig. 3c

Fig. 3d

Fig. 3e

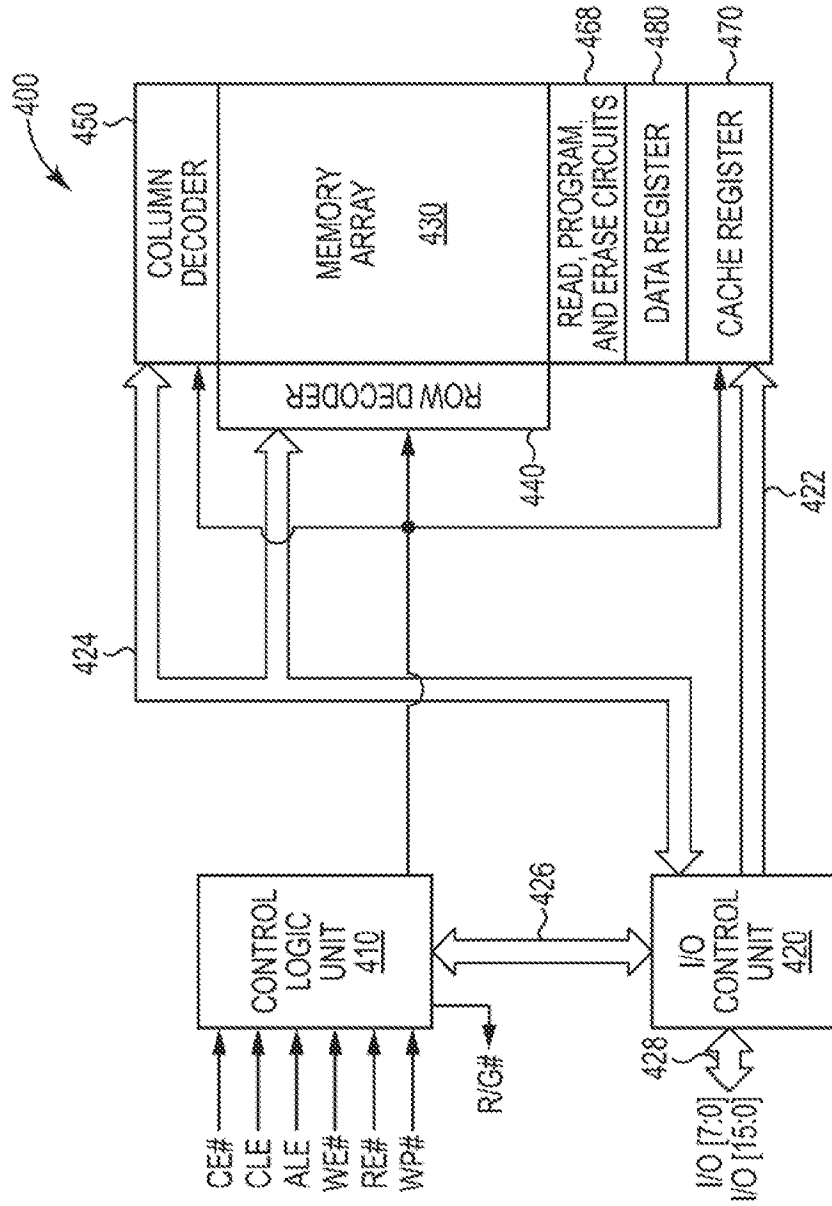


Fig. 4

A. CLASSIFICATION OF SUBJECT MATTER**G11C 16/04(2006.01)i, G11C 16/06(2006.01)i, G11C 16/26(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
G11C 16/04; G11C 11/34; G11C 16/26; G11C 16/10; G11C 16/34; G11C 16/06Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: memory, subblock, block, select, gate, control, line, switch, source, access, string, array, read, operation**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 2014-0160850 A1 (ZENGTAO LIU) 12 June 2014 See paragraphs [0023]-[0024], [0029]; and figure 1.	1-4, 6-7, 14-17 , 25-26, 28 5, 8-13, 18-24, 27
Y A	US 2013-0170299 A1 (AARON YIP) 04 July 2013 See paragraphs [0023]-[0024]; and figure 3.	1-4, 6-7, 14-17 , 25-26, 28
A	US 2005-0265076 A1 (LEONARD FORBES) 01 December 2005 See paragraphs [0035]-[0036]; and figure 4B.	1-28
A	US 2014-0063960 A1 (AKIRA GODA et al.) 06 March 2014 See paragraphs [0014]-[0015]; and figure 1.	1-28
A	US 2014-0211563 A1 (KUO-PIN CHANG et al.) 31 July 2014 See paragraphs [0040]-[0046]; and figure 1.	1-28

 Further documents are listed in the continuation of Box C. See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search

23 February 2016 (23.02.2016)

Date of mailing of the international search report

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Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

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Information on patent family members

International application No.

PCT/US2015/054412

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