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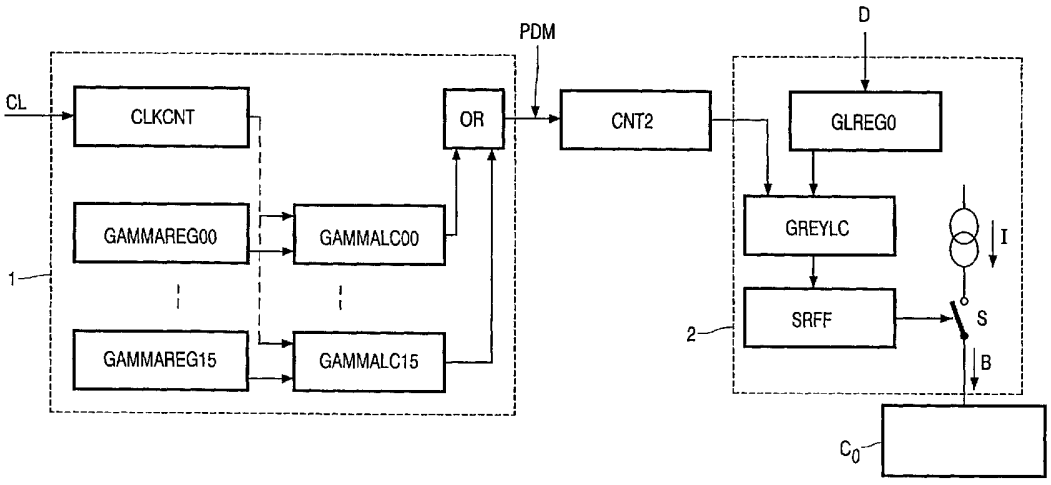

(57) Abstract: The invention relates to a display device, preferably an electroluminescent display device, comprising a matrix of pixels, each pixel being driven by a drive pulse (B), which is pulse width modulated. The device is characterized in that the width of the drive pulse is controlled by a gamma correction device, in which gamma correction information is supplied in the form of a separate pulse distribution-modulated signal (PDM). The invention also relates to a method of gamma correction in such a display device.

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Method and device for gamma correction

The present invention relates to a method of gamma correction for use in a display device comprising a matrix of pixels, each pixel being driven by a drive pulse, which is pulse width modulated.

The invention also relates to a display device, preferably an electroluminescent display device, comprising a matrix of display pixels, each pixel being driven by a drive pulse, which is pulse width modulated.

Displays of the above-described kind are known, for example from patent application EP-0 457 440.

There are several different types of displays on the market today, and even though other display technologies, such as those described above are rapidly increasing, a very common display device is still the cathode ray tube (CRT). However, the perception of gradual light intensity (i.e. grey scales) in CRT displays is not linearly proportional to the amount of light emanating from the display. Consequently, in existing CRT displays, this effect is taken into account, and since these types of displays having a non-linear luminance output/electrical input function are still very common, most video signal sources assume that they will be displayed on such a display. Therefore, the signals have a so-called gamma pre-correction.

However, in some recently developed display technologies, such as polymer light-emitting diode (PLED) displays or organic light-emitting diode (OLED) displays, both being of the kind described in the introduction, the relationship between applied current and emitted light is approximately linear. Extra measures are needed in order to include gamma-corrected performance, i.e. to correct the above-mentioned gamma pre-correction before the signal is displayed. If this is not taken into account, the displayed picture will have a softer appearance. Consequently, there is a need to optimally adapt the display to the human eye sensitivity curve.

In accordance with the prior art regarding gamma correction, as described in US-6 137 542, gamma correction may be implemented by using a memory circuit, included

on a drive electronics chip. In this memory, a gamma look-up table may be stored, which may be used to store values for each color luminance, which values are corrected with respect to the gamma function form. Consequently, an input signal may be converted to a gamma-corrected input signal by utilizing information stored in the memory. However, a problem with the prior art is that the above-described memory needs to be quite large, and therefore occupies a large area of the chip. Furthermore, this solution requires a high data rate for updating the memory each line, which severely loads the communication in the communication buses and also increases the power dissipation.

It is an object of the present invention to provide a method and a display device for gamma correction, avoiding the above-mentioned problems with the prior art.

The invention is defined by the independent claims. The dependent claims define advantageous embodiments.

These and other objects are achieved by a method as described in the opening paragraph, the method further comprising the steps of generating a pulse distribution-modulated signal, in which the pulse distribution is dependent on pre-determined gamma correction information, deriving an actual grey level information about each pixel from an input signal, and comparing said grey level information with a counter information based on the pulse distribution-modulated signal, in order to obtain a gamma-corrected specific width of the drive pulse. In doing so, the gamma information is provided as a separate signal, which is compared with the value of the desired grey level, in order to provide a drive pulse of a desired width. Since the gamma information is separated and further supplied as a pulse distribution-modulated signal, this information may be loaded more or less permanently into a gamma correction circuit, thereby avoiding rapid updates and heavy bus communication.

Furthermore, the method may also comprises the steps of inputting the pulse distribution-modulated signal to a pulse counter, and inputting the actual grey level information to a grey level register, the grey level register and the pulse counter having the same bit size and being connected to a comparator, the output of the comparator being coupled to a switch for controlling the drive pulse to the pixel. In doing so, a pulse width-modulated signal comprising, for example, a great plurality of bits, may be represented by a counter value having fewer bits, whereby the timing of the pulses in the pulse width-modulated signal is transferred to the changes of the counter value. Drive pulses with different durations may thereby easily be achieved, with a timing having a greater resolution

than the comparator generating the drive pulse. Compared to prior-art solutions, the inventive method provides a reduction of memory and component sizes.

Furthermore, the step of generating a pulse distribution-modulated signal preferably comprises the steps of storing, in a plurality of gamma registers, timing distribution information values for the pulse distribution-modulated signal, each gamma register being connected to a first input of a respective one of a plurality of gamma level comparators, inputting, into a second input of each gamma level comparator, a counter value from a clock counter, outputting a signal pulse from any one of the gamma level comparators, when the value stored in the respective one of the gamma registers equals the inputted clock counter value, combining, in an OR-component, the outputted signal pulses to a pulse distribution-modulated signal. This is an easy way of generating the inventive pulse distribution-modulated signal, requiring a comparatively small memory area on a chip. Furthermore, the gamma registers only need to be loaded with gamma correction information once, because these are constant throughout the drive of the display device.

In accordance with a preferred embodiment of the invention, the clock counter and each gamma register comprise a larger number of bits than the pulse counter or the grey level comparator. A suitable configuration for e.g. cellular telephone display application is N=16 grey levels. The gamma registers could in this embodiment, for example, comprise 8 bits, while the pulse counter and the grey level comparator could comprise 4 bits corresponding to the 2u=16 grey levels.

The display is suitably a polymer light-emitting diode display or an organic light-emitting diode display, and the method is preferably implemented in a fully digital gamma correction device, thereby being insensitive to production spreads. Furthermore, at least one of the registers is programmable, resulting in a flexible solution.

The objects of the invention are also achieved by a display device as defined in claim 5. A width of said drive pulse is controlled by a gamma correction device using a separate pulse distribution-modulated signal (PDM), which is dependent on predetermined using gamma correction information. Since the gamma information is separated and provided as a pulse distribution-modulated signal, this information may be loaded more or less permanently into a gamma correction circuit, thereby avoiding rapid updates and heavy bus communication.

The gamma correction device also comprises a first and a second block, wherein the first block 1 comprises means for generating the pulse distribution-modulated signal, and the second block 2 comprises means for generating the drive pulse, the pulse

distribution-modulated signal being arranged to be inputted to the second block from the first block. By dividing the gamma correction device into two separate parts, it is possible to pre-load gamma information into the first block, and thereafter this information may be unchanged, reducing the need for fast processing and large memory areas.

The first block may suitably comprise a plurality of gamma registers, in which timing distribution information values for the gamma correction pulse distribution-modulated signal are storable, each register being connected to a first input of a respective one of a plurality of gamma level comparators, a counter value from a clock counter being arranged to be inputted into a second input of each gamma level comparator, whereby a signal pulse from any one of said gamma level comparators is arranged to be outputted when the value stored in the respective one of said gamma registers equals the inputted clock counter value, whereafter the outputted signal pulses are inputted to an OR-component, in which they are combined to said pulse distribution-modulated signal being the output of said first block. This is an easy way of generating the inventive pulse distribution-modulated signal requiring a comparatively small memory area on a chip. Furthermore, the gamma registers only need to be loaded with gamma correction information once, because these are constant throughout the drive of the display device. This makes it possible to use a single common first block for all pixels or columns of a display.

The second block may suitably comprise a pulse counter, into which the gamma correction pulse distribution-modulated signal from the first block is arranged to be inputted, a grey level register, into which a grey level to be displayed is inputted, and a comparator, into which the outputs of the pulse counter and the grey level register are inputted, wherein the grey level register and the pulse counter have the same bit size, and the output of the comparator is coupled (directly or via a set/reset flip-flop) to a switch for controlling the power distribution to said pixel. In doing so, a pulse width-modulated signal comprising, for example, a great plurality of bits may be represented by a counter value having fewer bits, whereby the timing of the pulses in the pulse width-modulated signal is transferred to the changes of the counter value. Drive pulses with different durations may thereby easily be achieved, with a timing having a greater resolution than the comparator generating the drive pulse. Compared to prior-art solutions, the inventive method provides a reduction of memory and component sizes.

Finally, the display is preferably a polymer light-emitting diode display or an organic light-emitting diode display, and the gamma correction device is fully digital in order

to achieve a system which is insensitive to production spreads. Preferably, at least one of the registers is programmable, resulting in a flexible solution.

These and other aspects of the invention will be apparent from and elucidated with reference to the accompanying drawings, in which:

Fig. 1 is block diagram of a gamma correction circuit for use in an inventive display device, implementing the inventive method;

Fig. 2 illustrates a table of grey scale data for use in the circuit of Fig. 1;

Fig. 3 is an example of a timing diagram showing, at A, a part of a pulse distribution-modulated signal and, at B, a resulting drive pulse; and

Fig. 4 is a table showing the values of a pulse counter CNT2, a grey level comparator and a set/reset flip-flop for a selected one of the grey scale data as shown in Fig. 2, for the example shown in Fig. 3.

The invention relates to a gamma correction circuit for a monotonic display device, such as a PLED or an OLED display. A PLED display, for example, comprises a plurality of column electrodes $C_0, C_1 \ldots C_N$, and row electrodes together forming the entire display area. Each crossing of a row and a column electrode defines a pixel of the display. An electroluminescent material, here a light-emitting polymer, is arranged between the rows and columns.

However, in Fig. 1 only one column, C_0, is indicated. The circuit, as described above, is identical for all columns of the display.

Each column is connected in series with a current source I for driving the column, and the connection is provided with a switch S for switching between a closed position, in which current is allowed to flow through the column Co and an open position, in which the current supply to the column Co is interrupted. In the closed position of the switch S, a current flows through the layer of light-emitting polymer material, whereby light is emitted from the light-emitting polymer material. In the open position of the switch S, no light is emitted from that column Co or pixel.

In accordance with the invention, the switch S is connected to a gamma correction device.

A first embodiment of the gamma correction device in accordance with the invention is schematically shown in Fig. 1. This embodiment may be utilized, for example, in mobile applications, having a sixteen-level (i.e. 4-bit) grey scale and a quadratic gamma correction. This implementation comprises a first and a second block 1 and 2, respectively, wherein the first block 1 is a correction storage block and the second block 2 is a grey level comparison block. A separate second block 2 is needed for each column C_0, C1... C_N of the display, while the first block 1 may be common for all columns or for a group of columns. In this example, one common first block 1 is used for all columns. Consequently, a drive chip for the display may be manufactured, having a single first block 1 and N+1 second blocks 2, where N+1 is the total number of columns of the display device.

In the example shown, the first correction storage block 1 comprises sixteen gamma correction storage registers GAMMAREG00-GAMMAREG15; each of these registers being an 8-bit register. These registers are loadable with desired gamma correction information and need to be loaded only once. The output of each register GAMMAREG00-GAMMAREG15 is connected to an input of a respective one of sixteen gamma level comparators GAMMALC00-GAMMALC15. A second input of the gamma level comparators GAMMALC00-GAMMALC15 is connected to the output of an 8-bit clock counter CLKCNT. This clock counter CLKCNT is clocked by clock pulses CL, where every line period in this case comprises 256 clock pulses. By comparing the clock counter value with each value stored in the sixteen gamma correction storage registers GAMMAREG00-GAMMAREG15 in block 1, each gamma level comparator GAMMALC00-GAMMALC15 outputs a pulse, when the clock counter value equals the value stored in the registers connected to that comparator GAMMALC00-GAMMALC15. Consequently, during a full line time, a total of sixteen pulses is generated by the gamma level comparators GAMMALC00-GAMMALC15, and the timing and distribution of these pulses over the line time is determined by the exact values stored in the gamma correction storage registers GAMMAREG00-GAMMAREG15. A first pulse is generated from a first gamma level comparator at an instant t_0, the next at an instant t_1 and so forth.

All of the outputs of said gamma level comparators GAMMALC00-GAMMALC15 are connected to an OR-gate OR combining the generated pulses and resulting in an output signal from the OR-gate OR, which is a special control signal PDM having a modulated pulse distribution and a reduced average frequency (here 16x) in relation to the original clock signal CL. In the construction described above, gamma correction information, as represented by the pre-set gamma correction storage registers

GAMMAREG00-GAMMAREG15 has been translated into a timed signal comprising 16 pulses (one for each register), having a full 8-bit timing resolution which is due to the timing distribution.

The pulse distribution-modulated control signal (PDM) is thereafter inputted in a second pulse counter CNT 2 being a 4-bit counter. This pulse counter CNT 2 is connected to each second block 2, which in turn is connected to a respective one of the display columns C_0, C1... C_N. The outputted counter value from the second pulse counter CNT 2 is consequently inputted to each second block 2. In this example, the 4-bit pulse counter makes one full count (0-15) per line time, which is due to the fact that the pulse distribution-modulated control signal PDM comprises 16 pulses per line time.

Each second block 2 further comprises a 4-bit grey level register GLREG0, comprising subsequently the grey levels to be displayed of the pixels in the column to which the second block 2 is connected. For example, this register GLREGO may contain one of the data as shown in Fig. 2, depending on what grey scale is desired for a pixel in a column during a specific line time. This register GLREGO is updated every line via an input connection (D) in a manner known per se. The column GSL in the table in Fig. 2 comprises the possible grey scale values. The column BD in Fig. 2 shows the corresponding binary values as may be present at the output of the grey level register GLREGO.

The output from the grey level register GLREG0 is thereafter inputted to a grey level comparator GREYLC, together with the output from the above-described pulse counter CNT2, both having 4 bits. The output of this comparator is thereafter inputted to a set/reset flip-flop SRFF which is connected to the above-described switch S so as to realize a switching operation between a closed position, in which current is allowed to flow through the column, and an open position, in which the current supply to the column is interrupted.

When comparing the values of the pulse counter CNT2 and the grey level register GLREGO, a high signal is outputted from the set/reset flip-flop SRFF as long as the value of the grey level register GLREGO exceeds the value of the pulse counter CNT 2, thereby keeping the switch S in a closed position (current flows through display). When the value of the pulse counter exceeds or equals the value of the grey level register GLREGO, the set/reset flip-flop SRFF flips over to a low signal, thereby opening the switch S (no current flowing through display). At the beginning of a new line, the set/reset flip-flop SRFF is set back to the high signal state.

Figs. 3 and 4 show an example. In this case the desired grey scale is 4, i.e. the value of the grey level register GLREGO is 0100 in accordance with Fig. 2. As can be seen in

Fig. 3, the first pulse of the control signal PDM is generated at an instant t_0, the next at t_1, and so forth in accordance with the values pre-set in the gamma registers GAMMAREG00-GAMMAREG15. The second pulse counter CNT 2 receives the pulses generated at t_0, t_1 and so forth and adds one to the signal for each pulse received from the first block 1, i.e. outputs 0000 until the instant t_0, outputs 0001 until the instant t_1 and so forth. The table in Fig. 4 illustrates values, related to the example. Column GLREGO shows the value present in the grey level register GLREGO. Column CNT 2 shows the subsequent values, outputted by the second pulse counter CNT2. Column GREYLC shows the resulting output of the grey level comparator. Finally column SRFF shows the output of the set-reset flip-flop SRFF. If the output is "1", then the switch S is closed, if the output is "0" then the switch S is open. At the instant t_4 the fifth pulse reaches the second counter CNT 2, thereby outputting 0100, which equals the desired grey scale value stored in the grey level register GLREG 0. At this instant t_4 the output of the grey level comparator GREYLC switches from "1" to "0". As a result the output of the flip-flop SRFF becomes "0" and remains zero until the beginning of the next line. The output of the grey level comparator GREYLC returns to "1", when at the instant t5 the output of the second counter CNT 2 exceeds the grey level value in the grey level register GLREGO. So, at the instant the flip-flop SRFF sends a signal to the switch S so that the drive pulse B to the pixel is ended for the current line. The length T of the drive pulse B is thereby established as $T= t_4$, as can be seen in Fig. 3. The length T may be adjusted by choosing the values stored in the gamma registers GLREGO in a suitable way. Since each line time comprises 256 time slots, this is also the resolution for the length T of the drive pulse B, even if only 4-bit resolution is used in the second block 2.

EXAMPLE

Due to the use of pulse width modulation for controlling grey levels in the prior art, a simple straightforward implementation of gamma correction requires a large memory and a large data transfer for updating the column drivers each line. For typical cellular phone applications, sixteen-level grey scale (i.e. 4 bit) and quadratic gamma correction requires $256=2^8$ clock pulses per line. Addressing 102 parallel column drivers and 65 rows of the display at 60 Hz frame rate requires:

MEMORY:	102x65x8 bit=53 kbit
DATA RATE:	60x65x102x8 bit=3.2 Mbit/s
CLOCK FREQUENCY:	60x65x256=1 MHz

This memory requires a large chip area, while the high data rate severely loads the bus communication and the high clock frequency increases power dissipation.

However, for a system in accordance with the invention as described above, the requirements are:

MEMORY:	16x8 bit +102x65x4 bit=26.6 kbit
DATA RATE:	60x65x102x4 bit=1.6 Mbit/s
CLOCK FREQUENCY:	60x65x16=62 kHz

Consequently, in this example of the invention, both the memory chip area and the data rate are halved, while the 16x lower frequency of the control signal PDM ensures a low power dissipation. Due to the fully digital implementation, the system is insensitive to production spreads. Furthermore, full flexibility may be obtained by utilizing programmable registers in said circuit.

An appropriate initialization of the counters and the set/reset flip-flop is needed, but this may be done in known manner, and will therefore not be described nor shown in the drawings.

Although the above-described implementation of the invention is described with reference to PLED and OLED displays, the invention may be used for gamma correction in other types of displays, having a monotonic relationship, such as an essentially linear, almost linear or non-linear relationship, between the input electric signal and the output luminance signal. An example of such a display is a plasma display.

The invention is primarily intended for application in current-driven systems, but the inventive idea may also be implemented for optimizing voltage-driven output stages.

It should also be noted that the shown embodiment of the invention is only one way of implementing the idea digitally, and many variations of this design can be conceived by a person skilled in the art.

Furthermore, it should be noted that the above-described embodiment of the invention discloses driven display columns, but it is immaterial whether this invention is applied on driven columns or driven rows of the display.

In summary, the invention relates to a display device, preferably an electroluminescent display device, having a monotonic relationship between an input electric signal and an output luminance signal and comprising a matrix of display pixels, each pixel

being connected to means for illuminating the pixel with an intensity which is dependent on the width of a drive pulse. The device is characterized in that the width of the drive pulse is controlled by a gamma correction device, in which gamma correction information is supplied in the form of a separate pulse distribution-modulated signal.

The invention also relates to a method of gamma correction in such a display device.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A method of gamma correction for use in a display device comprising a matrix of pixels, each pixel being driven by a drive pulse (B), which is pulse width modulated, said method comprising the steps of:

generating a pulse distribution-modulated signal (PDM), in which the pulse distribution is dependent on pre-determined gamma correction information,

deriving an actual grey level information about each pixel from an input signal, and

comparing said grey level information with a counter information based on the pulse distribution-modulated signal, in order to obtain a gamma-corrected specific width of the drive pulse (B).

2. A method as claimed in claim 1, further comprising the steps of:

inputting said pulse distribution-modulated signal (PDM) to a pulse counter (CNT2), and

inputting said actual grey level information to a grey level register (GLREG0), said grey level register (GLREG0) and said pulse counter (CNT2) having the same bit size and being connected to a comparator (GREYLC), the output of said comparator (GREYLC) being coupled to a switch (S) for controlling the drive pulse (B) to said pixel.

3. A method as claimed in claim 1, wherein the step of generating a pulse distribution-modulated signal further comprises the steps of:

storing, in a plurality of gamma registers (GAMMAREG00-GAMMAREG15), timing distribution information values for said pulse distribution-modulated signal, each gamma register (GAMMAREG00-GAMMAREG15) being connected to a first input of a respective one of a plurality of gamma level comparators (GAMMALC00-GAMMALC15),

inputting, into a second input of each gamma level comparator (GAMMALC00-GAMMALC15), a counter value from a clock counter (CLKCNT),

outputting a signal pulse from any one of said gamma level comparators (GAMMALC00-GAMMALC15), when the value stored in the respective one of said gamma registers (GAMMAREG00-GAMMAREG15) equals the inputted clock counter value,

combining, in an OR-component, said outputted signal pulses to a pulse distribution modulated signal.

4. A method as claimed in claim 3, wherein said clock counter (CLKCNT) and each gamma register (GAMMAREG00-GAMMAREG15) comprise a larger number of bits, than the pulse counter or the grey level comparator.

5. A display device, preferably an electroluminescent display device, comprising a matrix of display pixels, each pixel being driven by a drive pulse which is pulse width modulated, characterized in that a width of said drive pulse is controlled by a gamma correction device using a separate pulse distribution-modulated signal (PDM), which is dependent on predetermined gamma correction information.

6. A display device as claimed in claim 5, wherein said gamma correction device comprises a first block (1) and a second block (2), wherein the first block (1) comprises means for generating said pulse distribution-modulated signal (PDM), and the second block (2) comprises means for generating said drive pulse (B), said pulse distribution-modulated signal (PDM) being arranged to be inputted to said second block (2) from said first block (1).

7. A display device as claimed in claim 6, wherein said first block comprises a plurality of gamma registers (GAMMAREG00-GAMMAREG15), in which timing distribution information values for said pulse distribution-modulated signal (PDM) are storable, each register being connected to a first input of a respective one of a plurality of gamma level comparators (GAMMALC00-GAMMALC15), a counter value from a clock counter (CLKCNT) being arranged to be inputted into a second input of each gamma level comparator (GAMMALC00-GAMMALC15), whereby a signal pulse from any one of said gamma level comparators (GAMMALC00-GAMMALC15) is arranged to be outputted when the value stored in the respective one of said gamma registers (GAMMAREG00-GAMMAREG15) equals the inputted clock counter value, whereafter said outputted signal pulses are inputted to an OR-component, in which they are combined to said pulse distribution-modulated signal (PDM) being the output of said first block (1).

8. A display device as claimed in claim 6, wherein said second block (2) comprises:

a pulse counter (CNT2), into which said gamma correction pulse distribution-modulated signal (PDM) from said first block (1) is arranged to be inputted,

a grey level register (GLREG0), into which a grey level to be displayed is inputted, and

a comparator (GREYLC), into which the outputs of said pulse counter (CNT2) and said grey level register (GLREG0) are inputted,

wherein said grey level register (GLREG0) and said pulse counter (CNT2) have the same bit size, and the output of said comparator (GREYLC) coupled to a switch (S) for controlling the drive pulse (B) to said pixel.

9. A display device as claimed in claim 8, wherein the output of the grey level comparator (GREYLC) is coupled via a set-reset flip-flop (SRFF) to the switch (S) and the set-reset flip-flop (SRFF) is reset each line period.

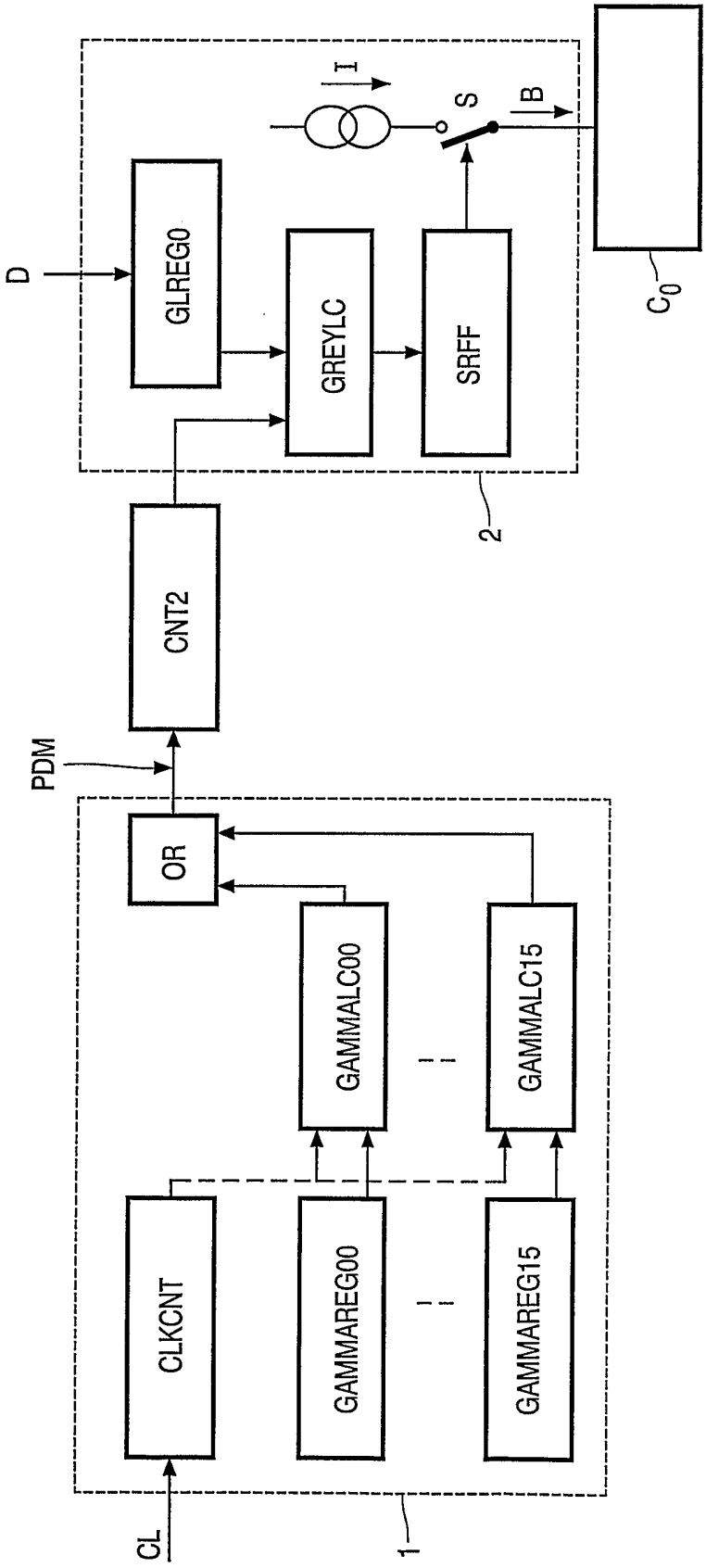
I
S
B
D
GLREG0
GREYLC
SRFF
C_0
2
CNT2
PDM
OR
GAMMALC00
GAMMALC15
CLKCNT
GAMMAREG00
GAMMAREG15
CL
1

FIG. 1

GSL	BD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

FIG. 2

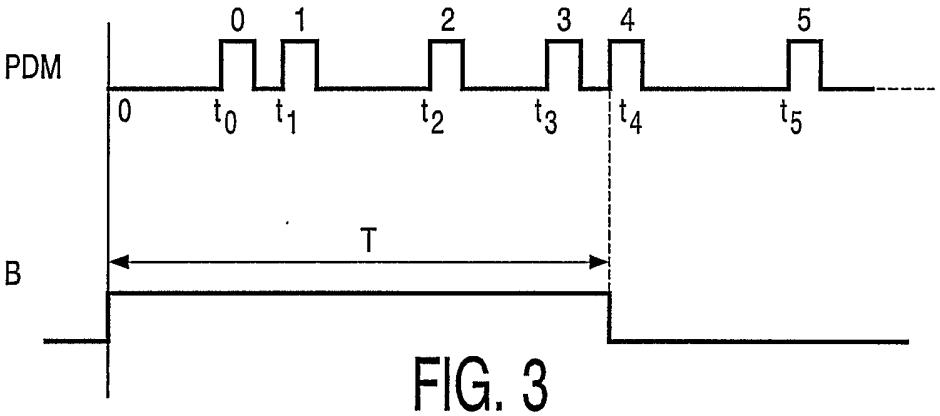

FIG. 3

GLREGO	CNT2	GREYLC	SRFF
0100	0000	1	1
	0001	1	1
	0010	1	1
	0011	1	1
	0100	0	0
	0101	1	0
	⋮		

FIG. 4