

IN SITU FORMED DRAIN AND SOURCE REGIONS INCLUDING A STRAIN INDUCING ALLOY AND A GRADED DOPANT PROFILE

FIELD OF THE PRESENT DISCLOSURE

Generally, the present disclosure relates to integrated circuits and more particularly to transistors having complex dopant profiles and including a strain inducing alloy, such as a silicon/germanium alloy, for creating strain in the channel region.

DESCRIPTION OF THE PRIOR ART

Integrated circuits comprise a large number of circuit elements on a given chip area according to a specified circuit layout, wherein transistors, such as field effect transistors, represent an important component that is used as switching element, current and/or voltage amplifier. The transistors are formed in and above substantially crystalline semiconductor regions with additional dopant materials that are formed at specified substrate locations to act as "active" regions, that is, to act, at least temporarily, as conductive areas for creating a controlled current flow. Generally, a plurality of process technologies are currently practiced, wherein for complex circuitry, such as microprocessors, storage chips, and the like, MOS technology is currently one of the most promising approaches due to the superior characteristics in view of operating speed and/or power consumption and/or cost efficiency. During the fabrication of complex integrated circuits using, for instance, MOS technology, millions of transistors, e.g., n-channel transistors and/or p-channel transistors, are formed on a substrate including a crystalline semiconductor layer. A transistor, irrespective of whether an n-channel transistor or a p-channel transistor or any other transistor architecture is considered, comprises so-called pn-junctions that are formed by an interface of highly doped regions, such as drain and source regions, with a lightly doped or non-doped region, such as a channel region, disposed adjacent to the highly doped regions. In case of a field effect transistor the conductivity of the channel region, i.e., the drive current capability of the conductive channel, is controlled by a gate electrode formed adjacent to the channel region and separated therefrom by a thin insulating layer. The conductivity of the channel region upon formation of a conductive channel due to the application of an

appropriate control voltage to the gate electrode, depends on the dopant concentration, the mobility of the charge carriers, and – for a given extension of the channel region in the transistor width direction – on the distance between the source and drain regions, which is also referred to as channel length. Hence, the conductivity of the channel region substantially affects the performance of the MOS transistors. Thus, the scaling of the channel length - and associated therewith the reduction of channel resistivity - renders the channel length a dominant design criterion for accomplishing an increase in the operating speed of the integrated circuits.

The continuing shrinkage of the transistor dimensions, however, entails a plurality of issues associated therewith that have to be addressed so as to not unduly offset the advantages obtained by steadily decreasing the dimensions of transistors. For example, highly sophisticated dopant profiles, in the vertical direction as well as in the lateral direction, are required in the drain and source regions so as to provide for low sheet and contact resistivity in combination with a desired channel controllability in order to counter so-called short channel effects, such as drain induced barrier lowering, and the like. In addition, the vertical location of the pn junctions with respect to the gate insulation layer also represents a critical design criterion in view of leakage current control, as reducing the channel length also requires reducing the depth of the drain and source regions with respect to the interface formed by the gate insulation layer and the channel region, thereby calling for sophisticated implantation techniques.

Furthermore, since the continuous size reduction of the critical dimensions, e.g., the gate length of the transistors, necessitates the adaptation and possibly the new development of highly complex process techniques concerning the above-identified process steps, it has been proposed to also enhance device performance of the transistor elements by increasing the charge carrier mobility, for instance, in the channel region for a given channel length, thereby offering the potential for achieving a performance improvement that is comparable with the advance to a future technology node of down-sized devices while avoiding many of the above process adaptations associated with device scaling. In principle, at least two mechanisms may be used, in combination or separately, to increase the mobility of the charge carriers in the channel region. First, in field effect transistors the dopant concentration within the channel region may be reduced, thereby reducing scattering events for the charge carriers and thus increasing the conductivity. However, reducing the dopant concentration in the channel region significantly affects

the threshold voltage of the transistor device, thereby presently making a reduction of the dopant concentration a less attractive approach unless other mechanisms are developed so as to adjust a desired threshold voltage. Second, the lattice structure in respective semiconductor regions, such as the channel region, may be dilated/stretched, for instance by creating tensile or compressive strain therein, which results in a modified mobility for electrons and holes, respectively. For example, creating uniaxial tensile strain in the channel region of a field effect transistor with respect to the current flow direction increases the mobility of electrons, which, in turn, may directly translate into a corresponding increase in the conductivity. On the other hand, compressive strain in the channel region may increase the mobility of holes, thereby providing the potential for enhancing the performance of p-type transistors. The introduction of stress or strain engineering into integrated circuit fabrication is an extremely promising approach for further device generations, since for example strained silicon may be considered as a "new" type of semiconductor, which may enable the fabrication of fast powerful semiconductor devices without requiring expensive semiconductor materials and manufacturing techniques.

Consequently, it has been proposed to introduce a silicon/germanium alloy in the drain and source regions of p-channel transistors so as to create compressive stress that may result in a corresponding strain.

With reference to Figs. 1a and 1b, typical conventional approaches will be described for enhancing performance of p-channel transistors with respect to reduce short channel effects, enhancing charge carrier mobility in the channel region and reducing overall series resistance of the drain/source path.

Fig 1a schematically illustrates a cross-sectional view of a p-channel transistor 100 including a substrate 101, such as a silicon bulk substrate, and SOI (silicon on insulator) substrate, ie. a buried insulating layer (not shown) may be formed on the substrate 101. Furthermore, a semiconductor layer 102, such as a silicon layer, is formed above the substrate 101 and may include isolation structures 103, such as shallow trench isolations and the like. The isolation structures 103 may define an "active" region in and above which one or more transistor elements may be formed, such as the transistor 100. It should be appreciated that an active region is to be understood as a semiconductor region receiving or having formed therein appropriate dopant profiles so as to adjust the

overall conductivity in accordance with device requirements, for instance for achieving transistor characteristics and the like. In the manufacturing stage shown a gate electrode structure 104 may be formed above the semiconductor layer 102, wherein a gate insulation layer 104a of the gate electrode structure 104 separates a gate electrode material, such as polysilicon and the like, from a channel region 105 in the semiconductor layer 102. Moreover, as illustrated, the gate electrode structure 104b may have formed on sidewalls thereof a non-electrode material in the form of spacer elements, such as silicon dioxide and the like. Furthermore, the gate electrode structure 104 is encapsulated by spacer elements 107 and a cap layer 108, which may for instance be comprised of silicon nitride. Furthermore, recesses or cavities 106 are formed in the semiconductor layer 102 laterally adjacent to and offset from the gate electrode structure 104, wherein a lateral offset is substantially determined by the width of the spacer 104b and the spacer 107.

A typical conventional process flow for forming the transistor 100 as shown in Fig 1a may comprise the following processes. After forming the isolation structures 103 an appropriate vertical dopant profile within the semiconductor layer 102 may be defined by accordingly designed implantation processes. Thereafter, material layers for the gate electrode structure 104, ie. a gate dielectric material and an electrode material, may be formed by appropriate techniques, such as thermal or wet chemical oxidation and/or deposition for the gate dielectric, while frequently low pressure chemical vapour deposition (LPCVD) may be used for depositing polysilicon as a gate electrode material. Moreover, further material layers such as material for the cap layer 108, which may act as a portion of an antireflective coating (ARC), may also be deposited in accordance with well-established process recipes. The resulting layer stack may then be patterned by advanced photolithography and etch techniques, followed by the formation of the spacer 104b, for instance by thermal oxidation, deposition and the like. Next, a spacer material may be deposited, for instance in combination with a liner material, if required, which may then be patterned by well-established anisotropic etch techniques to obtain the spacer elements 107, the width of which may substantially determine the lateral offset of the cavities 106.

As previously explained, uniaxial compressive strain in the channel region 105 in the current flow direction may significantly enhance the mobility of holes thereby enhancing overall performance of the transistor 100 when representing a p-channel transistor. In

order to provide the desired compressive strain the cavities 106 may be formed by well-established etch techniques using the spacers 107 and the cap layer 108 as an etch mask, wherein in the example shown also the isolation structures 103 may act as an etch mask. In other cases, an additional hard mask layer may be provided if the lateral extension of the cavities 106 is to be restricted so as to not entirely extend to the isolation structures 103. During the corresponding etch process, also a certain amount of template material of the layer 102 may be maintained if an SOI configuration is considered, in which a buried insulating layer may be positioned between the substrate 101 and the semiconductor layer 102. The cavities 106 may be refilled with an appropriate semiconductor material, such as silicon/germanium alloy, which has a natural lattice constant that is greater than the lattice constant of silicon, so that the corresponding epitaxially grown material may be formed in a strained state, thereby also exerting stress to the channel region 105 and thus creating a respective compressive strain therein. Selective epitaxial growth techniques for depositing silicon/germanium alloy materials are well-established in the art and may be performed on the basis of appropriately selected process parameters, such as temperature, pressure, flow rate of precursor gases and carrier gases in such a manner that a significant deposition of material is substantially restricted to the crystalline silicon surfaces, while a deposition on dielectric materials may be suppressed. Moreover, during the deposition of the silicon/germanium material, also a desired dopant species may be incorporated into the deposition atmosphere, such as boron, in order to obtain a desired base doping for drain and source regions, depending on the required complexity of the vertical and lateral profile of the drain and source regions. Generally, a reduced series resistance of the drain and source regions may be achieved by providing for high dopant concentrations, while on the other hand, for highly scaled semiconductor devices, the corresponding electric field generated across the channel region 105 may result in increased charge carrier injection into the gate insulation layer 104a at high dopant concentrations, thereby typically requiring a reduced dopant concentration and a shallow profile of the drain and source regions in the vicinity of the gate electrode structure 104.

Fig 1b schematically illustrates the transistor 100 in a further advanced manufacturing stage, in which the silicon/germanium alloy 109 may be formed in the cavities 106, as explained above, and wherein the spacers 107 and the cap layer 108 may be removed so as to expose the gate electrode structure 104. It should be appreciated that the spacers 104b may also be removed and may be replaced by appropriately designed

offset spacers, if desired. As explained above, upon reducing the transistor dimensions, ie. the gate length of the transistor 100, which is to be understood as the horizontal dimension of the gate electrode structure 104 in Fig 1b, controllability of the channel region 105 may become increasingly difficult due to the short channel effects which, in some conventional approaches, may be countered in part by providing counter-doped regions 110, which may also be referred to as halo regions, in which the dopant concentration of the channel region 105 and the remaining semiconductor region, also referred to as the body region 102a, is significantly increased thereby adjusting the inter gradient at corresponding pn junctions to be formed by providing shallow doped drain and source regions. Typically, the counter-doped regions or halo regions 110 may be formed by ion implantation, for instance using a tilt angle, in order to establish a certain degree of overlap with the gate electrode structure 104. However, upon further scaling the transistor dimensions, also the dopant concentration and thus implantation dose may have to be increased, thereby also increasing dopant induced charge carrier scattering, dopant diffusion and due to the high dose implantation processes involved, stress relaxation in the vicinity of the channel region 105. Furthermore, a dopant concentration in the drain and source regions is generally increased in order to obtain a reduced series resistance of the drain and source regions for not limiting device performance, also dose and energy for the implantation process for creating the halo regions 110 has to be increased. This in turn may further increase stress relaxation in the silicon/germanium alloy due to increased lattice damage and higher dopant diffusion. During the sophisticated implantation processes longer treatment times may be required so as to obtain the desired high dose during the creation of the halo regions 110. Thus, although the silicon/germanium material 109 may be provided with high intrinsic dopant concentration, nevertheless sophisticated and long implantation processes may be required for adjusting the pn junctions in the vicinity of the gate electrode structure 104 on the basis of the halo regions 110.

Due to the significant strain relaxation caused by the preceding implantation processes, it has also been proposed to incorporate the silicon/germanium alloy at a later manufacturing stage, ie. after incorporating the dopant species for the extension regions and the halo regions in order to avoid implantation induced damage. Furthermore, corresponding to this strategy the silicon/germanium alloy has to be highly doped to provide the corresponding high dopant concentration for the deep drain and source areas. Consequently, the intrinsic strain component may substantially be maintained

and may thus provide enhanced internal strain from the silicon/germanium alloy. On the other hand, however, a lateral distance of the heavily doped silicon/germanium alloy may be required with respect to the channel region since a moderately high dopant gradient may result in a significant dopant diffusion, which may result in a reduced conductivity in the channel region, if increasingly dopant atoms may be incorporated therein. The problem may even further become relevant when a certain degree of dopant diffusion is desirable in order to increase depth of the heavily doped drain and source areas, for instance so as to connect to a buried insulating layer in order to reduce the parasitic junction capacitance in SOI devices. Since both a high internal strain level of the silicon/germanium material and the lateral distance to the channel region substantially determine the overall strain component induced in the channel region, the advantage gained by reducing the implantation induced relaxation may be compensated or even over-compensated by requiring an increased offset of the in situ doped silicon/germanium material so that the approach may be less than desirable, in particular for sophisticated applications in which the deep drain and source regions have to extend down to the buried insulating layer in partially depleted SOI transistors. On the other hand, the reduction of the offset of heavily in situ doped silicon/germanium material may not represent an attractive approach since the significant dopant diffusion may contribute to an integrated overall drain and source dopant profile, which may finally result in increased leakage currents, which may finally lead to total failure of the transistor.

In view of the situation described above, the present disclosure relates to methods and transistor devices in which enhanced strain efficiency may be accomplished on the basis of strain inducing semiconductor alloys while avoiding or at least reducing one or more of the problems identified above.

SUMMARY OF THE DISCLOSURE

In general, the present disclosure relates to methods and transistor devices in which complex vertical and lateral dopant profiles may be established in the drain and source regions on the basis of a selective epitaxial growth process for incorporating a strain inducing semiconductor alloy, which may be provided with a specifically designed in situ dopant concentration, which may result in the desired profile. To this end, in situ dopant concentration may be provided as a graded dopant profile in which the drain/source

dopant species may be provided with a different concentration at different height levels within the epitaxially grown material, wherein a degree of dopant diffusion may thus be determined by the vertical distribution of the dopant species in combination with appropriately selected process parameters for one or more anneal processes, which may generally be performed at a significantly lower temperature compared to conventional strategies. According to other aspects disclosed herein, the in situ doped semiconductor alloy may advantageously be combined with one or more implantation steps, which may be performed prior to the epitaxial growth process so as to avoid implantation induced damage, while nevertheless providing for enhanced flexibility in designing the overall dopant profile. In some illustrative embodiments disclosed herein, the implantation process may be performed through the corresponding cavities, thereby providing for enhanced process efficiency, in particular in sophisticated semiconductor devices in which the gate height may not provide for sufficient ion blocking capability so as to allow implantation species to be positioned close to the buried insulating layer of an SOI device. Thus, by incorporating at least a portion of the drain/source dopant species through the cavities, significantly lower implantation energies may be used, thereby avoiding or at least significantly reducing the probability of implanting drain/source dopant species into the channel region through the gate electrode structure.

Hence, a very efficient manufacturing sequence for providing sophisticated drain and source regions may be accomplished since the number of complex spacer fabrication steps and lithography steps for forming drain and source regions compared to conventional techniques may be reduced.

One illustrative method disclosed herein comprises forming cavities in an active region of a transistor laterally adjacent to a gate electrode structure which comprises a gate dielectric material, an electrode material formed on the gate dielectric material and an offset sidewall spacer. The method further comprises forming a strain inducing semiconductor alloy in the cavities, wherein the strain inducing semiconductor alloy comprises a dopant species having a varying dopant concentration along a height direction of the cavities. Additionally, the method comprises performing a heat treatment so as to form drain and source extension regions on the basis of the varying dopant concentration of the dopant species, wherein the drain and source extension regions connect to a channel region of the transistor.

A further illustrative method disclosed herein relates to forming drain and source regions of a transistor. The method comprises implanting a first portion of a drain and source dopant species through cavities into an active region of the transistor. Additionally, the method comprises forming a strain inducing semiconductor alloy in the cavities, wherein the strain inducing semiconductor alloy comprises a second portion of the drain and source dopant species that has a graded concentration with respect to a height direction of the cavities. Finally, the method comprises performing at least one heat treatment to form a final dopant profile of the drain and source regions on the basis of the first and second portions of the drain and source dopant species.

One illustrative transistor device disclosed herein comprises a gate electrode structure formed above a channel region and drain and source regions formed in an active semiconductor region laterally adjacent to the channel region. Furthermore, the transistor device comprises a strain inducing semiconductor alloy formed within the drain and source regions, wherein the strain inducing semiconductor alloy has a graded dopant concentration along a height direction of the drain and source regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Further embodiments of the present disclosure are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figs 1a and 1b schematically illustrate cross-sectional views of a transistor during various manufacturing stages in forming drain and source regions on the basis of an epitaxially grown semiconductor alloy with in situ doping and subsequent implanted halo regions according to conventional strategies; and

Figs 2a – 2h schematically illustrate cross-sectional views of a transistor device during various manufacturing stages wherein a sophisticated drain and source dopant profile may be obtained on the basis of a graded in situ doping of a strain inducing semiconductor alloy according to illustrative embodiments.

DETAILED DESCRIPTION

While the present disclosure is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present disclosure to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present disclosure, the scope of which is defined by the appended claims.

Generally, the present disclosure addresses the problem of increased complexity of manufacturing techniques in which sophisticated drain and source dopant profiles may be accomplished on the basis of selective epitaxial growth techniques in combination with implantation processes. A significant reduction of the overall process complexity may be accomplished according to the principles disclosed herein by providing a graded in situ dopant concentration in a strain inducing semiconductor alloy, which may thus be positioned closely to the channel region of the transistor. Furthermore, in combination with appropriately designed anneal processes, which may be performed at lower temperatures, the graded dopant profile in the strain inducing semiconductor alloy may result in the desired lateral and vertical profile of the drain and source regions, wherein in some illustrative embodiments disclosed herein additionally the depth of the drain and source regions may separately be adjusted on the basis of an implantation process or any other process for incorporating the drain and source dopant species prior to actually growing the strain inducing semiconductor alloy. For this purpose, in one illustrative embodiment, the drain and source dopant species for the deep drain and source areas may be incorporated through the corresponding cavities so that the dopant species may be positioned at any desired depth within the active region, for instance at the interface to a buried insulating layer, without requiring unduly high implantation energies. Consequently, the integrity of the channel region and of sensitive gate dielectric materials may be preserved during the corresponding implantation process, even if a reduced gate height may be required due to a reduction of the fringing capacitance, or a less critical surface topography caused by the gate electrode structures. In still other illustrative embodiments other species may be

incorporated, such as counter doping species for forming halo regions or any other type of material species that may be used for adjusting the overall electronic characteristics of the transistor, for instance by positioning species for defining energy traps at shallow areas of the drain and source region, which may also be accomplished by implantation techniques performed through the cavities prior to depositing the strain inducing semiconductor alloy. Consequently, the entire dopant profile may be defined on the basis of single configuration of the gate electrode structure without requiring complex spacer configurations, thereby contributing to a reduced complexity of the overall manufacturing flow. Furthermore, in some illustrative embodiments, the deep drain and source regions as well as the halo regions and any other additional implantation species may be incorporated on the basis of the same lithography mask, the number of masking steps may be reduced compared to conventional strategies, thereby also contributing to a reduced and thus cost efficient manufacturing flow. Moreover, since sophisticated spacer techniques may not be required for defining a dopant profile of the drain and source regions, any additional spacer elements which may be used for forming metal silicide regions, may specifically be adjusted with respect to enhancing performance of the silicidation process, without necessitating any compromises with respect to also providing an implantation mask for defining deep drain and source regions, as may be the case in many conventional approaches. It should be appreciated that the principles disclosed herein may be highly advantageous in the context of sophisticated semiconductor devices in which transistor elements of critical dimensions on 50 nm and less may be provided, since here typically performance enhancing mechanism may be required, such as the incorporation of strain inducing semiconductor alloys while at the same time sophisticated drain and source profiles may be required in view of channel controllability and the like, as previously explained. In some illustrative embodiments disclosed herein, the sophisticated manufacturing flow and the resulting drain and source profiles may be applied in combination with advanced gate configurations since including high-k dielectric materials, which may be understood as dielectric materials having a dielectric constant of 10.0 or higher in combination with metal-containing electrode materials. Also in this case significant advantages may be gained, for instance by using anneal techniques of reduced temperature, which may reduce the probability of creating defects in sensitive high-k dielectric

material, wherein additionally an offset spacer element used for defining an offset of cavities to be etched in the active region may provide for enhanced integrity of sensitive high-k materials without requiring additional spacer elements.

With reference to Figs 2a – 2h further illustrative embodiments will now be described in more detail, wherein also reference may be made to Figs 1a and 1b, if required.

Fig 2a schematically illustrates a cross-sectional view of a semiconductor device 200, which may be provided in the form of transistors, such as a p-channel transistor that may receive a semiconductor alloy in drain and source areas by a selective epitaxial growth technique so as to provide a graded in situ dopant profile. The device 200 may comprise a substrate 201, above which may be formed a semiconductor layer 202, such as a silicon-based layer, which may be understood as a material layer having incorporated therein a significant amount of silicon, possibly in combination with other materials, such as germanium, carbon, fluorine, and the like. Furthermore, in the embodiment shown, a buried insulating layer 210a may be provided between the substrate 201 and the semiconductor layer 202, thereby forming an SOI architecture, which may be advantageous, for instance with respect to a reduced junction capacitance, as previously explained. In other illustrative embodiments (not shown in Fig 2a) the buried insulating layer 210a may be omitted, as is for instance described with reference to the transistor 100 of Figs 1a and 1b. Furthermore, the device 200 may comprise a gate electrode structure 204, which may include a gate electrode material 204c in the form of any appropriate conductive material, such as polysilicon, metal-containing materials and the like. For example, in sophisticated semiconductor devices, an enhanced conductivity may be required, which may be accomplished by providing a metal-containing material, which may be provided possibly in combination with other materials, such as polysilicon, at an early manufacturing stage. For instance, a corresponding metal-containing electrode material, such as titanium nitride, possibly in combination with additional species, may be provided in the material 204c so as to be formed on a gate insulation layer 204a, which may be provided in the form of any appropriate dielectric material, such as silicon dioxide, silicon oxynitride, silicon nitride and

the like, wherein a thickness may have to be adapted to a length of the gate electrode structure 204, as previously explained. In some cases, in the gate insulation layer 204a, a high-k dielectric material may be included in the layer 204a, thereby providing for enhanced controllability of a channel region 205 at reduced leakage currents compared to conventional dielectric materials. For example, the gate insulation layer 204 may comprise materials, such as hafnium oxide, hafnium zirconium oxide and the like, while additionally a metal-containing material may be formed on the layer 204a, thereby substantially avoiding the creation of a depletion zone, as may frequently be observed in gate electrodes formed on the basis of a polysilicon material. It should be appreciated that in illustrative embodiments the gate length, ie. the length of the electrode material 204c, as indicated as 204l, may be approximately 50 nm and less, since typically for such applications sophisticated drain and source profiles may be required in combination with additional performance enhancing mechanisms, as already discussed above. Moreover, in the embodiment shown, the gate electrode structure 204 may comprise an offset spacer element 204b, which may be comprised of any appropriate material, such as silicon nitride and the like, wherein a width of the spacer 204b may substantially determine a lateral offset of cavities to be formed laterally adjacent to the gate electrode structure 204 in the semiconductor layer 202, ie. in corresponding active region 202a of the device 200. Thus, the spacer element 204b may, in combination with a cap material 204d, preserve integrity of the electrode material 204c and the gate insulation layer 204a. For instance, high-k dielectric materials may exhibit pronounced sensitivity during a plurality of wet chemical etch processes, for instance processes including hydrofluoric acid and the like, which may be required for removing contaminants and the like. Thus, the spacer element 204b may encapsulate the gate insulation layer 204a and may additionally provide a high etch resistivity during the subsequent processing for forming corresponding cavities in the active region 202a. Furthermore, the cap layer 204d, which may be comprised of silicon nitride and the like, may act as an etch mask and a growth mask during the subsequent processing.

With respect to any manufacturing techniques and characteristics of the device 200, it may also be referred to the corresponding description given with reference to the device 100, wherein it should be appreciated that a cap material

204d and the offset spacer 204b may appropriately be selected in terms of material composition and thickness so as to comply with the further process requirements. For example, as previously discussed with reference to the cap layer 108 (cf. Fig 1a) the cap material 204d may be patterned along with at least a portion of the gate electrode material 204c, wherein the patterning sequence may depend on the composition of the electrode material 204d. For example, appropriate metal species may be deposited, for instance in combination with a polysilicon material, when sophisticated gate electrode structures are considered. Similarly, the gate insulation layer 204a may be provided on the basis of any appropriate manufacturing technique. Thereafter, a spacer material may be deposited, for instance by thermally activated CVD techniques so as to obtain a highly dense material and a well controlled thickness. Thereafter, the spacer layer may be patterned on the basis of well-established anisotropic etch techniques, thereby obtaining the spacer 204b having the required etch resistivity and width that is appropriate for the further processing. For example, the spacer 204b may have a width of approximately one nanometer to several nanometers, depending on the desired offset of a cavity to be formed in the region 202a.

Fig 2b schematically illustrates the semiconductor device 200 when exposed to an etch ambient 210, which may be established on the basis of a plasma assisted ambient using an etch chemistry, for instance on the basis of fluorine, chlorine and the like, in order to remove material of the region 202a selectively to the gate electrode structure 204 and also to the isolation structure 203, wherein however a corresponding etch resistivity may be less pronounced compared to the cap layer 204d and the spacer 204b. During the etch process 210 cavities 206 may be formed with a lateral offset with respect to the electrode material 204c that is substantially determined by the spacer 204b and the etch parameters of the process 210.

Fig 2c schematically illustrates the device 200 during an ion implantation sequence 212 according to one illustrative embodiment in order to introduce one or more dopant species into the region 202a on the basis of the cavities 206. In one illustrative embodiment the implantation process 212 may comprise an implantation step for introducing a portion of a drain and source dopant species,

which may be indicated by 214d, which may correspond to deep drain and source regions, the finally desired profile may be established on the basis of one or more further heat treatments, which cause a certain degree of dopant diffusion, if desired. As illustrated, the actual penetration depth for incorporating the deep drain and source species 214d may significantly be reduced due to the presence of the cavities 206, so that a moderately low implantation energy may be applied, while nevertheless depositing the species 214d so as to extend to a target depth, for instance at least to the buried insulating layer 201a. Due to the moderately low implantation energy, the ion blocking capability of the gate electrode structure 204 may reliably provide for integrity of the channel region 205 so that in general reduced gate heights may be used, which may be advantageous in view of a reduced fringing capacitance of the gate electrode 204 and also in view of a less pronounced surface topography. Moreover, the implantation sequence 212 may comprise one or more additional implantation steps for incorporating the dopant species, for instance a counter doping species, so as to define a counter doped or halo region 210, which may be accomplished on the basis of an appropriate tilt angle, wherein a symmetric or asymmetric configuration of the halo regions 210 may be applied, depending on the overall device requirements. As is illustrated, also in this case a moderately low penetration depth may be required and thus corresponding reduced implantation energies may be used. In some illustrative embodiments the implantation sequence 212 may also comprise an amorphization implantation, which may be performed as a tilted implantation process, when corresponding channeling effects during the incorporation of the counter doping species for the halo region 210 may be considered inappropriate. Thus, in this case a certain portion may be amorphized, thereby enhancing the uniformity of dopant penetration for defining the halo regions 210. It should be appreciated that significant amorphization of the material at the bottom of the cavities 206 may be avoided by using an appropriate tilt angle. Furthermore, the implantation sequence 212 may comprise one or more additional implantation steps, in which any other appropriate species, such as fluorine, carbon and the like may be introduced in order to define a shallow implantation region 213, depending on the overall electronic characteristics of the device 200. Thus, the deep drain and source species 214d, the halo region 210, any further shallow implantation species and possibly a corresponding amorphization process may be performed

without requiring a change of implantation mask or without additional spacer elements, thereby contributing an overall enhanced manufacturing and thus cost efficient process technique.

Fig 2d schematically illustrates the semiconductor device 200 according to some illustrative embodiments in which a heat treatment 215 may be applied when implantation induced damage, as indicated by 214s, may be considered inappropriate during a subsequent selective epitaxial growth process. In other cases a preceding amorphization may be recrystallized, thereby also activating dopant species to a certain degree. It should be appreciated that the heat treatment 215 may be performed on the basis of any appropriate process parameters using well-established techniques, such as laser anneal, flashlight anneal and the like. For instance, if desired, appropriate process parameters may be selected in which a recrystallization may occur without inducing significant dopant diffusion. In other cases, the heat treatment 215 may be omitted in this manufacturing stage when corresponding implantation induced damage is considered to be relevant. After the implantation sequence 212 or after the heat treatment 215, the device 215 may be prepared for a subsequent selective epitaxial growth process. For this purpose any appropriate wet chemical cleaning processes may be performed, wherein a spacer 204b may preserve integrity of the gate insulation layer 204a, if comprised of a sensitive high-k dielectric material.

Fig 2e schematically illustrates the semiconductor device 200 during a selective epitaxial growth process 216a, during which a strain inducing semiconductor material 209a may be grown within the cavities 206. During process 216a an appropriate dopant species, such as an n-type species or a p-type species, may be incorporated into the deposition ambient in order to form the material 209a as an in situ doped material. For this purpose, well-established deposition recipes may be used, as is also previously described. For example, the material 209a may represent a silicon/germanium alloy when the device 200 requires a compressive strain component. In other cases, a silicon/germanium/tin alloy may be deposited while in still other cases a silicon/tin mixture may be formed in order to obtain a desired compressive strain component. In other illustrative embodiments material 209a may be provided in the form of a silicon/carbon alloy

when the transistor 200 may require a tensile strain component. Thus, a high degree of flexibility may be obtained by selecting an appropriate material composition, which may significantly influence the overall strain component and also by selecting an appropriate dopant concentration. For example, the concentration of the layer 209a may be selected moderately high so as to establish in combination with a previously deep drain and source species 214d, a desired overall dopant concentration. In a subsequent phase or in a separate step, indicated as 216b, a further material layer 209b may be deposited, wherein at least a dopant concentration may be different compared to the concentration in the layer 209a. For example, a reduced dopant concentration 209 may be provided so that the layer 209b may act as a "buffer" layer. In other cases, the material 209a may be provided with a reduced dopant concentration compared to the layer 209b, depending on the desired final drain and source profile. Thus, the dopant concentration may vary along a height direction 206h due to the different process parameters of the deposition phases or steps 216a, 216b. It should be appreciated that a corresponding change of the dopant concentration within 1 nm or less along the direction 206h, depending on the corresponding process parameters. In this case, a more or less step-like variation of the dopant concentration may be obtained while in other cases a less pronounced transition may occur, wherein nevertheless a corresponding change of concentration may reliably be detected within the layers 209a, 209b along the direction 206h. It should be appreciated that a corresponding variation of a dopant concentration may also be referred to as a graded dopant concentration.

Fig 2f schematically illustrates the semiconductor device 200 during a further selective implantation process or phase, in which a final or extension layer 209c may be provided with an appropriate in situ concentration in order to provide drain and source extension regions in combination with one or more heat treatments to be performed in a later manufacturing stage. It should be appreciated that in addition to the in situ doping also the material composition may be modified with respect to the layers 209b, 209a, if considered appropriate. Consequently, on the basis of two or more of the deposition processes 216a, 216b, 216c any appropriate number of epitaxially grown layers of strain inducing semiconductor material may be formed, wherein in at least some of these layers a different in situ doping may be provided so as to comply with requirements for

forming a complex drain and source dopant profile in combination with any subsequent heat treatments. Thus, it should be appreciated that two layers of strain inducing semiconductor material or more than three layers may be provided, while in other cases a more or less continuous variation of the in situ dopant concentration may be applied. Thus, contrary to conventional approaches, a significantly non-constant in situ dopant concentration along the height direction 206a may be used in order to provide appropriate start conditions for a subsequent heat treatment during which the final dopant profile may be determined.

Fig 2g schematically illustrates the semiconductor device 200 when subjected to a heat treatment 217, for instance in the form of a laser anneal process, a flashlight anneal process and the like in which appropriate process parameters may be applied so as to obtain a desired degree of dopant diffusion in order to establish drain and source regions 214 on the basis of the drain and source dopant species 214d and the various source dopant species incorporated in the layers 209a, 209b, 209c. It should be appreciated that the diffusion behaviour may also depend on the previously implanted species 210 forming corresponding halo or counter doped regions so that during the process 217 a corresponding final dopant profile for the drain and source regions 214 may be obtained. For example, respective extension regions 214e may be obtained on the basis of the layer 209c, which may comprise an appropriate dopant concentration so as to avoid undue penetration of the channel region 205. Furthermore, an appropriate lateral shape may be obtained by correspondingly adjusting the in situ doping level in the layer 209b, which may act as a buffer layer while the layer 209a in combination with the species 214d may provide for a deep drain source area. It should be appreciated that one or more additional heat treatments may be performed at any appropriate manufacturing stage after providing the strain inducing semiconductor alloy 209a, 209b, 209c, depending on the overall process and device requirements. Furthermore, generally the heat treatment 217 may be performed at reduced process temperatures since a pronounced recrystallization of implantation induced damage may not be required. Thus, the materials 209a, 209b, 209c may be provided in a substantially non-damaged state thereby obtaining a high strain transfer efficiency into the channel region 205, wherein also a desired reduced offset defined by the spacer element 204b

may contribute to a high strain inducing efficiency. Consequently, the drain and source regions 214 may be provided on the basis of a manufacturing sequence without requiring complex spacer structures and a plurality of masking steps, as may typically be required in conventional strategies.

It should be appreciated that prior to or after the anneal process 217, the offset spacer 204b in combination with the mask layer 204d may be removed, for instance on the basis of well-established wet chemical etch recipes and the like. Thereafter, the further processing may be continued, for instance by forming a spacer element and performing a silicidation process, if required. Thus, during the preceding process sequence the spacer 204b may reliably preserve integrity of the gate insulation layer 204a and of the gate electrode material 204c and may be removed at a manufacturing stage in which exposure to critical wet chemical etch recipes, such as diluted hydrofluoric acid, may be avoided.

Fig 2h schematically illustrates the device 200 with a spacer structure 218, which may have an appropriate width so as to adjust an offset 219d of metal silicide regions 219 with respect to the channel region 205. The spacer structure 218 may be comprised of any appropriate material, such as silicon nitride, possibly in combination with silicon dioxide as an etch stop material and the like. Furthermore, a metal silicide region 204s may be formed in the electrode material 204c when comprised of polysilicon material. In other cases, material 204s may be removed in a later manufacturing stage, for instance by replacing at least a part of the electrode material 204c by highly conductive metal. It should be appreciated that the spacer structure 218 may be provided on the basis of a target width that has been selected so as to obtain the offset 219 so as to provide for enhanced transistor performance, for instance by avoiding undue "transfer" of dopants towards the channel region 205, which may be caused during the silicidation process. Thus, the characteristics of the spacer structure 218 may be adapted to process parameters of the silicidation process and corresponding materials used, such as nickel, platinum, cobalt and the like, thereby also contributing to enhanced overall transistor performance. If desired, the spacer structure 218 may be removed after forming the metal silicide regions 219, for instance in view of enhancing stress transfer of any dielectric material that may be deposited above the completed transistor structure, thereby enabling

the deposition of an increased amount of highly stressed dielectric material in close proximity to the channel region 205.

As a consequence, the transistor 200 may comprise a strain inducing material 209a, 209b, 209c in a superior crystalline state, thereby inducing a high strain component 205c or 205t, such as a compressive component or tensile component, depending on the material composition of the strain inducing alloy. Furthermore, a graded in situ dopant concentration in materials 209a, ..., 209c may result in a desired lateral and vertical profile of the drain and source regions 214, thereby allowing the materials 209c, 209b, 209a to be positioned in close proximity to the channel region 205, which may also contribute to superior strain transfer efficiency.

As a result, the present disclosure provides semiconductor devices and techniques for forming the same, in which a graded dopant profile may be established in an epitaxially grown strain inducing semiconductor material, which may therefore be positioned in close proximity to the channel region without compromising the resulting dopant profile. Furthermore, additional implant species may be incorporated prior to the epitaxial growth of the strain inducing semiconductor alloy, wherein the presence of the corresponding cavities may provide for enhanced implantation conditions. The drain and source dopant profiles may be obtained without requiring complex spacer structures, which may contribute to a significantly reduced complexity in forming sophisticated transistor elements.

Further modifications and variations of the present disclosure will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the principles disclosed herein. It is to be understood that the forms shown and described herein are to be taken as the presently preferred embodiments.

CLAIMS**1. A method comprising:**

forming cavities in an active region of a transistor laterally adjacent to a gate electrode structure, said gate electrode structure comprising a gate dielectric material, an electrode material formed on said gate dielectric material and an offset sidewall spacer;

forming a strain inducing semiconductor alloy in said cavities, said strain inducing semiconductor alloy comprising a dopant species having a varying dopant concentration along a height direction of said cavities; and

performing a heat treatment so as to form drain and source extension regions on the basis of said varying dopant concentration of said dopant species, said drain and source extension regions connecting to a channel region of said transistor.

- 2.** The method of claim 1, further comprising introducing at least one further dopant species into said active region through said cavities.
- 3.** The method of claim 2, wherein introducing said at least one further dopant species comprises introducing a dopant species determining the same conductivity type as said dopant species for forming drain and source regions in combination with said dopant species.
- 4.** The method of claim 3, wherein introducing said at least one further dopant species comprises introducing a counter-doping species relative to said dopant species for forming a counter-doped region relative to said drain and source regions.
- 5.** The method of claim 2, wherein introducing said at least one further dopant species comprises performing an implantation process.

6. The method of claim 5, further comprising performing a second heat treatment so as to recrystallize crystalline damage prior to forming said strain inducing semiconductor alloy.
7. The method of claim 1, wherein forming said strain inducing semiconductor alloy comprises forming a buffer layer and forming an extension layer above said buffer layer, wherein a dopant concentration of said buffer layer is less than a dopant concentration of said extension layer.
8. The method of claim 1, wherein forming said strain inducing semiconductor alloy comprises forming a buffer layer and forming an extension layer above said buffer layer, wherein a dopant concentration of said buffer layer is higher than a dopant concentration of said extension layer..
9. The method of claim 1, wherein forming said strain inducing semiconductor layer comprises forming a germanium containing material by performing a selective epitaxial growth process.
10. The method of claim 1, wherein forming said strain inducing semiconductor layer comprises forming a tin containing material by performing a selective epitaxial growth process.
11. The method of claim 1, wherein forming said strain inducing semiconductor layer comprises forming a carbon containing material by performing a selective epitaxial growth process.
12. A method of forming drain and source regions of a transistor, the method comprising:

implanting a first portion of a drain and source dopant species through cavities into an active region of said transistor;

forming a strain inducing semiconductor alloy in said cavities, said strain inducing semiconductor alloy comprising a second portion of said drain

and source dopant species having a graded concentration with respect to height direction of said cavities; and

performing at least one heat treatment to form a final dopant profile of said drain and source regions on the basis of said first and second portions of said drain and source dopant species.

13. The method of claim 12, wherein forming said strain inducing semiconductor alloy comprises forming a buffer layer in said cavities and forming an extension layer above said buffer layer, wherein a dopant concentration of said buffer layer is less than a dopant concentration of said extension layer.
14. The method of claim 13, wherein forming said strain inducing semiconductor alloy comprises forming a buffer layer and forming an extension layer above said buffer layer, wherein a dopant concentration of said buffer layer is higher than a dopant concentration of said extension layer.
15. The method of claim 12, wherein said strain inducing semiconductor alloy comprises at least one of germanium and tin.
16. The method of claim 12, wherein said strain inducing semiconductor layer comprises carbon.
17. The method of claim 12, further comprising implanting a further dopant species that is counter-doping relative to said drain and source dopant species prior to forming said strain inducing semiconductor alloy.
18. The method of claim 12, wherein said first portion of said drain and source dopant species is implanted to as to extend to a buried insulating layer.
19. A transistor device comprising:

a gate electrode structure formed above a channel region;

drain and source regions formed in an active semiconductor region laterally adjacent to said channel region; and

a strain inducing semiconductor alloy formed within said drain and source regions, said strain inducing semiconductor alloy having a graded dopant concentration along a height direction of said drain and source regions.

20. The transistor device of claim 19, wherein a length of a gate electrode material of said gate electrode structure is approximately 50 nanometer or less.
21. The transistor device of claim 19, wherein said semiconductor alloy comprises at least one of germanium and tin.
22. The transistor device of claim 19, wherein said strain inducing semiconductor alloy comprises a carbon/silicon alloy.
23. The transistor device of claim 19, further comprising a buried insulating layer formed adjacent to and below said active semiconductor region, wherein said drain and source regions extend to said buried insulating layer.
24. The transistor device of claim 20, wherein said gate electrode structure comprises a gate insulation layer comprising a high-k dielectric material and wherein said gate electrode material comprises a metal containing material formed on said gate insulation layer.

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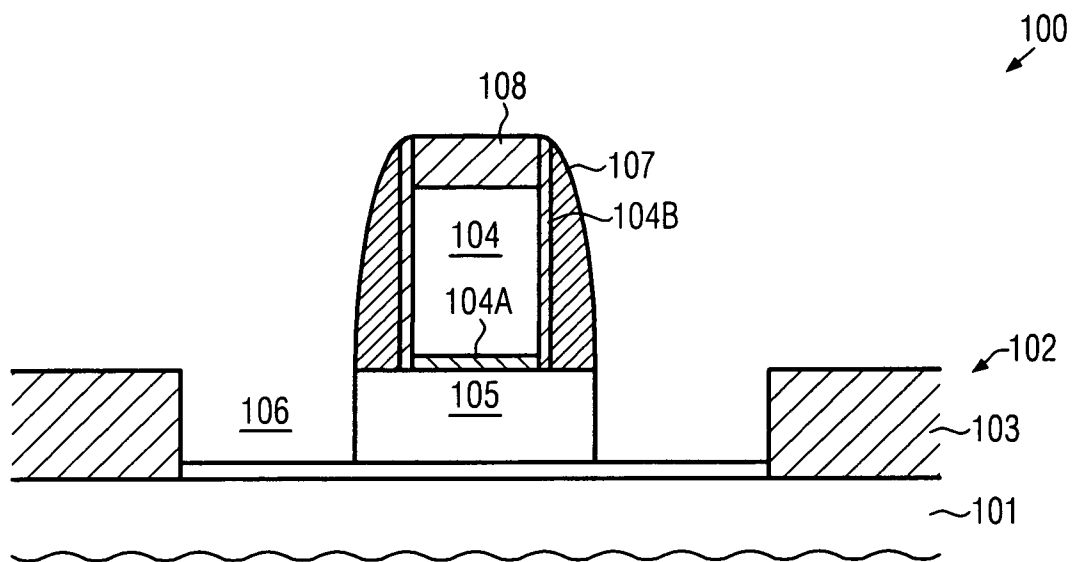


FIG. 1a
(prior art)

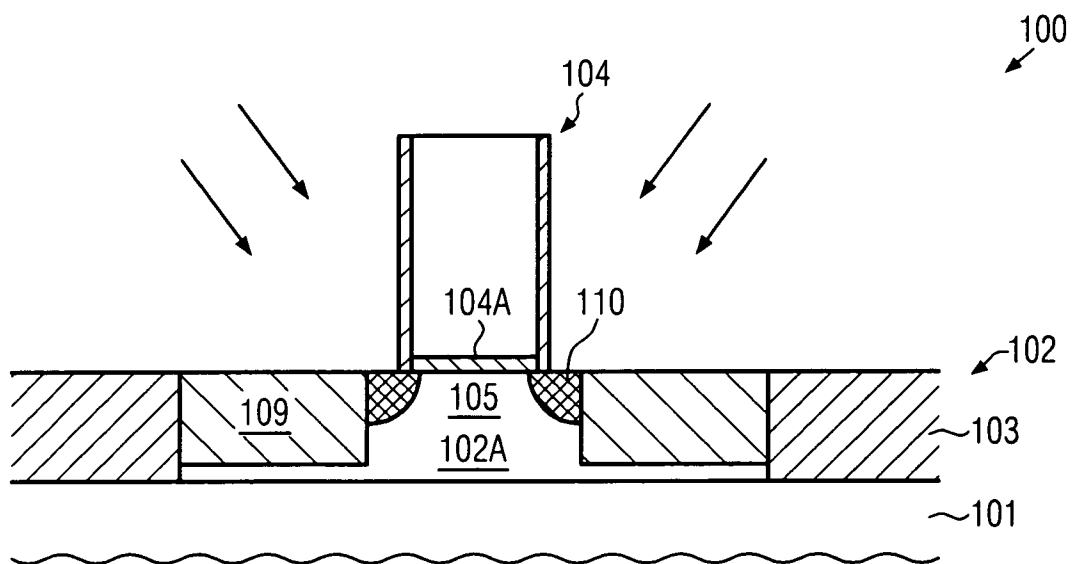


FIG. 1b
(prior art)

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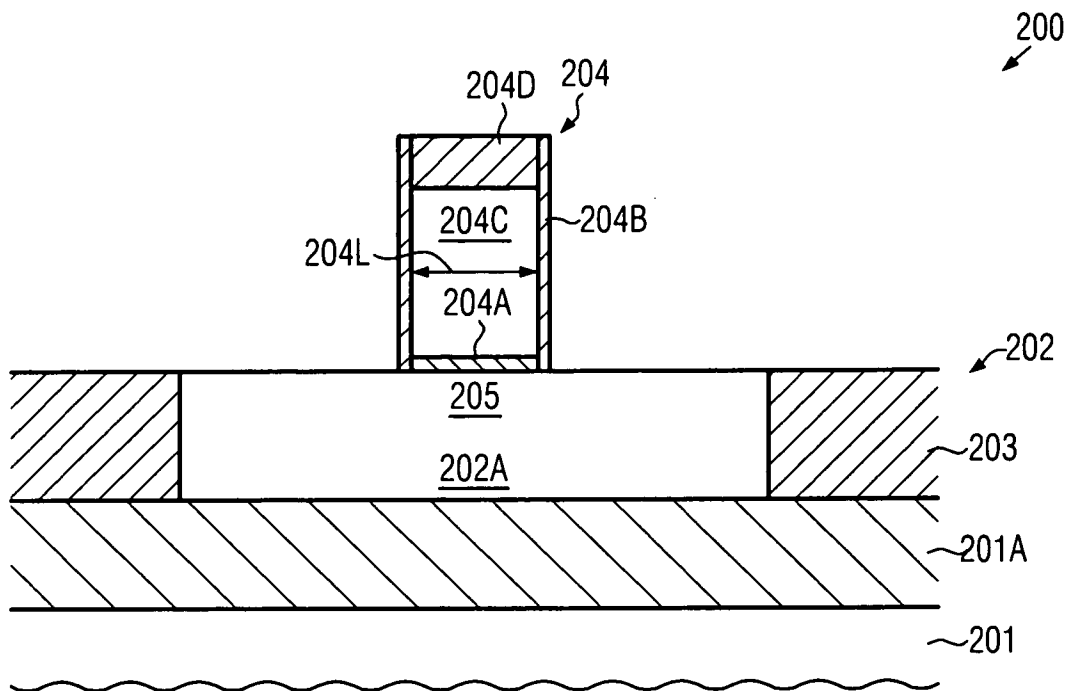


FIG. 2a

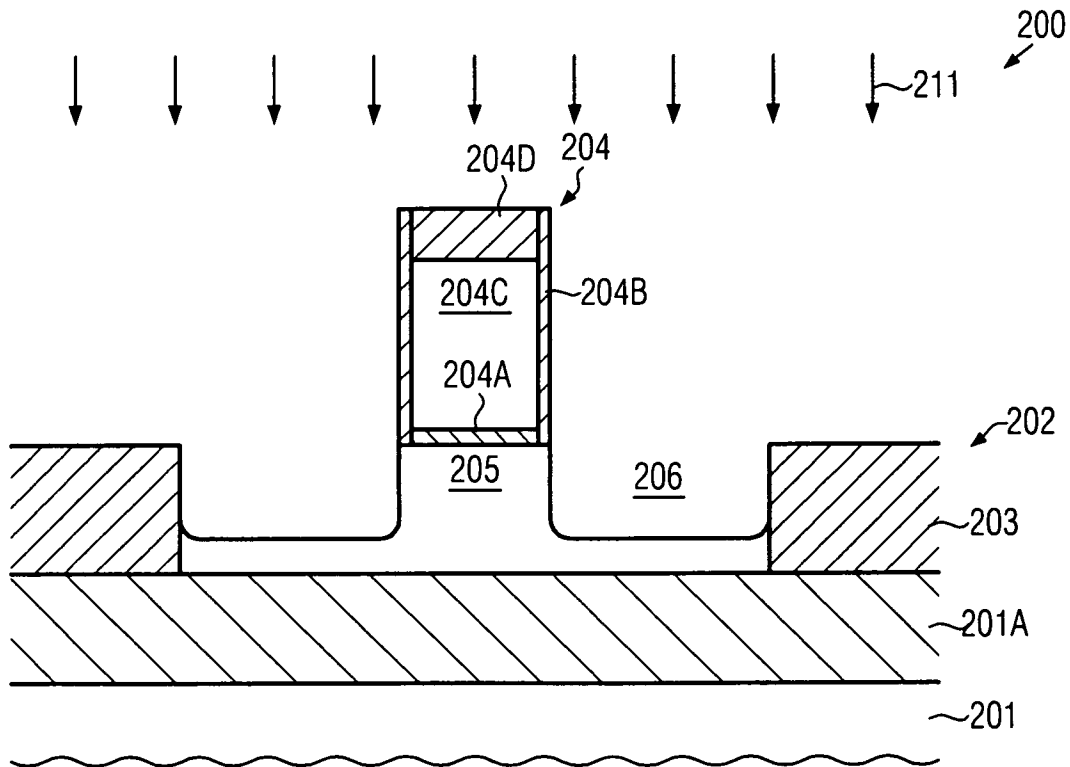


FIG. 2b

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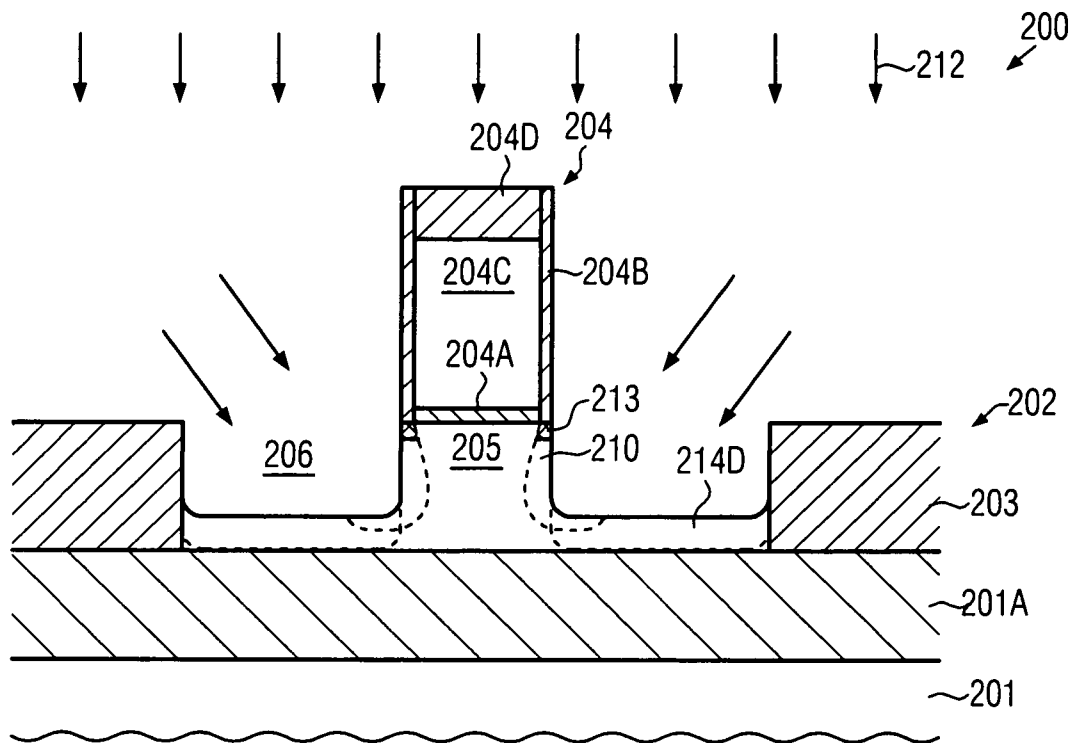


FIG. 2c

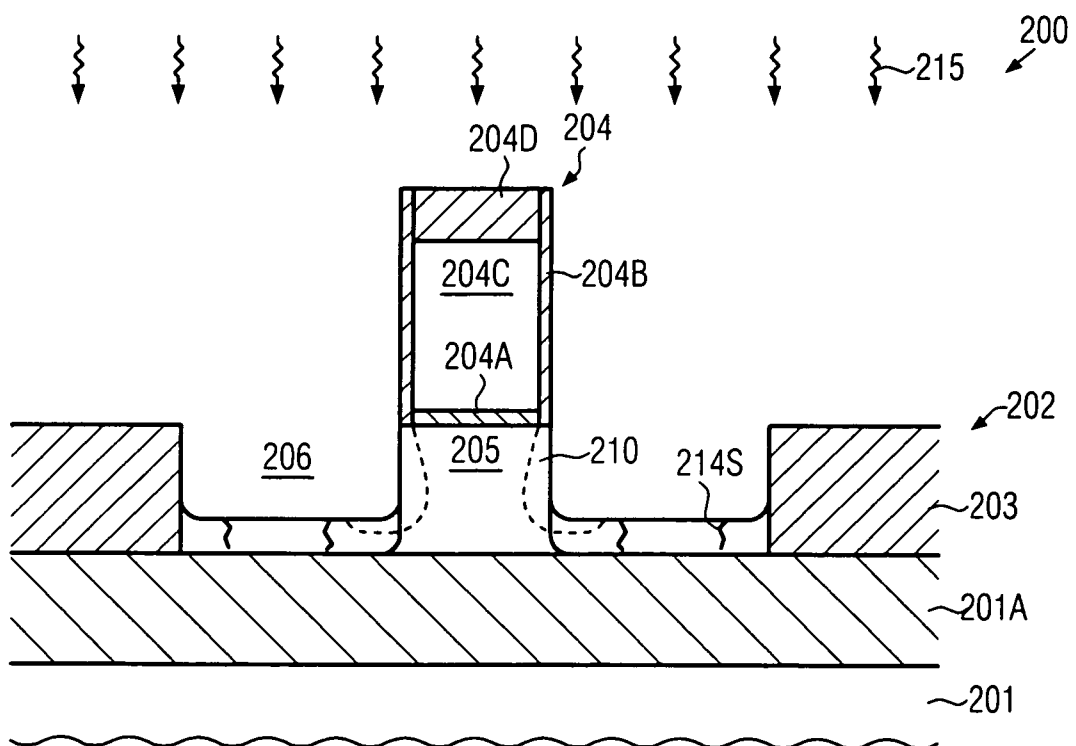


FIG. 2d

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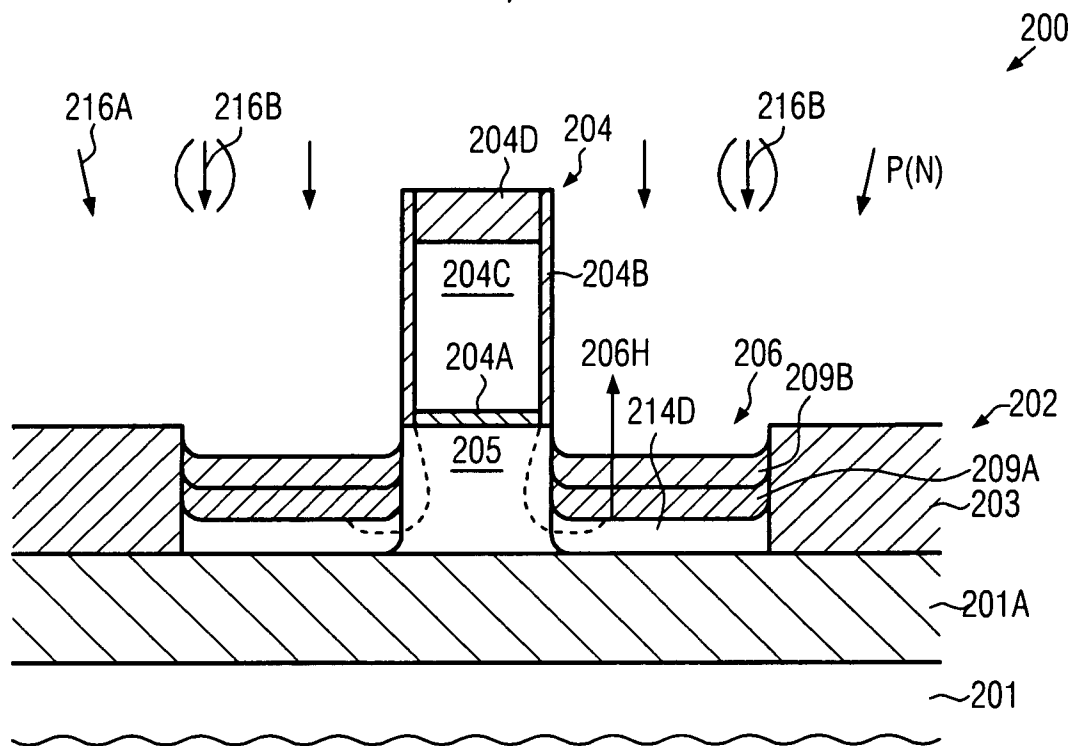


FIG. 2e

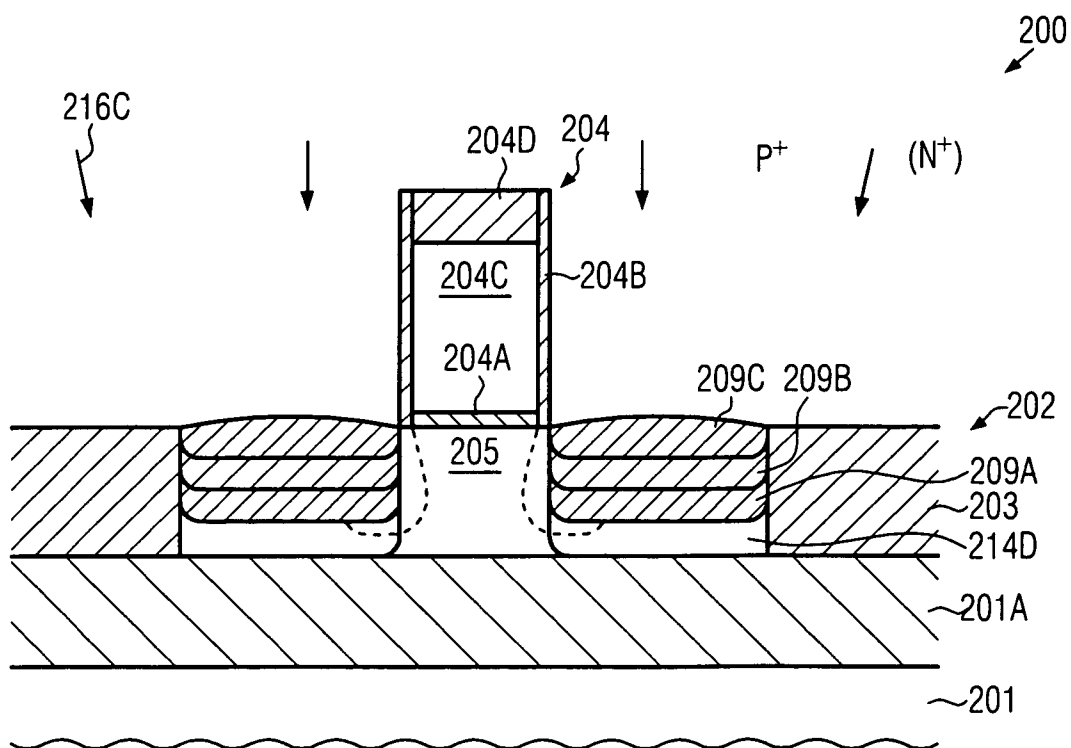


FIG. 2f

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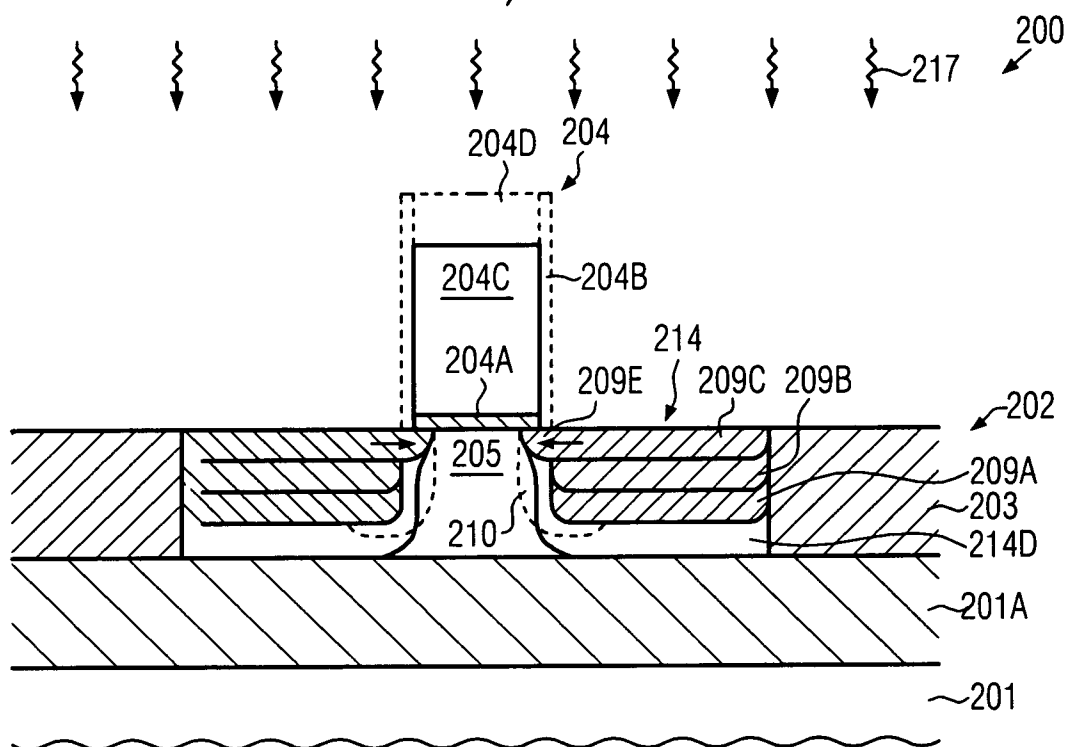


FIG. 2g

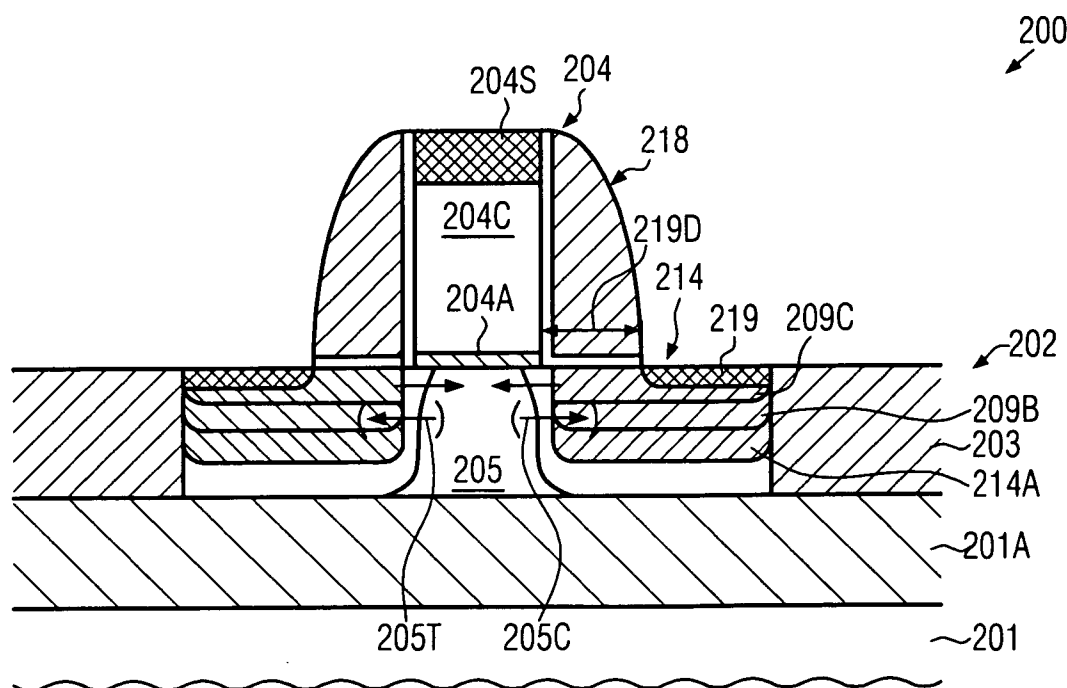


FIG. 2h

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2010/000492

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/336

ADD. H01L21/225 H01L21/265 H01L29/51 H01L29/165 H01L29/786

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

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Y	WO 2007/115585 A1 (FREESCALE SEMICONDUCTOR INC [US]; GRANT JOHN M [FR]) 18 October 2007 (2007-10-18) page 10, lines 1-2 page 7, lines 23-27	2,3,5, 12,13,16
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Further documents are listed in the continuation of Box C.



See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

11 June 2010

Date of mailing of the international search report

21/06/2010

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Authorized officer

Gélébart, Jacques

INTERNATIONAL SEARCH REPORT

International application No

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Information on patent family members

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