



(51) International Patent Classification:

G06N 10/40 (2022.01)

(21) International Application Number:

PCT/NL2024/050608

(22) International Filing Date:

04 November 2024 (04.11.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

2036190

06 November 2023 (06.11.2023) NL

(71) Applicant: TECHNISCHE UNIVERSITEIT DELFT

[NL/NL]; Stevinweg 1, 2628 CN Delft (NL).

(72) Inventor: VANDERSYPEN, Lieven Mark Koenraad; p/

a Postbus 5, 2600 AA Delft (NL).

(74) Agent: PATENTWERK B.V.; P.O. Box 1514, 5200 BN 's-

Hertogenbosch (NL).

(81) Designated States (unless otherwise indicated, for every

kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every

kind of regional protection available): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: QUBIT DEVICE

(57) Abstract: The invention related to a qubit device, comprising at least one primary gate layer comprising multiple electrodes configured for forming at least quantum dot array, in particular at least one bilinear quantum dot array; and at least one screening gate layer configured for forming at least one sensing dot; wherein at least one screening gate layer comprises at least one screening gate, wherein at least one screening gate comprises at least two outer legs which are mutually connected via at least one bridge element, wherein said at least one bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs.



WO 2025/101072 A1

Qubit device

The invention relates to a qubit device. The invention further relates to the use of a qubit device. The invention also relates to a process of manufacturing a qubit
5 device.

Electrostatically defined quantum dots hosting one or more electrons or holes form the basis for a promising realisation of a quantum computer and therefore gain broad interest. Presently, linear and bilinear quantum dot arrays are the most
10 widely studied. They also are seen as promising unit cells of a future large-scale quantum computer. Most commonly, so-called screening gates are used to define the channel or channels in which linear or bilinear quantum dot arrays are formed. The quantum dot potential can for example be induced using so-called barrier and/or plunger gates that run over the screening gate at a right angle. An example
15 of a conventional qubit device comprises for example makes use of sensing dots at the distal ends of a quantum dot array. However, such configuration has several limitations in its architecture when it comes to scaling up.

Hence, it is therefore a goal of the invention to provide an improved and scalable
20 qubit device, or at least an alternative to the known qubit devices.

The invention provides thereto a qubit device, comprising at least one primary gate layer comprising multiple electrodes configured for forming at least one quantum dot array, in particular at least one bilinear quantum dot array, and at least one
25 screening gate layer configured for forming at least one sensing dot and/or at least one quantum dot array, in particular at least one bilinear quantum dot array, wherein at least one screening gate layer comprises at least one screening gate, wherein at least one screening gate comprises at least two outer legs which are mutually connected via at least one bridge element, wherein at least one bridge
30 element comprises at least one inner leg which extends into an area defined by said at least two outer legs.

The qubit device according to the present invention benefits of the presence of the specific embodiments of at least one primary gate layer and at least one screening
35 gate layer according to the present invention. The use of at least one screening

gate layer comprising at least one screening gate comprising at least two outer legs which are mutually connected via at least one bridge element, wherein at least one bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs in combination with at least one primary gate layer
5 comprising multiple electrodes configured for forming at least one quantum dot array, in particular at least one bilinear quantum dot array, is beneficial as said screening gate layer enables the formation of sensing dots alongside at least one quantum dot array, in particular at least one bilinear quantum dot array. The at least one screening gate layer and in particular the screening gates of the screening gate
10 layer are preferably configured for forming an array of sensing dots, or a sensing dot array. At least one screening gate layer can also be configured for forming at least one quantum dot array, in particular at least one bilinear quantum dot array. The qubit device configuration according to the invention enables that sensing dots can be formed close to and thus being sensitive to the quantum dots and/or the
15 qubits held by the quantum dots of at least one quantum dot array, and in particular of the bilinear quantum dot array. A benefit of sensing dots being alongside the quantum dots, formed by for example at least one primary gate layer and/or at least one screening layer, is that it enables extending the length of the quantum dot array, and thus the number of qubits, without affecting the sensitivity of the sensing
20 dots. The qubit device according to the present invention enables qubit arrangement in a relatively simple but highly effective configuration. It is for example imaginable that at least one bilinear array of quantum dots according to the present invention can form a unit cell of a future large-scale architecture.

25 The device according to the present invention further benefits of a relatively simple and compact design which comprises at least two gate layers, in particular at least one primary electrode gate layer and at least one screening gate layer. The device therefore does not require additional gate layers to form sensing dots. The screening gate layer according to the present invention can contribute to controlled
30 positioning of the quantum dots in the quantum dot array(s) and also the controlled positioning of the sensing dots. The screening gate layer in particular has both a barrier function and a sensing function. The configuration according to the present invention thus enables that sensing dots are integrated in the screening gate layer. A sensing dot will in particular be positioned at the bridge element of a screening
35 gate, more in particular at the inner leg of a screening gate. Manufacturing of

layered electrode configuration is often a challenge. The configuration according to the present invention results in a more compact configuration of the device and in that the manufacturing of the device is relatively simple or at least less complex than configurations using typically at least three gate layers. At least one screening gate of at least one screening gate layer could also be referred to as sensing gate layer and/or barrier gate layer. It can also be said that the screening gate layer is configured to define at least one channel or channels in which a linear or bilinear quantum dot arrays can be formed.

10 Within the context of the present invention, when it is referred to a qubit device also a quantum dot device or a quantum device can be meant. At least one primary gate layer and at least one screening gate layer are in particular conductive layers. At least one primary gate layer according to the present invention comprises multiple electrodes configured for forming at least one quantum dot array, in particular at
15 least one bilinear quantum dot array. At least one primary gate layer is preferably configured such that at least one (two dimensional) quantum dot array, and preferably at least one (two dimensional) bilinear quantum dot array can be formed by applying voltages to the electrodes, or gates, of the primary gate layer. The device according to the present invention enables the creation of large bilinear
20 arrays of quantum dots with for example up to tens of quantum dots. The electrodes of the primary gate layer could also be referred to as gates. Within the context of the present invention, each quantum dot basically forms a potential well and a qubit corresponds to the spin orientation of an electron or hole confined in such potential well, or quantum dot. Alternatively, a qubit corresponds to the joint
25 state of two or more electron or hole spins confined in one or more quantum dots.

At least one sensing dot, and in particular the plurality of sensing dots, is/are configured for quantum dot and/or qubit detection. At least one sensing dot can also be formed by at least one quantum dot or potential well. At least one potential
30 well forms a region surrounding a local minimum of potential energy in the energy landscape. At least one sensing dot could also be referred to as a charge sensor and/or as charge sensing dot. The device according to the present invention is in particular configured to be operated as qubit device.

At least one screening gate layer according to the invention is configured for forming at least one sensing dot and in particular a plurality of sensing dots. It is for example imaginable that at least one screening gate is configured for forming at least one array of sensing dots and/or at least one quantum dot array, in particular at least one bilinear quantum dot array. At least one screening gate layer comprises at least one screening gate which comprises at least two outer legs which are mutually connected via at least one bridge element. Said at least two outer legs, and/or the combination of said at least two outer legs and part of at least one bridge element enclose an area, or a region. At least one bridge element comprises at least one inner leg which extends into the area defined by the at least two outer legs and optionally also the bridge element. Alternatively, it can also be said that at least one bridge element comprises at least one inner leg which extends in the same direction as at least one outer leg, and preferably as at least two outer legs. In this configuration, at least part of at least one inner leg is positioned substantially between the at least two outer legs. At least one inner leg can be at least partially enclosed by the at least two outer legs and at least part of at least one bridge element. At least one bridge element according to the present invention could have possibly at least one substantially straight side. It is also imaginable that at least one bridge element has at least one angular, angled and/or curved side wall. At least one screening gate layer according to the present invention is in particular a patterned screening gate layer. The screening gate layer according to the present invention basically does not comprise homogeneous, non-patterned screening gates but screening gates which define a predetermined pattern and/or configuration/spatial orientation. The patterned screening gates according to the present invention benefit of more controllability in sensing dot positioning. The outer legs of the screening gate are in particular configured for electrical contact. A current or voltage can be applied to at least one screening gate preferably via at least one outer leg and/or at least one screening gate can be connected to a power supply, for example a current or voltage source.

Consequently, current can flow through the quantum dot(s) and/or the electron reservoir(s) which are formed below the screening gate layer and/or primary gate layer through a semiconductor region in which electrons or holes move primarily in a plane. Such plane can be, for instance a semiconductor quantum well with other semiconductor layers below and above, or it can be formed at a semiconductor-semiconductor heterointerface. Alternatively, it could be formed in the

semiconductor right against a dielectric layer. At least one sensing dot can possibly be capacitively coupled to at least one of the quantum dots of the quantum dot array. A charge transition in the quantum dot array may be detected by the sensing dot, for example as a change in the conductance of the sensing dot.

5

It is preferred that part of the electrodes of at least one primary gate layer are positioned substantially parallel to each other. In this way the electrodes can form at least one quantum dot array, in particular at least one bilinear quantum dot array, in a controlled manner. Preferably, part of the electrodes of at least one primary gate layer are substantially elongated. It is preferred that all electrodes of at least one primary gate which are configured for forming at least one quantum dot array, and preferably at least one bilinear quantum dot array, are substantially elongated. It is for example imaginable that at least one primary gate layer comprises at least two adjacent arrays of electrodes. Each array could comprise multiple electrodes.

15 The dimensions, for example the width and/or length of the electrodes can be determined based on the desired dimensions of the quantum dots. In a possible embodiment, at least one primary gate layer comprises at least two arrays of electrodes which substantially oppose each other and/or are substantially parallel to each other. At least one primary gate layer could for example comprise at least two adjacent and/or parallel arrays of electrodes. It is imaginable that at least one array of electrodes, or each array of electrodes, comprises a first type of electrodes and a second type of electrodes, wherein at least part of the first type electrodes and the second type of electrodes are alternately positioned. It is for example possible that a first type of electrodes has a larger surface area than a second type of electrodes. It is also imaginable that one of the types of electrodes is configured for quantum dot formation and a further type of electrode provides a barrier function.

20
25

Each quantum dot array basically comprises a plurality of quantum dots, or thus potential wells. The configuration of the gates according to the present invention are in particular configured such that quantum dots are typically formed at the distal ends of at least part of the electrodes of the primary gate layer. The electrodes of at least one primary gate layer are preferably positioned such that a square, rectangular, triangular, trapezoid and/or parallelogrammatic topology of quantum dots will be obtained. In a preferred embodiment, the electrodes of at least one

30
35

primary gate layer are positioned such that a substantially square and/or rectangular topology of quantum dots will be obtained. This will result in a consistent and repeatable configuration of quantum dots and/or qubits. It is also imaginable that the electrodes of at least one primary gate layer are positioned
5 such that a triangular topology of quantum dots will be obtained. This might be beneficial from sensing point of view. It is beneficial if the electrodes of at least one primary gate layer are positioned such that a repeated pattern of quantum dots and/or qubits can be obtained. A repeated pattern can also be beneficial for the detection process and/or the scalability of the architecture of the device. The
10 distance between at least two quantum dots in an array is for example in the range of 10 to 500 nm, in particular 25 to 250 nm, more in particular 50 to 200 nm, for example in the range of 75 to 150 nm or in the range of 100 to 125 nm. The distance between at least two adjacent quantum dots can for example be smaller than or substantially equal to the distance between a quantum dot and an adjacent
15 sensing dot. It is also imaginable that the distance between a quantum dot and a sensing dot is smaller than the distance between at least two adjacent sensing dots. At least one sensing dot can be configured to sense multiple quantum dots. It is for example imaginable that the distance between at least two adjacent quantum dots formed by a primary gate layer is smaller than or substantially equal to the
20 distance between a quantum dot formed by said primary gate layer and an adjacent sensing dot formed by a screening gate layer. It is also imaginable that the distance between a quantum dot of a primary gate layer and a sensing dot of a screening gate layer is smaller than the distance between at least two adjacent sensing dots. The distance referred to is the distance determined from center to center.

25

At least one screening gate of at least one screening gate layer can have several possible configurations. In a beneficial embodiment, at least one inner leg of at least one screening gate is shorter than at least one outer leg of said at least one screening gate, preferably shorter than the at least two outer legs of said at least
30 one screening gate and more preferably shorter than each outer leg of said at least one screening gate. In this embodiment, at least one inner leg basically forms a defined area for at least one sensing dot and/or quantum dot to be positioned or located. It is for example imaginable that at least one outer leg, and preferably each outer leg, is at least 1.5 times longer than at least one inner leg. It is also
35 conceivable that at least one outer leg, and preferably each outer leg, is at least 2

times, preferably at least 2.5 times and more preferably at least 3 times longer than at least one inner leg. It is also conceivable that the area defined by at least one outer leg, and preferably each outer leg, is larger than the area defined by at least one inner leg, for example at least 2 times larger, preferably at least 3 times larger, more preferably at least 4 times larger.

In a further preferred embodiment, at least one inner leg of at least one screening gate is interrupted. It is for example conceivable that at least one inner leg comprises at least two inner leg parts which are positioned at a distance from each other. It is possible that at least one inner leg comprises at least one inner leg part which is connected to at least one bridge element and at least one additional inner leg part which is positioned at a distance from said at least one inner leg part. At least one inner leg of at least one screening gate can for example define a combination of a peninsula (integrally) connected to at least one bridge element and at least one island positioned at a distance from said peninsula. In case at least one screening gate comprises at least one interrupted inner leg, it is beneficial if the inner leg parts are positioned within an area defined by the at least two outer legs. The use of a screening gate layer comprising at least one interrupted inner leg can positively contribute to the positioning and sensitivity of at least one sensing dot, and thus to a better sensing ability. The configuration could also positively contribute to the positioning of at least one quantum dot in the screening gate layer. At least one inner leg part which is connected to at least one bridge part can be configured to enable controlled formation of at least one sensing dot and at least one additional inner leg part can be configured for adjustment of the sensing position. At least one additional inner leg part can be configured as plunger gate or sensing dot plunger gate. It is also imaginable that at least one additional inner leg part is referred to as plunger gate or sensing dot plunger gate. At least one plunger gate can be configured to tune the electrostatic potential of at least one quantum dot or sensing dot relative to its corresponding electron reservoir.

In a beneficial embodiment, at least one screening gate of at least one screening gate layer is mirror symmetrical. This could positively contribute to the controllability of the sensing dot and/or quantum dot formation. It is for example imaginable that at least one screening gate is mirror symmetrical over an axis which extends along a central part of at least one inner leg. However, in yet a further possible

embodiment, at least one screening gate of at least one screening gate layer can be a-symmetrical.

5 It is beneficial if the width of at least one bridge element of at least one screening gate is smaller than the width of at least one outer leg and/or the width of at least one inner leg of said at least one screening gate. It is possible that the smallest width of at least one bridge element of at least one screening gate is smaller than the smallest width of at least one outer leg and/or the smallest width of at least one inner leg of said at least one screening gate. However, it is also possible that the
10 smallest width of at least one bridge element of at least one screening gate is smaller than the average width of at least one outer leg and/or the average width of at least one inner leg of said at least one screening gate. The width of at least one bridge element, and preferably of each bridge element is relatively small. This could positively contribute to the controllability of the sensing dot and/or quantum dot
15 positioning. The configuration of at least one screening gate could also be described as comprising at least two outer legs and at least one inner leg, wherein each outer leg is connected to the inner leg via at least one bridge element part. In such configuration, the bridge element parts preferably defined a smaller surface than the outer legs and/or inner leg.

20

It is possible that at least part of at least one screening gate defines an M-shape and/or a W-shape. It is also possible that at least one screening gate as such defines an M-shape and/or a W-shape. The two outer legs of at least one screening gate thereby define the outer legs of the letter and at least one bridge element and the
25 inner leg are configured such that the screening gate defines the middle part of the letter. It is conceivable that the inner leg is an interrupted inner leg comprising preferably two inner leg parts. In a possible embodiment, at least two outer legs of at least one screening gate are substantially parallel to each other. However, it is also imaginable that at least two outer legs of at least one screening gate diverge
30 from each other. Preferably at least two outer legs of at least one screening gate are substantially elongated and/or substantially straight. The outer legs are preferably configured such that they are readily connectable to at least one power supply.

In a beneficial embodiment, at least one screening gate layer comprises multiple screening gates, wherein at least two screening gates, and preferably multiple screening gates are substantially parallel to each other. It is for example imaginable that at least one screening gate layer comprises at least one array of screening gates. Multiple screening gates in such array of screening gates can be oriented adjacently. It is for example imaginable that at least one array comprises a repeated pattern of substantially identical screening gates. It is also possible that at least part of the at least one array of screening gates is formed by a repeated pattern of at least two screening gates which are positioned substantially parallel.

Possibly, at least part of the at least one array of screening gates is formed by a repeated pattern of multiple screening gates which are positioned substantially parallel, wherein at least one distal screening gate, and preferably each screening gate is similar to at least one centrally positioned screening gate. Within the context of the present invention, a repeated pattern can be defined as a sequence of elements and in particular screening gates arranged in a consistent and recurring way over the at least one array. The use of an array of screening gates can further contribute to the scalability of the device. Possibly, at least part of the at least one array of screening gates is formed by a repeated pattern of at least two screening gates which are positioned substantially parallel preferably such that the at least one screening gate layer enables the formation of at least one sensing dot array alongside at least one quantum dot array formed by the at least one primary gate layer.

It is also imaginable that the device according to the present invention, and in particular the screening gate layer comprises at least one plunger gate and preferably multiple plunger gates. It is imaginable that at least plunger gate is at least partially enclosed by at least one screening gate. It is for example also imaginable that at least one plunger gate is formed by at least one additional inner leg part of at least one screening gate. The screening gate layer can for example comprise at least one array of plunger gates, wherein multiple plunger gates are oriented adjacently. It is also imaginable that screening gates and plunger gates are applied in an alternating configuration. Within the context of the present invention, a plunger gate could also be referred to as sensing dot plunger gate.

In a further beneficial embodiment, at least one screening gate layer comprises at least two arrays of screening gates, wherein each array of screening gates comprises multiple screening gates. This is in particular beneficial for quantum dot and/or qubit detection in at least one bilinear quantum dot array. The at least two
5 arrays of screening gates can be positioned substantially parallel to each other. Preferably, each array of screening gates comprises multiple screening gates comprising at least two outer legs which are mutually connected via at least one bridge element, wherein said at least one bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs. In yet a
10 further preferred embodiment, at least the outer legs of the screening gates of a first screening gate array extend away from the outer legs of the screening gates of a second screening gate array. It can also be defined that the bridge elements of the screening gates of a first array of screening gates faces the bridge elements of the screening gates of a second array screening gates. The screening gates of a
15 first array of screening gates can be positioned in line with the screening gates of a second array of screening gates. Alternatively, it is conceivable that the screening gates of a first array of screening gates are positioned off set with the screening gates of a second array of screening gates. It is for example conceivable that the screening gates of a first array of screening gates and the screening gates of a
20 second array of screening gates are positioned in a repeated square and/or triangular configuration. The at least two arrays of screening gates preferably substantially oppose each other such that the legs of different arrays of screening gates extend away from each other.

25 In yet a further possible embodiment of the device according to the present invention, at least one screening gate layer comprises at least one barrier gate. At least one barrier gate is preferably configured to provide a barrier function for at least one quantum dot and/or at least one sensing dot and preferably for the arrays of quantum dots and/or sensing dots. It is also possible that at least one barrier
30 gate is configured to control tunnel coupling between at least one sensing dot and its corresponding electron reservoir. At least one barrier gate can for example be configured to form a tunnel barrier between the quantum dots and/or qubits and the sensing dots. It is beneficial to integrate at least one barrier gate, and optionally multiple barrier gates and/or multiple plunger gates, and at least one screening
35 gate, and preferably multiple screening gates in the same layer, in particular the

screening gate layer according to the present invention. This results in a more compact configuration of the device due to the reduced number of required gate layers and thus in that the manufacturing of the device is simplified and less prone to aligning deficiencies. The device, and in particular the screening gate layer, could also comprise multiple barrier gates. In a beneficial embodiment at least one barrier gate is substantially elongated and extends adjacent and/or parallel to at least one array of screening gates. It is also conceivable that at least one barrier gate is substantially elongated and extends between a first array of screening gates and a second array of screening gates. In such embodiment, the barrier gates can contribute to the controlled formation of the bilinear quantum dot array. Preferably, at least one first barrier gate is positioned between a first array of sensing dots and a first array of quantum dots and/or at least one second barrier gate is positioned between a second array of sensing dots and a second array of quantum dots. It is further possible that at least part of at least one screening gate layer is mirror symmetrical.

At least one barrier gate preferably extends at least over a distance defined by at least two screening gates. More preferably, at least one barrier gate extends at least over a distance defined by at least one array of screening gates. It is also conceivable that at least one barrier gate extends over a distance defined by at least one array of electrodes of at least one primary gate layer. In said embodiment, the at least one barrier can effectively contribute to shaping of the potential landscape.

In a beneficial embodiment, at least one screening gate layer comprises at least two arrays of screening gates which substantially enclose at least two barrier gates. At least two barrier gates can for example extend between a first array of screening gates and a second array of screening gates, wherein the smallest distance between at least one barrier gate and an adjacent screening gate is smaller than the distance between said at least two barrier gates. The bilinear array of quantum dots can subsequently be effectively formed between said at least two barrier gates. The distance between a first barrier gate and a second barrier gate is thus preferably larger than distance between each barrier gate and its adjacent screening gate. It can also be said that at least one barrier gate is positioned closer

to at least one screening gate than to a distal end of at least one electrode of at least one primary gate layer.

Typically, at least one screening gate layer substantially overlaps with at least one
5 primary gate layer. It is for example imaginable that at least one screening gate layer is applied upon at least part of at least one primary gate layer. Alternatively, at least one primary gate layer can be applied upon at least part of at least one screening gate layer. At least part of the electrodes of at least one primary gate layer preferably overlap with at least part of the screening gates and/or barrier
10 gates, if applied, of at least one screening gate layer. Such embodiment can positively contribute to further control of the quantum dot positioning.

Optionally, the device according to the present invention could comprise at least one control layer configured for controlling and/or verifying the coupling of and/or
15 between at least part of the electrodes of at least one primary gate layer. At least one control layer can at least partially overlap with at least one primary gate layer and/or at least one screening gate layer. At least one control layer can for example comprise a plurality of control electrodes, for example elongates electrodes which extend in the same direction as the electrodes of the primary gate layer. At least
20 one control layer can for example comprise at least one array of control electrodes wherein at least part of the control electrodes overlap with at least part of the electrodes of at least one primary gate layer and/or with at least part of the screening gates and/or with at least part of the barrier gates of at least one screening gate layer, if applied.

25 The device according to the present invention preferably comprises at least one substrate, wherein said substrate comprises at least one primary gate layer and at least one screening gate layer. At least one substrate can for example be a semiconductor substrate. At least one substrate could also be referred to as a
30 ground plane. Any conventional substrate for qubit devices could be applied, for example a silicon-based substrate such as but not limited to a silicon-silicongermanium substrate, a germanium-silicongermanium or a silicon dioxide on silicon substrate. At least part of the gates and/or electrodes according to the present invention can for example be made of any suitable metallic material, such
35 as but not limited to aluminium, gold, copper, titanium nitride, palladium, tungsten,

niobium, and/or polysilicon. It is imaginable that the gates and/or electrodes of at least one screening gate layer are made of a different material than the gates and/or electrodes of at least one primary gate layer.

5 In an alternative embodiment, the device could comprise multiple primary gate layers and/or multiple screening gate layers. At least one primary gate layer and at least one screening gate layer are in particular conductive layers. It is also imaginable that the device comprises one or more insulating layers. At least one insulating layer can for example be an electrically insulating layer and can be
10 configured to insulate gate layers, electrodes and/or gates from another. It is for example possible that the device according to the invention comprises at least one electrically insulating layer which is located between at least one primary gate layer and at least one screening gate layer. In case multiple gate layers are applied, it is preferred that at least one electrically insulating layer is present between two
15 adjacent gate layers. The use of at least one electrically insulating layer can prevent short circuits. At least one electrically insulating layer could also be present between at least one substrate and at least one screening gate layer. In yet another configuration, at least one electrically insulating layer could be present between at least one substrate and at least one primary gate layer. It is for example possible
20 that at least one electrically insulating layer comprises at least one dielectric material and/or that at least one electrically insulating layer is at least partially made of at least one dielectric material. It is for example possible that at least one electrically insulating layer comprises at least one oxide and/or at least one nitride, such as but not limited to aluminium (III) oxide (Al_2O_3), silicon dioxide (SiO_2) and/or
25 hafnium (IV) oxide (HfO_2). It is also imaginable that multiple devices according to the present invention are combined in a large-scale architecture. Any of the described configurations of embodiments could be combined for such embodiment.

In a further possible embodiment, it is conceivable that at least one functional
30 component, and preferably multiple functional components are provided upon at least one screening gate layer and/or at least one primary gate layer. At least one functional component can for example be configured to rotate at least one qubit in particular in a controlled manner. It is for example imaginable that at least one functional component comprises at least one magnet, in particular at least one
35 micro magnet. It is for example imaginable that at least one magnet, or micro

magnet, is at least partially made of at least one magnetic material such as but not limited to cobalt. It is also imaginable that at least one functional element comprises at least one stripline and/or that at least one functional element is formed by at least one stripline. At least one stripline can be configured for controlled distribution of current and/or relatively large current flow.

The invention also relates to the use of a device according to any of the previous claims.

The invention further relates to a process of manufacturing at least one qubit device, in particular according to the present invention, comprising the steps of:

- providing at least one substrate;
- applying at least one screening gate layer to said substrate, wherein the at least one screening gate layer is configured for forming at least one sensing dot and/or at least one quantum dot array, in particular at least one bilinear quantum dot array;
- applying at least one primary gate layer comprising multiple electrodes to said substrate, wherein the at least one primary gate layer is configured for forming at least one bilinear quantum dot array, in particular at least one bilinear quantum dot array;

wherein at least one screening gate layer comprises at least one screening gate, wherein at least one screening gate comprises at least two outer legs which are mutually connected via at least one bridge element, wherein said bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs.

The steps of the process are in particular subsequent steps. The process enables the provision of a device according to the present invention. Any of the embodiments described for the qubit device according to the present invention, in particular for the screening gate layer and the primary gate layer apply to the process according to the present invention. As indicated above, the method benefits of a relatively compact layer configuration which is less complex to manufacture than configurations using typically at least three gate layers. It is imaginable that the process according to the present invention comprises the step of applying at least one electrically insulating layer to the substrate. At least one electrically insulating layer which is preferably located between at least one primary

gate layer and at least one screening gate layer. Depending on the layer configuration of the device, it is possible that at least one electrically insulating layer is applied after at least one screening gate layer is applied and prior to at least one primary gate layer is applied, or vice versa.

5

The invention will be further elucidated based on the following non-limitative clauses.

1. A qubit device, comprising:
 - 10 – at least one primary gate layer comprising multiple electrodes configured for forming at least one quantum dot array, in particular at least one bilinear quantum dot array; and
 - at least one screening gate layer configured for forming at least one sensing dot and/or at least one quantum dot array, in particular at least one bilinear
 - 15 quantum dot array;

wherein at least one screening gate layer comprises at least one screening gate, wherein at least one screening gate comprises at least two outer legs which are mutually connected via at least one bridge element, wherein said at least one bridge element comprises at least one inner leg which extends into an area defined

20 by said at least two outer legs.

2. Device according to clause 1, wherein part of the electrodes of at least one primary gate layer are positioned substantially parallel to each other and/or wherein part of the electrodes of at least one primary gate layer are substantially elongated.

25

3. Device according to any of the previous clauses, wherein at least one primary gate layer comprises at least two parallel arrays of electrodes.

4. Device according to any of the previous clauses, wherein the electrodes of
- 30 at least one primary gate layer are positioned such that a square, rectangular, triangular, trapezoid and/or parallelogrammatical topology of quantum dots will be obtained.

5. Device according to any of the previous clauses, wherein at least one inner
- 35 leg of at least one screening gate is shorter than at least one outer leg of said at

least one screening gate, and preferably shorter than each outer leg of said at least one screening gate.

5 6. Device according to any of the previous clauses, wherein at least one inner leg of at least one screening gate is interrupted.

10 7. Device according to clause 6, wherein at least one inner leg comprises at least one inner leg part which is connected to at least one bridge element and at least one additional inner leg part which is positioned at a distance from said at least one inner leg part.

8. Device according to any of the previous clauses, wherein at least one screening gate is mirror symmetrical.

15 9. Device according to any of the previous clauses, wherein the width of at least one bridge element of at least one screening gate is smaller than the width of at least one outer leg and/or of at least one inner leg of said at least one screening gate.

20 10. Device according to any of the previous clauses, wherein at least part of at least one screening gate defines an M-shape.

25 11. Device according to any of the previous clauses, wherein at least two outer legs of at least one screening gate are substantially parallel to each other.

12. Device according to any of the previous clauses, wherein at least two outer legs of at least one screening gate diverge from each other.

30 13. Device according to any of the previous clauses, wherein at least one screening gate layer comprises multiple screening gates, wherein at least two screening gates, and preferably multiple screening gates are substantially parallel to each other.

14. Device according to any of the previous clauses, wherein at least one screening gate layer comprises at least two arrays of screening gates, wherein each array of screening gates comprises multiple screening gates.

5 15. Device according to clause 14, wherein each array of screening gates comprises multiple screening gates comprising at least two outer legs which are mutually connected via at least one bridge element, wherein said at least one bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs, and wherein at least the outer legs of the screening
10 gates of a first screening gate array extend away from the outer legs of the screening gates of a second screening gate array.

16. Device according to any of the previous clauses, wherein at least one screening gate layer comprises at least one barrier gate.
15

17. Device according to clause 14 or 15 and clause 16, wherein at least one barrier gate is substantially elongated and extends between a first array of screening gates and a second array of screening gates.

20 18. Device according to clause 17, wherein at least one barrier gate extends at least over a distance defined by at least one array of screening gates.

19. Device according to clause 17 or clause 18, comprising at least two barrier gates which extend between a first array of screening gates and a second array of
25 screening gates and wherein the smallest distance between at least one barrier gate and an adjacent screening gate is smaller than the distance between said at least two barrier gates.

20. Device according to any of the previous clauses, wherein at least one
30 screening gate layer substantially overlaps with at least one primary gate layer.

21. Device according to any of the previous clauses, wherein at least part of the electrodes of at least one primary gate layer overlap with at least part of the screening gates and/or barrier gates of at least one screening gate layer.

35

22. Device according to any of the previous clauses, comprising at least one electrically insulating layer, wherein at least one electrically insulating layer which is located between at least one primary gate layer and at least one screening gate layer.

5

23. Device according to any of the previous clauses, comprising at least one functional component, and preferably multiple functional components, provided upon at least one screening gate layer and/or at least one primary gate layer.

10 24. Device according to any of the previous clauses, comprising at least one control layer configured for controlling the coupling of at least part of the electrodes of at least one primary gate layer.

15 25. Device according to clause 24, wherein at least one control layer comprises at least one array of control electrodes wherein at least part of the control electrodes overlap with at least part of the electrodes of at least one primary gate layer.

20 26. Device according to any of the previous clauses, comprising at least one substrate, said substrate comprising at least one primary gate layer and at least one screening gate layer.

27. Use of a device according to any of the previous clauses.

25 28. Process of manufacturing at least one qubit device, in particular according to any of clauses 1-26, comprising the steps of:

- providing at least one substrate;
 - applying at least one screening gate layer to said substrate, wherein said at least one screening gate is configured for forming at least one sensing dot and/or at least one quantum dot array, in particular at least one bilinear quantum dot array is formed; and
 - applying at least one primary gate layer comprising multiple electrodes to said substrate, wherein said at least one primary gate layer is configured for forming at least one quantum dot array, in particular at least one bilinear quantum dot array;
- 30
- 35

wherein at least one screening gate layer comprises at least one screening gate, wherein at least one screening gate comprises at least two outer legs which are mutually connected via at least one bridge element, wherein said bridge element comprises at least one inner leg which extends into an area defined by said at least
5 two outer legs.

29. Process according to clause 28, wherein the steps are subsequent steps.

30. Process according to clause 28 or clause 29, comprising the step of
10 applying at least one electrically insulating layer to said substrate after at least one screening gate layer is applied and prior to at least one primary gate layer is applied.

The invention will be further elucidated by means of non-limiting exemplary
15 embodiments illustrated in the following figures, in which:

- figure 1 shows a qubit device according to the prior art;
- figure 2 shows a first possible embodiment of a device according to the present invention;
- figure 3 shows a second possible embodiment a device according to the
20 present invention; and
- figures 4a-4d show possible embodiments of screening gate configurations according to the present invention.

Within these figures, similar reference numbers correspond to similar or equivalent elements or features.

25

Figure 1 shows a schematic representation of a qubit device 1 according to the prior art. The figure shows a top view of the device 1. The qubit device 1 comprises a screening gate layer comprising a plurality of screening gates 2 and a primary gate layer comprising a plurality of electrodes 3 which could also be referred to as
30 gates 3. At least one of the screening gates can act as a barrier gate. The gates 3 are configured to shape the potential landscape in the channel and to form quantum dots Q and sensing dots S. The figure shows that two sensing dots S and four quantum dots Q, or qubits, are formed. The qubits Q are present in a linear array. The sensing dots S are positioned adjacent to part of the quantum dots Q. A
35 difficulty of the shown configuration is that scaling up the configuration or adjusting

the configuration such that bilinear arrays of quantum dots can be formed is a challenge, wherefore the shown device experiences several limitations in practice.

Figure 2 shows a first possible embodiment of a qubit device 10 according to the present invention. The device shows a schematic representation shown in top view. The qubit device 10 as shown comprises two overlapping gate layers, in particular a primary gate layer PL and a screening gate layer SL, as indicated in the legenda, which at least partially overlap with each other. The primary gate layer comprises multiple electrodes 11 configured for forming a bilinear quantum dot array formed by multiple quantum dots Q. The bilinear array of quantum dots Q is in particular formed in a channel defined by the screening gate layer. The screening gate layer is further configured for forming sensing dots S and/or quantum dots. For clarity reasons, only sensing dots are indicated in the figures. The screening gate layer comprises multiple screening gates 12. In the shown embodiment, as indicated in the detailed part, each screening gate 12 comprises two outer legs 12a which are mutually connected via a bridge element 12b. The bridge element 12b comprises an inner leg 12c which extends into an area defined by the two outer legs 12a. In the shown embodiment, the inner leg 12c is interrupted and comprises an additional inner leg part 12d. The additional inner leg part 12d can also be referred to as plunger gate 12d. A possible current direction is indicated with an arrow. The electrodes 11 of the primary gate layer PL are substantially elongated and are positioned substantially parallel to each other. The width W_B of at least one bridge element 12b, and in particular the smallest width W_B defined by at least one bridge element is smaller than the smallest and/or average width W_O of at least one outer leg 12a and the smallest and/or average width W_I of at least one inner leg 12c of the screening gate 12. Further, the length L_I at least one inner leg 12a, and in particular the length L_I , L_A of each inner leg part 12a, 12d is shorter than the length L_O of at least one outer leg of the screening gate 12. In the shown embodiment, the electrodes 11 are divided over two parallel arrays of electrodes 11. As is indicated in the figure, the electrodes 11 are positioned such that a triangular topology of quantum dots Q is obtained. Each sensing dot S is configured for interaction with multiple quantum dots Q. The screening gates 12 are also positioned in off set with respect to each other, such that also a triangular topology of sensing dots S is obtained. The outer legs 12a of each screening gate 12 are substantially parallel to each other and also to the outer legs 12a of an adjacent screening gate. The

embodiment as shown, further comprises two barrier gates 13 which form part of the screening gate layer SL. Each barrier gate 13 is substantially elongated and extends between a first array of screening gates 12 and a second array of screening gates 12. The barrier gates 13 extends over a distance defined by the arrays of screening gates 12. It can be seen that the distance between a barrier gate 13 and an adjacent screening gate 12 is smaller than the distance between the two barrier gates 13.

Figure 3 shows a second possible embodiment of a qubit device 20 according to the present invention. The figure shows a schematic representation of the device 20 in top view. In line with the embodiment as shown in figure 2, the device 20 comprises a primary gate layer PL and a screening gate layer SL, as indicated in the legenda, which at least partially overlap with each other. The primary gate layer comprises multiple electrodes 21 configured for forming a bilinear quantum dot array formed by multiple quantum dots Q. The screening gate layer is configured for forming sensing dots S and/or quantum dots. The screening gate layer comprises thereto multiple screening gates 22 and barrier gates 23. In the shown embodiment, the screening gates 22 have the same shape and dimensions as the screening gates as shown in figure 2. The topology is slightly different than seen in figure 2. The electrodes 21 of the primary gate layer PL are positioned such that a square topology of quantum dots Q is obtained, as is indicated in the figure. Further, the screening gates 22 as such are mirror symmetrical. And the screening layer SL as such is mirror symmetrical too. Additionally, the embodiment as shown comprises an additional control layer CL configured for controlling the coupling of at least part of the electrodes 21 of the primary gate layer PL. The control layer CL comprises an array of control electrodes 24 wherein the control electrodes 24 overlap with the electrodes 21 of the primary gate layer PL. The layers according to the present invention could be provided upon a semiconductor substrate 25.

Figures 4a, 4b, 4c and 4d show alternative embodiments of screening gates 32, 42, 52 according to the present invention. The figures shown non-limitative embodiments of screening gates 32, 42, 52, 62 which could be applied in a screening gate layer, and this a device according to the present invention. Figure 4a shows a screening gate 32 wherein the two outer legs 32a diverge from each other. The inner leg 32c is shorter than the outer legs 32a. The screening gate 32

could optionally comprise an inner leg part 32d. The inner leg 32c and the outer legs 32a are mutually connected via bridge element parts 23b. Figure 4a shows a pair of screening gates 42. Each screening gate 42 comprises a straight outer leg 42a and a diverging outer leg 42a. The bridge elements 42b comprise an inner leg 42c, 42b which is interrupted and formed by an inner leg part 42c and an additional inner leg part 42d or plunger gate 42d. Figure 4c shows yet a further possible embodiment of a screening gate 52 according to the present invention. The screening gate 52 comprises two outer legs 52a which are substantially parallel to each other and which define an area 56. The outer legs 52a are mutually connected via a bridge element 52b. The bridge element 52b comprises an inner leg 52c. Additionally an additional inner leg part 52d or plunger gate 52d is received within the area 56 defined by the outer legs 52a. The bridge element 52b of the shown embodiment had an angular configuration. Figure 4d shows a further possible embodiment of a screening gate 62 according to the present invention. The screening gate 62 comprises two outer legs 62a which are substantially parallel to each other and which define an area 66. The outer legs 62a are mutually connected via a bridge element 62b. The bridge element 62b comprises an inner leg 62c which at least partially extends into the area 66 defined by the outer legs 62a. The bridge element 62b of the shown embodiment has a non uniform side wall which opposes the inner leg 62c. Where the bridge elements 32b, 42b of the screening gates 32, 42 of figures 4a and 4b have a substantially straight side wall, the bridge elements 52b, 62b of the screening gates of figures 4c and 4b each have an angled side wall.

It will be clear that the invention is not limited to the exemplary embodiments which are illustrated and described here, but that countless variants are possible within the framework of the attached claims, which will be obvious to the person skilled in the art. In this case, it is conceivable for different inventive concepts and/or technical measures of the above-described variant embodiments to be completely or partly combined without departing from the inventive idea described in the attached claims.

The verb 'comprise' and its conjugations as used in this patent document are understood to mean not only 'comprise', but to also include the expressions 'contain', 'substantially contain', 'formed by' and conjugations thereof.

Claims

1. A qubit device, comprising:
 - at least one primary gate layer comprising multiple electrodes configured for forming at least one quantum dot array, in particular at least one bilinear quantum dot array; and
 - at least one screening gate layer configured for forming at least one sensing dot and in particular at least one sensing dot array;wherein the at least one screening gate layer comprises at least one array of screening gates,
 - wherein each screening gate comprises at least two outer legs which are mutually connected via at least one bridge element, wherein said at least one bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs and wherein the at least one inner leg of at least one screening gate is shorter than the at least two outer legs of said at least one screening gate, and
 - wherein at least part of the at least one array of screening gates is formed by a repeated pattern of at least two screening gates which are positioned substantially parallel such that the at least one screening gate layer enables the formation of at least one sensing dot array alongside at least one quantum dot array formed by the at least one primary gate layer.
2. Device according to claim 1, wherein part of the electrodes of at least one primary gate layer are positioned substantially parallel to each other and/or wherein part of the electrodes of at least one primary gate layer are substantially elongated.
3. Device according to any of the previous claims, wherein at least one primary gate layer comprises at least two parallel arrays of electrodes.
4. Device according to any of the previous claims, wherein the electrodes of at least one primary gate layer are positioned such that a square, rectangular, triangular, trapezoid and/or parallelogrammatical topology of quantum dots will be obtained.

5. Device according to any of the previous claims, wherein at least one outer leg is at least 1.5 times longer than at least one inner leg of at least one screening gate.
- 5 6. Device according to any of the previous claims, wherein at least one inner leg of at least one screening gate is interrupted.
7. Device according to claim 6, wherein at least one inner leg comprises at least one inner leg part which is connected to at least one bridge element and at
10 least one additional inner leg part which is positioned at a distance from said at least one inner leg part.
8. Device according to any of the previous claims, wherein at least one screening gate is mirror symmetrical.
- 15 9. Device according to any of the previous claims, wherein the width of at least one bridge element of at least one screening gate is smaller than the width of at least one outer leg and/or of at least one inner leg of said at least one screening gate.
- 20 10. Device according to any of the previous claims, wherein at least part of at least one screening gate defines an M-shape.
11. Device according to any of the previous claims, wherein at least two outer
25 legs of at least one screening gate are substantially parallel to each other.
12. Device according to any of the previous claims, wherein at least two outer legs of at least one screening gate diverge from each other.
- 30 13. Device according to any of the previous claims, wherein multiple screening gates are substantially parallel to each other and preferably all screening gates are substantially parallel to each other.

14. Device according to any of the previous claims, wherein at least one screening gate layer comprises at least two arrays of screening gates, wherein each array of screening gates comprises multiple screening gates.

5 15. Device according to claim 14, wherein each array of screening gates comprises multiple screening gates comprising at least two outer legs which are mutually connected via at least one bridge element, wherein said at least one bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs, and wherein at least the outer legs of the screening
10 gates of a first screening gate array extend away from the outer legs of the screening gates of a second screening gate array.

16. Device according to any of the previous claims, wherein at least one screening gate layer comprises at least one barrier gate.

15

17. Device according to claim 14 or 15 and claim 16, wherein at least one barrier gate is substantially elongated and extends between a first array of screening gates and a second array of screening gates.

20 18. Device according to claim 17, wherein at least one barrier gate extends at least over a distance defined by at least one array of screening gates.

19. Device according to claim 17 or claim 18, comprising at least two barrier gates which extend between a first array of screening gates and a second array of
25 screening gates and wherein the smallest distance between at least one barrier gate and an adjacent screening gate is smaller than the distance between said at least two barrier gates.

20. Device according to any of the previous claims, wherein at least one
30 screening gate layer substantially overlaps with at least one primary gate layer.

21. Device according to any of the previous claims, wherein at least part of the electrodes of at least one primary gate layer overlap with at least part of the screening gates and/or barrier gates of at least one screening gate layer.

35

22. Device according to any of the previous claims, comprising at least one electrically insulating layer, wherein at least one electrically insulating layer which is located between at least one primary gate layer and at least one screening gate layer.

5

23. Device according to any of the previous claims, comprising at least one functional component, and preferably multiple functional components, provided upon at least one screening gate layer and/or at least one primary gate layer.

10 24. Device according to any of the previous claims, comprising at least one control layer configured for controlling the coupling of at least part of the electrodes of at least one primary gate layer.

15 25. Device according to claim 24, wherein at least one control layer comprises at least one array of control electrodes wherein at least part of the control electrodes overlap with at least part of the electrodes of at least one primary gate layer.

20 26. Device according to any of the previous claims, comprising at least one substrate, said substrate comprising at least one primary gate layer and at least one screening gate layer.

27. Use of a device according to any of the previous claims.

25 28. Process of manufacturing at least one qubit device, in particular according to any of claims 1-26, comprising the steps of:

- 30
- providing at least one substrate;
 - applying at least one screening gate layer to said substrate, wherein said at least one screening gate is configured for forming at least one sensing dot and in particular at least one sensing dot array; and
 - applying at least one primary gate layer comprising multiple electrodes to said substrate, wherein said at least one primary gate layer is configured for forming at least one quantum dot array, in particular at least one bilinear quantum dot array;

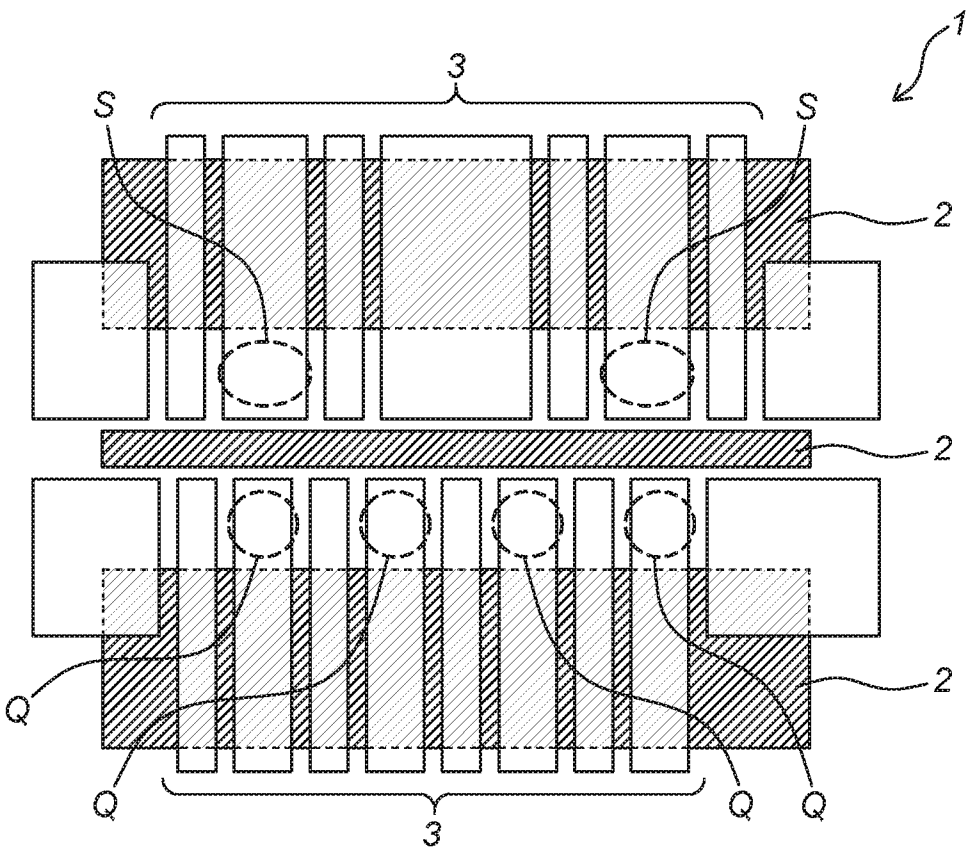
wherein the at least one screening gate layer comprises at least one array of screening gates ,

5 wherein each screening gate comprises at least two outer legs which are mutually connected via at least one bridge element, wherein said bridge element comprises at least one inner leg which extends into an area defined by said at least two outer legs and wherein the at least one inner leg of at least one screening gate is shorter than the at least two outer legs of said at least one screening gate, and

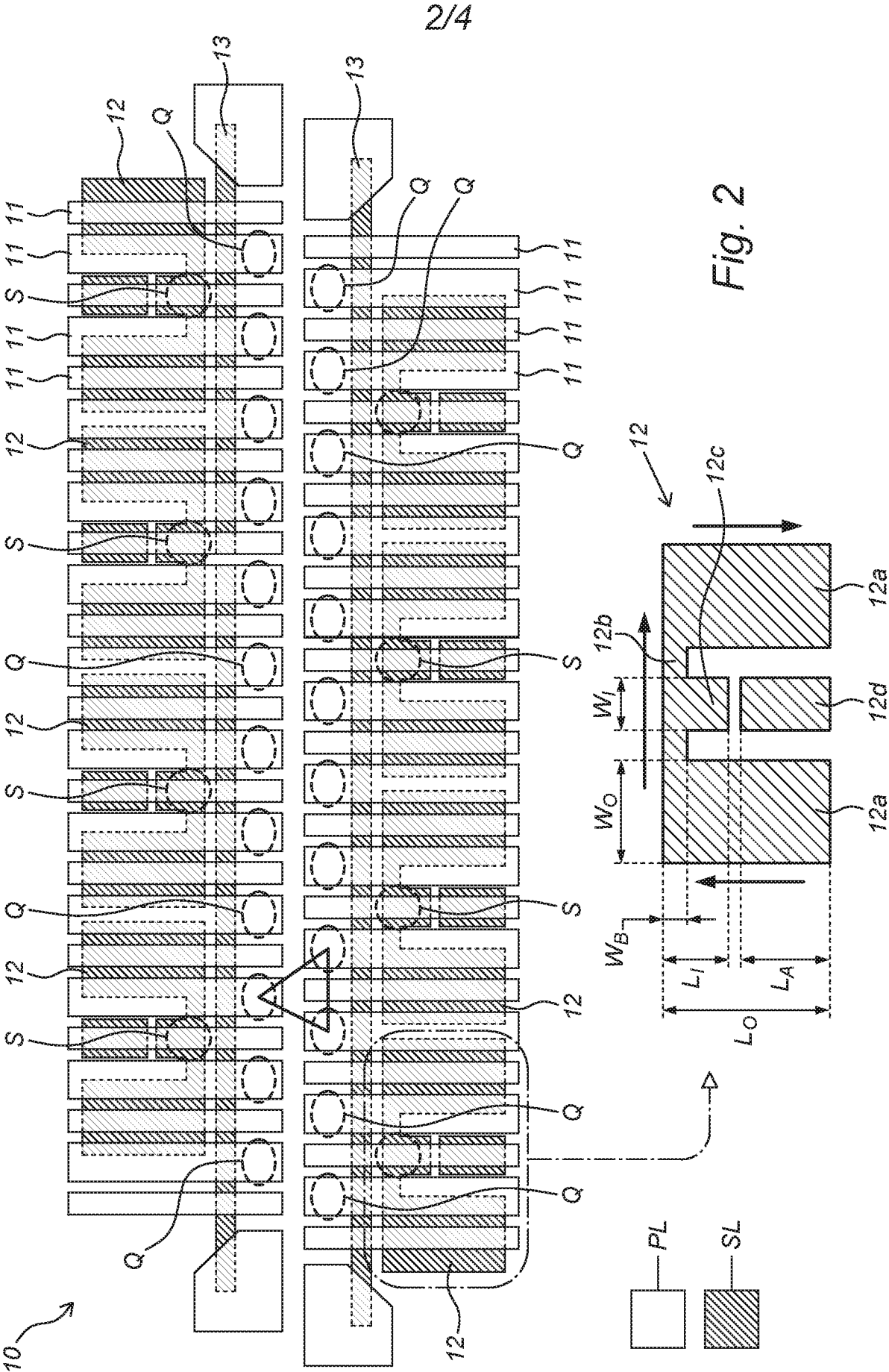
10 wherein at least part of the at least one array of screening gates is formed by a repeated pattern of at least two screening gates which are positioned substantially parallel such that the at least one screening gate layer enables the formation of at least one sensing dot array alongside at least one quantum dot array formed by the at least one primary gate layer.

15 29. Process according to claim 28, wherein the steps are subsequent steps.

30. Process according to claim 28 or claim 29, comprising the step of applying at least one electrically insulating layer to said substrate after at least one screening gate layer is applied and prior to at least one primary gate layer is applied.



(Prior Art)
Fig. 1



3/4

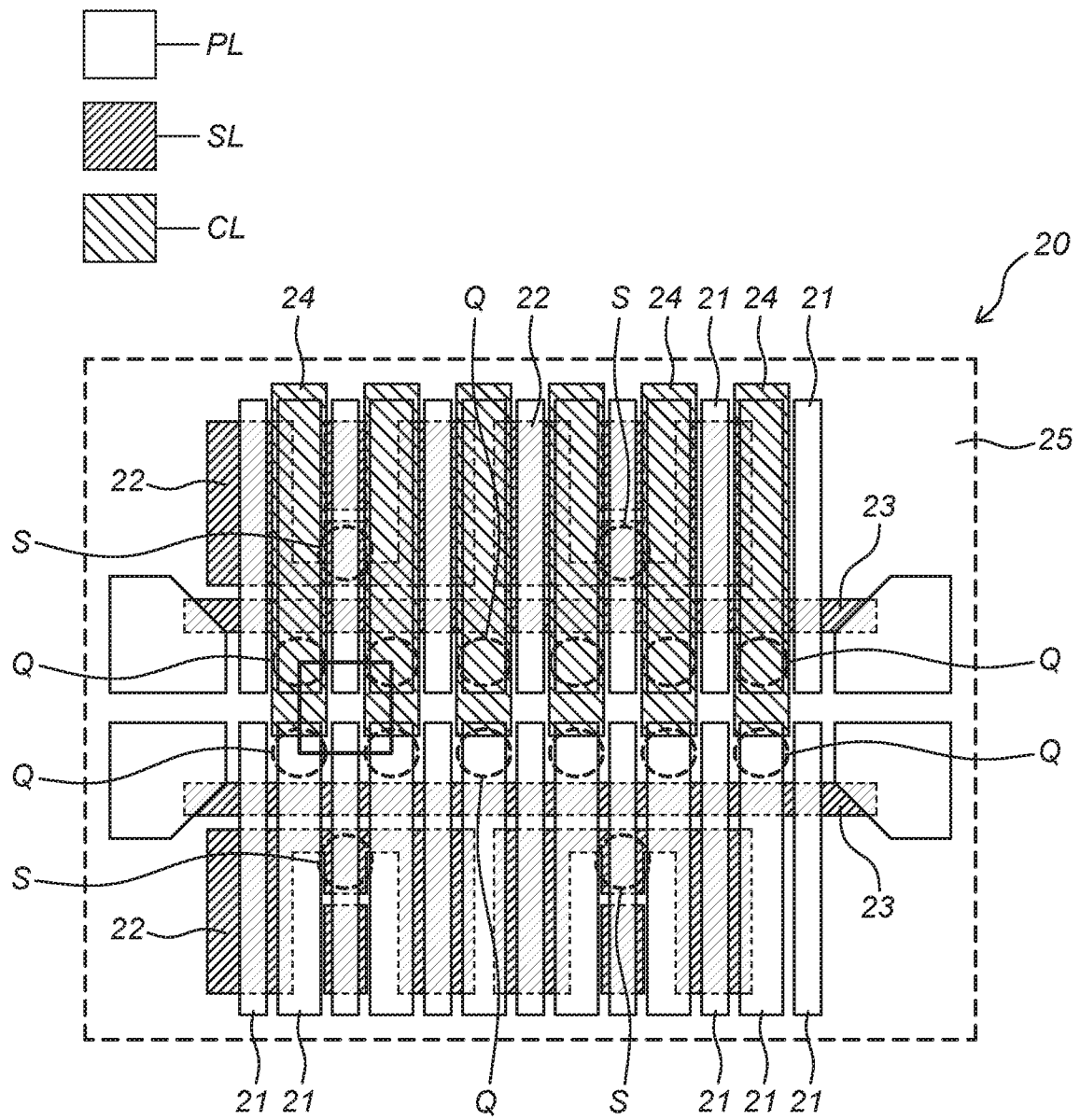


Fig. 3

4/4

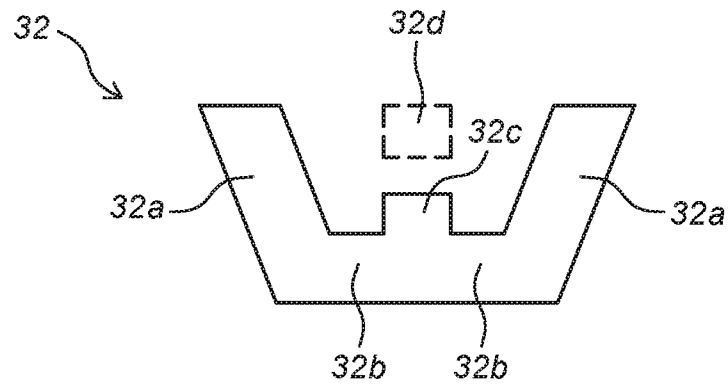


Fig. 4a

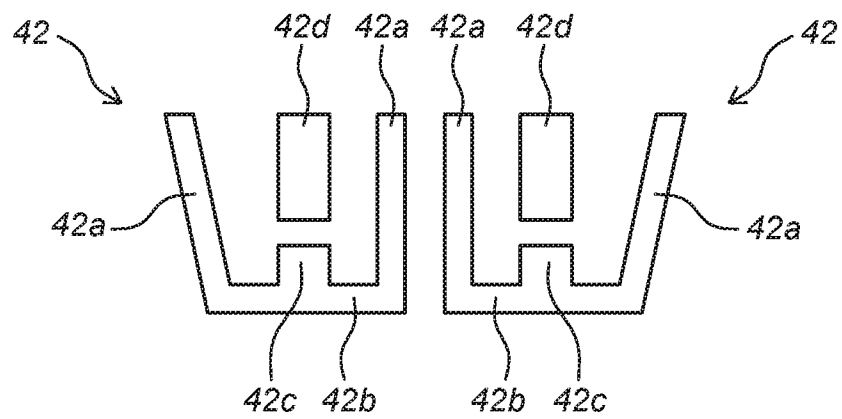


Fig. 4b

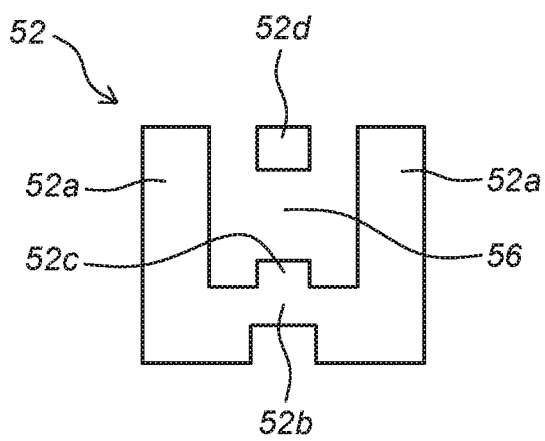


Fig. 4c

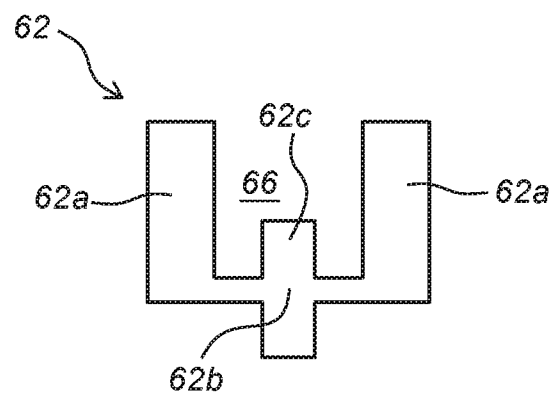


Fig. 4d

INTERNATIONAL SEARCH REPORT

International application No
PCT/NL2024/050608

A. CLASSIFICATION OF SUBJECT MATTER INV. G06N10/40 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) G06N		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	T-K HSIAO ET AL: "Exciton transport in a germanium quantum dot ladder", ARXIV.ORG, CORNELL UNIVERSITY LIBRARY, 201 OLIN LIBRARY CORNELL UNIVERSITY ITHACA, NY 14853, 5 July 2023 (2023-07-05), XP091556348, section II, lines 1-9 figures 1(a), 1(b) section III page 7, section 1 (Device fabrication and experiment setup) ----- -/-	1-30
☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 21 January 2025		Date of mailing of the international search report 04/02/2025
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Aoun, Marc

INTERNATIONAL SEARCH REPORT

International application No

PCT/NL2024/050608

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DODSON J P ET AL: "Fabrication process and failure analysis for robust quantum dots in silicon", ARXIV.ORG, CORNELL UNIVERSITY LIBRARY, 201 OLIN LIBRARY CORNELL UNIVERSITY ITHACA, NY 14853, 15 September 2020 (2020-09-15), XP081762894, the whole document -----	1 - 30