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(54) **Title:** RADIOFREQUENCY INTERCONNECTION BETWEEN A PRINTED CIRCUIT BOARD AND A WAVEGUIDE

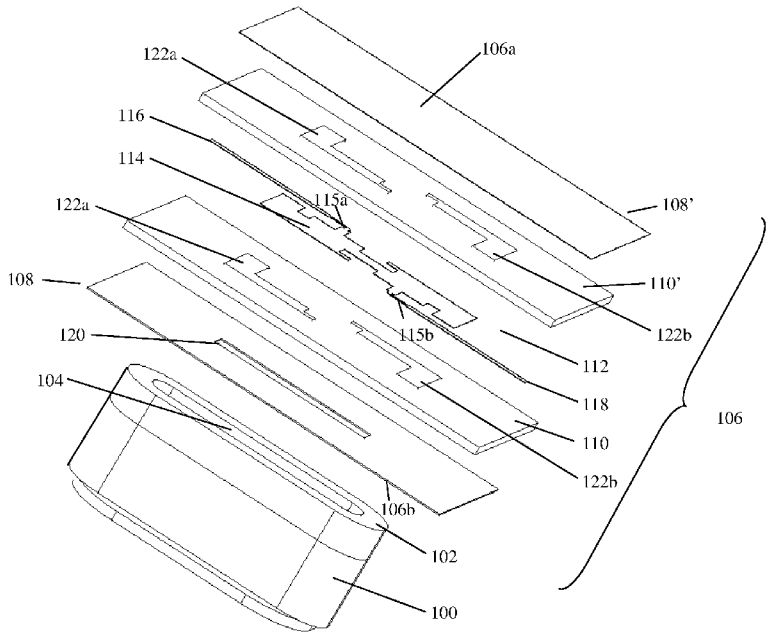

Fig. 1

(57) **Abstract:** A system comprising a waveguide (100) having a body with a first end (102) having an opening (104), and a printed circuit board, PCB (106), having a bottom side (106b) and an opposed top side (106a), wherein the PCB (106) comprises a ground layer (108), a dielectric material layer (110) and a signal layer (112) arranged in a layer stack from the bottom side (106b) to the top side (106a) of the PCB (106), wherein the dielectric material layer (110) is arranged between the ground layer (108) and the signal layer (112), wherein the signal layer (112) comprises a coupling pad (114) and a first and a second output transmission lines (116,118) both connected to the coupling pad (114), further comprising a non-conducting slot (120) in the ground layer (108), further comprising a electric wall (122) galvanically connecting the coupling pad (114) through the dielectric material layer (110) to the ground layer (108), wherein the first end (102) of the waveguide (100) is arranged on the bottom side (106b) and is galvanically connected with the ground

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layer (108), wherein the opening (104), the non-conducting slot (120) and the coupling pad (114) are aligned such that in a stacking direction of the layer stack the opening (104), the non-conducting slot (120) and the coupling pad (114) at least partially overlap.

Radiofrequency interconnection between a printed circuit board and a waveguide

TECHNICAL FIELD

The present invention is directed to a system comprising a waveguide and a printed circuit board (PCB) and the printed circuit board itself.

BACKGROUND

Rectangular waveguides are frequently used in high frequency/millimeter wave (mmW) applications to transmit or filter mmW signals with minimal power losses and/or signal distortion. Further, rectangular waveguide-based transmission lines/filters are commonly built from aluminum blocks by milling rectangular cavities in the aluminum. Therefore, they are bulky, heavy and mechanically incompatible with other components of a complete radio system, such as an RF transceiver or antenna, which are frequently developed on printed circuit boards (PCBs). Therefore, carefully designed signal transitions from/to rectangular waveguides to/from PCB-based transmission lines (e.g. microstrip lines, strip lines etc.) are required for the integration of PCB- based radio frequency components with waveguide-based components. For example, in the context of 5G mmW massive MIMO systems, in which multiple transceivers are integrated and coherently operated within a single radio unit, such transitions should be as compact as possible and preferably implement more than one function.

SUMMARY

Therefore, there is a need for providing a system comprising a waveguide and a PCB and the PCB itself, which are very compact. The objective of the present invention is achieved by the solution provided in the enclosed independent claims. Advantageous

implementations of the present invention are further defined in the respective dependent claims.

In a first aspect, a system is provided comprising a waveguide having a body with a first end having an opening, and a printed circuit board, PCB, having a bottom side and an opposed top side, wherein the PCB comprises a ground layer, a dielectric material layer and a signal layer arranged in a layer stack from the bottom side to the top side of the PCB, wherein the dielectric layer is arranged between the ground layer and the signal layer, wherein the signal layer comprises a coupling pad and a first and a second output transmission lines both connected to the coupling pad, further comprising a non-conducting slot in the ground layer; further comprising an electric wall galvanically connecting the coupling pad through the dielectric layer to the ground layer, wherein the first end of the waveguide is arranged on the bottom side and is galvanically connected with the ground layer, wherein the opening, the non-conducting slot and the coupling pad are aligned such that in a stacking direction of the layer stack the opening, the slot and the coupling pad at least partially overlap.

Therefore, due to the above-mentioned solution in the present invention, by using a galvanic concept no back short is required and therefore a very compact system comprising the waveguide and the PCB can be provided, wherein the system works at the same time as a power divider/balun. Therefore, the proposed solution is particularly suitable for applications that require high integration between the waveguide and the printed circuit board.

In a first implementation form of the system according to the first aspect, the electric wall is arranged on and contacts at least one edge portion of the coupling pad.

This is one implementation form for providing a galvanic contact between the coupling pad and the ground layer and on certain edge portions the electric wall has to galvanically contact the coupling pad for ensuring the galvanic contact between the coupling pad and the ground layer. Therefore, only a minimum area of the coupling

pad is needed for ensuring a galvanic contact between the coupling pad and the ground layer.

In a second implementation form of the system according to the first aspect, the coupling pad together with the first and second output transmission lines is point-symmetric with respect to a symmetry point of the coupling pad.

In a third implementation form of the system according to the first aspect, the coupling pad together with the first and second output transmission lines is mirror-symmetric with respect to an axis extending through a symmetry point of the coupling pad perpendicularly to a main extension direction of the coupling pad, wherein the main extension direction of the coupling pad is the direction, in which the coupling pad has its largest extension.

This is another alternative for providing a specific shape of the coupling pad also serving for high integration purposes and contributes for providing a compact coupling pad being part of the signal layer.

In a fourth implementation form according to the first aspect, the electric wall is formed at least by a plurality of conducting vias extending at least between the signal layer and the ground layer through the dielectric material layer.

Thereby, due to the arrangement of conducting (plated) vias, a very easy implementation form of the electric wall is provided, since conducting vias can be easily manufactured in a manufacturing process. Due to the arrangement of the vias and since these vias extend at least between the signal layer and the ground layer through the dielectric material layer, a galvanic contact between the signal layer and the ground layer is possible in a simple way.

In a fifth implementation form according to the first aspect, the electric wall includes a first and second electric wall portion, which are separated.

In particular, due to the arrangement of such an opening between the first and second electric wall portion it is possible that the output transmission lines can be directed away from the coupling pad at the shortest way possible and, for example, do not have to circumvent the whole coupling pad, but can penetrate through the coupling pad within the opening defined by the first and second electric wall portions. Therefore, an effective way of leading the first and second output transmission lines away from the coupling pad is possible.

In a sixth implementation form according to the first aspect, a first impedance matching portion and a second impedance matching portion are provided in the signal layer, wherein the first output transmission line is connected to the coupling pad by the first impedance matching portion and wherein the second output transmission line is connected to the coupling pad by the second impedance matching portion.

Due to the arrangement of the impedance matching portions it is possible to achieve a maximization of power transfer from the coupling pad to the first and second output transmission lines and a minimization of signal reflection.

In a seventh implementation form according to the first aspect, the layer stack further comprises a further dielectric material layer and a further ground layer, wherein the further dielectric material layer is arranged above the signal layer and wherein the further ground layer is arranged above the further dielectric material layer.

Therefore, in principle the coupling pad cannot only be coupled to the ground layer but also to the further ground layer, so that the coupling pad couples via the electric wall to both, the ground layer and the further ground layer.

In an eighth implementation form according to the first aspect, the electric wall further galvanically connects the further ground layer to the coupling pad and the ground layer.

Thereby, a galvanic connection between both, the ground layer and the further ground layer is possible.

In a ninth implementation form according to the first aspect, each of the layers of the PCB is provided with a through-hole configured for accepting a screw for screwing the PCB to the waveguide and the through-holes of each layer are aligned such that in the stack direction the through-holes coincide, thereby forming a hole extending from the top side of the PCB to the bottom side of the PCB, wherein the hole extending from the top side of the PCB to the bottom side of the PCB does not overlap with the opening in the waveguide, the non-conducting slot and the coupling pad.

Thereby, a tight fixing of the PCB with the waveguide is possible and a good galvanic contact between the ground layer and the walls of the waveguide is also possible. Since the through-hole extending from the top to the bottom side of the PCB does not overlap with the opening in the waveguide and the non-conducting slot, the overall operation and functioning of the whole system is not affected by the provision of the through-holes.

In a tenth implementation form according to the first aspect, the through-holes are metallized (plated) and form a part of the electric wall. Due to the metallization of the inner walls of the through-holes, a galvanic contact between the coupling pad and the ground layer is possible. Therefore, less additional vias have to be arranged, since the through holes are at least partly used as a part of the electronic wall. Furthermore, metallizing the inner wall of the through-hole can be easily implemented in the manufacturing process and therefore saves manufacturing costs.

In an eleventh implementation form according to the first aspect, the through-hole is arranged in close proximity to the coupling pad, so that a distance between a center axis of the through-hole of the signal layer to a center point of the opening of the wave guide is between 60% to 300% of a width of the opening of the waveguide, preferably between 100% to 250% of the width of the opening of the waveguide.

Thereby, it is possible to mechanically fix the coupling pad as good as possible in its position and impart stress on the coupling pad as close as possible to the opening of the waveguide

In a twelfth implementation form according to the first aspect, the system further comprises a waveguide-based stepped-impedance transformer attached to the open end of the waveguide between the first end of the waveguide and the bottom side of the PCB.

Thereby, it is possible to match the dimensions of the waveguide to the desired impedance level at the plane of the non-conductive slot. Thereby, also a very compact and small footprint non-conducting slot and coupling pad can be achieved on the PCB.

According to a second aspect of the present invention, a printed circuit board, PCB, is provided having a bottom side and an opposed top side, wherein the PCB comprises a ground layer, a dielectric material layer and a signal layer arranged in a layer stack from the bottom side to the top side of the PCB, wherein the dielectric material layer is arranged between the ground layer and the signal layer, wherein the signal layer comprises a coupling pad and a first and second output transmission line, both connected to the coupling pad, further comprising a non-conducting slot in the ground layer, further comprising an electric wall galvanically connecting the coupling pad through the dielectric material layer to the ground layer, wherein the non-conducting slot and the coupling pad are aligned, such that in a stack direction of the layer stack the non-conducting slot and the coupling pad at least partially overlap.

Thereby, a very compact PCB board can be provided, which can be used for providing a system of a waveguide and the PCB board, wherein this system does not need any waveguide back short.

BRIEF DESCRIPTION OF DRAWINGS

The above-described aspects and implementation forms of the present invention will be explained in the following description of specific embodiments in relation to enclosed drawings in which

FIG. 1 shows an exploded view of a system according to an embodiment of the present invention.

FIG. 2 shows a schematic cross-sectional view of the transition between the waveguide and the PCB.

FIG. 3 shows another schematic cross-sectional view of a system comprising a waveguide and a PCB according to an embodiment of the present invention.

FIG. 4 shows another schematic cross-sectional view of another system comprising a waveguide and a PCB according to an embodiment of the present invention.

FIG. 5 shows a top view on a signal layer of a PCB according to an embodiment of the present invention.

FIG. 6 shows on the left side a top view of a PCB and on the right side a bottom view of the PCB according to an embodiment of the present invention.

FIG. 7 shows a perspective side view on a signal layer of a PCB according to an embodiment of the present invention.

FIG. 8 shows a top view of an arrangement comprising a PCB according to the present invention and an antenna array.

FIG. 9 shows simulated S-parameters depending on the frequency of the proposed solution according to the present invention.

FIG. 10 shows simulated phase differences between the first and second output transmission lines of a PCB according to an embodiment of the present invention.

Generally, it has to be noted that all arrangements, devices, elements, units and means and so forth, described in the present application, could be implemented by software or hardware elements or any kind of combination thereof. All steps which are performed by the various entities described in the present application as well as the functionality described to be performed by the various entities are intended to mean that the respective entity is adapted to or configured to perform the respective steps and functionalities. Even if in the following description of specific embodiments a specific functionality or step to be performed by a general entity is not reflected in the description of a specific detailed element of that entity which performs that specific step or functionality, it should be clear for a skilled person that these elements and functionalities can be implemented in respective hardware or software elements or any kind of combination thereof. Further, the method of the present invention and its various steps are embodied in the functionalities of the various described apparatus elements.

In FIG. 1 a system comprising a waveguide 100 and a PCB 106 are shown. As one can see, waveguide 100 has a body having a first end 102 and an opening 104. The opening 104 is shown in FIG. 1 as an elongated opening 104. The length of opening 104 is defined as the extension of opening 104 in the main extension direction of the opening 104, wherein the main extension direction is the direction in which the opening 104 has its largest extension. A width of the opening 104 is perpendicular to the length of the opening 104. Furthermore, in the exploded view of FIG. 1, PCB 106 comprises a ground layer 108, a dielectric material layer 110 and a signal layer 112 in the stack direction. In this context, the further dielectric material layer 110' and the further

ground layer 108', above signal layer 112 and therefore above coupling pad 114, as can be seen in FIG. 1, are just optional features and not absolutely necessary for enabling the present invention. Therefore, the essential elements are the ground layer 108, the dielectric material layer 110 together with electric wall 122a, 122b and signal layer 112 in the stack direction starting from the bottom side 106b of PCB 106.

In particular, the signal layer 112 comprises a coupling pad 114 and a first output transmission line 116 and a second output transmission line 118. As shown in FIG. 1, the first output transmission line 116 and the second output transmission line 118 can be separately connected to the coupling pad 114 via a first impedance matching section 115a and a second impedance matching section 115b, respectively. Further, as shown in FIG. 1, the structure comprising the first and second output transmission lines 116 and 118 together with the coupling pad 114 can be point-symmetric with respect to a symmetry point of the coupling pad 114 being a center point of the coupling pad 114. Furthermore, the first and second output transmission lines 116 and 118 can be microstrip lines in one example.

Further, in a stack direction of the system of Fig. 1, above ground layer 108 dielectric material layer 110 is provided, wherein electric wall extends through dielectric material layer 110 so that coupling pad 114 is galvanically connected to ground layer 108 through the dielectric material layer 110. In this context, the electric wall consists of a first electric wall portion 122a and a second electric wall portion 122b, both arranged within dielectric material layer 110, so as to cover at least an edge portion 124 of coupling pad 114. In one implementation form, electric wall 122a, 122b can be implemented by vias instead of providing the elongated portions 122a, 122b as can be seen in FIG. 1. Furthermore, ground layer 108 comprises a non conducting slot 120. In the embodiment of FIG. 1, non-conducting slot 120 is arranged so that in the stack direction non-conducting slot 120 overlaps with elongated opening 104. Furthermore, ground layer 108 is galvanically connected to waveguide 100 and opening 104 of waveguide 100 at least partially overlaps with non-conducting slot 120 and coupling pad 114.

Furthermore, waveguide 100 and/or ground layers 108, 108' and/or the signal layer 112 and/or electric wall 122 can be made of an electrically conductive material, e.g. copper or aluminium. In this context, non conducting slot 120 is needed to couple the fields from the waveguide 100 to the first and second output transmission lines 116 and 118 via electric wall 122a, 122b. In this context, as said above, optionally an additional further dielectric material layer 110' can be arranged above signal layer 112. Above further dielectric material layer 110' the further ground layer 108' can be provided in the stack direction. Furthermore, within further dielectric material layer 110' electric wall 122a, 122b is extended also into the further dielectric material layer 110 in the same position as within dielectric material layer 110 and preferably having also the same dimensions as within dielectric material layer 110. Thereby, it is possible that the signal layer 112 is galvanically coupled to the ground layer 108 and to the further ground layer 108' at the same time via electric wall 122 provided respectively on dielectric material layer 110 and further dielectric material layer 110. Further, dielectric wall 122a, 122b is shaped so as to ensure proper field distribution.

Further, on the first end 102 of waveguide 100 a stepped impedance transformer can be attached and on an opposed second end of the stepped impedance transformer the bottom side 106b of the PCB 106 can be attached. Thereby, a small footprint of the opposed end of the stepped impedance transformer can be achieved on the bottom surface of the bottom side 106b of PCB 106.

With this arrangement of FIG. 1, an incoming signal from the waveguide is split into two separate signals by the coupling pad 114 provided within the PCB 106, wherein those signals preferably have equal amplitudes and are out-of-phase by 180°. The area required on the PCB for the transition and the power division function is particularly small, and no waveguide back short is required on the top side 106a of the PCB 106. In the arrangement according to the present invention, the dimensions of the coupling pad 114 can also be made much smaller as in state of the art solutions.

FIG. 2 shows a schematic cross-sectional view of a system according to an embodiment of the present invention. There, waveguide 100 is galvanically connected to the ground

layers 108, 108' of PCB 106. The system of the waveguide 100 together with the PCB 106 is fixed by screws 202. The screws 202 extend from the top side 106a of the PCB 106 beyond the bottom side 106b of the PCB 106 for fixing and galvanically connecting the ground plane of the PCB 106 to waveguide 100. The screws 202 are separated from non-conducting slot 120 in the stack direction, so that screws 202 and the non-conducting slot 120 together with opening 104 do not overlap. Further in the stack direction above ground layer 108 dielectric material layer 110 is provided. Above dielectric material layer 110 signal layer 112 is provided followed by further (optional) dielectric material layer 110'. Above the further dielectric material layer 110' the further (optional) ground layer 108' is provided. Screws 202 extend respectively through a through hole extending from the top side 106a of the PCB 106 to the bottom side 106b of PCB 106. Screws 202 enable good galvanic contact between waveguide 100, ground layer 108, coupling pad 114 in signal layer 112 and the further ground layer 108' and a tight fixation of the elements of the system.

FIG. 3 shows another schematic cross-sectional view of another embodiment of the present invention. There, again PCB 106 is attached to waveguide 100. Furthermore, in the stack direction, the ground layer 108, dielectric material layer 110, signal layer 112, further dielectric material layer 110 and further ground layer 108 can be provided.

Figure 4 shows another schematic cross-sectional view of another embodiment of the present invention. In the stack direction, on the bottom side 106b of PCB 106 the first end 102 of waveguide 100 is attached. Further, in the stack direction, the bottom layer 108, the dielectric material layer 110, the signal layer 112, the further dielectric material layer 110', the further signal layer 112', a further dielectric material layer 110'' and a further ground layer 108' can be provided.

Fig. 5 shows a top view on a signal layer of a PCB according to a further embodiment of the present invention. There, electric wall is separated into two electric wall portions, namely the first electric wall portion 122a and the second electric wall portion 122b. These two electric wall portions 122a and 122b are separated from each other,

thereby forming a first opening 502 and a second opening 504 through which at least partially first output transmission line 116 and second output transmission line 118 respectively can extend. Furthermore, both, the first electric wall portion 122a and the second electric wall portion 122b, respectively, contact the edge portion 124 of coupling pad 114. Both, the first electric wall portion 122a and the second electric wall portion 122b extend through dielectric material layer 110 and contact ground layer 108, so that coupling pad 114 is galvanically coupled to ground layer 108. In this context, opening 104 of the waveguide 100, the non-conducting slot 120 and coupling pad 114 are aligned in the stack direction, so that opening 104, non-conducting slot 120 and coupling pad 114 at least partially overlap, which can also be seen in FIG. 5. Coupling pad 114 together with first and second output transmission lines 116 and 118 are point symmetric with respect to a center point of the coupling pad 114.

In this context, it should be noted that first and second electric wall portions 122a and 122b are shown in FIG. 5 as elongated portions and therefore consuming much of the volume of dielectric material layer 110. However, it is typically sufficient that electric wall 122a, 122b contacts the edge portion 124 of coupling pad 114 and therefore the dimensions of the electric wall 122a, 122b can be made much smaller than shown in Fig. 5. In particular the first and second electric wall portions 122a and 122b can be made as small as a portion of each electric wall portions 122a and 122b overlaps with an edge portion 124 of coupling pad 114. Further, instead of the elongated continuous electric wall portions 122a and 122b the first and second electric wall portions 122a and 122b can consist of or comprise series of vias at least extending from the coupling pad to ground layer 108 through dielectric material layer 110. The distance between the vias is chosen such that for a lowest frequency of signals transmitted using the system the vias form an electric wall.

Further, FIG. 6 shows another embodiment of the present invention showing on the left side the signal layer 112 of PCB 106 and on the right side the ground layer 108 of PCB 106. The dark grey structures indicate copper material, the bright grey structures indicate holes and vias. Further, the black structures show copper free areas. On the left side showing signal layer 112 three separate coupling pads 114 are provided in

sequence from the top of the left side figure to the bottom of the left side figure. Each of these coupling pads 114 together with first and second output transmission lines 116 and 118 is point-symmetric with respect to a center point of coupling pad 114. Furthermore, first and second electric wall portions 122a and 122b are provided next to each coupling pad 114 by arranging a plurality of vias 602 in a series, so that each of the electric wall portions 122a and 122b consists of a plurality of vias 602. Further, screw openings (through holes) 202' are provided in close proximity to coupling pad 114. In this context, the distance between the center of the screw openings 202' and the center of the waveguide opening 104 can be minimum 0.6 times the width of the waveguide opening. In a preferred implementation, this distance should be between 100%-250% of the width of the waveguide opening, also depending on the diameter of the used screws and the corresponding though hole.

The off-centered feeding of the coupling pad is advantageous for a close placing of the screws to the coupling pad 114. Therefore, it is possible to arrange screws 202 as close as possible to each coupling pad 114, thereby ensuring a tight mechanical fixing of each coupling pad 114 in the arrangement and mechanical stress is exerted on each coupling pad 114 as high as possible. Furthermore, in particular due to the point-symmetric arrangement of coupling pad 114, a very dense arrangement of the coupling pads 114 together with screws 202 is possible. The right half of FIG. 6 shows the ground layer 108 of the PCB 106 with non-conducting slots 120, the vias 602 and the screw openings 202'.

Further, FIG. 7 shows another embodiment of the present invention in a perspective view on signal layer 112, wherein coupling pad 114 is mirror-symmetric with respect to an axis extending through a symmetry point of coupling pad 114 perpendicular to a main extension direction of the coupling pad 114, wherein the main extension direction is the direction of the largest extension of the coupling pad 114. Furthermore, electric wall is made up of four electric wall portions, 122 a, b, c, and d, which at least partially contact respectively coupling pad 114 on a respective edge portions 124.

Furthermore, FIG. 8 shows a PCB of the present invention together with first radiators 811a, second radiators 811b, third radiators 812a and fourth radiators 812b. The first, second, third and fourth radiators 811a, 811b, 812a and 812b are arranged in columns, wherein each column can contain one first radiator 811a, one second radiator 811b, one third radiator 812a and one fourth radiator 812b. However, each column can also contain more than four radiators. Further, between the second radiator 811b and the third radiator 812a the coupling pad 114 together with first and second output transmission lines 116 and 118 are provided in the point symmetric arrangement. Further, the first output transmission line 116 is connected to the first and second radiators 811a and 811b. Further, the third and fourth radiators 812a and 812b are connected to the second output transmission line 118. Further first and second electric wall portions 122a and 122b are implemented by a plurality of vias 602. Further in a direction perpendicular to the columns, screws 202 are provided as close as possible to coupling pad 114 for ensuring a tight fixing of the coupling pad 114.

The first and second radiators 811a and 811b resemble a first subarray and the third and fourth radiators 812a and 812b resemble a second subarray, wherein the two subarrays are fed with 180° phase difference. Due to the compact arrangement of the coupling pad 114 together with vias 602 the distance between the two sub-arrays can also be minimized and the column width can be minimized. This leads to a better performance regarding side lobes for large tilt angles.

Further, FIG. 9 shows a graph indicating the S-parameter (in dB) on the y-axis and the corresponding frequency (in GHz) on the x-axis and shows simulated S-parameters of the present invention. As can be seen in FIG. 9, the return loss is better than 15 dB within a relative bandwidth of around 15% and better than 10 dB within a relative bandwidth of around 20%.

Furthermore, FIG. 10 shows a simulated phase difference between the first and second output transmission lines 116 and 118 of the PCB 106, wherein there one can clearly see that the phase difference is very stable at 180° for the entire simulated frequency range. The phase jump shown in the figure can be ignored, as this is caused in by phase

wrapping in the simulation program. Therefore the waveguide transition has at the same time the functionality of a balun.

The invention has been described in conjunction with various embodiments herein. However, other variations to the enclosed embodiments can be understood and effected by those skilled in the art and practicing the claimed invention, from a study of the drawings, the disclosure and the appended claims. In these claims, the word "comprising" does not exclude other elements or steps and the indefinite article "a" or "an" does not exclude a plurality. A single processor or another unit may fulfill the function of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. A computer program may be stored/distributed on a suitable medium, such as an optical storage medium or a solid state medium supplied together with or as part of other hardware, but may also be distributed in other forms, such as via the internet or other wired or wireless telecommunication systems.

CLAIMS

1. A system comprising:

a waveguide (100) having a body with a first end (102) having an opening (104), and

a printed circuit board, PCB, (106) having a bottom side (106b) and an opposed top side (106a), wherein the PCB (106) comprises a ground layer (108), a dielectric material layer (110) and a signal layer (112) arranged in a layer stack from the bottom side (106b) to the top side (106a) of the PCB (106), wherein the dielectric material layer (110) is arranged between the ground layer (108) and the signal layer (112), wherein the signal layer (112) comprises a coupling pad (114) and a first and a second output transmission line (116, 118) both connected to the coupling pad (114);

wherein the PCB further comprises a non-conducting slot (120) in the ground layer (108);

wherein the PCB further comprises an electric wall galvanically connecting the coupling pad (114) through the dielectric material layer (110) to the ground layer (108);

wherein the first end (102) of the waveguide (100) is arranged on the bottom side (106b) of the PCB (106) and is galvanically connected with the ground layer(108);

wherein the opening (104), the non-conducting slot (120) and the coupling pad (114) are aligned such that in a stacking direction of the layer stack the opening (104), the non-conducting slot (120) and the coupling pad (114) at least partially overlap.

2. The system according to claim 1, wherein

the electric wall (122) is arranged on and contacts at least one edge portion (124) of the coupling pad (114).

3. The system according to any of the preceding claims, wherein

the coupling pad (114) together with the first and second output transmission lines (116, 118) is point symmetric with respect to a symmetry point of the coupling pad (114).

4. The system according to claim 1 or 2, wherein

the coupling pad (114) together with the first and second output transmission lines (116, 118) is mirror symmetric with respect to an axis extending through a symmetry point of the coupling pad (114) perpendicular to a main extension direction of the coupling pad (114), wherein the main extension direction of the coupling pad (114) is the direction in which the coupling pad (114) has its largest extension.

5. The system according to any of the preceding claims,

wherein the electric wall is formed at least by a plurality of conducting vias (602) extending at least between the signal layer (112) and the ground layer (108) through the dielectric material layer (110).

6. The system according to any of the preceding claims,

wherein the electric wall includes a first and a second electric wall portion (122a, 122b), which are separated, thereby forming at least two openings (502, 504) through which the first and second output transmission lines (116, 118) extend.

7. The system according to any of claims 1 -6,

wherein the PCB further comprises a first impedance matching portion (115a) and a second impedance portion (115b) in the signal layer(112);

wherein the first output transmission line (116) is connected to the coupling pad (114) by the first impedance matching portion (115a); and

wherein the second output transmission line (118) is connected to the coupling pad (114) by the second impedance matching portion(115b).

8. The system according to any of the preceding claims, wherein the layer stack further comprises a further dielectric material layer (110') and a further ground layer(108');

wherein the further dielectric material layer (110') is arranged above the signal layer (112); and

wherein the further ground layer (108') is arranged above the further dielectric layer (110).

9. The system according to claim 8,

wherein the electric wall (122) further galvanically connects the further ground layer (108) to the coupling pad (114) and the ground layer (108).

10. The system according to any of the preceding claims, wherein

each of the layers of the PCB (106) is provided with a through-hole configured for accepting a screw (202) for screwing the PCB (106) to the waveguide (110) and the through-holes of each layer are aligned such that in the stacking direction the through-holes coincide, thereby forming a hole extending from the top side (106a) of the PCB (106) to the bottom side (106b) of the PCB (106), wherein the hole extending from the top side (106a) of the PCB (106) to the bottom side (106b) of the PCB (106) does not overlap with the opening (104) in the waveguide (100), the non-conducting slot (120) and the coupling pad (114).

11. The system according to claim 10, wherein the through-holes are metalized and form a part of the electric wall.

12. The system according to claim 10 or 11, wherein

the through hole of the signal layer (112), and therefore the hole extending from the top side (106a) of the PCB (106) to the bottom side (106b) of the PCB (106), is arranged in close proximity to the coupling pad (114), so that a distance between a center axis of the through hole of the signal layer (112) to the symmetry point of the

waveguide opening (104) is between 60% to 300% of a width of the opening (104) of the waveguide (100), preferably between 100% to 250% of the width of the opening (104) of the waveguide (100).

13. The system according to any of the preceding claims,

further comprising a stepped impedance transformer attached to the first end (102) of the waveguide (100) between the first end (102) of the waveguide (100) and the bottom side (106b) of the PCB (106).

14. A printed circuit board, PCB, (106) having a bottom side (106b) and a opposed top side (106a), wherein the PCB (106) comprises a ground layer (108), a dielectric material layer (110) and a signal layer (112) arranged in a layer stack from the bottom side (106b) to the top side (106a) of the PCB (106), wherein the dielectric material layer (110) is arranged between the ground layer (108) and the signal layer (112), wherein the signal layer (112) comprises a coupling pad (114) and a first and a second output transmission line (116, 118) both connected to the coupling pad (114);

further comprising a non-conducting slot (120) in the ground layer (108);

further comprising a electric wall (122) galvanically connecting the coupling pad (114) through the dielectric material layer (110) to the ground layer (108);

wherein the non-conducting slot (120) and the coupling pad (114) are aligned such that in a stacking direction of the layer stack the non-conducting slot (120) and the coupling pad (114) at least partially overlap.

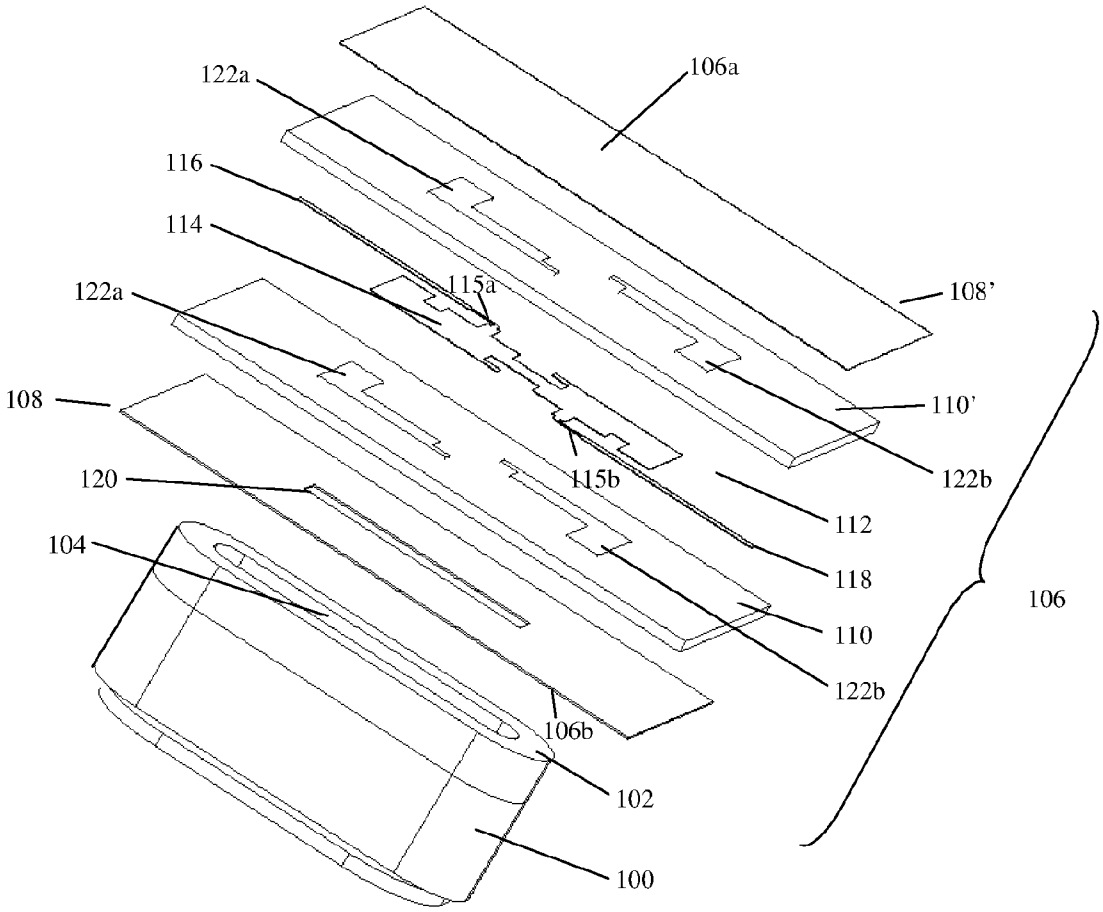
106a
122a
116
114
115a
122a
108'
108
110'
115b
122b
120
112
104
118
110
106
122b
106b
102
100

Fig. 1

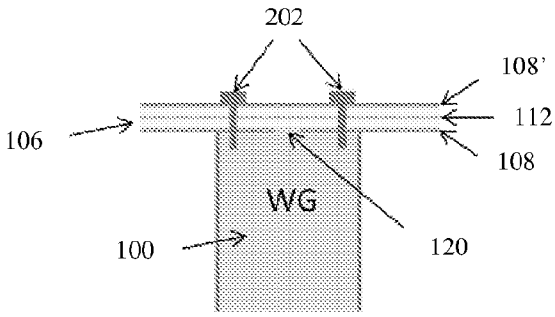

Fig. 2

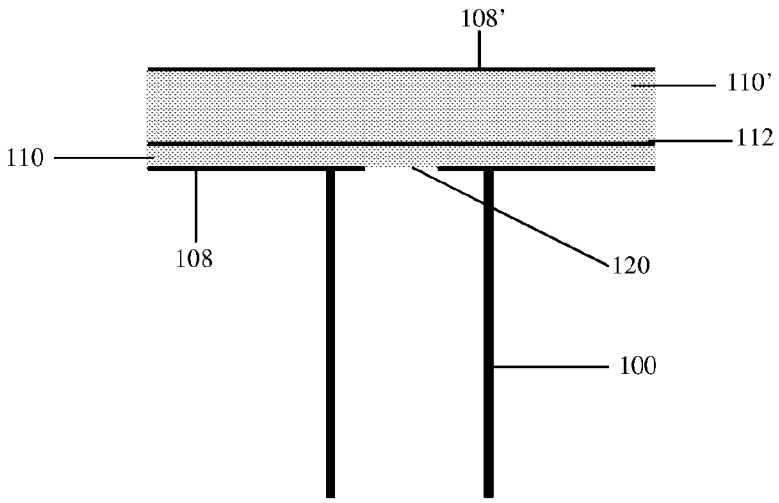

Fig. 3

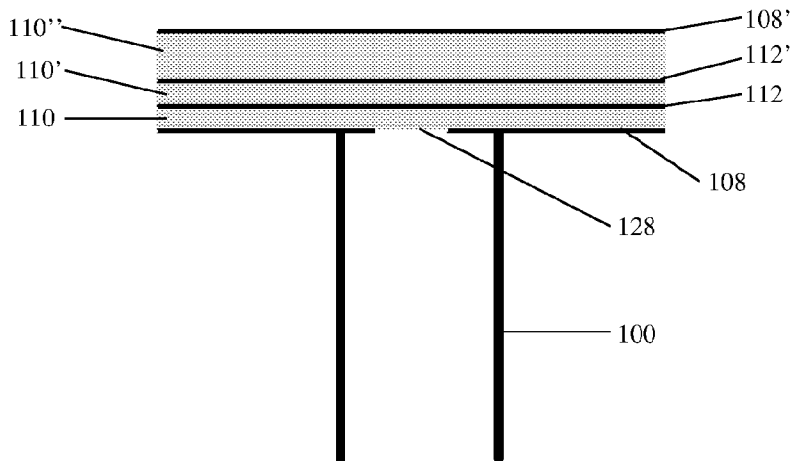

Fig. 4

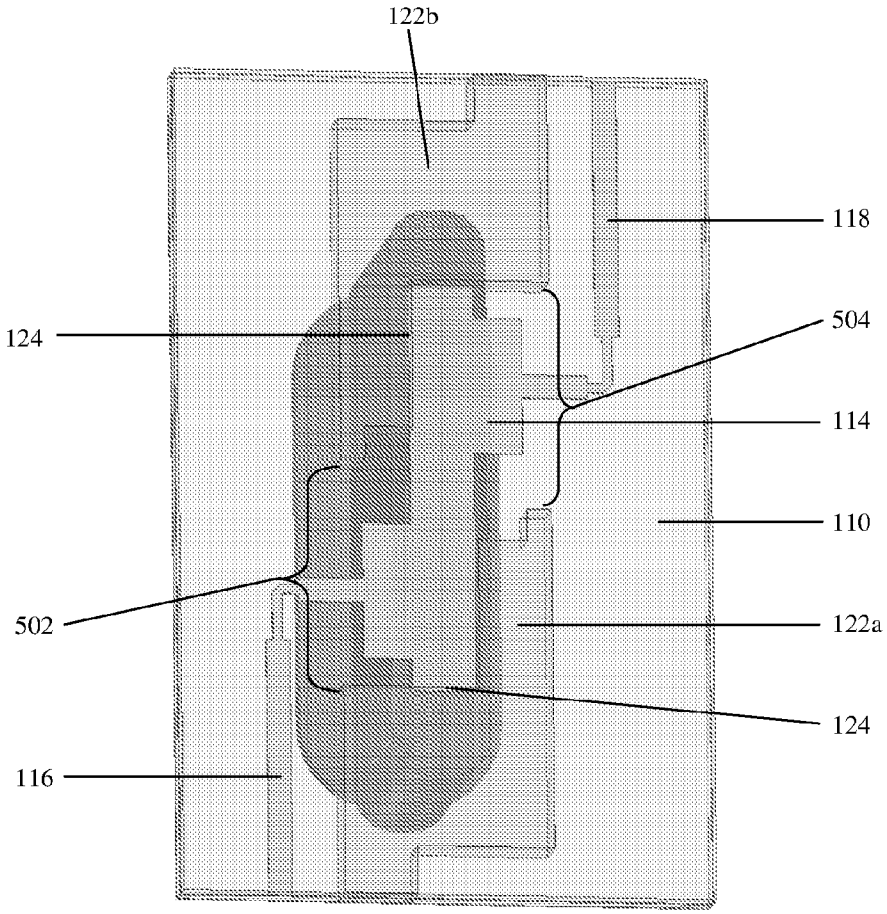

Fig. 5

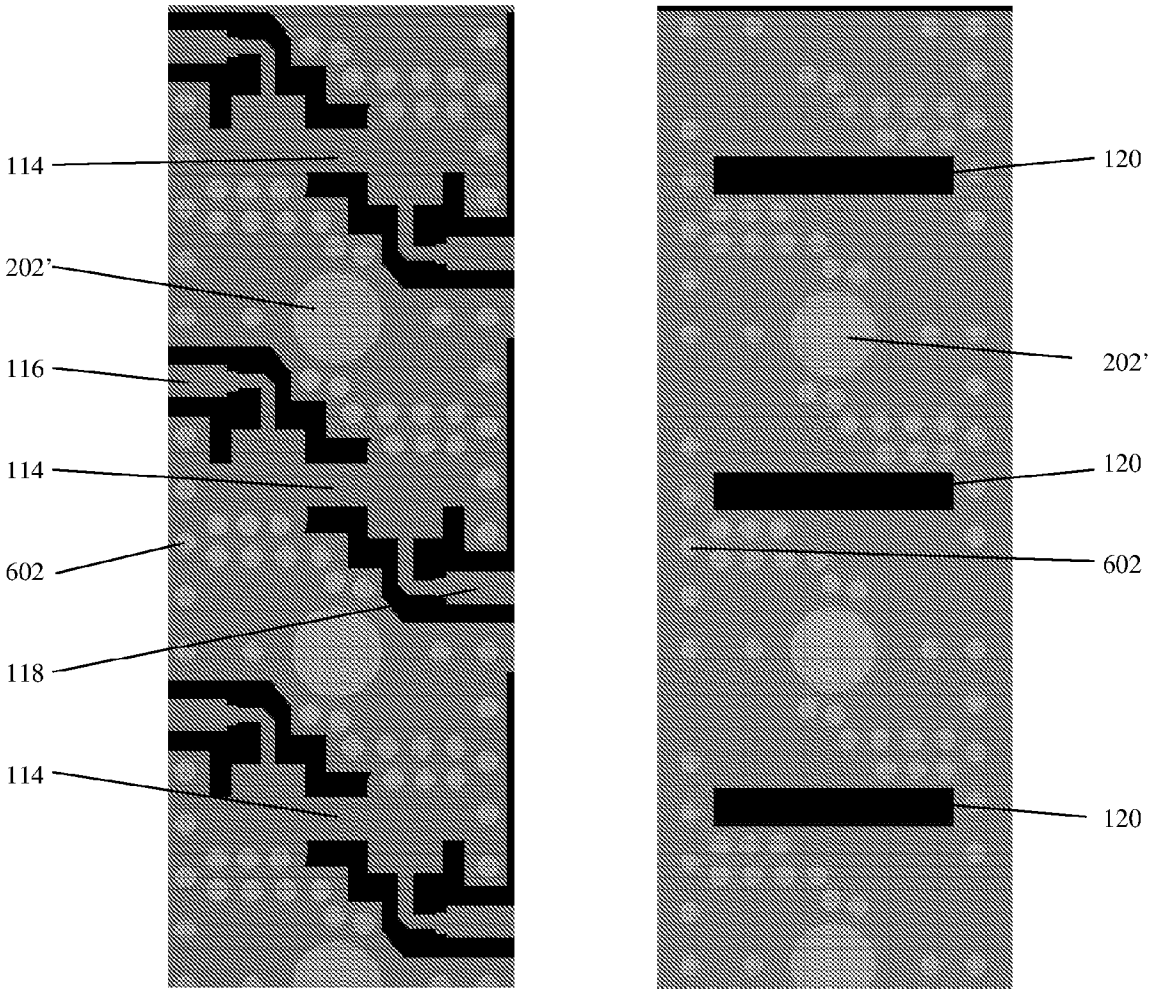

Fig. 6

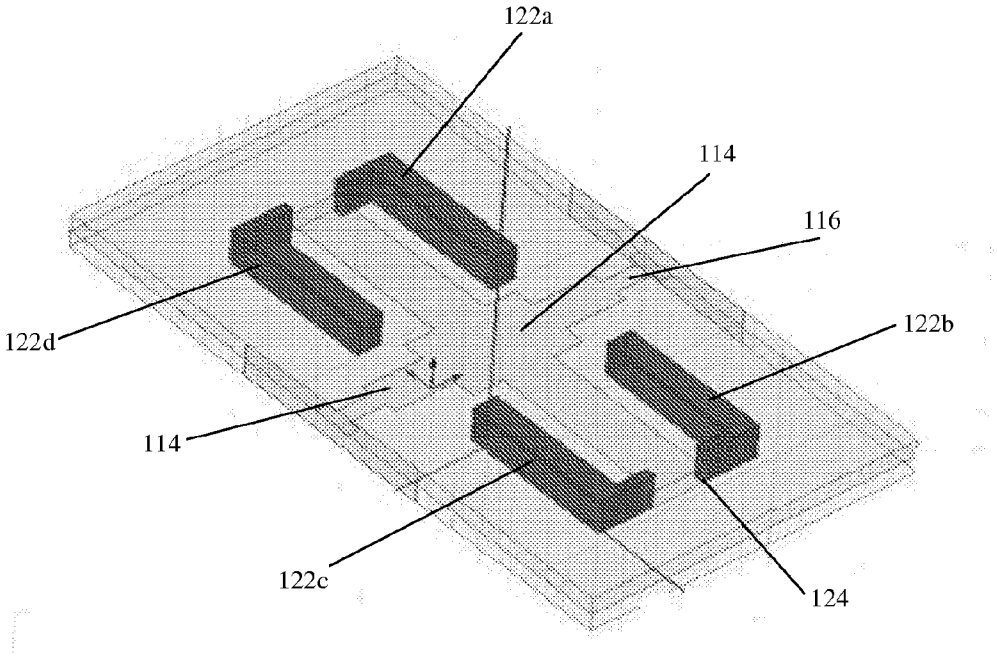

Fig. 7

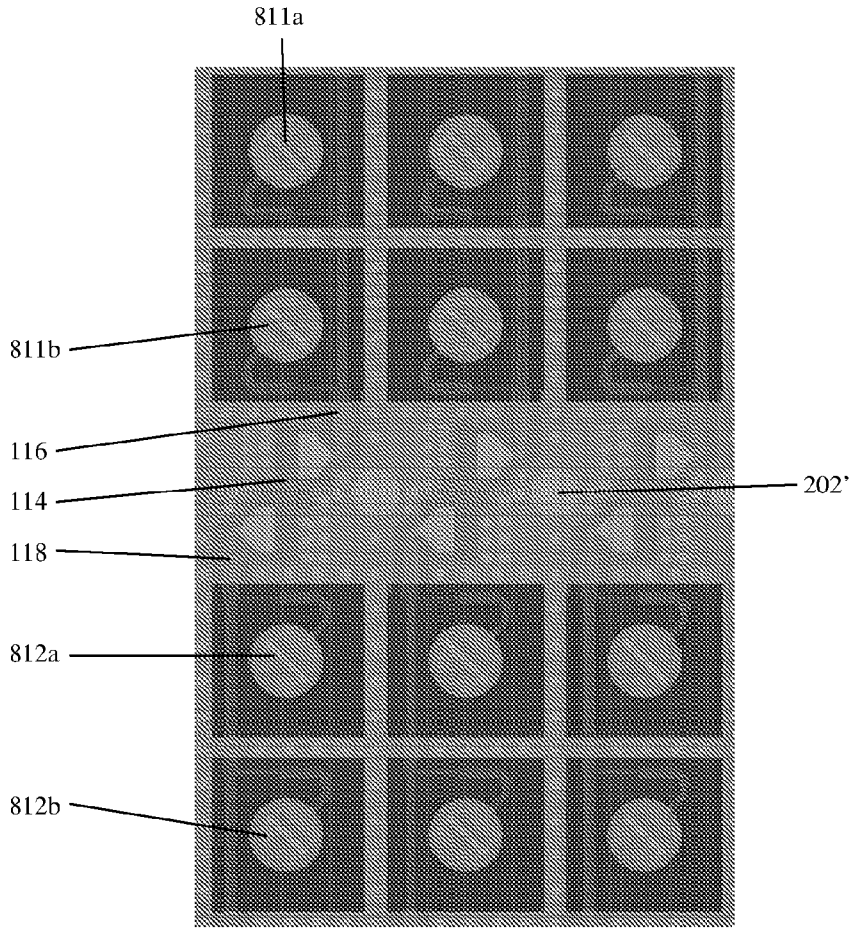

Fig. 8

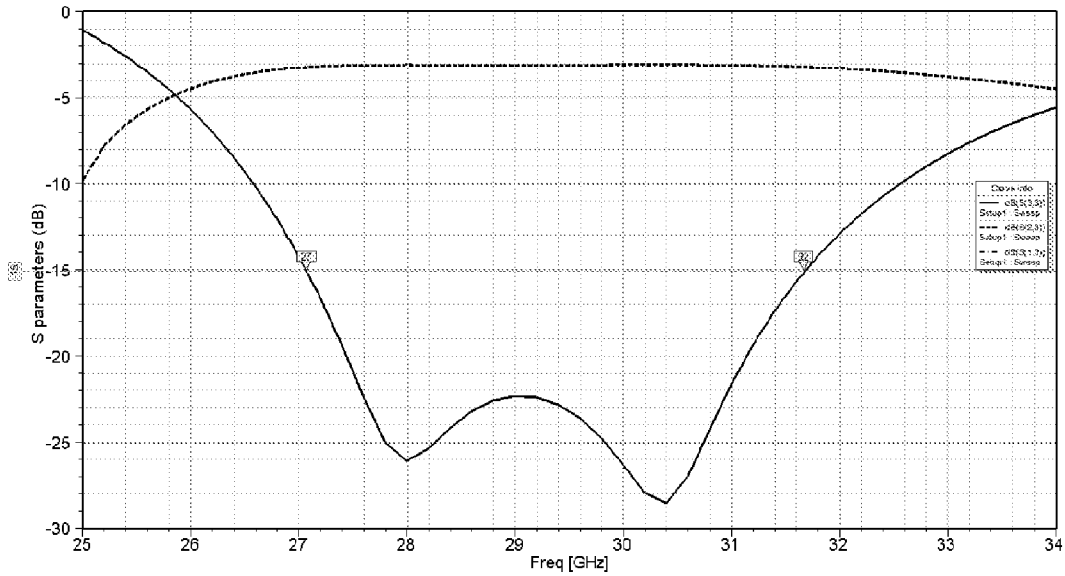
0
-5
-10
-15
-20
-25
-30
S parameters (dB)
25
26
27
28
29
30
31
32
33
34
Freq [GHz]

Fig. 9

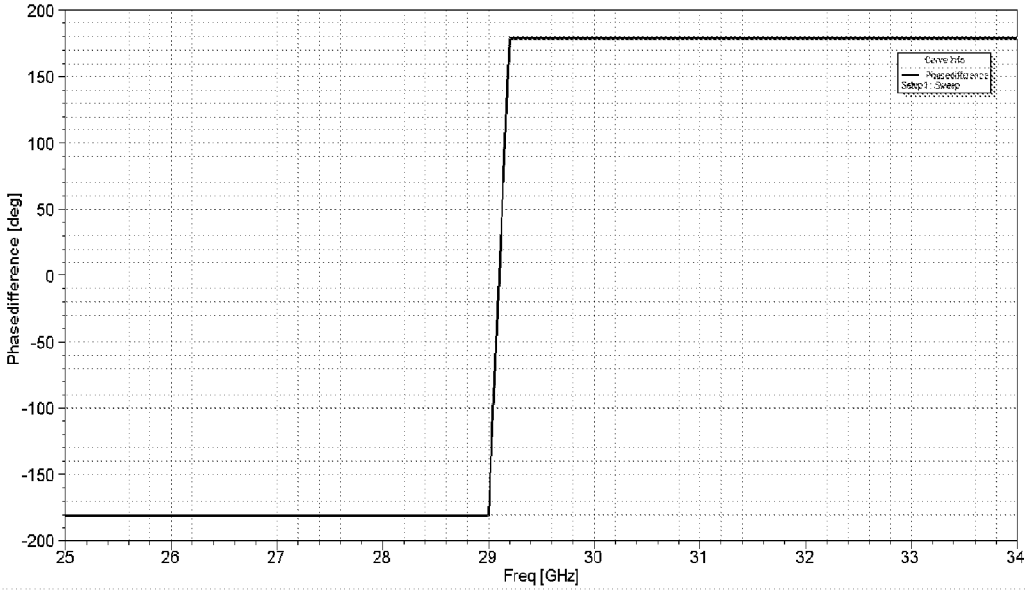
200
150
100
50
0
-50
-100
-150
-200
Phasedifference [deg]
25
26
27
28
29
30
31
32
33
34
Freq [GHz]
Curve Info
Phasedifference
Setup1 : Sweep

Fig. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/081886

A. CLASSIFICATION OF SUBJECT MATTER

H01P 5/107(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01P

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: waveguide?, PCB, printed circuit board, interconnect+, rf, radiofrequency, millimeter wave, opening, slot, cavity

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 203119074 U (10TH RESEARCH INSTITUET OF CETC) 07 August 2013 (2013-08-07) description, paragraphs [0004]-[0019], figures 1-6	1-14
A	US 2016111764 A1 (HYUNDAI MOBIS CO., LTD.) 21 April 2016 (2016-04-21) the whole document	1-14
A	EP 1367668 A1 (SIEMENS INFORMATION AND COMMUNICATION NETWORKS S.P.A.) 03 December 2003 (2003-12-03) the whole document	1-14
A	CN 101847769 A (TOKO, INC.) 29 September 2010 (2010-09-29) the whole document	1-14
A	JP 2006345340 A (TOKO, INC.) 21 December 2006 (2006-12-21) the whole document	1-14
A	KR 100907271 B1 (SAMSUNG THALES CO., LTD.) 13 July 2009 (2009-07-13) the whole document	1-14

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 June 2017	**12 July 2017**

Name and mailing address of the ISA/CN	Authorized officer
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Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)61648476**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/081886

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	203119074	U	07 August 2013	None			
US	2016111764	A1	21 April 2016	KR	20160044873	A	26 April 2016
				CN	105680135	A	15 June 2016
				US	9450281	B2	20 September 2016
				KR	101621480	B1	16 May 2016
EP	1367668	A1	03 December 2003	None			
CN	101847769	A	29 September 2010	JP	2010141644	A	24 June 2010
				US	2010148891	A1	17 June 2010
				EP	2197072	B1	10 August 2011
				JP	5123154	B2	16 January 2013
				CN	101847769	B	09 July 2014
				EP	2197072	A1	16 June 2010
				US	8368482	B2	05 February 2013
				AT	520166	T	15 August 2011
JP	2006345340	A	21 December 2006	JP	4384620	B2	16 December 2009
KR	100907271	B1	13 July 2009	None			