



(51) International Patent Classification:

G02B 6/28 (2006.01) G02B 6/27 (2006.01)
G02B 6/122 (2006.01) G02B 6/30 (2006.01)

(21) International Application Number:

PCT/US2016/040795

(22) International Filing Date:

01 July 2016 (01.07.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventor: FESHALI, Avinash; 2755 South Barrington Ave., Los Angeles, California 90064 (US).

(74) Agent: RICHARDS, Edwin E. et al.; Trop, Pruner & Hu, P.C., 1616 S. Voss Rd., Ste. 750, Houston, Texas 77057-2631 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA,

LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

- with international search report (Art. 21(3))

(54) Title: ISOTROPIC ETCHED LENS FOR VERTICAL COUPLING OF PHOTONICS CIRCUITS

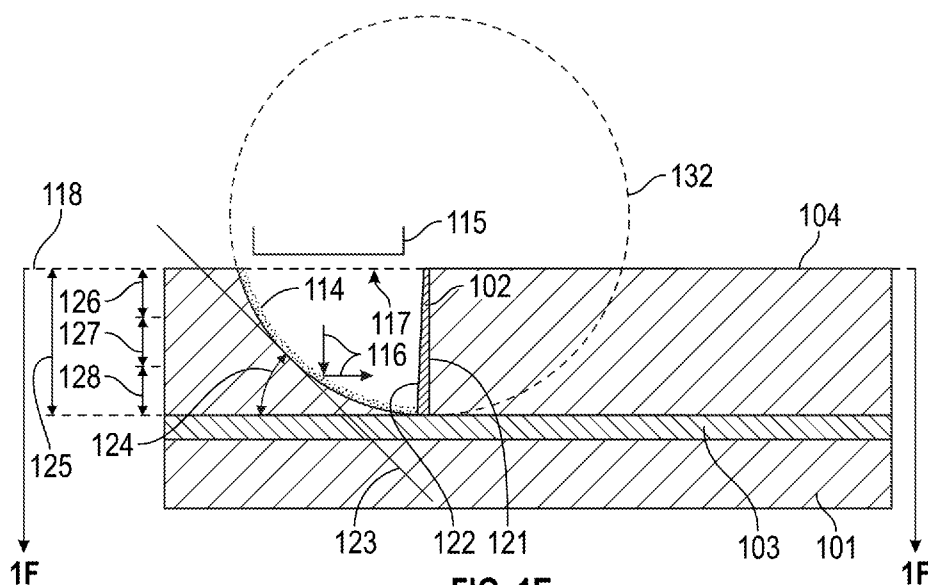
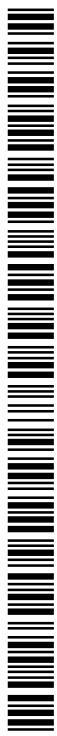


FIG. 1E

(57) Abstract: An embodiment includes an apparatus comprising: a silicon layer that includes a concave surface; an aluminum layer on the surface; and a waveguide coupled to the surface; wherein (a) the surface is curved and concave in both vertical and horizontal planes that intersect the surface, and (b) the surface has a horizontal and vertical radii of curvature (ROC) substantially equal to each other. Other embodiments are described herein.



Isotropic Etched Lens for Vertical Coupling of Photonics Circuits

Technical Field

[0001] Embodiments of the invention relate to optical couplers. More particularly, embodiments of the invention relate to multimode optical coupler interfaces for interfacing, for example, optical fibers and photonic integrated circuits.

Background

[0002] As described in U.S. Patent No. 8,488,923 (assigned to Intel Corp., Santa Clara, CA, USA), photonic based systems comprise various components including waveguides, modulators, optic sources, and optic couplers. An optical waveguide is a structure that conveys an optical light signal from an optic source (e.g., laser diode). Conventionally, an optical waveguide may include a substrate and a core encased within an upper and lower cladding. The bulk of the light signal typically travels within the core along the axis of the waveguide structure. Optical waveguides may be used in optical modulators, such as phase modulators, absorption modulators, and Mach-Zehnder Modulators (MZM). An optical modulator may be optically coupled to an external optical device (using an optical coupler), such as an optical fiber or photodetector. An optical modulator is a device which is used to modulate a beam of light. Depending on the parameter of a light beam which is manipulated, modulators may be categorized into amplitude modulators, phase modulators, polarization modulators, and the like.

[0003] As mentioned above, optical couplers couple light from, for example, a fiber to a waveguide. However, performing such coupling with high efficiency (e.g., low loss of data included in the light communication) is difficult and a challenge for those involved in the development of integrated photonics.

Brief Description of the Drawings

[0004] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures. Where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0005] Figures 1(a)-(f) depict a process for forming a concave mirror coupler in an embodiment.

[0006] Figure 2 includes a process for forming a concave mirror coupler in an embodiment.

[0007] Figures 3(a)-(b) depict a process for forming a concave mirror coupler in an embodiment.

[0008] Figure 4 includes an embodiment of a concave mirror coupler.

[0009] Figure 5 includes an embodiment of a concave mirror coupler.

[0010] Figures 6, 7, 8 include systems that comprise an embodiment of a concave mirror coupler.

Detailed Description

[0011] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of semiconductor/circuit structures. Thus, the actual appearance of the fabricated integrated circuit structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. For example, not every layer of a semiconductor device is necessarily shown. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are in direct physical or electrical contact with each other and "coupled" may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact.

[0012] As referenced above, coupling light efficiently from an integrated photonics chip to a fiber (or vice versa) is difficult. More specifically, while several architectures (e.g., grating couplers and mirrors) have been developed to solve the coupling problem for single mode (SM) or multi-mode (MM) waveguides, vertical coupling of light from a SM or MM fiber into a SM or MM high index waveguide is a complex problem. Conventionally expensive optical/micro-optical structures involving complex fabrication and alignment procedures are required to achieve efficient coupling. For example, ways to couple light into or out of a waveguide include use of a vertical grating coupler and/or 45 degree mirror. These methods are usually very hard to control and involve multiple fabrication steps that are hard and expensive to realize. Such steps include a deep dry etching into silicon substrates, long depositions of oxides, and polishing. For example, such conventional systems include a 45 degree mirror dry etched in silicon, then covered with oxide, and finally filled with 30 μm of poly silicon deposition and polish.

[0013] However, embodiments provide a solution that is simple to fabricate and integrate into known processes (e.g., high volume CMOS manufacturing). An embodiment includes a coupler having a concave mirror formed using an isotropic etch fabrication process. The fabrication process is controlled based on dimensions of the hard mask and/or the etch chemistry used to perform the etch. Further, “self-stopping” of the etch (i.e., control of the etch) is possible due to the use of anti-reflective (AR) coatings (e.g., coating that include etch stop materials) and/or the insulation layer of the silicon on isolator (SOI) substrate from which the coupler is formed. An embodiment includes a concave mirror that includes a shape similar to a portion of a sphere. Thus, light is directed to a waveguide from various angles (e.g., light received at a portion of the mirror that is collinear with a waveguide as well as portions of the mirror that are not collinear with the waveguide).

[0014] More generally, described herein are embodiments of optical interfaces (sometimes referred to herein as “couplers” or “optical couplers”) that may be employed between optical fibers (e.g., large-core optical fibers) and chip-scale optoelectronic devices (e.g., ring resonators for biosensors, photodetectors, and the like). Photons can be coupled efficiently from one side of the coupler to another side

of the coupler in a fully coherent way. Described herein are couplers that improve the tolerance of misalignment when, for example, a SM or MM fiber is used as a waveguide input or output. This enables the possibility of passive/automatic alignment and therefore reduces the production cost of such optoelectronic bases systems.

[0015] Embodiments may operate with, for example, a waveguide-based Ge (e.g., Ge grown on silicon), SiGe, III-V, or hybrid III-V on silicon semiconductor photodetector. Embodiments of optical couplers may be used for interfacing SM or MM light sources and chip-scale photonic devices. Embodiments have applications including sensors (e.g., biosensors), high performance computing (HPC), coarse wavelength division multiplexing (CWDM), and the like. Embodiments are applicable in equipment employing digital techniques designed to operate at a “total digital transfer rate” exceeding 50 Gbit/s (e.g., via electrical, optical, or wireless transmission). For telecommunication switching equipment the total digital transfer rate is the unidirectional speed of a single interface, measured at the highest speed port or line.

[0016] Figures 1(a)-(d) depict a process for forming a concave mirror coupler in an embodiment. Figure 1(a) includes a SOI substrate including silicon layer 101, insulation layer 103 (e.g., SiO₂), and silicon layer 104. In alternate embodiments, other substrates may be used including layers such as, for example, gallium arsenide (GaAs).

[0017] An AR film (e.g., silicon nitride) 102 serving as etchstop has already been formed within silicon portion 104. The AR film is optional and not included in all embodiments. AR film 102 contacts insulation layer 103. Hardmask 105, having exposure area 106, is on portion 104. Figure 1(b) shows a top view of the device of Figure 1(a). Waveguide 107 is shown coupled to AR layer or film 102. In one embodiment, waveguide 107 is created from silicon but in other embodiments other materials can be used such as, for example, aluminum gallium arsenide (AlGaAs), silicon germanium (Si_xGe_{1-x}), and/or aluminum arsenide (AlAs).

[0018] Figure 1(b) includes concave surface 108, which is formed from silicon layer 104. Surface 104 is formed by way of an isotropic etch. Isotropic etching (e.g., wet etching or chemical etching) removes material from a substrate via a chemical process using an etchant substance. The etchant may be a corrosive liquid or a chemically active ionized gas, known as a plasma. Unlike dry etching, isotropic etching does not etch in a single direction, but rather etches horizontally as well as vertically into the surface of the substrate. Figure 1(b) leverages this aspect of isotropic etching to form the smooth spherical surface 108.

[0019] Surface 108 is curved and concave in both vertical and horizontal planes that intersect the surface. For example, such a vertical plane is the X-Y plane shown in Figure 1(c) and such a horizontal plane is the X-Z plane shown in Figure 1(d). Surface 108 has a horizontal radius of curvature (ROC) 113 (Figure 1(d)) and a vertical ROC 112 (Figure 1(c)) substantially equal to each other. The ROC, as used herein, is the radius of the circle formed with the curved part of the lens or mirror (i.e., surface 108 in the X-Y and X-Z planes). Figure 1(d) is a top view of the device of Figure 1(c). More specifically, when a circle is drawn with the help of the curved part of the lens, and the circle's center is located, then the ROC is obtained by measuring the radius of the circle.

[0020] Figure 1(e) includes a deposited or sputtered aluminum layer by chemical vapor deposition or atomic layer deposition 114 on surface 108. Figure 1(f) is a top view of the device of Figure 1(e). The optical coupler couples light 116 from optic fiber 115 to waveguide 107. Waveguide 107 may be any of various types of waveguides including, but not limited to, circular optical fibers, buried channel waveguides, strip-loaded waveguides, ridge waveguides, rib waveguides, diffused waveguides, arrayed waveguides, and the like.

[0021] In one embodiment, the input/output port 117 is designed to interface a MM fiber such that port 117 has adequate cross-section area (e.g., about $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$) to interface such a fiber. However, in other embodiments port 117 is configured to interface a smaller SM fiber. A SM fiber may be, for example, 9/125 in construction meaning the core to cladding diameter ratio is 9 microns to 125 microns. A MM fiber may have, for example, a larger diameter core (compared to

SM fiber) that allows multiple modes of light to propagate. The MM fiber may have between 50/125 and 62.5/125 in construction meaning that the core to cladding diameter ratio is between 50 microns to 125 microns and 62.5 microns to 125 microns.

[0022] In an embodiment, surface 108 includes at least a portion of a spherical zone having at least one base. A spherical zone is that portion of the surface of a sphere included between two parallel planes. The bases of the zone are the circumference of the sections made by the two parallel planes. The altitude of the zone is the perpendicular distance between these two parallel planes. If one of the bounding parallel planes is tangent to the sphere, the surface bounded is a zone of one base. Figure 1(e) illustrates a sphere 132 with a zone of one base defined by plane 118.

[0023] Figure 4 includes an embodiment of a concave mirror surface 408 (as seen from perspective of the waveguide looking towards the surface 408). Like Figure 1(e), shown is a sphere with a zone of one base defined by plane 418. Bottom area 429 of surface 408 generally maintains the same ROC as middle portion 430 of surface 408. In contrast, Figure 5 includes a spherical zone with two bases defined by planes 518, 519. Plane 519 occurs as a result of the etch interfacing the insulative layer of the SOI substrate. The etching may stop due to a hydrogen implant region near the silicon layer 504, oxide layer 503 or may stop simply due to the oxide layer 503. In Figure 5 a bottom portion 520 of the surface 508 directly contacts insulation layer 503 of the SOI substrate.

[0024] In an embodiment, Figure 1(e) shows a situation where surface 108 directly contacts AR layer 102. Thus, an embodiment provides two bounds for etching—layer 102 and layer 103. Further, etch chemistry and time also helps dictate the shape of surface 108. The AR layer 102 is between the surface 408 and the waveguide 107 in the embodiment of Figure 1(e). In the same embodiment, the AR layer 102 includes a sidewall 121 that is generally orthogonal to the insulation layer (e.g., between 85 and 95 degrees with regard to a long axis of substrate layer 103). In an embodiment, AR layer 102 includes a nitride (but may include an oxide or carbide in other embodiments). Notably, sidewall 122 is thicker as it approaches

insulative layer 103 due to the longer etch time experienced by the upper portion 111 of wall 122 (versus the thicker lower portion 110 of wall 122). In an embodiment, AR 102 is composed of silicon nitride and may be a single layer or multi-layer AR coating. The AR coating may be used to improve coupling by reducing reflection from the surface. It may also be used to couple light into and/or out of the waveguide.

[0025] In an embodiment, as shown in Figure 1(e), a tangent plane 123 to surface 108 intersects insulation layer 103 at an angle 124 between 40 and 50 degrees (e.g., 40, 42, 44, 45, 47, 49 degrees). Such an angle promotes direction of light 116 into waveguide 107. A tangent plane to a spherical surface at a given point is the plane that "just touches" the surface at that point. In an embodiment, the tangent plane 123 intersects surface 108 about midway up the height 125 of layer 104. For example, height 125 may be divided into thirds 126, 127, 128 and tangent plane 123 intersects surface 108 within third 128. In other words, silicon layer 104 includes a height 125 and the tangent plane 123 intersects the surface 108 generally within a middle third 127 of the height 125. Doing so helps prevent signal loss.

[0026] Figure 1(e) illustrates an embodiment where surface 108 is configured to join optic fiber 115 to waveguide 107 such that the fiber 115 is generally orthogonal to the waveguide 107.

[0027] In an embodiment, waveguide 107 is a MM waveguide but may be a SM waveguide in other embodiments. An embodiment includes a system comprising the concave mirror surface along with a waveguide, laser, modulator formed together as a single system.

[0028] Figures 3(a) and 3(b) illustrate how a hardmask 305 may be fashioned with an exposure 306 that will avoid exposing the AR layer/coating 302 yet still provide an isotropic etch the opportunity to recess etch beneath mask portion 331 to form port 417, surface 408, and aluminum surface 414.

[0029] Various embodiments include a semiconductive substrate. Such a substrate may be a bulk semiconductive material that is part of a wafer. In an embodiment, the semiconductive substrate is a bulk semiconductive material as part of a chip that has

been singulated from a wafer. In an embodiment, the semiconductive substrate is a semiconductive material on an insulator such as the aforementioned SOI substrate.

[0030] Figure 2 includes a process 600 for forming a concave mirror coupler in an embodiment. Block 601 includes forming a generally vertical etchstop layer in a silicon layer of a SOI substrate; and block 602 includes performing an isotropic etch on the silicon layer to form a concave surface having a bottom surface adjacent the etchstop layer and an insulation layer of the SOI substrate.

[0031] Referring now to Figure 6, shown is a block diagram of an example system with which embodiments can be used. As seen, system 900 may be a smartphone or other wireless communicator or any other Internet of Things (IoT) device. A baseband processor 905 is configured to perform various signal processing with regard to communication signals to be transmitted from or received by the system. In turn, baseband processor 905 is coupled to an application processor 910, which may be a main CPU of the system to execute an OS and other system software, in addition to user applications such as many well-known social media and multimedia apps. Application processor 910 may further be configured to perform a variety of other computing operations for the device.

[0032] In turn, application processor 910 can couple to a user interface/display 920 (e.g., touch screen display). In addition, application processor 910 may couple to a memory system including a non-volatile memory, namely a flash memory 930 and a system memory, namely a DRAM 935. In some embodiments, flash memory 930 may include a secure portion 932 in which secrets and other sensitive information may be stored. As further seen, application processor 910 also couples to a capture device 945 such as one or more image capture devices that can record video and/or still images.

[0033] A universal integrated circuit card (UICC) 940 comprises a subscriber identity module, which in some embodiments includes a secure storage 942 to store secure user information. System 900 may further include a security processor 950 (e.g., Trusted Platform Module (TPM)) that may couple to application processor 910. A plurality of sensors 925, including one or more multi-axis accelerometers may

couple to application processor 910 to enable input of a variety of sensed information such as motion and other environmental information. Such sensors may include one of the aforementioned embodiments of concave mirror surfaces and waveguide systems. In addition, one or more authentication devices 995 may be used to receive, for example, user biometric input for use in authentication operations.

[0034] As further illustrated, a near field communication (NFC) contactless interface 960 is provided that communicates in a NFC near field via an NFC antenna 965. While separate antennae are shown, understand that in some implementations one antenna or a different set of antennae may be provided to enable various wireless functionalities.

[0035] A power management integrated circuit (PMIC) 915 couples to application processor 910 to perform platform level power management. To this end, PMIC 915 may issue power management requests to application processor 910 to enter certain low power states as desired. Furthermore, based on platform constraints, PMIC 915 may also control the power level of other components of system 900.

[0036] To enable communications to be transmitted and received such as in one or more IoT networks, various circuitry may be coupled between baseband processor 905 and an antenna 990. Specifically, a radio frequency (RF) transceiver 970 and a wireless local area network (WLAN) transceiver 975 may be present. In general, RF transceiver 970 may be used to receive and transmit wireless data and calls according to a given wireless communication protocol such as 3G or 4G wireless communication protocol such as in accordance with a code division multiple access (CDMA), global system for mobile communication (GSM), long term evolution (LTE) or other protocol. In addition a GPS sensor 980 may be present, with location information being provided to security processor 950 for use as described herein when context information is to be used in a pairing process. Other wireless communications such as receipt or transmission of radio signals (e.g., AM/FM) and other signals may also be provided. In addition, via WLAN transceiver 975, local wireless communications, such as according to a Bluetooth™ or IEEE 802.11 standard can also be realized.

[0037] Referring now to Figure 7, shown is a block diagram of a system in accordance with another embodiment of the present invention. Multiprocessor system 1000 is a point-to-point interconnect system such as a server system, and includes a first processor 1070 and a second processor 1080 coupled via a point-to-point interconnect 1050 (which may include embodiments of optics systems with concave surfaces and waveguides described herein). Each of processors 1070 and 1080 may be multicore processors such as SoCs, including first and second processor cores (i.e., processor cores 1074a and 1074b and processor cores 1084a and 1084b), although potentially many more cores may be present in the processors. In addition, processors 1070 and 1080 each may include a secure engine 1075 and 1085 to perform security operations such as attestations, IoT network onboarding or so forth.

[0038] First processor 1070 further includes a memory controller hub (MCH) 1072 and point-to-point (P-P) interfaces 1076 and 1078. Similarly, second processor 1080 includes a MCH 1082 and P-P interfaces 1086 and 1088. MCH's 1072 and 1082 couple the processors to respective memories, namely a memory 1032 and a memory 1034, which may be portions of main memory (e.g., a DRAM) locally attached to the respective processors. First processor 1070 and second processor 1080 may be coupled to a chipset 1090 via P-P interconnects 1052 and 1054, respectively. Chipset 1090 includes P-P interfaces 1094 and 1098.

[0039] Furthermore, chipset 1090 includes an interface 1092 to couple chipset 1090 with a high performance graphics engine 1038, by a P-P interconnect 1039. In turn, chipset 1090 may be coupled to a first bus 1016 via an interface 1096. Various input/output (I/O) devices 1014 may be coupled to first bus 1016, along with a bus bridge 1018 which couples first bus 1016 to a second bus 1020. Various devices may be coupled to second bus 1020 including, for example, a keyboard/mouse 1022, communication devices 1026 and a data storage unit 1028 such as a non-volatile storage or other mass storage device. As seen, data storage unit 1028 may include code 1030, in one embodiment. As further seen, data storage unit 1028 also includes a trusted storage 1029 to store sensitive information to be protected. Further, an audio I/O 1024 may be coupled to second bus 1020.

[0040] Embodiments may be used in environments where IoT devices may include wearable devices or other small form factor IoT devices. Referring now to Figure 8, shown is a block diagram of a wearable module 1300 in accordance with another embodiment. In one particular implementation, module 1300 may be an Intel® Curie™ module that includes multiple components adapted within a single small module that can be implemented as all or part of a wearable device. As seen, module 1300 includes a core 1310 (of course in other embodiments more than one core may be present). Such core may be a relatively low complexity in-order core, such as based on an Intel Architecture® Quark™ design. In some embodiments, core 1310 may implement a TEE as described herein. Core 1310 couples to various components including a sensor hub 1320, which may be configured to interact with a plurality of sensors 1380, such as one or more biometric, motion environmental or other sensors. Such sensors may include one of the aforementioned embodiments of concave mirror surfaces and waveguide systems. A power delivery circuit 1330 is present, along with a non-volatile storage 1340. In an embodiment, this circuit may include a rechargeable battery and a recharging circuit, which may in one embodiment receive charging power wirelessly. One or more input/output (IO) interfaces 1350, such as one or more interfaces compatible with one or more of USB/SPI/I2C/GPIO protocols, may be present. In addition, a wireless transceiver 1390, which may be a Bluetooth™ low energy or other short-range wireless transceiver is present to enable wireless communications as described herein. Understand that in different implementations a wearable module can take many other forms. Wearable and/or IoT devices have, in comparison with a typical general purpose CPU or a GPU, a small form factor, low power requirements, limited instruction sets, relatively slow computation throughput, or any of the above.

[0041] The following examples pertain to further embodiments.

[0042] Example 1 includes an apparatus comprising: a silicon layer that includes a concave surface; an aluminum layer on the surface; and a waveguide coupled to the surface; wherein (a) the surface is curved and concave in both vertical and horizontal planes that intersect the surface, and (b) the surface has a horizontal and vertical radii of curvature (ROC) substantially equal to each other.

[0043] The terms “reflective surface”, “mirror”, and “lens” are used interchangeably herein to connote a surface that reflects light from one angle (incident angle) to another angle.

[0044] Also, in an embodiment the waveguide and the concave surface are each formed in the same monolithic layer (e.g., layer 104 of the SOI substrate of Figure 1(e)). However, in other embodiments the waveguide and the concave surface are each formed in different monolithic layers that are later coupled to one another.

[0045] In an embodiment the waveguide and the concave surface and a frontend including transistors are all formed in the same monolithic layer (e.g., layer 104 of the SOI substrate of Figure 1(e)). Thus, for an optoelectronic chip circuitry (e.g., transistors such as Fin-FETs) may be formed in the same semiconductor layer as the concave surface and/or waveguide.

[0046] Example 2 includes the apparatus of example 1, wherein the surface is isotropically etched.

[0047] Example 3 includes the apparatus of example 1, wherein the silicon layer is included in a silicon on insulator (SOI) substrate.

[0048] Example 4 includes the apparatus of example 3, wherein the surface includes at least a portion of a spherical zone having at least one base.

[0049] Example 5 includes the apparatus of example 4, wherein the spherical zone has two bases.

[0050] Example 6 includes the apparatus of example 3, wherein a bottom portion of the surface directly contacts an insulation layer of the SOI substrate.

[0051] Example 7 includes the apparatus of example 6 wherein the surface directly contacts an antireflective (AR) layer.

[0052] Example 8 includes the apparatus of example 7 wherein the AR layer is between the surface and the waveguide.

[0053] Example 9 includes the apparatus of example 8 wherein the AR layer includes a sidewall that is generally orthogonal to the insulation layer.

[0054] For instance, the sidewall is 90 degrees (+/- 5 degrees) to the insulation layer.

[0055] Another version of example 9 includes the apparatus of example 8 wherein the AR layer includes a sidewall that is within 85-95 degrees to the insulation layer.

[0056] Example 10 includes the apparatus of example 9 wherein the AR layer thickens closer to the insulation layer and thins further away from the insulation layer.

[0057] Example 11 includes the apparatus of example 7 wherein the AR layer includes a nitride.

[0058] In various embodiments the AR layer may include a single or multiple layers.

[0059] Example 12 includes the apparatus of example 3 wherein a plane tangent to the surface intersects the insulation layer at an angle between 40 and 50 degrees.

[0060] Example 13 includes the apparatus of example 12, wherein the silicon layer includes a height and the plane intersects the surface generally within a middle third of the height.

[0061] Example 14 includes the apparatus of example 3, wherein the surface is configured to join an optic fiber to waveguide such that the fiber is generally orthogonal to the waveguide.

[0062] Example 15 includes the apparatus of example 3, wherein the waveguide is a multimode waveguide.

[0063] Example 16 includes the apparatus of example 3 comprising a laser and a modulator.

[0064] Another version of Example 16 includes the apparatus of any of examples 1-14, wherein the waveguide is a multimode waveguide and the apparatus includes a laser and a modulator.

[0065] For instance, the apparatus may work with various modulators including, without limitation, Electroabsorption Modulators (EAM), Mach-Zehnder interferometers (MZI), and the like.

[0066] Example 17 includes a method comprising: forming a generally vertical etchstop layer in a silicon layer of a silicon on insulator (SOI) substrate; and performing an isotropic etch on the silicon layer to form a concave surface having a bottom surface adjacent the etchstop layer and an insulation layer of the SOI substrate; wherein (a) a waveguide is coupled to the surface; and (b) the surface is curved and concave in both vertical and horizontal planes that intersect the surface.

[0067] Example 18 includes the method of example 17, wherein the surface has horizontal and vertical radii of curvature (ROC) substantially equal to each other.

[0068] Example 19 includes the method of example 18 comprising performing the isotropic etch on the silicon layer to form the concave surface having the bottom surface directly contacting the etchstop layer and the insulation layer of the SOI substrate.

[0069] Example 20 includes an apparatus comprising: a silicon on insulator (SOI) substrate that includes a concave surface; a waveguide coupled to the surface; wherein (a) the surface is curved and concave in both vertical and horizontal planes that intersect the surface, (b) a bottom portion of the surface directly contacts an insulation layer of the SOI substrate.

[0070] The waveguide coupled to the surface may include, for example, a single waveguide or an array of waveguides (e.g., star coupler).

[0071] Example 21 includes the apparatus of example 20 wherein the surface directly contacts an etchstop layer comprising a nitride.

[0072] Example 22 includes the apparatus of example 21 wherein a plane tangent to the surface intersects the insulation layer at an angle between 40 and 50 degrees.

[0073] Example 23 includes the apparatus of example 22 comprising a laser and a modulator.

[0074] Example 24 includes a system comprising an optic source, a modulator, and the apparatus according to any one of examples 1-15, 20-22.

[0075] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. For example, terms designating relative vertical position refer to a situation where a device side (or active surface) of a substrate or integrated circuit is the "top" surface of that substrate; the substrate may actually be in any orientation so that a "top" side of a substrate may be lower than the "bottom" side in a standard terrestrial frame of reference and still fall within the meaning of the term "top." For example, a "vertical coupler" may be a "horizontal coupler" depending on the orientation of the coupler. The term "on" as used herein (including in the claims) does not indicate that a first layer "on" a second layer is directly on and in immediate contact with the second layer unless such is specifically stated; there may be a third layer or other structure between the first layer and the second layer on the first layer. The embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

- 1 1. An apparatus comprising:
2 a silicon layer that includes a concave surface;
3 an aluminum layer on the surface; and
4 a waveguide coupled to the surface;
5 wherein (a) the surface is curved and concave in both vertical and horizontal
6 planes that intersect the surface, and (b) the surface has horizontal and vertical radii
7 of curvature (ROC) substantially equal to each other.
- 1 2. The apparatus of claim 1, wherein the surface is isotropically etched.
- 1 3. The apparatus of claim 1, wherein the silicon layer is included in a silicon on
2 insulator (SOI) substrate.
- 1 4. The apparatus of claim 3, wherein the surface includes at least a portion of a
2 spherical zone having at least one base.
- 1 5. The apparatus of claim 4, wherein the spherical zone has two bases.
- 1 6. The apparatus of claim 3, wherein a bottom portion of the surface directly
2 contacts an insulation layer of the SOI substrate.
- 1 7. The apparatus of claim 6 wherein the surface directly contacts an
2 antireflective (AR) layer.
- 1 8. The apparatus of claim 7 wherein the AR layer is between the surface and the
2 waveguide.
- 1 9. The apparatus of claim 8 wherein the AR layer includes a sidewall that is
2 generally orthogonal to the insulation layer.

- 1 10. The apparatus of claim 9 wherein the AR layer thickens closer to the
2 insulation layer and thins further away from the insulation layer.
- 1 11. The apparatus of claim 7 wherein the AR layer includes a nitride.
- 1 12. The apparatus of claim 3 wherein a plane tangent to the surface intersects the
2 insulation layer at an angle between 40 and 50 degrees.
- 1 13. The apparatus of claim 12, wherein the silicon layer includes a height and the
2 plane intersects the surface generally within a middle third of the height.
- 1 14. The apparatus of claim 3, wherein the surface is configured to join an optic
2 fiber to waveguide such that the fiber is generally orthogonal to the waveguide.
- 1 15. The apparatus of claim 3, wherein the waveguide is a multimode waveguide.
- 1 16. The apparatus of claim 3 comprising a laser and a modulator.
- 1 17. A method comprising:
2 forming a generally vertical etchstop layer in a silicon layer of a silicon on
3 insulator (SOI) substrate; and
4 performing an isotropic etch on the silicon layer to form a concave surface
5 having a bottom surface adjacent the etchstop layer and an insulation layer of the
6 SOI substrate;
7 wherein (a) a waveguide is coupled to the surface; and (b) the surface is
8 curved and concave in both vertical and horizontal planes that intersect the surface.
- 1 18. The method of claim 17, wherein the surface has horizontal and vertical radii
2 of curvature (ROC) substantially equal to each other.

- 1 19. The method of claim 18 comprising performing the isotropic etch on the silicon
2 layer to form the concave surface having the bottom surface directly contacting the
3 etchstop layer and the insulation layer of the SOI substrate.
- 1 20. An apparatus comprising:
2 a silicon on insulator (SOI) substrate that includes a concave surface;
3 a waveguide coupled to the surface;
4 wherein (a) the surface is curved and concave in both vertical and horizontal
5 planes that intersect the surface, (b) a bottom portion of the surface directly contacts
6 an insulation layer of the SOI substrate.
- 1 21. The apparatus of claim 20 wherein the surface directly contacts an etchstop
2 layer comprising a nitride.
- 1 22. The apparatus of claim 21 wherein a plane tangent to the surface intersects
2 the insulation layer at an angle between 40 and 50 degrees.
- 1 23. A system comprising an optic source, a modulator, and the apparatus
2 according to any one of claims 1-15, 20-22.

1/9

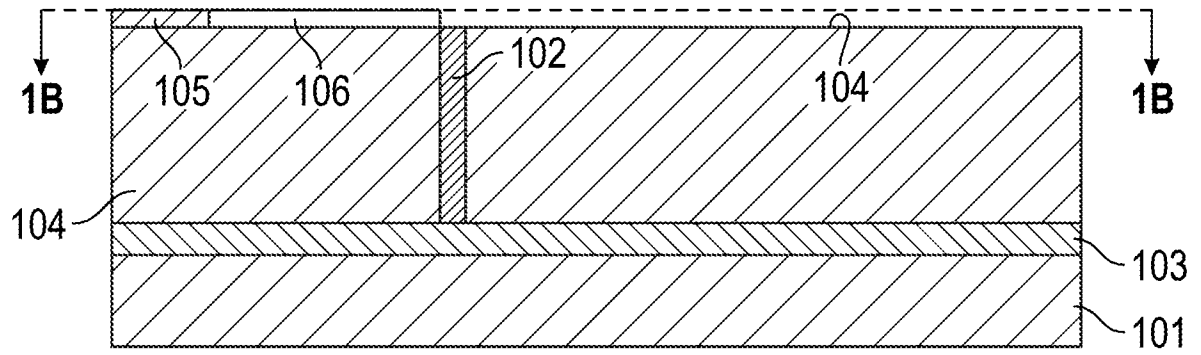


FIG. 1A

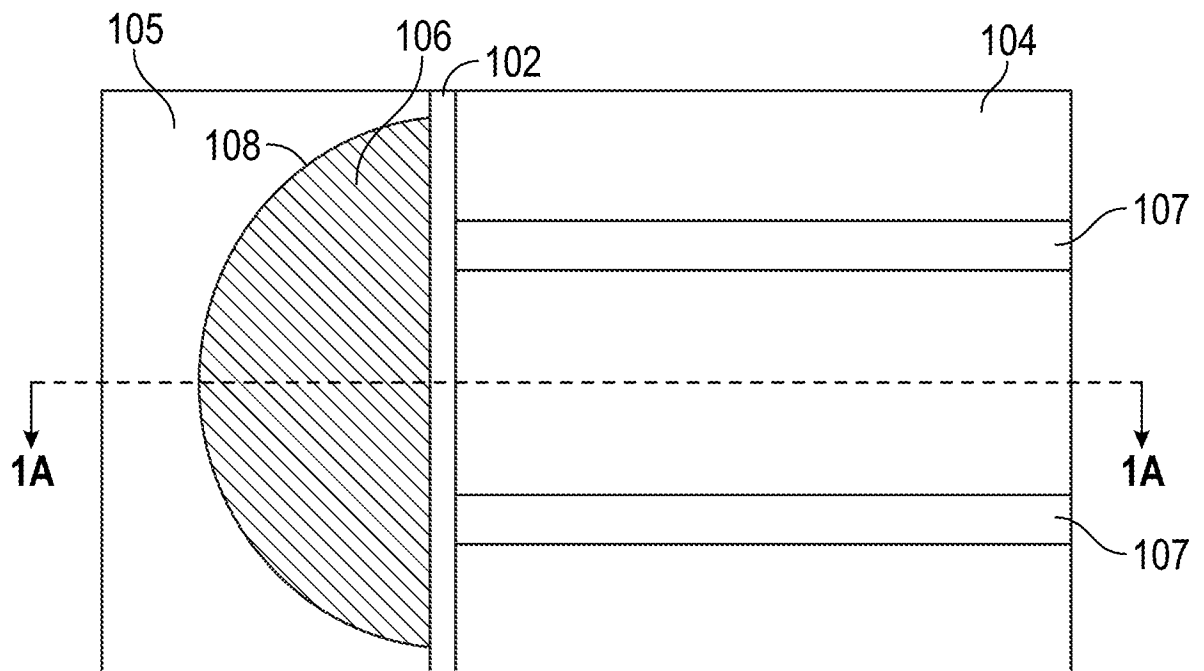


FIG. 1B

2/9

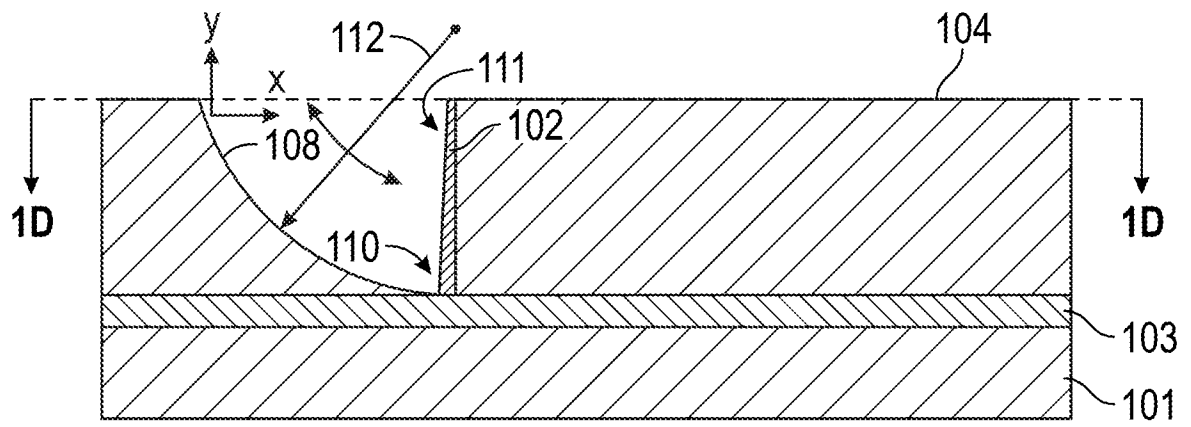


FIG. 1C

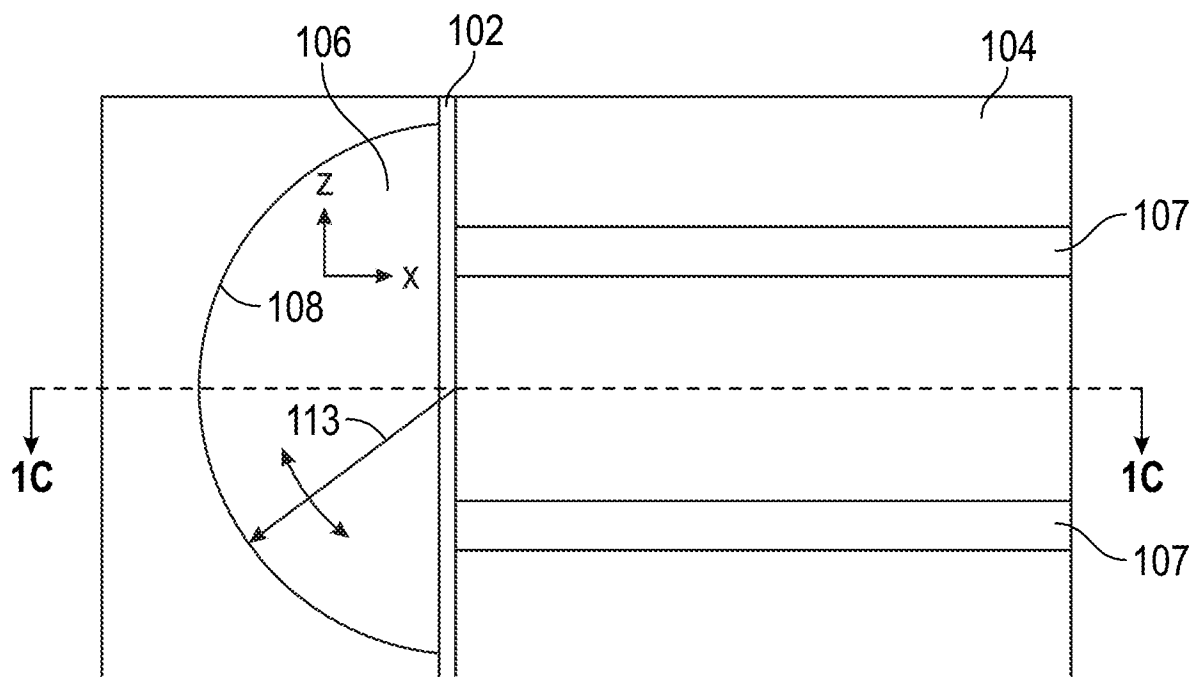


FIG. 1D

3/9

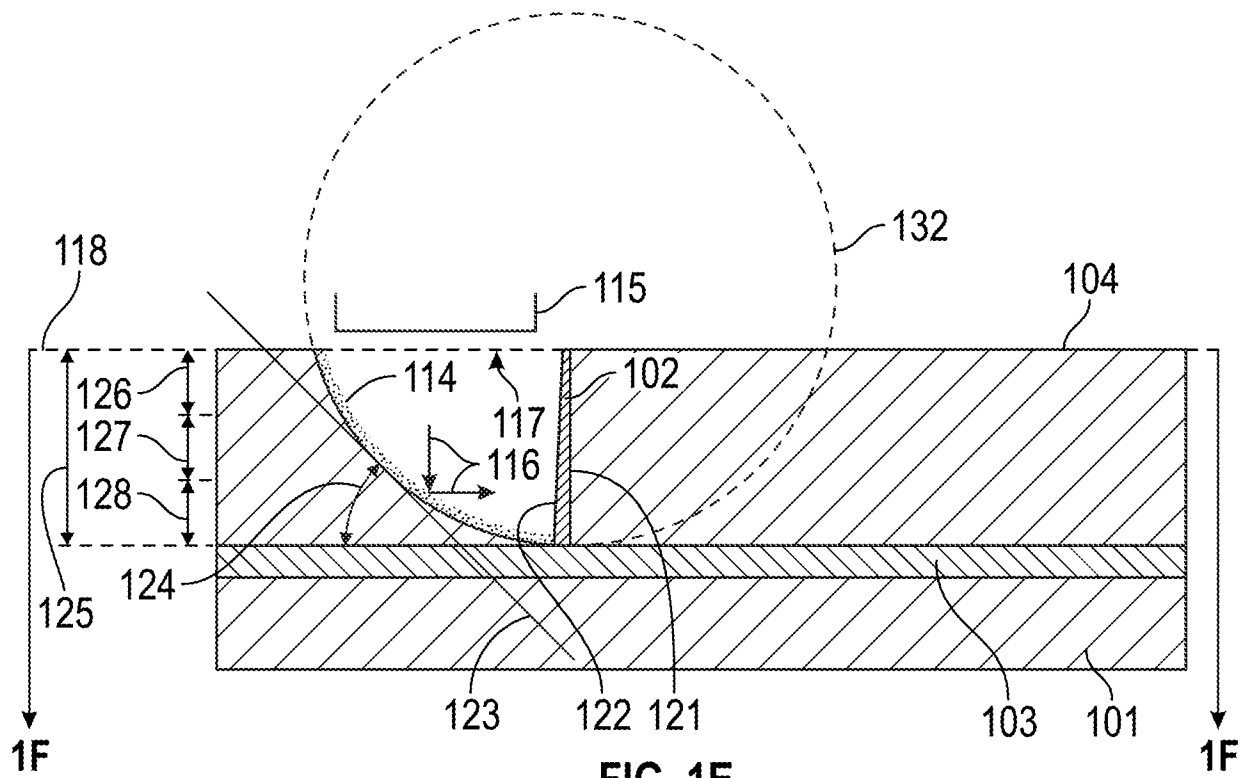


FIG. 1E

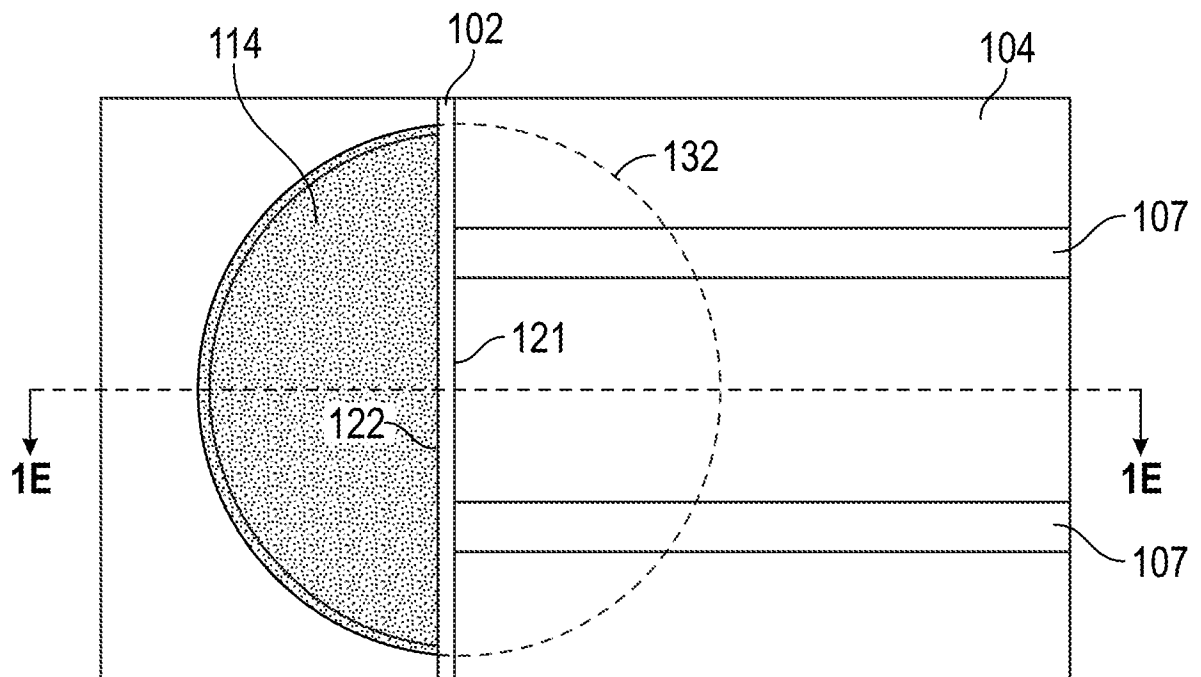


FIG. 1F

600

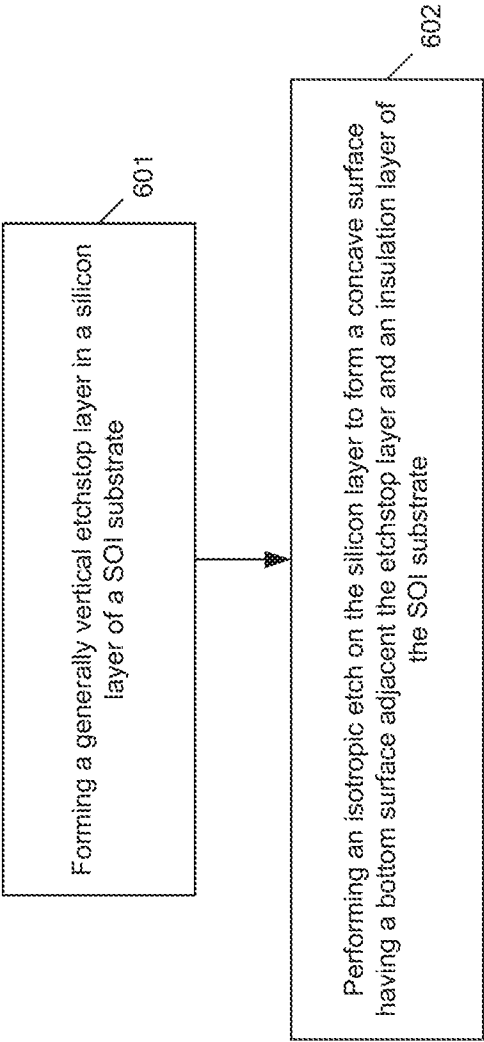


Figure 2

5/9

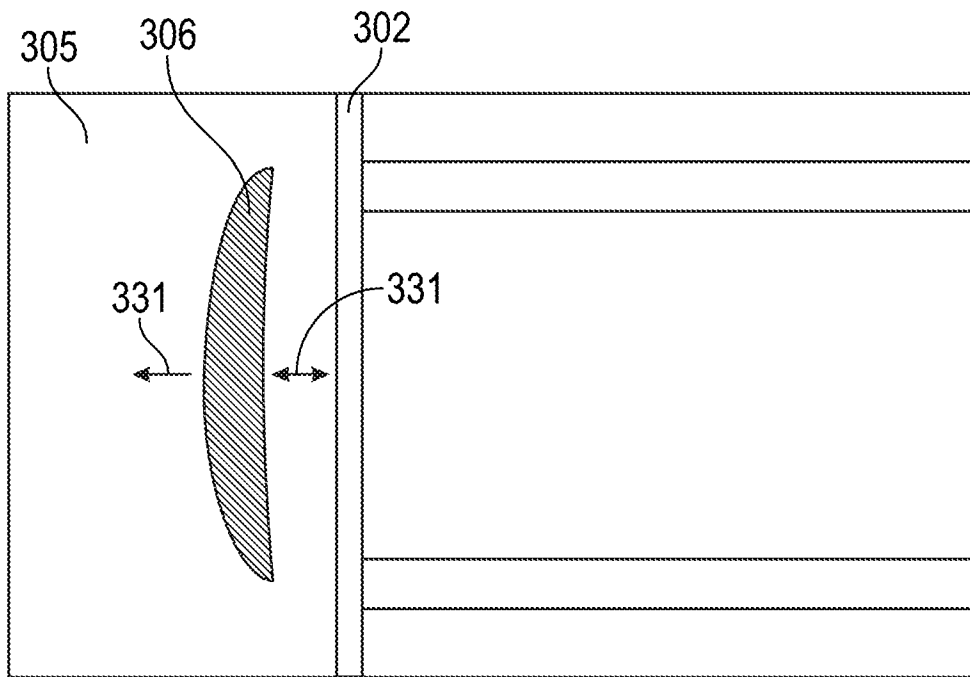


FIG. 3A

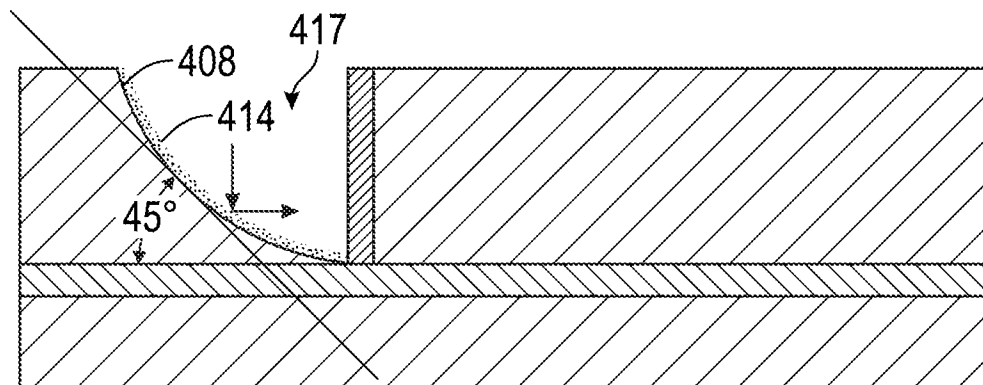


FIG. 3B

6/9

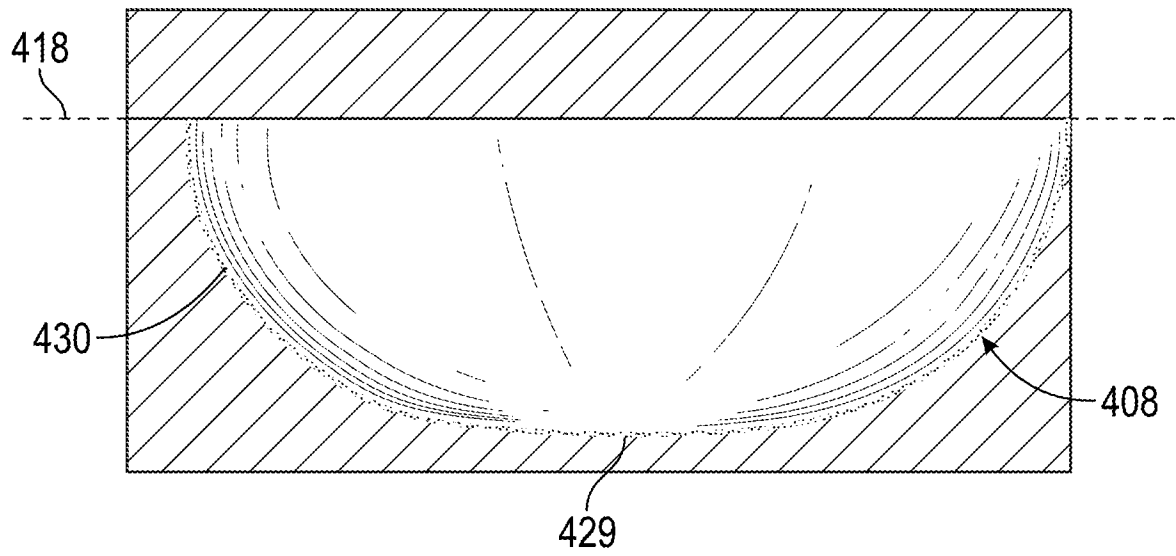


FIG. 4

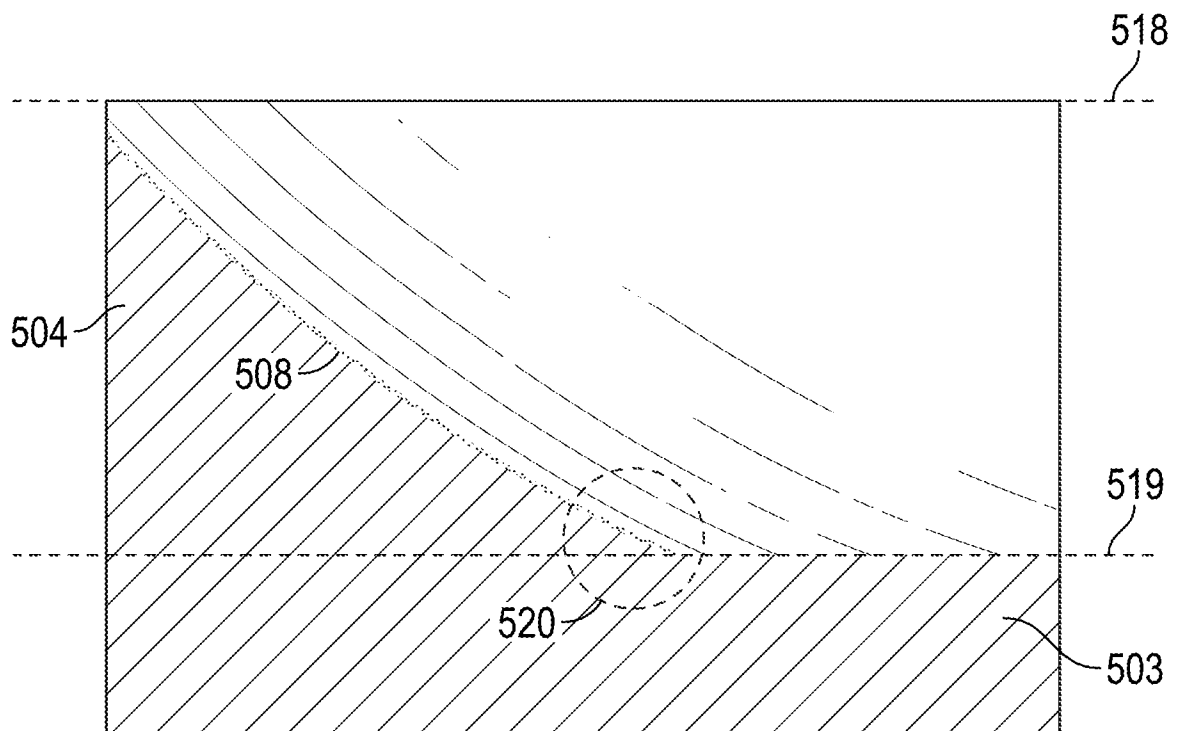


FIG. 5

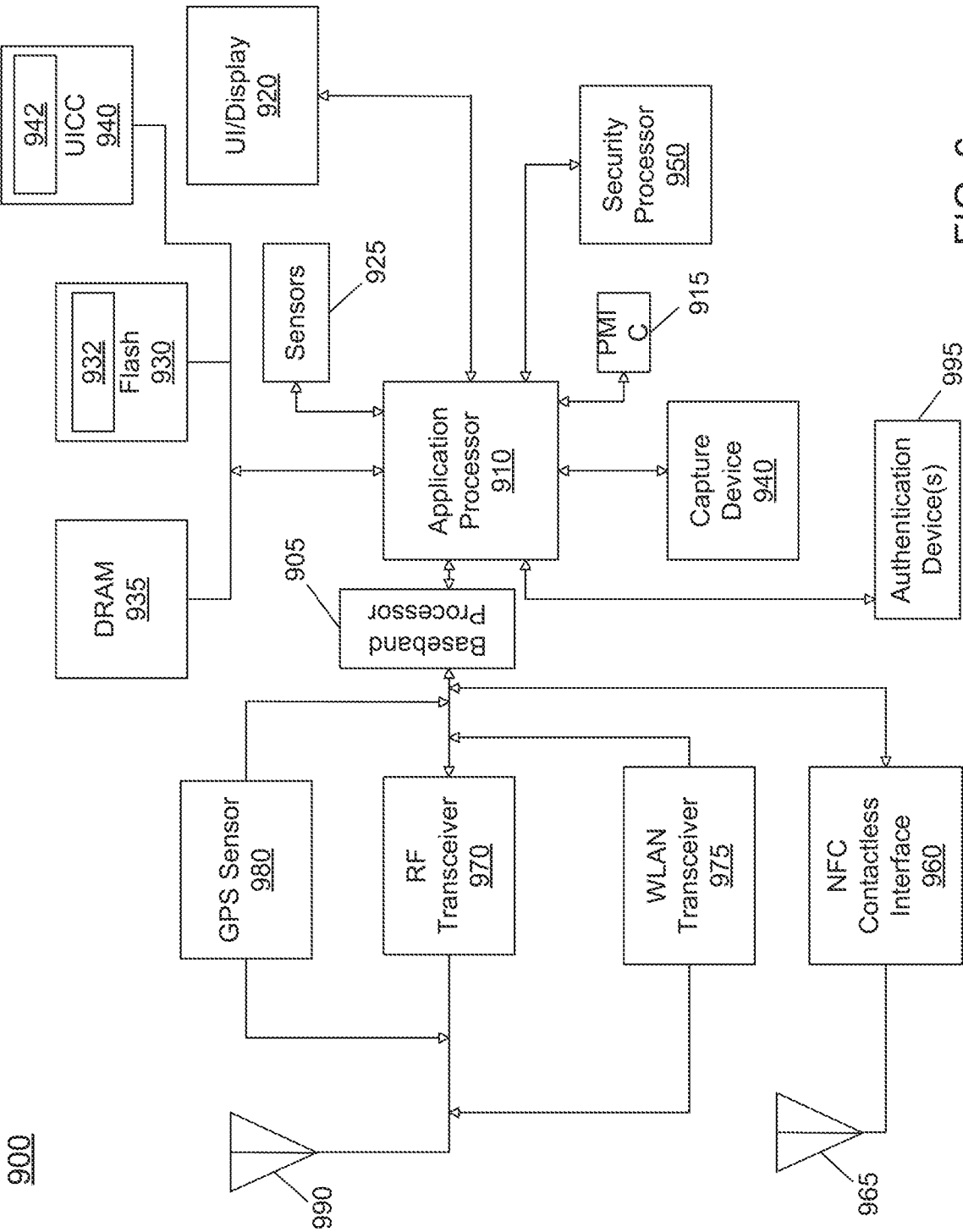


FIG. 6

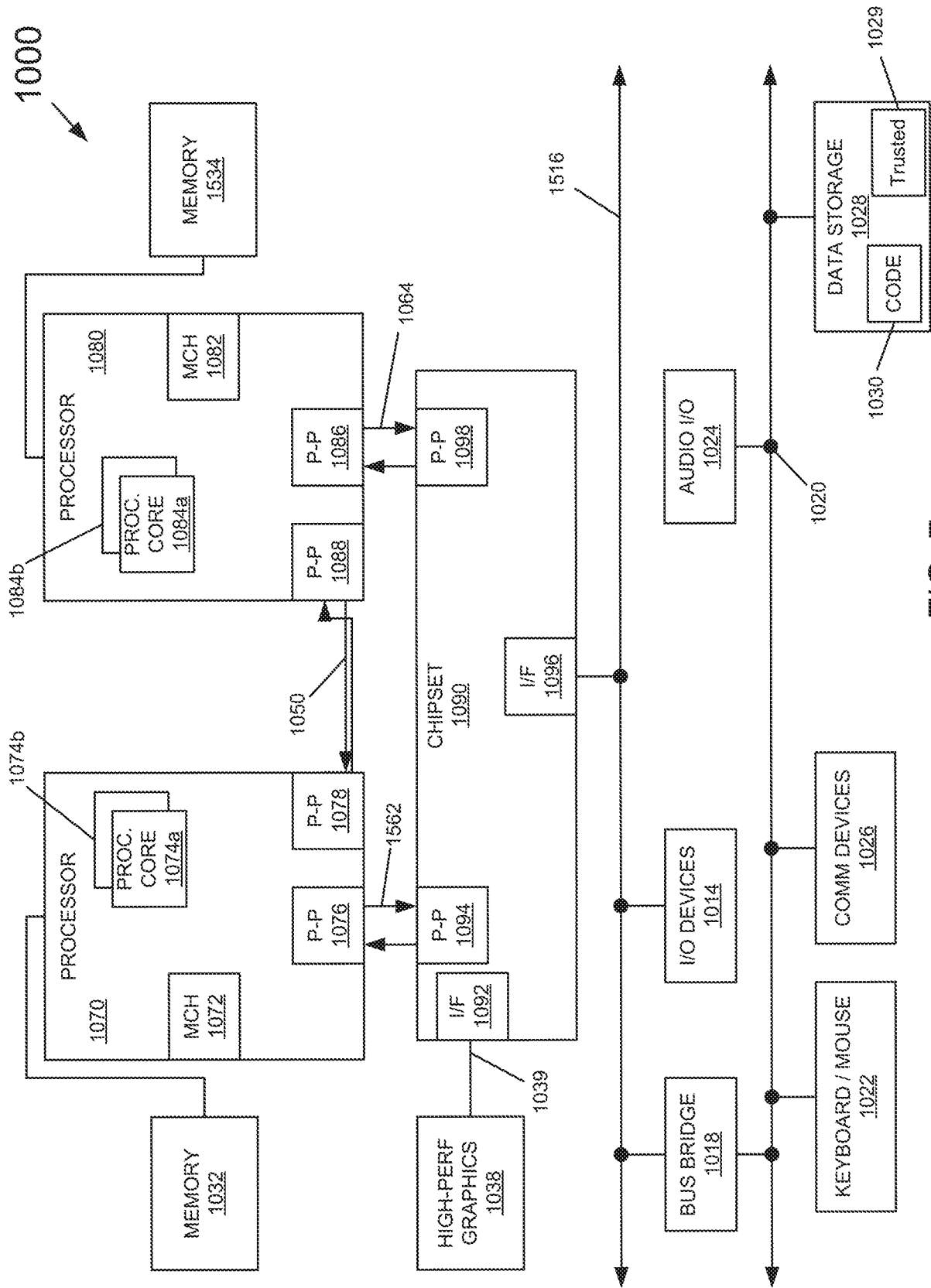


FIG. 7

1300

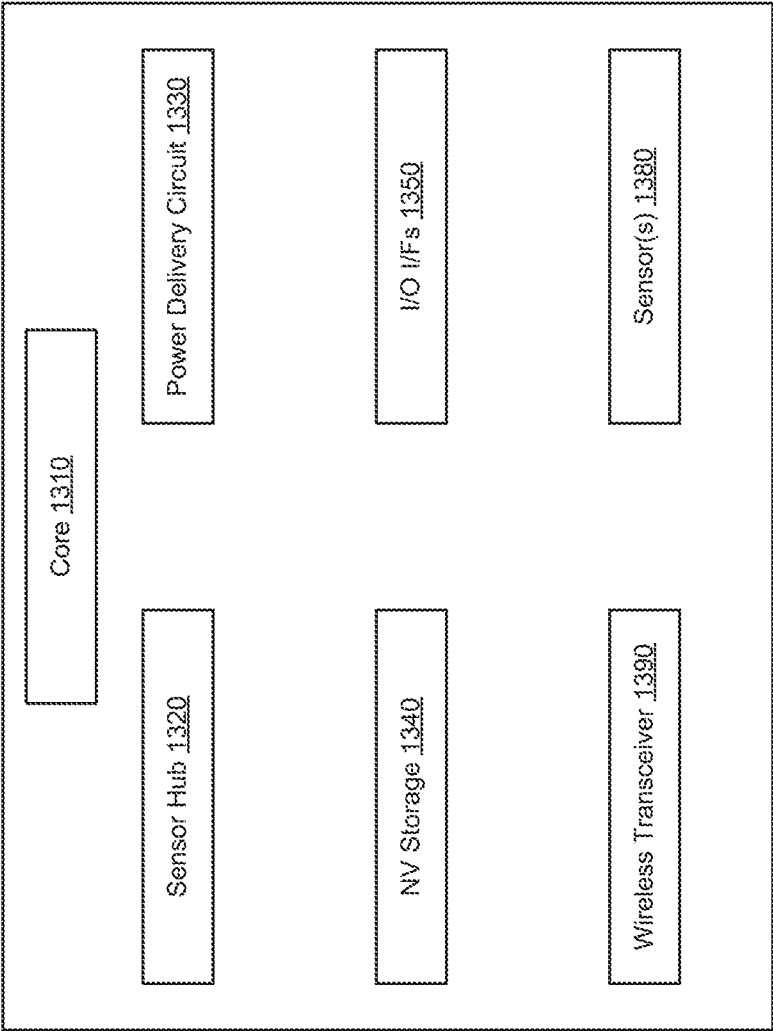


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/040795**A. CLASSIFICATION OF SUBJECT MATTER****G02B 6/28(2006.01)i, G02B 6/122(2006.01)i, G02B 6/27(2006.01)i, G02B 6/30(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02B 6/28; G11B 5/02; G02B 6/293; G02B 6/42; G02B 6/122; G02B 5/30; B29D 11/00; G11B 5/31; G02B 6/13; G02B 6/27; G02B 6/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: optical coupler, waveguide, aluminum layer, concave surface, radius of curvature, silicon on insulator (SOI), etchstop, isotropic etch

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2001-141965 A (CANON INC.) 25 May 2001	1-6, 12-16, 20, 23
A	See paragraphs [0027]-[0028], [0031] and figures 1, 2(c-1), 2(d-1).	7-11, 17-19, 21-22
Y	US 2009-0261488 A1 (SHIMIZU) 22 October 2009	1-6, 12-16, 20, 23
A	See paragraphs [0024], [0037] and figures 1D, 3.	
A	JP 2014-077825 A (FUJITSU LTD.) 01 May 2014	1-23
A	See paragraphs [0016]-[0038] and figures 2-9(B).	
A	JP 2013-004160 A (KONICA MINOLTA ADVANCED LAYERS INC.) 07 January 2013	1-23
A	See paragraphs [0013]-[0021], [0026] and figures 2A-2B.	
A	JP 2007-003782 A (HITACHI CABLE LTD.) 11 January 2007	1-23
A	See paragraphs [0146]-[0147], claim 1 and figures 1(a)-1(b), 7.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

13 January 2017 (13.01.2017)

Date of mailing of the international search report

16 January 2017 (16.01.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KANG, Sung Chul

Telephone No. +82-42-481-8405



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040795

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2001-141965 A	25/05/2001	None	
US 2009-0261488 A1	22/10/2009	CN 101561532 A	21/10/2009
		CN 101561532 B	28/08/2013
		EP 2136228 A1	23/12/2009
		EP 2136228 B1	10/09/2014
		JP 2009-258417 A	05/11/2009
		JP 5160941 B2	13/03/2013
		KR 10-1558584 B1	07/10/2015
		KR 10-2009-0110225 A	21/10/2009
JP 2014-077825 A	01/05/2014	JP 5907035 B2	20/04/2016
JP 2013-004160 A	07/01/2013	None	
JP 2007-003782 A	11/01/2007	JP 4330560 B2	16/09/2009