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[54] **X-RAY SCAN AREA MAPPING SYSTEM**

[75] Inventors: **Morris W. Barnhart**, Buffalo Grove, Ill.; **John C. Russ**, Raleigh, N.C.

[73] Assignee: **Edax International, Inc.**, Prairie View, Ill.

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[52] **U.S. Cl.** **250/306**, 250/310

[51] **Int. Cl.** **H01j 37/26**

[58] **Field of Search** 250/306, 307, 309, 310

[56] **References Cited**

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Primary Examiner—Archie R. Borchelt
Assistant Examiner—C. E. Church
Attorney, Agent, or Firm—James M. Wetzel

[57] **ABSTRACT**

An X-ray scan area mapping system for a scanning electron microscope provides a spacial area map display of X-ray events emitted from a specimen within at least one energy range as the specimen is scanned at scanning electron microscope rates by an electron beam. A background X-ray noise reduction circuit enables intensification of the scanning electron microscope cathode-ray tube display upon the occurrence of an X-ray event within the energy range and disables intensification when the time between consecutive X-ray events within the energy range exceeds a predetermined time period. Background X-ray events occur at much slower rates than the X-ray events emitted from the specimen within the energy range, and therefor, a substantial reduction in background noise on the scanning electron microscope display is obtained.

11 Claims, 3 Drawing Figures

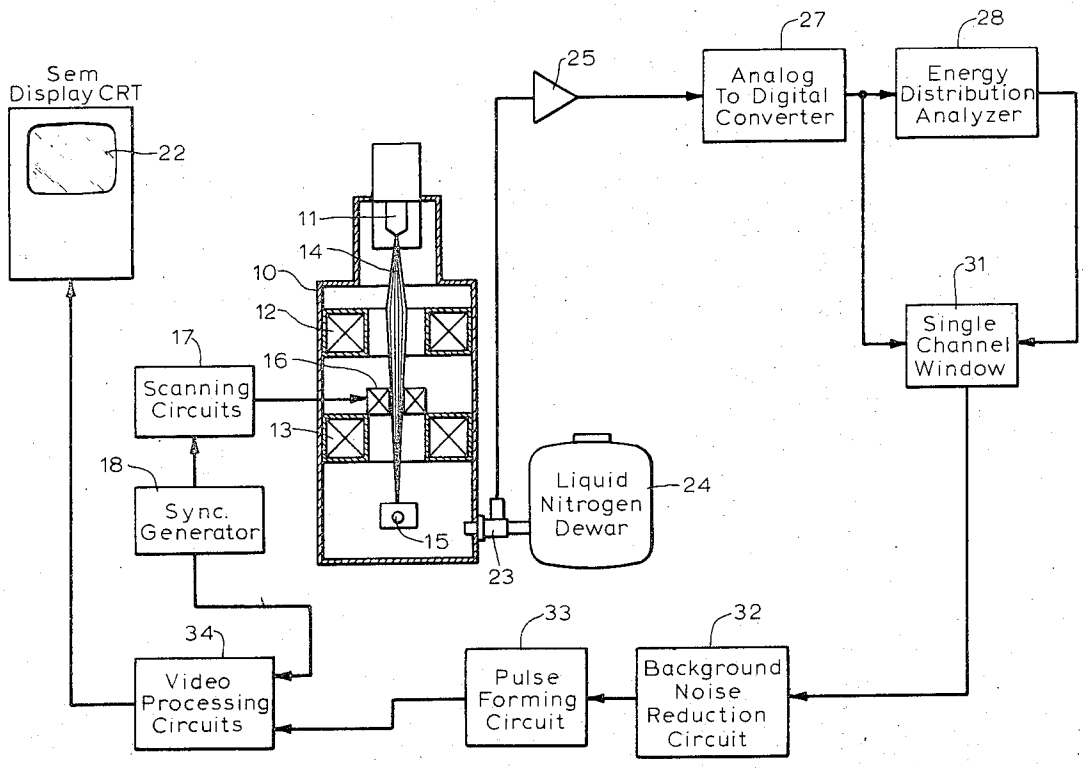


FIG. 1

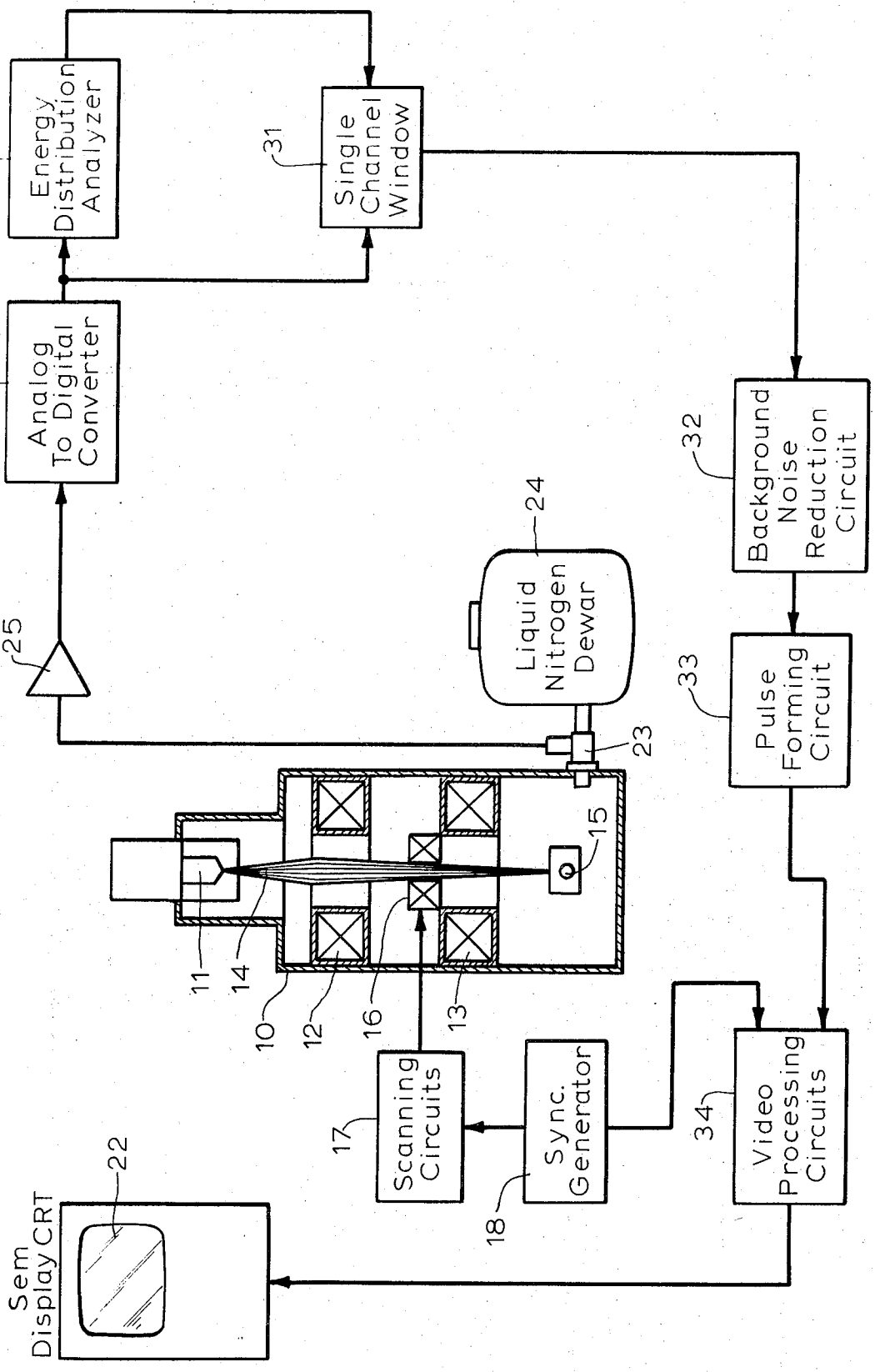

Energy Distribution Analyzer
28
Single Channel Window
31
Analog To Digital Converter
27
Background Noise Reduction Circuit
32
Liquid Nitrogen Dewar
24
25
Pulse Forming Circuit
33
23
15
11
14
10
12
16
13
Scanning Circuits
17
Sync. Generator
18
Video Processing Circuits
34
Sem Display CRT
22

FIG. 2

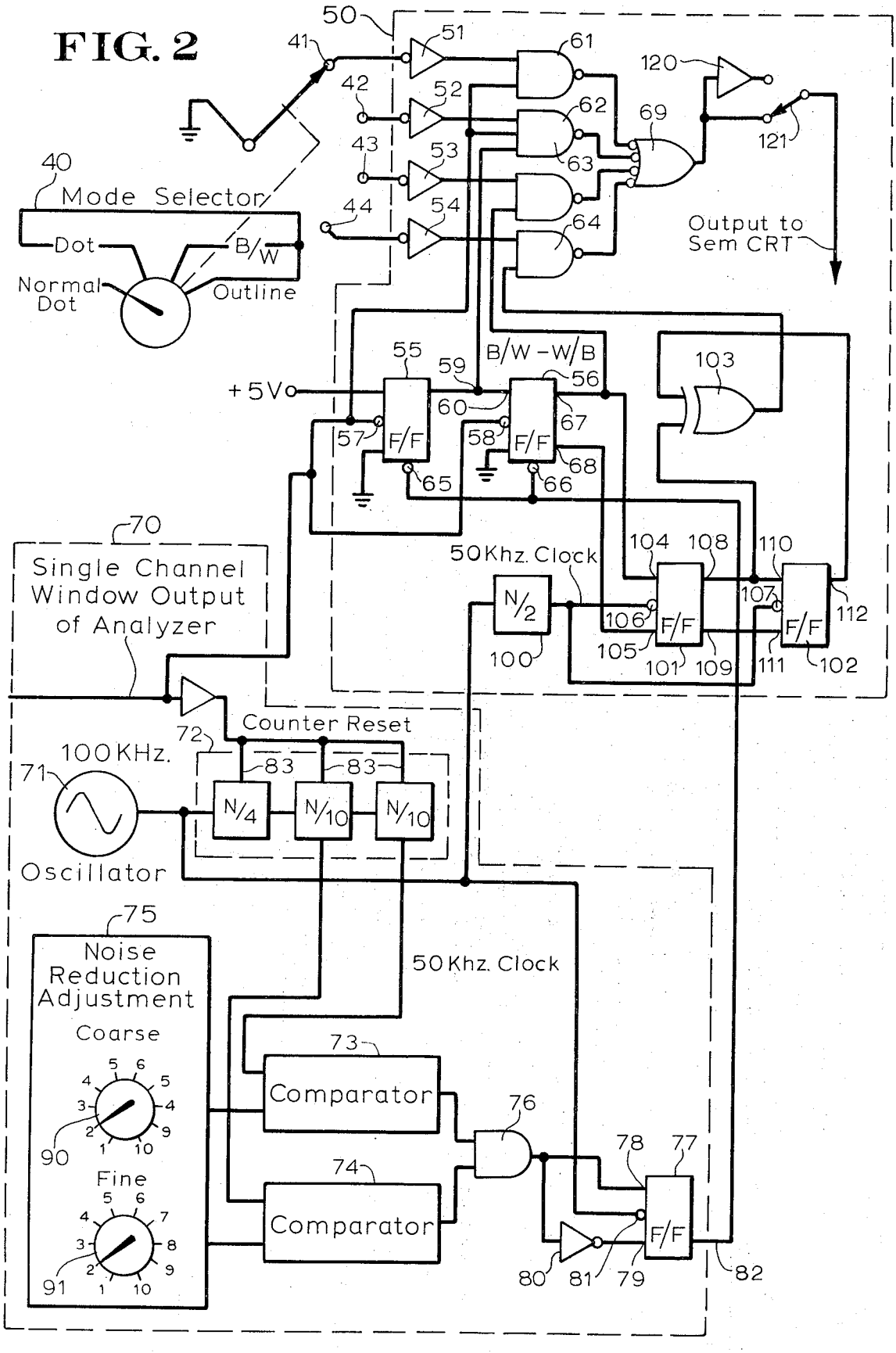
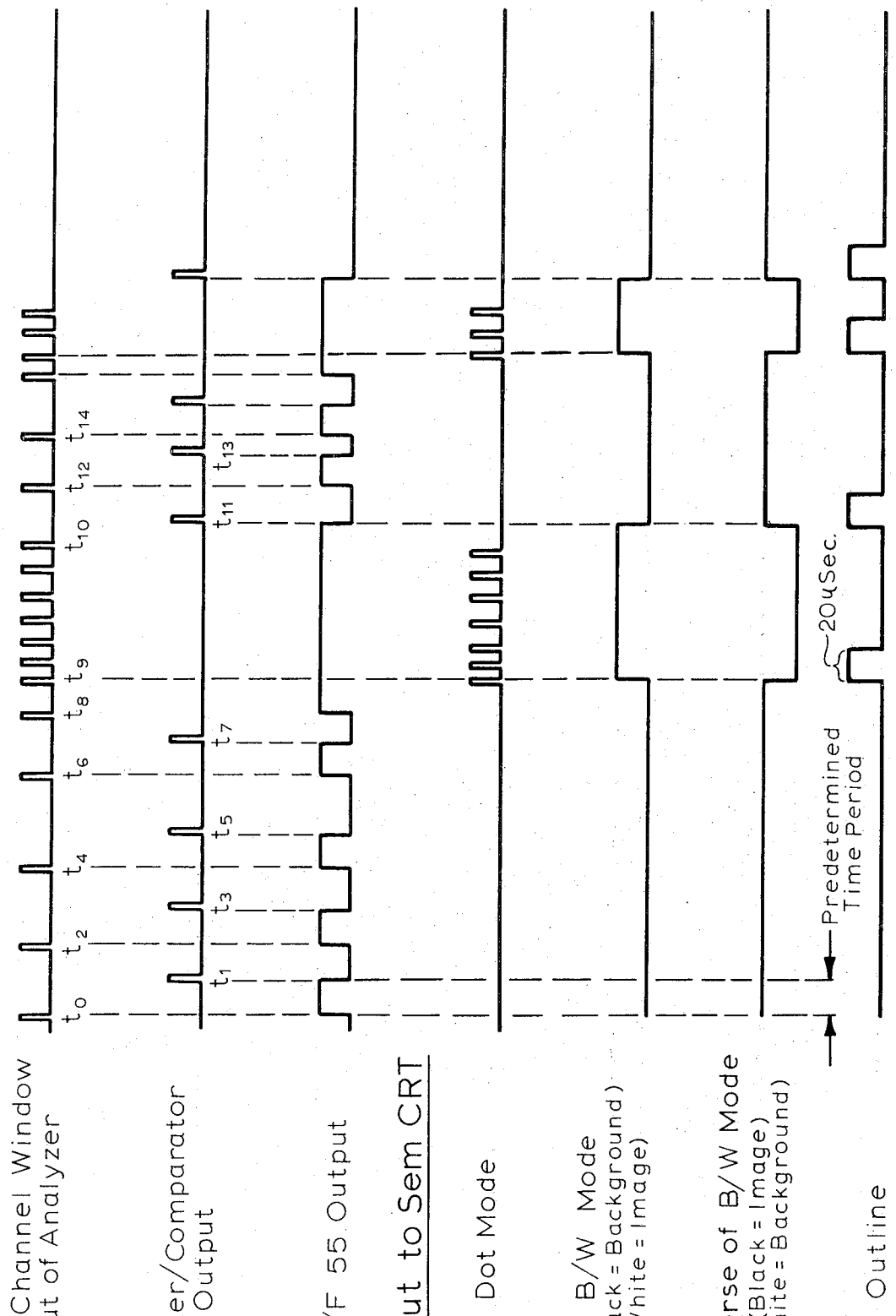

50
41
42
43
44
51
52
53
54
61
62
63
64
69
120
121
Output to Sem CRT
40
Mode Selector
Dot
B/W
Normal Dot
Outline
+5Vo
55
59
B/W - W/B
56
60
57
F/F
58
F/F
67
68
65
66
103
70
Single Channel Window Output of Analyzer
50Khz. Clock
N/2
100
104
108
110
106
F/F
105
101
109
107
F/F
111
112
102
Counter Reset
72
100KHz.
71
83
83
N/4
N/10
N/10
Oscillator
75
Noise Reduction Adjustment
Coarse
90
Fine
91
50Khz. Clock
73
Comparator
74
Comparator
76
78
77
F/F
80
81
79
82

FIG. 3


Single-Channel Window Output of Analyzer
Counter/Comparator Output
F/F 55 Output
Output to Sem CRT
Dot Mode
B/W Mode (Black = Background) (White = Image)
Reverse of B/W Mode (Black = Image) (White = Background)
Outline
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10} t_{11} t_{12} t_{13} t_{14}
Predetermined Time Period
20μSec.

X-RAY SCAN AREA MAPPING SYSTEM

BACKGROUND OF THE INVENTION

This invention pertains to X-ray area mapping systems, and more particularly to X-ray area mapping systems which provide a scanning electron microscope display with visual information.

Scanning-type electron microscope (SEM) systems, wherein a narrow electron beam is caused to scan across the surface of a specimen, have come into wide use for the examination of rough specimens, such as a fracture or a particle in a substrate. In such systems a detector, mounted adjacent the specimen, detects the incidence of secondary electrons as the specimen is scanned to develop a video signal indicative of the topography of the specimen. This video signal, after amplification, is utilized to intensity-modulate the electron beam of the SEM cathode-ray tube. When this electron beam is caused to scan in synchronism with the electron beam of the SEM display, an output display is formed on the face of the cathode-ray tube showing the three dimensional surface features of the specimen with magnification typically from 20 to 20,000 times.

The usefulness of a SEM system is greatly enhanced if an elemental analysis can be made of the specimen at the same time the specimen is being scanned. This is accomplished by detecting and measuring the X-rays emitted from the specimen as it is scanned. The energy level of these X-rays is proportional to the atomic number of the element emitting the X-rays, and thus can be used to unequivocably identify the element. Furthermore, the relative number of X-rays of various energies can be used to calculate the relative abundance of the different elements in the specimen. Energy-dispersive analysis systems commonly used in conjunction with SEM systems for elemental analysis employ a highly purified silicon diode detector for developing current pulses proportional to the energy level of the X-ray events. After amplification, these pulses are sorted and tabulated according to their energy level in a multichannel energy distribution analyzer to ascertain the complete energy spectrum of the specimen. All or portions of the spectrum can then be displayed as a histogram on a cathode-ray tube, or can be printed-out by means of a teletype terminal or data plotter.

Energy-dispersive analysis systems can also be equipped to single out specific energy level pulses, and hence specific elements. This is accomplished by means of a single channel window circuit which is set to recognize only signals with a predetermined energy range, or window, and to ignore all others. All X-ray events falling within this window can be separately processed and tabulated, allowing the presence of a selected element to be accurately determined.

One particularly useful application for the single channel window is to provide an area map of the selected element on the output display of the SEM system. This may be done by intensity-modulating the electron beam of the cathode-ray display tube so that the selected element will be made to stand out in some manner from the rest of the display.

Unfortunately, X-ray area mapping systems of the prior art operate in such a way as to continuously enable intensification of the SEM cathode-ray tube display. During the electron beam scanning of the specimen, background X-ray events having energies within the electron energy range of the window cause intensification of the display at times when intensification in inappropriate. This, of course, detracts from the usefulness of an X-ray map and results in faulty information.

It is, therefore, an object of the invention to provide an improved X-ray area mapping system.

It is a more specific object of the present invention to provide an X-ray area mapping system which substantially reduces the background X-ray noise on a scanning electron microscope cathode-ray tube display.

It is a still further object of the present invention to provide a background noise reduction circuit capable of being incorporated into an X-ray area mapping system of the prior art rendering it more useful to the operator.

SUMMARY OF THE INVENTION

The invention provides in an X-ray scanning area mapping system of the type which utilizes emitted X-rays from a specimen upon scanning by an electron beam and of the type which includes detecting means for detecting the occurrence of emitted X-rays, analyzing means for analyzing the energies of the emitted X-rays and for producing an output in response to the energies of the emitted X-rays for deriving an intensifying signal for a scanning visual display device, the improvement rendering the visual display more free from background X-ray noise than theretofore obtainable comprising enabling means coupled to the analyzing means and to the display device for enabling intensification of the display device in response to the analyzing means upon the occurrence of one of the emitted X-rays and disabling means coupled to the enabling means for disabling the intensification of the display device when the time between consecutively emitted X-rays exceeds a predetermined time period.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims. The invention, together with further objects and advantages thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings, in the several figures of which like reference numerals identify like elements, and in which:

FIG. 1 is a simplified functional block diagram of a scanning-type electron microscope display system constructed in accordance with the invention to present a spacial X-ray area map;

FIG. 2 is a schematic circuit diagram of an X-ray background noise reduction circuit partially in block form embodying the present invention; and

FIG. 3 is a graphic representation of signal waveforms as a function of time, which are helpful in understanding the operation of the circuit of FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1, the display system of the invention is shown in conjunction with a scanning-type electron microscope and which may be entirely conventional in design and operation. The microscope may include an electron gun 11, an electromagnetic condens-

ing lens **12**, and an electro-magnetic objective lens **13** for establishing and focusing an electron beam **14** onto the surface of a specimen **15**. Because the scanning electron microscope is intended primarily for high resolution imaging, the electron beam is of relatively low density, typically in the order of 10^{-12} amperes, to obtain the smallest possible contact point with the specimen.

The electron beam **14** is caused to scan specimen **15** by means of an electro-magnetic scanning coil **16**. This scanning action may be two dimensional and preferably occurs at the scanning rate of the SEM cathode-ray tube display scanning rate. Scanning coil **16** is driven by scanning circuits **17**, which may include both horizontal and vertical circuits for establishing the necessary deflection currents in coil **16**. These circuits are synchronized by means of a sync generator **18**, which also has an output for synchronizing associated output display devices.

Electron microscope **10** also has associated with it an X-ray area mapping system for providing a spacial area map display of X-ray events emitted from specimen **15**. Data for this system is obtained by means of X-ray detector **23** positioned adjacent to the specimen. As the electron beam scans the specimen **15**, X-rays are emitted from specimen **15**. This detector may consist of a lithium-drifted silicon conductor, which when appropriately biased, develops a charge proportional to the energy of the incident X-ray. This charge is integrated into a current pulse by a field effect transistor (FET) pre-amplifier. The silicon detector and its FET pre-amplifier are cooled with liquid nitrogen from an adjacent dewar **24** to stabilize the detector and to reduce the dark current, (noise).

The signal from the pre-amplifier is amplified in a linear amplifier **25**. The gain of this amplifier is variable but stable over extended time periods, thereby providing a means of calibrating the system and accommodating variations in detector efficiency. The amplifier current pulses from amplifier **25** are applied to an analog to digital converter **27**, one at a time, wherein each is converted to a binary information signal indicative of its magnitude, and hence the energy level of the X-ray event. This information signal is applied to an energy distribution analyzer **28** which contains a memory unit having a large number of locations each corresponding to a possible X-ray event energy level. A number stored in each such memory location indicates the number of X-ray events which have been received at that energy level. By adjusting the gain of amplifier **25**, the binary number developed by converter **27** in response to an X-ray event is made to correspond to the address of the memory location corresponding to the energy level of the event. Then, by utilizing the digital number from converter **27** as an address to locate a particular memory location, and up-dating the contents of that location by adding one count, it is possible to develop within the memory a complete energy spectrum for the specimen being analyzed. In practice, **400** or more such memory locations may be utilized.

It is usually desirable for X-ray area mapping purposes to analyze a certain energy level or range of energy levels to determine the location of a particular element or group of elements within a specimen. To this end, the X-ray analysis system of FIG. **1** includes a single channel window **31** which can be set to recognize and display one particular energy level, or alternatively, a range of alternative levels. It accomplishes this by comparing an applied digital number with an internally stored digital number, and producing an output only when the numbers agree or are within the selected range. The stored numbers and the permissible range can be set by means of switches, or can be extremely selected and retained in a portion of the memory of analyzer **28**.

During the scanning of specimen **15**, the digital output signal from converter **27**, representing energy-levels of occurring X-ray events are applied to single channel window **31**, wherein they are compared with the internally stored number to determine whether the events fall within the window limits. If they do, an output pulse is produced by window **31** for the purpose of producing an X-ray area map indicating the spacial distribution of the selected element on the SEM system display cathode-ray tube **22**.

However, in prior art X-ray area mapping systems, the SEM display cathode-ray tube **22** is continuously enabled for intensification by the pulses produced by single channel window **31**. As previously mentioned, during the scanning of specimen **15**, background X-rays are produced and some of these background X-rays have energies within the range of the single channel window **31**. In the case when the SEM display **22** is continuously enabled, the background X-ray events having energies within the selected energy range will produce a pulse from single channel window **31** intensifying the SEM display cathode ray tube. This background noise produces intensification of the SEM display when such intensification is inappropriate resulting in background noise intensification of the SEM display and making the area map produced less useful to the operator. Therefore, and in accordance with the present invention, the pulses produced by single channel window **31** are applied to background noise reduction circuit **32**. Background noise reduction circuit **32** operates on the principle that the background X-ray events having energies within the energy range of the single channel window occur at slower rates than the legitimate X-ray events having energies within the predetermined range. Background noise reduction circuit **32** enables intensification of the SEM display cathode-ray tube **22** upon the occurrence of an emitted X-ray falling within the predetermined range of the single channel window and has means for disabling intensification of the display when consecutive X-ray events within the predetermined energy range are spaced apart by a time which exceeds a predetermined time period. Therefore, when consecutive X-ray events are not occurring within the predetermined time period, no background noise is permitted to cause intensification of the SEM display cathode-ray tube.

In accordance with another aspect of the present invention, background noise reduction circuit **32** has means for accommodating a number of different X-ray area mapping operating modes. For instance, a standard operating mode of X-ray area mapping systems is commonly referred to as a NORMAL DOT mode where the pulses supplying intensification of the SEM display cause dot images on the display. While background noise reduction circuit **32** can accommodate such an operating mode, it may be preferred to utilize one of the three additional modes which background noise reduction circuit **32** can accommodate in which it reduces the background noise of the SEM display.

One of these modes, the DOT mode, produces a dot image like that of the normal DOT mode when the SEM display is intensified. However, unlike the NORMAL DOT mode, the dot mode only enables intensification of the SEM display upon the occurrence of an X-ray event which falls within the predetermined time period. This enablement continues as long as consecutively occurring X-ray events within the window occur within the predetermined time period as established by the background noise reduction circuit. During the enabling period, the background noise reduction circuit only produces pulses in response to the pulses produced by single-channel window 31 to produce a dot image on the SEM display. Intensification of the SEM display is disabled when consecutive X-ray events within the window are spaced apart by a time period exceeding the predetermined time period. During this time, no intensification can occur, reducing the background noise.

The second additional operating mode of background noise reduction circuit 32 provides a white on black line image on the SEM display as opposed to a dot image. The line display occurs because during those time periods when intensification is to take place, background noise reduction circuit 32 applies a continuous enabling signal to the SEM display CRT as it scans.

The third additional operating mode provides an outline image. The outline image intensification occurs at what would be the beginning and end of the line image intensification period for a duration longer than the dot image periods but shorter than the line image periods. As a result, an outline image of the particles of the particular element can be mapped.

The present invention also provides for reversing the images so that instead of a white on black representation, a black on white representation may be obtained for each of the modes.

The output pulses, whether of the dot image type, the line image type or the outline image type, are applied to pulse forming circuit 33 which merely assures that the video information applied to video processing circuits 34 are of sufficient amplitude to intensify the SEM display.

The operation of noise reduction circuit 32 may best be understood by making reference to FIG. 2 which shows a circuit configuration partly in schematic and partly in block form embodying the present invention. The different operating modes of noise reduction circuit 32 may be selected with mode selector 40 which has provision for selection the NORMAL DOT, DOT, White on Black and Outline operating modes.

The noise reduction circuit of FIG. 2 comprises enabling means 50 and disabling means 70. Enabling means 50 comprises four inverters, 51, 52, 53, and 54, each associated with a given one of NAND gates 61, 62, 63, and 64 respectively. The output of NAND gates 61 through 64 are each coupled to an assigned one of the four inputs to OR gate 69. Enabling means 50 additionally comprises a first flip-flop 55 and a second flip-flop 56. The clock input 57 of flip-flop 55 is coupled to the single channel window of the system, to an input of NAND gates 61 and 62 and also to clock input 58 of flip-flop 56. Output 59 of flip-flop 55 is coupled to another input of NAND gate 62 and to set input 60 of flip-flop 56. Outputs 67 of flip-flop 56 is coupled to an input of NAND gate 63.

Enabling means 50 additionally comprises N/2 clock 100, flip-flops 101 and 102, and exclusive OR gate 103. Inputs 104 and 105 of flip-flop 101 are coupled to outputs 67 and 68 of flip-flop 56 respectively. Clock inputs 106 and 107 of flip-flops 101 and 102 respectively are coupled to clock 100. Outputs 108 and 109 of flip-flop 101 are coupled to inputs 110 and 111 respectively of flip-flop 102. Output 108 of flip-flop 101 and output 112 of flip-flop 102 are each coupled to an input of exclusive OR gate 103 and Exclusive OR gate 103 is coupled to an input of NAND gate 64. At the output of OR gate 69 is an inverter 120 which may be switched into the circuit by switch 121. This provides the capacity for inverting the output of OR gate 69 if desired.

Disabling means 70 comprises an oscillator 71, a counter 72, of the type well known in the art and shown in block form for simplicity, a pair of comparators 73 and 74, noise reduction adjustment 75 which establishes input conditions on comparators 73 and 74, AND gate 76 having two inputs, and a flip-flop to an assigned one of the comparator outputs, and a flip-flop 77 having inputs 78 and 79. Input 78 is directly coupled to the output of AND gate 76, and input 79 is directly coupled to output of AND gate 76, and input 79 is directly coupled to output of AND gate 76 via an inverter 80. Clock input 81 of flip-flop 77 is coupled to oscillator 71.

In operation, when enabling means 50 enables intensification of the SEM display in a manner hereinafter described, counter 72 driven by oscillator 71, after being reset by the output of single channel window 31, begins a count. The predetermined time period is established by noise reduction adjustment 75 which establishes input conditions on comparators 73 and 74. When counter 72 achieves a sufficient count, upon completion of the predetermined time period, indicating that a consecutive X-ray event has not occurred within the predetermined time period, comparators 73 and 74 compare the output conditions of counter 72 with the input conditions established by noise reduction adjustment 75 to produce suitable outputs for driving AND gate 76 which in turn establishes a logical one at input 78 of flip-flop 77 and a logical zero at input 79 of flip-flop 77. Immediately after these input conditions are established at flip-flop 77, on the next cycle of oscillator 71, output 82 of flip-flop 77, which is coupled to flip-flop 55 and 56 of enabling means 50, disables the enabling means 50 by applying a logical zero signal to reset inputs 65 and 66 of flip-flops 55 and 56 respectively. This causes disablement of the SEM display and enablement will not reoccur until the single channel window produces another pulse in response to an X-ray event within the window to then reset counter 72 and flip-flop 55.

It it is desired to operate the X-ray area scan mapping system in the NORMAL DOT mode, selector means 40 is placed into the position as shown in FIG. 2. Mode selector 40 is coupled to switch 41 which, for the NORMAL DOT mode, places switch 41 in the position indicated in FIG. 2. This places the input inverter 51 at ground potential which in turn establishes a logical one voltage on the input to NAND gate 61. Once mode selector 40 is placed into the NORMAL DOT position, any pulse produced from the single channel window is impressed upon NAND gate 61 enabling it and causing a logical zero at its output. As can be seen from FIG. 2, the input to inverters 52, 53 and 54 are left floating

thereby producing a logical zero at the inputs to their respective NAND gates **62, 62,** and **64** producing at the output of these NAND gates a logical one which are applied to OR gate **69.** The logical zero from NAND gate **61** which is produced when an X-ray event occurs, causes the output of OR gate **69** to obtain the logical one state or in other words to produce at the output of OR gate **69** a positive pulse which is then applied to the pulse forming circuit **33** of FIG. **1** and subsequently to the video processing circuits **34,** causing intensification of the SEM display cathode-ray tube.

A pulse applied to intensify the SEM display produces a dot image. Since the SEM display cathode-ray tube is scanning in synchronism with the scanning electron microscope, intensification of the SEM display occurs at the proper point relative to the point on the specimen. Thus, an accurate spacial representation of the presence of that element which emits X-rays within the energy range of the single channel window is obtained. This is also attributable to the fact that the scanning rate of the scanning electron microscope is relatively slow compared to scanning rates of say, a television cathode-ray tube, minimizing horizontal distortion in the display image. As previously mentioned, the NORMAL DOT mode of the noise reduction circuit produces the same result as does the NORMAL DOT mode for conventional X-ray area mapping systems. It will be noted from the circuit diagram that the SEM display is continuously enabled. Thus, background X-ray noise events falling within the single channel window will likewise be intensified upon the SEM display. To reduce this obviously disadvantageous feature, the noise reduction circuit is preferably operated in anyone of the DOT, the White on Black, or the Outline modes.

If the DOT mode is desired, mode selector **40** is set in the DOT mode position thereby causing switch **41** to contact switch position **42.** This places the input to inverter **52** at ground potential resulting in a logical one being impressed on the input of NAND gate **62** to which the output of inverter **52** is coupled. Since the inputs of inverters **51, 53** and **54** are left floating, the inputs to their respective NAND gates **61, 63** and **64** to which their outputs are coupled will attain logical zero states. Upon the first X-ray event falling with the single channel window, flip-flop **55** is clocked by the pulse produced from the single channel window, establishing a logical one at output **59** and accordingly at the input to NAND gate **62** to which it is coupled. Clock input **57** of flip-flop **55** is also coupled to an input of NAND gate **62** so that a pulse produced from single channel window **31** upon the first X-ray event occurring within the single channel window also places a logical one at that input of NAND gate **62.** The inputs to NAND gates **62** are now in the logical one state while at least one of the inputs to NAND gates **61, 63** and **64** are in the logical zero state. Thus, and future pulse produced from single channel window **31** evidencing an X-ray event within the window will produce a positive going pulse from the output of OR gate **69** which is applied to pulse forming circuit **33** and subsequently to intensify SEM display **22.**

Intensification of the display will occur from future single channel window pulses as long as these pulses are consecutively occurring within a predetermined time period. This period is selectable by noise reduction adjustment **75** which establishes input conditions on comparators **73** and **74.** The first single channel window pulse to occur resets counter **72** back to its original state from which, it once again resumes counting down. If another single channel window pulse does not occur within the time it takes for counter **72** to count down a sufficient number of counts to establish input conditions at comparators **73** and **74** which match the input conditions applied by noise reduction adjustment **75,** comparators **73** and **74** will produce a suitable output, such as a logical one, causing AND gate **76** to produce a logical one at its output to establish a logical one at clock input **78** and a logical zero at clock input **79.** Upon the next cycle of oscillator **71,** clock input **81** of flip-flop **77** will be triggered, causing output **82** to obtain the logical zero state resetting flip-flop **65,** causing output **59** to reassume zero state, disabling NAND gate **62,** and thus disabling enabling means **50.** However, if a consecutively produced pulse from the single channel window occurs within the predetermined time, the counter reset of counter **72** will be reset back to zero and disablement will not occur.

Even though a background X-ray event with the single channel window may occur within the predetermined time period, such occurrences are highly unlikely since the background X-ray events occur at much slower rates than do the legitimate X-ray passed without a subsequent X-ray event within the single channel window, the enabling means is disabled, precluding intensification of the SEM display CRT by background X-ray events which may fall within the single channel window. Therefore, substantial reduction of background noise in the displayed area maps is obtained.

The operation of the circuit of FIG. **2** and the DOT mode may best be understood with reference to FIG. **3** which shows the wavefroms produced within the circuit as a function of time. For example, a pulse within single channel window evidencing an X-ray event at T_0 causes the output of flip-flop **55** to go high and as explained earlier, enables enabling means **50.** However, as can be seen from FIG. **3** another single channel window pulse does not occur until T_2 which is after the predetermined time period which ended at T_1. At T_1 the counter produces a pulse to disable the enabling means. There is no intensification of the SEM display until T_9 when a single channel window pulse occurs within the predetermined time following a pulse at T_8. This maintains flip-flop **55** at output **59** in the logical one position and resets counter **72** precluding AND gate **76** from producing a disabling pulse. The consecutive single channel window pulses after T_9 are all within the predetermined time period until a pulse T_{10} occurs. The next pulse produced in the single channel window at T_{12} is spaced from the pulse produced at T_{10} by time period exceeding the predetermined period which ended at T_{11}. The output of flip-flop **55** at T_{11} is therefore reset to the low position by the pulse produced by AND gate **76** and once again is not raised to the logical one level until pulse T_{12} is produced by the single channel window.

As can be seen, during the times which output **59** of flip-flop **55** is in the logical zero state the enabling means **50** is disabled precluding intensification of the SEM diaplsy. Background X-ray noise events falling within the single channel window are not displayed during these times, reducing substantially the background noise of the X-ray area map. Also noted from FIG. **3** is

the fact that a dot image on the display is produced. Even though the SEM display intensification is enabled, it is actually only intensified during the short pulse intervals of the single channel window pulses. Thus, a dot image on the display is created.

In the White on Black mode, a white line image is formed on a black background. If this mode is desired, mode selector 40 is positioned in the B/W position as shown in FIG. 2. This places switch 41 in contact with terminal 43, grounding the input to inverter 53, and thus producing a logical one potential at the input to NAND gate 63 to which the output of inverter 53 is coupled. As previously explained, the inverters which are not coupled to ground by switch 41 produce at their respective inputs a logical zero potential. This causes the outputs of NAND gates 61, 62 and 64 to be in the logical one state, and these potentials are applied to the respective inputs of OR gate 69. When the first single channel window pulse occurs, output 59 of flip-flop 55 is established in the logical one position, setting input 60 to flip-flop 56 in the logical one state. As in the DOT mode, when the first single channel window pulse is produced, counter 72 is reset back to zero and begins to count down. If the next single channel window pulse produced occurs within the predetermined time, flip-flop 56 will be set, driving output 67 to the logical one state and impressing the resulting potential on the input to NAND gate 63 to which it is coupled. This causes the output of NAND gate 63 to go to the logical zero state and in conjunction with the logical one state at the rest of the inputs to OR gate 69, causes the output of OR gate 69 to achieve the logical one state, causing intensification of the SEM display. Since there is no input of NAND gate 63 coupled to the single channel window, and since flip-flop 56 maintains a logical one at its output 67 until reset by the disabling means 70, the intensification of the SEM display is continuous, causing a line image to be displayed on the SEM cathode-ray tube. If the next consecutive pulse produced by the single channel window does not occur within the predetermined time after flip-flop 56 is set, the disabling means 70 will disable the enabling means 50 by producing an output at the output of AND gate 76 which establishes a logical one at input 78 and a logical zero at input 79 of flip-flop 77. The next oscillator cycle which occurs after inputs 78 and 79 are established in the logical one and logical zero states respectively causes flip-flop 77 to attain at output 82 a logical zero, resetting flip-flops 55 and 56 to thereby cause the output of OR gate 69 to go back to the logical zero state precluding further intensification of the SEM display.

Referring back to FIG. 3 and remembering the fact that it takes two successive single channel window pulses occurring within the predetermined time to cause intensification of the SEM display, it can be noted from FIG. 3 that such a situation does not occur until T_9. The single channel window produces a pulse at T_8. This sets flip-flop 55 causing input 60 of flip-flop 56 to attain the logical one state and the next succeeding pulse at T_9 occurring within the predetermined time from the pulse produced at T_8 causes output 67 of flip-flop 56 to go to logical one, thus achieving enablement and intensification of the SEM display. The SEM display remains continuously intensified until T_{11}. The single channel window pulse at T_{10} is not followed by a succeeding pulse until T_{12} which is subsequent to the end of the predetermined time period at T_{11} since T_{10}. Therefore, the pulse produced by the disabling means at T_{11} resets flip-flops 55 and 56 causing the output to the SEM display to go back to zero. While the pulse produced at T_{12} does set flip-flop 55, flip-flop 56 is not clocked by another consecutive single channel window pulse until T_{14} which is after the predetermined time period expiring at T_{13}. At T_{13} flip-flop 55 is reset to zero and is set once again at T_{14} when a single channel window pulse once again occurs.

The line image displayed in this mode is virtually noise free. During the times in which the SEM CRT is intensified, it is continuously intensified and any background X-ray events occurring within that time have no effect on the display. During the times in which intensification of the SEM display is disabled, background noise is not intensified on the SEM display. While it is possible that background noise within the window could occur within the predetermined time period after a single channel window pulse, this is highly unlikely since the background noise events occur at much slower rates than do the legitimate X-ray events emitted from the specimen 15, falling within the window.

If the Outline mode is preferred, mode selector 40 is positioned in the outline position as shown in FIG. 2. This places switch 41 in contact with terminal 44, grounding the input to inverter 53 and thus producing a logical one potential at the input to NAND gate 64 to which the output of inverter 54 is coupled. As in the case of the White on Black line mode, when the first single channel window pulse is produced, counter 72 is reset back to zero and begins to count down. If the next single channel window pulse produced occurs within the predetermined time, flip-flop 56 will be set, driving output 67 to the logical one state and impressing the resulting potential on input 104 of flip-flop 101. Clock counter 100 then clocks input 106 of flip-flop 101 producing at output 108 a logical one potential which is impressed upon exclusive OR gate 103 and input 110 of flip-flop 102, setting flip-flop 102. Because output 112 of flip-flop 102 is still at logical zero, exclusive OR gate 103 provides a logical one to NAND gate 64 causing NAND gate 64 to produce a logical zero signal to OR gate 69 and thus producing an intensification signal. Upon the next clock pulse from clock counter 100, which for purposes of this embodiment, is 20 microseconds, input 107 of flip-flop 102 is clocked causing a logical one at output 112 which is impressed upon its input to exclusive OR gate 103 forcing the output of exclusive OR gate 103 to go to logical zero to thereby proclude intensification.

Because there is no input of NAND gate 64 coupled to the single channel window, and because flip-flop 56 is maintained at logical one at output 67 until reset by disabling means 70, intensification of the SEM display will not re-occur until disablement of the SEM intensification. For instance, if the next consecutive pulse produced by the single channel window does not occur within the predetermined time after flip-flop 56 is set, the disabling means 70 will disable the enabling means 50 producing an output at the output of NAND gate 76 establishing a logical one at input 78 and a logical zero at input 79 of flip-flop 77.

The next oscillator cycle which occurs after input 78 and 79 are established in the logical one and logical zero states respectively causes flip-flop 77 to obtain a logical zero at output 82, resetting flip-flops 55 and 56 to thereby cause output 67 to go to the logical zero

state and output **68** to obtain the logical one state. These logical potentials are impressed upon inputs **104** and **105** of flip-flop **101** so that upon the next clock input from clock counter **100**, a logical zero is produced at output **108** of flip-flop **101**. Because output **112** of flip-flop **102** is in the logical one state, exclusive OR gate **103** will produce a logical one at its output causing NAND gate **64** to impress upon OR gate **69** the logical zero causing intensification of the SEM display. Another clock pulse is produced **20** microseconds later from clock counter **100** which causes output **112** of flip-flop **102** to attain the logical zero state causing exclusive OR gate **103** to impress upon NAND gate **64** a logical one to thereby preclude further intensification.

From the foregoing, it can be understood that the timing of the disabling means **70** for the outline mode is identical to the timing for the white on black line image mode. An intensification output is produced at the beginning and at the end of what would otherwise be the intensification period for the line image reproduction, each lasting however, for a duration shorter than the line image intensification. Therefore, an outline image is formed on the SEM display.

Referring back to FIG. **3** and in accordance with the previous description, it can be noticed that at the times when the B/W mode would begin intensification, the outline mode begins intensification as well. However the duration of intensification is relatively short, for this embodiment 20 microseconds. Intensification once again takes place, when the B/W mode would disable intensification, for a 20 microsecond duration. Thus, an outline reproduction is produced. Effective noise reduction is still obtained however since during the interval between outline intensification, X-ray events within the window, and background noise within the window, cannot cause intensification of the SEM display. Therefore, a low noise outline image is obtained.

For each of the modes previously discussed, it has been assumed that switch **121** is in the position shown in FIG. **2**, producing a white on block reproduction. By placing switch **121** in contact with the output of inverter **120** coupled to the output of OR gate **69**, a reverse image for each of the modes can be obtained. Therefore, for each mode, the white on black image may be reversed producing a black on white reproduction as well.

Comparators **73** and **74** may be a pair of multiple input exclusive OR gates where noise reduction adjustment **75** establishes input conditions at the input of the gates. Such structures are well known in the art. The amount of background noise reduction of the circuit shown in FIG. **2** is variable and can be adjusted by setting different positions on the noise reduction adjust knobs **90** and **91** to obtain different amounts of background noise reduction. This varies the predetermined time period by establishing different input conditions to comparators **73** and **74** and to vary the degree of counting that counter **72** must go through in order to provide input conditions to comparators **73** and **74** which match those conditions established by noise reduction adjust **75**.

The present invention is most attractive for the user of an X-ray scan area mapping system. It not only affords the NORMAL DOT operating mode, but also the inventive improvement of a DOT, White on Black line, and Outline operating modes each affording substantially reduced background noise in the displayed area map. The invention provides a means for obtaining a reversed image if desired. The noise reduction is variable and can be set to the amount of noise reduction desired. Also, the present invention can be used as an accessory item to update X-ray area mapping systems of the prior art.

While particular embodiments of the invention have been shown and described, modifications may be made, and it is intended in the appended claims to cover all such modifications as may fall within the true spirit and scope of the invention.

We claim:

1. An improved background X-ray noise reduction circuit in a system where X-rays are emitted from a specimen along with background X-rays upon scanning by an electron beam, and where said system has an X-ray detector, analyzing means for analyzing the energies of said detected X-rays and for producing an output pulse for each detected X-ray having an energy falling within a predetermined range of energies, said output pulses providing modulating signals for a scanning visual display device, and said background X-rays occurring at slower rates than said emitted X-rays having energies within said range, the improvement comprising:

an enabler means coupled between said analyzer and said display device for applying said modulating signals to said display device for pulse modulating said display device; and

a disabler means responsive to the rate of said output pulses and coupled to said enabler and to said analyzer for causing said enabler to terminate said modulating signal application to said display device when the time between consecutive output pulses exceeds a predetermined time period which is less than or equal to the expected period between consecutive noise pulses.

2. A background X-ray noise reduction circuit in accordance with claim **1** where said enabler means is conditioned to apply said modulating signals to said display device by the first one of said output pulses.

3. A background X-ray noise reduction circuit in accordance with claim **2** where said enabler means additionally comprises means responsive to the first output pulse following said conditioning for providing said display device with a modulating signal of a fixed duration and means responsive to said disabler means for providing said display device with another modulating signal of said fixed time duration when said disabler means acts to cause said enabler means to terminate said modulating signal application to thereby provide an outline image on said device.

4. A background X-ray noise reduction circuit in accordance with claim **2** where said enabler means additionally comprises means for providing said display device with continuous modulating signals in response to said output pulses.

5. A background X-ray noise reduction circuit in accordance with claim **1** where said disabler means comprises:

a counter;

an oscillator coupled to said counter for driving said counter;

comparator input means for providing an input condition; and

a comparator coupled to said counter and to said comparator input means for comparing the condition of said counter to said input condition for providing a disabling signal when they match.

6. A background X-ray noise reduction circuit in accordance with claim 5 where said counter comprises a reset input.

7. An X-ray scan area mapping system of the type which utilizes X-rays emitted from a specimen upon scanning by an electron beam comprising:

a detector means for detecting said emitted X-rays;

an analyzer means coupled to said detector for analyzing the energies of said detected X-rays and for producing an output pulse for each detected X-ray having an energy falling within a predetermined energy range, said output pulses providing modulating signals for a scanning visual display device;

an enabler means coupled between said analyzer and said display device for applying said modulating signals to said display device for pulse modulating said display device; and

a disabler means responsive to the rate of said output pulses coupled to said enabler and to said analyzer for causing said enabler to terminate said modulating signal application to said display device when the time between consecutive output pulses exceeds a predetermined time period which is less than or equal to the expected period between consecutive noise pulses.

8. An X-ray scan area mapping system in accordance with claim 7 where said enabler means is conditioned to apply said modulating signals to said display device by the first one of said output pulses.

9. An X-ray scan area mapping system in accordance with claim 8 where said enabler means additionally comprises means for providing said display device with continuous modulating signals in response to said outupt pulses.

10. An X-ray scan area mapping system in accordance with claim 8 where said enabler means additionally comprises means responsive to the first output pulse following said conditioning for providing said display device with a modulating signal of a fixed time duration and means responsive to said disabler means for providing said display device with another modulating signal of said fixed time duration when said disabler means acts to cause said enabler means to terminate said modulating signal application to thereby provide an outline image on said device.

11. An X-ray scan area mapping system in accordance with claim 7 where said disabler means comprises:

a counter coupled to said analyzer means;

an oscillator coupled to said counter for driving said counter;

comparator input means for providing an input condition; and

a comparator coupled to said counter and to said comparator input means for comparing the condition of said counter to said input condition supplied by said comparator input means for providing a disabling signal when they match.

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