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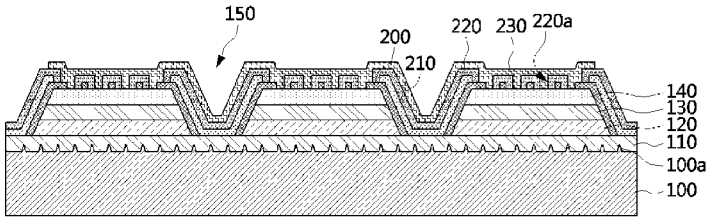
(54) Title: LIGHT EMITTING DIODE MODULE FOR SURFACE MOUNT TECHNOLOGY AND METHOD OF MANUFACTURING THE SAME



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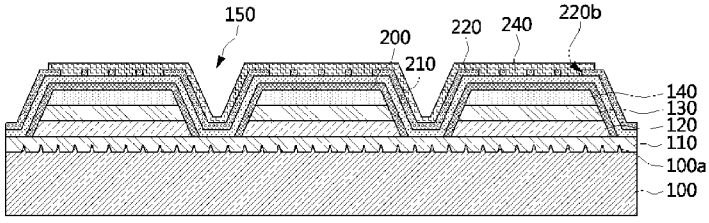

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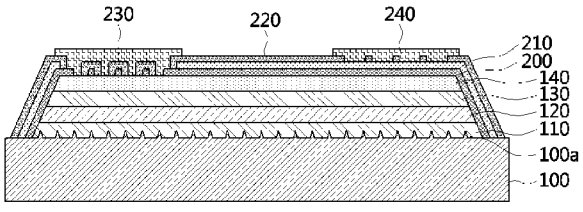

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(57) Abstract: Provided is a light emitting diode (LED) in which a side surface of a reflective metal layer has a predetermined angle, and occurrence of cracks in a conductive barrier layer formed on the reflective metal layer can be prevented. Also, an LED module using LEDs is disclosed. A reflection pattern electrically connected to a second semiconductor layer is partially exposed by patterning a first insulating layer. Accordingly, a first pad is formed through the partially opened first pad region. Also, a conductive reflection layer electrically connected to a first semiconductor layer forms a second pad region formed by patterning a second insulating layer. A second pad is formed on the second pad region.

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Description

Title of Invention: LIGHT EMITTING DIODE MODULE FOR SURFACE MOUNT TECHNOLOGY AND METHOD OF MANUFACTURING THE SAME

Technical Field

[1] The present invention relates to a light emitting diode (LED), and more particularly, to an LED module for surface mount technology and a method of manufacturing the same.

Background Art

[2] A light emitting diode (LED) is a device including an n-type semiconductor layer, a p-type semiconductor layer, and an active layer interposed between the n- and p-type semiconductor layers. When a forward electric field is applied to the n- and p-type semiconductor layers, electrons and holes may be injected into the active layer and recombine in the active layer to emit light.

[3] An LED module including a plurality of LEDs is disclosed in U.S. Patent Publication No. 2011-0127568. The LED module is a surface-mount type in which a p-type pad and an n-type pad are formed on a top surface of an LED. However, since the p-type pad is electrically connected to the entire surface of p-GaN exposed by an insulating layer, current crowding may occur.

[4] In addition, an LED may include a reflection layer according to the type of a chip. That is, a flip-chip type is characterized by emitting light through a substrate. Accordingly, after a semiconductor layer is formed on the substrate, a reflection layer formed of a metal is introduced on the semiconductor layer or a current spreading layer, and light is reflected by the reflection layer. Also, a barrier layer is provided on the reflection layer. The barrier layer is provided to prevent diffusion of the metal forming the reflection layer.

[5] FIG. 1 is an image of a conventional LED into which a reflection layer and a barrier layer are introduced.

[6] A reflection layer 20 is formed on a p-type semiconductor layer 10. The formation of the reflection layer 20 is performed using an e-beam evaporation process. Accordingly, a shape of the reflection layer 20 may be determined by an angle at which metal ions or atoms having directionality enter due to e-beams. In particular, a side portion of the reflection layer 20 does not have a substantially vertical profile with respect to the p-type semiconductor layer 10, and is formed at a predetermined angle to a surface of the p-type semiconductor layer 10. In particular, when the reflection layer 20 is formed of silver (Ag), it is difficult for the reflection layer 20 to have a vertical profile due to

specific diffusivity. Accordingly, it is generally intended to obtain a nearly vertical profile by controlling an angle of a substrate with respect to a direction in which metal ions or atoms proceed from a target.

[7] Also, a barrier layer 30 is introduced on the reflection layer 20. In FIG. 1, the barrier layer 30 has a structure in which two kinds of metal layers are alternately formed. The barrier layer 30 is provided to prevent diffusion of metal atoms constituting the reflection layer 20. For example, the barrier layer 30 is formed by alternately stacking a Ti layer and a TiW layer. Alternatively, the barrier layer 30 may be obtained by repetitively forming a single kind of metal layer instead of two kinds of metal layers.

[8] However, the structure of the barrier layer 30 is spontaneously destroyed or cracks occur due to various causes, such as the diffusion coefficient and coefficient of thermal expansion of a metal forming the barrier layer 30 stacked during the formation of the barrier layer 30. This problem becomes more serious as a profile of the underlying reflection layer 20 becomes closer to a vertical profile.

[9] In FIG. 1, titanium (Ti) is used for a first barrier layer 31 formed on the reflection layer 20 formed of Ag, and titanium tungsten (TiW) is used for a second barrier layer 32. An angle formed by a surface of a p-type semiconductor layer 10 with a side surface of the reflection layer 20 exceeds an angle of about 45°. The barrier layer 30 is deposited on a profile having a high inclination. The deposition process is generally performed using a sputtering process.

[10] The first barrier layer 31 and the second barrier layer 32 are alternately stacked along the inclined profile. However, as the number of times the first and second barrier layers 31 and 32 are stacked increases and the thickness of the barrier layer 30 increases, the barrier layer 30 cracks in the inclined side surfaces of the reflection layer 20. Occurrence of cracks becomes serious in a structure in which two different kinds of metals are alternately stacked, and worsens as an inclination angle of a side profile of the reflection layer 20 increases. In FIG. 1, a crack portion 40 is formed due to the above-described phenomenon.

[11] FIG. 2 is a cross-sectional view of the crack portion of FIG. 1.

[12] Referring to FIG. 2, as the numbers of the first barrier layer 31 and the second barrier layer 32 alternately formed on side surfaces of the reflection layer 20 increase, the thicknesses of the first and second barrier layers 31 and 32 formed on the side surfaces of the reflection layer 20 decrease, and deposition of the first and second barrier layers 31 and 32 on the side surfaces of the reflection layer 20 is omitted. Accordingly, a portion of the barrier layer 30 formed of the same material is discontinuous. Thus, cracks occur in the barrier layer 30. The cracks in the barrier layer 30 cause diffusion of metal atoms forming the reflection layer 20. Accordingly, electrical properties of subsequent electrodes are degraded due to the supply of heterogeneous metals.

[13] The causes of formation of the crack portion shown in FIGS. 1 and 2 may be analyzed in various approaches.

[14] For example, the barrier layer 30 may be formed to a relatively great thickness near a top surface of the reflection layer 20, while the barrier layer 30 may be formed to a small thickness on side surfaces of the reflection layer 20. When this phenomenon worsens, a discontinuous portion is formed in the first barrier layer 31 or the second barrier layer 32.

[15] Furthermore, cracks may occur in a specific barrier layer due to a difference in coefficient of thermal expansion between two kinds of metal materials during deposition of the two kinds of metal materials. The cracks in the first barrier layer 31 or the second barrier layer 32 are not cured during a subsequent deposition process, and the occurrence of the cracks worsens during a deposition process. It can be seen from FIG. 1 that a crack or discontinuity worsens toward an upper portion of the crack portion 40.

[16] Cracks in a barrier layer, which are predicted to occur for various causes, adversely affect characteristics of an LED. For example, metal atoms may diffuse from a reflection layer, thereby degrading electrical properties. Also, since an LED has a stack structure of a plurality of layers, cracks in the barrier layer worsen depending on the environment in which an LED is used. The cracks in the barrier layer fatally affect the reliability of the LED.

[17] Furthermore, when a surface-mount LED module is manufactured using the above-described LED, local crowding of current supplied from a pad occurs due to the cracks in the barrier layer. For instance, even if a high voltage or current is applied to increase luminance, since the current crowds in a p-GaN layer, luminance is reduced.

Disclosure of Invention

Technical Problem

[18] Accordingly, the present invention is directed to a light emitting diode (LED) module that reduces current crowding.

[19] The present invention is also directed to a method of manufacturing an LED module, which is used to attain the first objective.

Solution to Problem

[20] One aspect of the present invention provides a light emitting diode (LED) module including: an LED having a first semiconductor layer, an active layer, a second semiconductor layer, and a reflection pattern formed on a substrate, and including a mesa region formed to expose the first semiconductor layer, a first insulating layer formed on the mesa region exposing a portion of a surface of the first semiconductor layer, patterned on the reflection pattern and configured to form a first pad region, a conductive reflection layer formed on the first insulating layer and the first semi-

conductor layer exposed in the mesa region, a second insulating layer formed on the conductive reflection layer and configured to form a second pad region exposing a portion of the conductive reflection layer, a first pad formed on the first pad region, and a second pad formed on the second pad region.

[21] Another aspect of the present invention provides a method of manufacturing an LED module, including: coating a first insulating layer on a structure in which a first semiconductor layer, an active layer, a second semiconductor layer, and a reflection pattern are formed on a substrate, forming a first pad region by exposing a portion of the reflection pattern, and exposing the first semiconductor layer disposed on a mesa region, forming a conductive reflection layer on the first insulating layer, electrically connecting the conductive reflection layer to the exposed first semiconductor layer, and maintaining the first pad region in an opened state, coating a second insulating layer on the conductive reflection layer to expose the reflection pattern disposed in the first pad region, and forming a second pad region exposing a portion of the conductive reflection layer electrically connected to the first semiconductor layer, and forming a first pad on the first pad region and forming a second pad on the second pad region.

Advantageous Effects of Invention

[22] According to the present invention, pads are formed on a patterned pad region during manufacture of light emitting diode (LED) modules. Thus, local current crowding can be prevented. Also, diffusion of metals is prevented due to a reflection barrier layer provided between a conductive reflection layer and the pads. For example, a phenomenon in which a metal forming the conductive reflection layer moves to a second pad and increase the resistivity of the second pad can be prevented. In addition, a second semiconductor layer is electrically connected to a first pad. A pad barrier layer is formed on each of the pads. The pad barrier layer prevents diffusion of a metal generated during a bonding or soldering process so that the first pad or the second pad can have a high conductivity and be in electrical contact with the outside.

[23] Furthermore, in the present invention, a phosphor layer may be provided on an LED chip and include a plurality of phosphor layers. Accordingly, an operation of correcting color coordinates is enabled using at least one wavelength conversion operation, and correction of the color coordinates may be simplified by controlling the concentrations of phosphors.

[24] Aspects of the present invention should not be limited by the above description, and other unmentioned aspects will be clearly understood by one of ordinary skill in the art from exemplary embodiments described herein.

Brief Description of Drawings

[25] FIG. 1 is an image of a conventional light emitting diode (LED) into which a re-

flection layer and a barrier layer are introduced.

[26] FIG. 2 is a cross-sectional view of a crack portion of FIG. 1.

[27] FIG. 3 is a cross-sectional view of an LED according to a first exemplary embodiment of the present invention.

[28] FIGS. 4 through 8 are cross-sectional views illustrating a method of manufacturing the LED of FIG. 3 according to a first exemplary embodiment of the present invention.

[29] FIGS. 9 through 18 are plan views and cross-sectional views illustrating a method of manufacturing an LED module using the LED of FIG. 3 according to a second exemplary embodiment of the present invention.

[30] FIG. 19 is a cross-sectional view of an LED package according to a third exemplary embodiment of the present invention.

Mode for the Invention

[31] Hereinafter, exemplary embodiments of the present invention will be described in detail. It should be understood, however, that there is no intent to limit the invention to the particular forms disclosed.

[32] It will be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate or intervening layers may also be present. Terms that describe spatial relationships, such as "on," "upper," "top surface," "under," "lower," "bottom surface" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that such terms are intended to encompass different orientations of the device in use or operation in addition to the orientation(s) depicted in the figures.

[33] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms.

[34] In the drawings, the thicknesses of layers and regions may be exaggerated for clarity. Like reference numerals refer to like elements throughout.

[35]

[36] Embodiment 1

[37] FIG. 3 is a cross-sectional view of a light emitting diode (LED) according to a first exemplary embodiment of the present invention.

[38] Referring to FIG. 3, a first semiconductor layer 110, an active layer 120, a second semiconductor layer 130, and a reflection pattern 140 are formed on a substrate 100.

[39] The substrate 100 may be formed of any material capable of inducing the first semiconductor layer 110 to be grown. Accordingly, the substrate 100 may include sapphire (Al2O3), silicon carbide (SiC), gallium nitride (GaN), indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN), aluminum nitride (AlN), gallium oxide (Ga2O3),

or silicon. Specifically, the substrate 100 may be a sapphire substrate.

[40] Also, the substrate 100 may be a substrate on which surface treatment is not performed. The substrate 100 may be a patterned substrate. Also, a surface of the substrate 100 may have a moth-eye structure. For example, the substrate 100 may have a protrusion protruding in a roughly hemispherical shape, and pointed structures may be densely disposed on the protrusion.

[41] In addition, the first semiconductor layer 110 is provided on the substrate 100. The first semiconductor layer 110 preferably has an n conductivity type.

[42] Furthermore, the active layer 120 formed on the first semiconductor layer 110 may have a single quantum well(SQW) structure in which a well layer and a barrier layer are stacked, or a multi-quantum well(MQW) structure in which well layers and barrier layers are alternately stacked.

[43] The second semiconductor layer 130 is provided on the active layer 120. The second semiconductor layer 130 preferably has a p conductivity type.

[44] Furthermore, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 may include Si, GaN, AlN, InGaN, or AlInGaN. When the first semiconductor layer 110 includes GaN, the active layer 120 and the second semiconductor layer 130 preferably include GaN. However, since the second semiconductor layer 130 has a complementary conductivity type to the first semiconductor layer 110, a different dopant from that of the first semiconductor layer 110 is introduced into the second semiconductor layer 130. That is, when a dopant serving as a donor is introduced into the first semiconductor layer 110, a dopant serving as an acceptor is introduced into the second semiconductor layer 130. Also, the active layer 120 preferably includes a material on which bandgap engineering is performed to form barrier layers and well layers.

[45] The reflection pattern 140 is formed on the second semiconductor layer 130.

[46] The reflection pattern 140 includes a reflective metal layer 142 and a conductive barrier layer 144. Also, in some embodiments, an ohmic contact layer (not shown) may be formed under the reflective metal layer 142, and a stress relaxation layer (not shown) may be additionally formed between the reflective metal layer 142 and the conductive barrier layer 144.

[47] An ohmic contact layer may be formed of any material capable of enabling ohmic contact between the reflective metal layer 142 and the second semiconductor layer 130. Accordingly, the ohmic contact layer may include a metal including nickel (Ni) or platinum (Pt) or include a conductive oxide, such as indium tin oxide (ITO) or zinc oxide (ZnO). However, the ohmic contact layer may be omitted in some embodiments.

[48] The reflective metal layer 142 is formed on the ohmic contact layer. The reflective metal layer 142 reflects light generated in the active layer 120. Accordingly, the re-

flective metal layer 142 is formed by selecting a material having conductivity and high optical reflectance. The reflective metal layer 142 includes silver (Ag), a Ag alloy, aluminum (Al), or an Al alloy.

[49] In addition, a stress relaxation layer may be formed on the reflective metal layer 142. The stress relaxation layer preferably has a coefficient of thermal expansion equal to or higher than that of the conductive barrier layer 144, and equal to or lower than that of the reflective metal layer 142. Thus, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 may be reduced. Accordingly, a material forming the stress relaxation layer may be selected differently according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144.

[50] However, the ohmic contact layer or the stress relaxation layer may be omitted in some embodiments.

[51] In addition, an angle α formed by the reflective metal layer 142 with a plane surface of the underlying second semiconductor layer 130 preferably ranges from about 5° to about 45°. When an angle α formed by a side surface of the reflective metal layer 142 is less than about 5°, it is difficult to ensure a sufficient thickness of the reflective metal layer 142. When the angle α formed by the side surface of the reflective metal layer 142 is more than about 45°, cracks occur in a side profile of the conductive barrier layer 144 formed on the reflective metal layer 142. When an ohmic contact layer is introduced, an inclination angle formed by the ohmic contact layer with the side surface of the reflective metal layer 142 should be within the above-described angle range.

[52] The conductive barrier layer 144 is formed on the reflective metal layer 142 or the stress relaxation layer 143. For example, when a stress relaxation layer is omitted, the conductive barrier layer 144 is formed on the reflective metal layer 142, and when the stress relaxation layer is formed, the conductive barrier layer 144 is formed on the stress relaxation layer. The conductive barrier layer 144 is formed to surround at least the side surface of the reflective metal layer 142 and surround top and side surfaces of the stress relaxation layer. Accordingly, diffusion of metal atoms or ions constituting the reflective metal layer 142 is prevented. Also, stress caused due to a difference in coefficient of thermal expansion between the conductive barrier layer 144 and the reflective metal layer 142 may be absorbed in the stress relaxation layer. In particular, the conductive barrier layer 144 may be formed to a different thickness according to a surface state of the underlying reflective metal layer or stress relaxation layer. For example, assuming that the thickness of the conductive barrier layer 144 formed on a top surface of the reflective metal layer 142 is t1, the thickness of the conductive barrier layer 144 formed on the side surface of the reflective metal layer 142 is t2, and

the thickness of the conductive barrier layer 144 formed on the surface of the second semiconductor layer 130 is t3, a relationship of t1>t3>t2 is preferably set.

[53] In addition, the conductive barrier layer 144 is formed to completely shield the reflective metal layer 142 or the stress relaxation layer and extend to the surface of the second semiconductor layer 130.

[54] In addition, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer may be a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag.

[55] Furthermore, when the reflective metal layer 142 includes Ag or a Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or a Ag alloy, and the conductive barrier layer 144 includes Cr or Ni, the stress relaxation layer may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination formed of Ni, Au, or Cu.

[56] In addition, the conductive barrier layer 144 coats the surface of the second semiconductor layer 130.

[57] FIGS. 4 through 8 are cross-sectional views illustrating a method of manufacturing the LED of FIG. 3 according to a first exemplary embodiment of the present invention.

[58] Referring to FIG. 4, a first semiconductor layer 110, an active layer 120, and a second semiconductor layer 130 are sequentially formed on a substrate 100.

[59] The substrate 100 may include sapphire (Al2O3), silicon carbide (SiC), gallium nitride (GaN), indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN), aluminum nitride (AlN), gallium oxide (Ga2O3), or silicon. Specifically, the substrate 100 may be a sapphire substrate. Also, the substrate 100 may be a patterned substrate or a substrate having a surface with a moth-eye structure.

[60] Also, the first semiconductor layer 110 is provided on the substrate 100. The first semiconductor layer 110 preferably has an n conductivity type.

[61] In addition, the active layer 120 formed on the first semiconductor layer 110 may have an SQW structure in which a well layer and a barrier layer are stacked, or an MQW structure in which well layers and barrier layers are alternately stacked.

[62] The second semiconductor layer 130 is provided on the active layer 120. The second semiconductor layer 130 preferably has a p conductivity type.

[63] Furthermore, materials and constructions of the first semiconductor layer 110, the

active layer 120, and the second semiconductor layer 130 are the same as described with reference to FIG. 3, and thus a description thereof is omitted.

[64] In addition, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are formed using an epitaxial growth process. Accordingly, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are preferably formed using an MOCVD process.

[65] Referring to FIG. 5, portions of the active layer 120 and the second semiconductor layer 130 are removed using an ordinary etching process. Thus, a portion of the first semiconductor layer 110 is exposed. Due to the etching process, a top surface of the first semiconductor layer 110 is exposed, and side surfaces of the active layer 120 and the second semiconductor layer 130 are exposed. Accordingly, a trench or a hole may be formed by removing the portions of the active layer 120 and the second semiconductor layer 130 using the etching process. That is, a mesa region 150 etched from the surface of the second semiconductor layer 130 of FIG. 5 to the surface of the first semiconductor layer 110 may be a stripe type having a trench shape or a hole type.

[66] In addition, when the mesa region 150 is the stripe type, the mesa region 150 may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region 150 has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. Also, when the mesa region 150 is a hole type having a roughly circular shape, the mesa region 150 may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region 150 has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. When the profile is inclined at an angle of less than 20°, a width of the mesa region 150 greatly increases upward. Accordingly, convergence of light generated is degraded due to an emission structure. Also, when the profile is inclined at an angle of more than 70°, the mesa region 150 has an approximately vertical profile. Accordingly, the effect of reflection of generated light by sidewalls of layers become immaterial.

[67] Referring to FIG. 6, a photoresist pattern 160 is formed on the first semiconductor layer 110 exposed by forming a bottom surface of the mesa region. The photoresist pattern 160 may have a vertical profile with respect to the surface of the first semiconductor layer 110. In some embodiments, the photoresist pattern 160 may be formed to have an overhang structure having a bottom surface with a smaller width than a top surface thereof. The photoresist pattern 160 is preferably a negative type. Accordingly, exposed portions are cross-linked. To form the overhang structure, the photoresist pattern 160 is preferably exposed at a predetermined angle. In the case of the overhang structure, a distance between bottom surfaces of the photoresist patterns 160 is

preferably set to be at least about 1 μm greater than or equal to a distance between top surfaces thereof.

[68] Furthermore, the photoresist pattern 160 is preferably provided to cover a portion of the surface of the second semiconductor layer 130. Accordingly, the portion of the top surface of the second semiconductor layer 130 may remain shielded by the photoresist pattern 160.

[69] Referring to FIG. 7, a reflective metal layer 142 and a conductive barrier layer 144 are sequentially stacked on the second semiconductor layer 130 to form a reflection pattern 140. Also, in some embodiments, an ohmic contact layer 141 may be formed under the reflective metal layer 142, and a stress relaxation layer 143 may be additionally formed between the reflective metal layer 142 and the conductive barrier layer 144.

[70] The reflective metal layer 142 includes Al, an Al alloy, Ag, or a Ag alloy. The reflective metal layer 142 may be formed using an ordinary metal deposition process. However, the reflective metal layer 142 is preferably formed using an electronic beam (e-beam) evaporation process capable of moving most metal atoms or ions onto the surface of the second semiconductor layer 130 in a vertical direction. Thus, the metal atoms or ions may have anisotropic etching characteristics and enter a space between the photoresist patterns 160 to form the reflective metal layer 142.

[71] The reflective metal layer 142 preferably has a thickness of about 100 nm to about 1 μm. When the reflective metal layer 142 has a thickness of less than about 100 nm, light generated in the active layer 120 is not smoothly reflected. Also, when the reflective metal layer 142 has a thickness of more than about 1 μm, process loss may occur due to an excessive process time.

[72] The ohmic contact layer 141 may be formed before forming the reflective metal layer 142, as needed. The ohmic contact layer 141 may include Ni, Pt, ITO, or ZnO. Also, the ohmic contact layer 141 is preferably formed to a thickness of about 0.1 nm to about 20 nm. When the ohmic contact layer 141 has a thickness of less than about 0.1 nm, sufficient ohmic characteristics cannot be ensured due to a very small layer thickness. Also, when the ohmic contact layer 141 has a thickness of more than about 20 nm, the transmitted amount of light is reduced, thus relaxation the quantity of light reflected by the reflective metal layer 142 disposed on the ohmic contact layer 141.

[73] The stress relaxation layer 143 is formed on the reflective metal layer 142.

[74] The stress relaxation layer 143 may be formed using an ordinary metal deposition process, but is preferably formed using an e-beam evaporation method having high directionality during a deposition process. That is, metal atoms or ions evaporated by e-beams may have directionality and anisotropy in a space between the photoresist patterns 160, and the stress relaxation layer 143 may be formed of a metal layer. Also,

the stress relaxation layer 143 may have a lower coefficient of thermal expansion than the reflective metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144 of FIG. 3. Accordingly, a material forming the stress relaxation layer 143 may be selected differently according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144.

[75] When the reflective metal layer 142 and the stress relaxation layer 143 are formed using an e-beam evaporation method, a side surface of the reflective metal layer 142 and a side surface of the stress relaxation layer 143 are exposed. Also, the reflective metal layer 142 and the stress relaxation layer 143 corresponding to an open upper region of the photoresist pattern 160 are formed using an anisotropic deposition process.

[76] Also, in an e-beam evaporation process, upper layers are formed along a profile of a side surface of the stress relaxation layer 143, but the upper layers are provided to cover or shield lower layers. A side surface of a structure including the stress relaxation layer 143 or the reflective metal layer 142 formed using the e-beam evaporation process is preferably inclined at an angle α of about 5° to about 45°.

[77] In addition, FIG. 7 illustrates a state in which formation of a metal on the photoresist pattern 160 is omitted during the formation of the reflective metal layer 142 and the stress relaxation layer 143.

[78] Subsequently, a conductive barrier layer 144 is formed through the opened region of the photoresist pattern 160.

[79] The conductive barrier layer 144 includes W, TiW, Mo, Cr, Ni, Pt, Rh, Pd, or Ti. In particular, a material forming the conductive barrier layer 144 may vary according to selected materials forming the reflective metal layer 142 and the stress relaxation layer 143.

[80] The conductive barrier layer 144 is formed on the stress relaxation layer 143 and shields side surfaces of the reflective metal layer 142 or the stress relaxation layer 143. Accordingly, a metal forming the reflective metal layer 142 is prevented from diffusing into the second semiconductor layer 130 due to lateral diffusion. The formation of the conductive barrier layer 144 is performed using an ordinary metal deposition process. However, the conductive barrier layer 144 is preferably formed using an isotropic etching process. This is because the conductive barrier layer 144 is configured to surround the side surfaces of the stress relaxation layer 143 and the reflective metal layer 142. For example, the conductive barrier layer 144 may be formed using a sputtering process.

[81] In addition, the conductive barrier layer 144 may be a single layer formed to a thickness of about 100 nm or more by selecting a specific metal. Also, the conductive barrier layer 144 may be formed by alternately selecting at least two metal materials,

and each of layers forming the conductive barrier layer 144 may be formed to a thickness of about 20 nm or more. For example, the conductive barrier layer 144 may be formed by alternately depositing a TiW layer having a thickness of about 50 nm and a Ni layer or Ti layer having a thickness of about 50 nm.

[82] In particular, the conductive barrier layer 144 has a different thickness according to a state or gradient of an underlying layer, and is formed to extend to an upper portion of the second semiconductor layer 130. Since a gradient α of a side surface of the underlying layer has an angle of about 45° or less, occurrence of cracks in the conductive barrier layer 144 due to sharp gradient is prevented.

[83] Furthermore, a Ni/Au/Ti layer may be additionally formed on the conductive barrier layer 144 to enable stable contact of the conductive barrier layer 144 with a subsequent material.

[84] As described above, a material forming the stress relaxation layer 143 may be selected according to materials forming the reflective metal layer 142 and the conductive barrier layer 144. This is because a coefficient of thermal expansion of the stress relaxation layer 143 is higher than that of the conductive barrier layer 144 and lower than that of the reflective metal layer 142. Accordingly, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Ti, Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer 143 may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag. Furthermore, when the reflective metal layer 142 includes Ag or a Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or a Ag alloy, and the conductive barrier layer 144 includes Pt or Ni, the stress relaxation layer 143 may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination formed of Ni, Au, or Cu.

[85] Referring to FIG. 8, the photoresist pattern 160 is removed. Accordingly, the underlying second semiconductor layer 130 and the reflection pattern 140 disposed thereon are exposed. Also, the mesa region 150 is exposed by removing the photoresist pattern 160. This is the same as described with reference to FIG. 3.

[86] Due to the above-described processes, the reflection pattern 140 is formed on the second semiconductor layer 130. The reflection pattern 140 includes a reflective metal layer 142, a stress relaxation layer 143, and a conductive barrier layer 144. The stress relaxation layer 143 has a lower coefficient of thermal expansion than the reflective

metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144. Accordingly, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 is absorbed in the stress relaxation layer 143.

[87] In addition, the conductive barrier layer 144, which is formed on the reflective metal layer 142 or the stress relaxation layer 143, has a different thickness according to the shape and kind of an underlying layer. For example, a thickness t1 of the conductive barrier layer 144 formed on the surface of the reflective metal layer 142 or the stress relaxation layer 143 is greater than a thickness t3 of the conductive barrier layer 144 formed on the surface of the second semiconductor layer 130. Also, the thickness t3 is greater than a thickness t2 of the conductive barrier layer 144 formed on side surfaces of the reflective metal layer 142 or the stress relaxation layer 143.

[88] The difference in thickness is a result obtained by performing an isotropic deposition process after a photoresist pattern having an overhang structure is formed. That is, deposition is performed to the highest extent on a top surface of the reflective metal layer 142 or stress relaxation layer 144, which is opened by the photoresist pattern, and deposition may be performed to a relatively high extent on a surface of the second semiconductor layer 130 because the second semiconductor layer 130 has a planar structure. In contrast, since a side surface of the reflective metal layer 142 or the stress relaxation layer 143 has a predetermined inclination and a deposited metal should be adhered to sidewalls of the reflective metal layer 142 or the stress relaxation layer 143, deposition is performed to a relatively low extent on the side surface of the reflective metal layer 142 or the stress relaxation layer 143.

[89] Furthermore, the side surface of the reflective metal layer 142 or the stress relaxation layer 143 is formed at an inclination angle α of about 5° to about 45°. A required inclination angle may be formed by controlling an angle of a substrate during an e-beam evaporation process. That is, by orienting the substrate at a predetermined angle with respect to an imaginary direction in which metal ions or particles are predicted to proceed, the inclination angle α of the side surface of the reflective metal layer 142 or the stress relaxation layer 143 may be controlled. By setting the inclination angle α of the side surface, occurrence of cracks in a conductive barrier layer 144 that will be formed subsequently is prevented.

[90]

[91] Embodiment 2

[92] FIGS. 9 through 18 are plan views and cross-sectional views illustrating a method of manufacturing an LED module according to a second exemplary embodiment of the present invention.

[93] Referring to FIGS. 9 and 10, a cross-sectional view obtained by cutting a plan view

of FIG. 9 in a direction A-A' is illustrated in FIG. 10.

[94] That is, a first semiconductor layer 110, an active layer 120, and a second semiconductor layer 130 are sequentially stacked on a substrate 100, and a mesa region 150 is formed using an etching process. A portion of a surface of the first semiconductor layer 110 is exposed through the mesa region 150. Also, a reflection pattern 140 is formed on the second semiconductor layer 130 as shown in Embodiment 1.

[95] In the drawings of the present embodiment, the reflection pattern 140 is exaggerated for brevity. The exaggerated reflection pattern 140 is the reflection pattern 140 formed according to Embodiment 1. However, the present invention is not limited thereto, and the reflection pattern 140 may be formed using other method.

[96] Also, the substrate 100 may be a substrate on which surface treatment is not performed, or a patterned substrate. Also, a surface of the substrate 100 may have a moth-eye structure. For example, pointed structures 100a may be densely disposed on the surface of the substrate 100. Alternatively, the substrate 100 may have a protrusion protruding in a roughly hemispherical shape, and pointed structures may be densely disposed on the protrusion.

[97] Referring to FIGS. 11 and 12, a first insulating layer 200 is formed on the resultant structure of FIG. 9. The first insulating layer 200 is preferably formed of a transparent nonconductor. Accordingly, silicon oxide may be used as the first insulating layer 200. The first insulating layer 200 is patterned using an ordinary photoresist process. By patterning the first insulating layer 200, the first semiconductor layer 110 formed in the mesa region 150 is exposed, and a portion of the reflection pattern 140 is exposed. A region in which the exposed reflection pattern 140 and the first insulating layer 200 shielding a portion of the reflection pattern 140 are formed will be referred to as a first pad region 205.

[98] This will be apparent from FIG. 12, which illustrates a cross-sectional view obtained by cutting a plan view of FIG. 11 in a direction A1-A1' and a cross-sectional view obtained by cutting the plan view of FIG. 11 in a direction B1-B1'.

[99] To begin with, on analysis of the cross-sectional view taken along the direction A1-A1', the first insulating layer 200 is provided in a patterned shape on the reflection pattern 140 to expose a portion of the reflection pattern 140. Also, the first insulating layer 200 is opened in the mesa region 150 to expose the first semiconductor layer 110. In particular, the reflection pattern 140 opened by the first insulating layer 200 in the first pad region 205 may be provided in the form of a hole 200a as shown in FIG. 12. However, the present invention is not limited thereto, and the reflection pattern 140 opened by the first insulating layer 200 in the first pad region 205 may be a stripe form.

[100] In addition, on analysis of the cross-sectional view taken along the direction B1-B1',

the first insulating layer 200 completely shields the reflection pattern 140. In contrast, the first semiconductor layer 110 is exposed in the mesa region 150.

[101] Referring to FIGS. 13 and 14, a conductive reflection layer 210 is formed.

[102] Referring to FIG. 13, the conductive reflection layer 210 is coated on the entire surface of the resultant structure of FIG. 11, and includes an opening 210a. The first pad region 205 is exposed within the opening 210a. Also, the conductive reflection layer 210 is also formed in the mesa region 150 and electrically connected to the first semiconductor layer 110.

[103] Referring to FIG. 14, a cross-sectional view obtained by cutting a plan view of FIG. 13 along a line A2-A2' and a cross-sectional view obtained by cutting the plan view of FIG. 13 along a line B2-B2' are shown.

[104] To begin with, on analysis of the cross-sectional view taken along the line A2-A2', the conductive reflection layer 210 is formed on the first insulating layer 200 and the exposed first semiconductor layer 110.

[105] Accordingly, the conductive reflection layer 210 is coated on the entire surface except the first pad region 205, and formed on the first semiconductor layer 110 exposed in the mesa region 150 and electrically connected to the first semiconductor layer 110.

[106] The conductive reflection layer 210 is formed of a conductive material. The conductive reflection layer 210 may include Al. Accordingly, the first semiconductor layer 110 and the conductive reflection layer 210 are electrically connected, and the reflection pattern 140 is electrically insulated from the conductive reflection layer 210 by the first insulating layer 200.

[107] In addition, a reflection barrier layer (not shown) may be formed on the conductive reflection layer 210. The reflection barrier layer prevents diffusion of a metal forming the conductive reflection layer 210. The reflection barrier layer may be a single layer formed of Ni, Cr, or Au, or a combination thereof. The reflection barrier layer is preferably a combination formed of Ti/Al/Ti/Ni/Au. Also, an adhesive layer (not shown) may be further provided under the conductive reflection layer 210. The adhesive layer may include Ti, Cr, or Ni.

[108] The formation of the conductive reflection layer 210 may be performed by stacking the conductive reflection layer 210 and patterning the conductive reflection layer 210 using an etching process. In addition, the conductive reflection layer 210 may be formed using a lift-off process. That is, photoresist is coated on the first pad region 205 in which the portion of the reflection pattern 140 is exposed, and the conductive reflection layer 210 is formed using an ordinary deposition process. Subsequently, by removing the photoresist from the first pad region 205, the conductive reflection layer 210 is formed to expose the first pad region 205.

[109] Referring to FIGS. 15 and 16, a second insulating layer 220 is formed on the resultant structure of FIG. 13.

[110] Initially, referring to a plan view of FIG. 15, the second insulating layer 220 includes first holes 220a and second holes 220b. The first holes 220a are formed in the first pad region 205, and an underlying second pad region 225 is defined by the second holes 220b. A portion of the conductive reflection layer 210 is exposed by the second holes 220b formed in the second pad region 225. When a reflection barrier layer is formed on the conductive reflection layer 210, a portion of the reflection barrier layer may be exposed by the second holes 220b formed in the second pad region 225.

[111] In FIG. 15, the number of first holes 220a is preferably equal to or greater than the number of second holes 220b. This facilitates diffusion of current through the reflection pattern 140 exposed by the first holes 220a. Since the second semiconductor layer 130 is generally a p-type semiconductor layer, division of current into the p-type semiconductor layer is problematic during application of current. Accordingly, by controlling the number of first holes 220a to be equal to or greater than the number of second holes 220b, current may be smoothly divided into the second semiconductor layer 130.

[112] This will be clearly described with reference to a cross-sectional view of FIG. 16.

[113] FIG. 16 illustrates cross-sectional views obtained by cutting the plan view of FIG. 15 along lines A3-A3', B3-B3', and C-C'.

[114] The line A3-A3' crosses the first pad region 205, and the second insulating layer 220 is formed on the conductive reflection layer 210 in the cross-sectional view taken along the line A3-A3'. When a reflection barrier layer is formed on the conductive reflection layer 210, the second insulating layer 220 is preferably formed on the reflection barrier layer. The second insulating layer 220 has the first holes 220a in the first pad region 205, and is also formed on the mesa region 150. Also, the second insulating layer 220 may be formed on the first insulating layer 200 formed on the first pad region 205. However, in some embodiments, the formation of the second insulating layer 220 on the first insulating layer 200 disposed on the first pad region 205 may be omitted.

[115] Also, the line B3-B3' crosses the second pad region 225, and the second insulating layer 220 is formed on the conductive reflection layer 210 disposed on the mesa region 150 in the cross-sectional view taken along the line B3-B3'. In addition, the second insulating layer 220 is formed to expose a portion of the conductive reflection layer 210 formed on the reflection pattern 140 except the mesa region 150. That is, the second insulating layer 220 is provided in a patterned shape on the conductive reflection layer 210 disposed on the reflection pattern 140. Accordingly, the portion of the conductive reflection layer 210 is exposed and defined as the second pad region 225. The exposure

of the portion of the conductive reflection layer 210 may be performed on the mesa region 150, as needed. Furthermore, the second insulating layer 220 forming the second pad region 225 may expose the conductive reflection layer 210 in the shape of the second holes 220b, and expose the conductive reflection layer 210 in a stripe form.

[116] Furthermore, the line C-C' crosses the first pad region 205 and the second pad region 225, and the second insulating layer 220 is formed on the conductive reflection layer 210 in the cross-sectional view taken along the line C-C'. The second insulating layer 220 exposes a portion of the underlying reflection pattern 140 in the first pad region 205, and shields the conductive reflection layer 210 on a space between the first and second pad regions 205 and 225. Also, the second insulating layer 220 is provided in a patterned shape in the second pad region 225 and exposes the underlying conductive reflection layer 210.

[117] The second insulating layer 220 may be formed of any insulating material. Accordingly, an oxide-based insulating material, a nitride-based insulating material, a polymer (e.g., polyimide, Teflon, or parylene) may be used to form the second insulating layer 220.

[118] Referring to FIGS. 17 and 18, a first pad 230 and a second pad 240 are formed on the resultant structure of FIG. 15. The first pad 230 is electrically connected to the exposed reflection pattern 140 of the first pad region 205 in FIGS. 15 and 16. Accordingly, the first pad 230 and the second semiconductor layer 130 are electrically connected. This indicates that the second semiconductor layer 130 is electrically connected to an external power source or power supply line through the first pad 230.

[119] Also, the second pad 240 is electrically connected to the exposed conductive reflection layer 140 of the second pad region 225 in FIGS. 15 and 16. Accordingly, the second pad 240 and the first semiconductor layer 110 are electrically connected. This indicates that the first semiconductor layer 110 is electrically connected to an external power source or power supply line through the second pad 240.

[120] In addition, an area of the first pad 230 electrically connected to the second semiconductor layer 130 is preferably controlled to be greater than an area of the second pad 240 electrically connected to the first semiconductor layer 110. The second semiconductor layer 130 is mostly a p-type semiconductor layer, and emission of heat through the p-type semiconductor layer may be problematic. Accordingly, as a contact area between the second pad 240 and a printed circuit board (PCB) becomes greater than the area of the first pad 230, heat may be smoothly emitted.

[121] The first pad 230 and the second pad 240 may have a double structure including a layer including Ti, Cr, or Ni and a layer including Al, Cu, Ag, or Au. Also, the first pad 230 and the second pad 240 may be formed by patterning photoresist, depositing a metal material between patterned spaces, and removing the deposited metal material

using a lift-off process. Also, a double or single metal layer is formed, and then a pattern is formed using an ordinary photolithography process, and the first and second pads 230 and 240 may be formed by means of a dry etching process or wet etching process using the pattern. Here, an etchant used during the dry or wet etching process may be determined differently according to characteristics of an etched metal material.

[122] In addition, a pad barrier layer (not shown) formed of a conductive material may be formed on the first pad 230 or the second pad 240. The pad barrier layer is provided to prevent diffusion of a metal during a process of bonding or soldering the pads 230 and 240. For example, during the bonding or soldering process, tin (Sn) atoms contained in a bonding metal or soldering material are prevented from diffusing into the pads 230 and 240 and increasing the resistivity of the pads 230 and 240. To this end, the pad barrier layer may include Cr, Ni, Ti W, TiW, Mo, Pt, or a combination thereof.

[123] FIG. 18 illustrates a cross-sectional view obtained by cutting the plan view of FIG. 17 along a line A4-A4', a cross-sectional view obtained by cutting the plan view of FIG. 17 along a line B4-B4', and a cross-sectional view obtained by cutting the plan view of FIG. 17 along a line C1-C1'.

[124] Initially, the line A4-A4' crosses the first pad 230, and the first pad 230 shields a first pad region and is electrically connected to the reflection pattern 140 with reference to the cross-sectional view taken along the line A4-A4'. Accordingly, the second semiconductor layer 130 and the first pad 230 are electrically connected. Also, the first pad 230 may be formed also in a mesa region 150.

[125] In addition, the line B4-B4' crosses the second pad 240, and the second pad 240 is formed on a second pad region with reference to the cross-sectional view taken along the line B4-B4'. Since a portion of a conductive reflection layer 210 is exposed through a patterned second insulating layer 220 in the second pad region, the second pad 240 filling the second pad region is electrically connected to the conductive reflection layer 210. Since the conductive reflection layer 210 is electrically connected to the first semiconductor layer 110 in the mesa region 150, the first semiconductor layer 110 is electrically connected to the second pad 240.

[126] Furthermore, the line C1-C1' crosses the first pad 230 and the second pad 240, and the first semiconductor layer 110, an active layer 120, and the second semiconductor layer 130 formed on a substrate 100 using a mesa etching process have a predetermined inclination angle with respect to the surface of the substrate 100. Also, a first insulating layer 200, the conductive reflection layer 210, and the second insulating layer 220 are sequentially stacked on sidewalls of the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130.

[127] In the first pad region, the first insulating layer 200 or the second insulating layer 220 is formed in a patterned shape, and a portion of the reflection pattern 140 is opened.

Also, the first pad 230 is formed on the first pad region. The first pad 230 is isolated from the second pad 240, which is another pad, by the second insulating layer 220. Accordingly, the first pad 230 is electrically connected to the second semiconductor layer 130 through the reflection pattern 140.

[128] Also, the second insulating layer 220 is formed in a patterned shape in the second pad region, and the conductive reflection layer 210 is opened in a region opened by the second pad 240. Accordingly, the second pad 240 is connected to the conductive reflection layer 210. The conductive reflection layer 210 is connected to the first semiconductor layer 110 in the mesa region 150. Accordingly, the second pad 240 is electrically connected to the first semiconductor layer 110.

[129] In addition, an area of the reflection pattern 140 opend by the first insulating layer 200 or the second insulating layer 220 patterned in the first pad region exceeds an area of the conductive reflection layer 210 opened by the second insulating layer 220 patterned in the second pad region. This is due to the fact that the reflection pattern 140 electrically connected to the first pad 230 is connected to the second semiconductor layer 130, and the conductive reflection layer 210 electrically connected to the second pad 240 is connected to the first semiconductor layer 110. In general, the second semiconductor layer 130 has a p conductivity type. Also, the first semiconductor layer 110 has an n conductivity type. The mobility of holes in a p-type semiconductor layer is lower than the mobility of electrons in an n-type semiconductor layer. Accordingly, a channel in which current is supplied through an electrode is preferably wider in a p type than in an n type.

[130] In addition, the first insulating layer 200 or the second insulating layer 220 patterned on the reflection pattern 140 connected to the second semiconductor layer 130 prevents local current crowding. Direct supply of current through a pad is excluded in high-voltage or high-power conditions. With the first insulating layer 200 or the second insulating layer 220 patterned, the insulating layer 200, 220 screens part of current supplied from the first pad 230 disposed on the insulating layer, and divides the screened current into a space between insulating layers. Thus, uniform current is supplied to the second semiconductor layer 130.

[131] Furthermore, the first insulating layer 200 formed on side surfaces of the active layer 120, the second semiconductor layer 130, and the reflection pattern 140 functions as a reflection plate for light generated in the active layer 120. For instance, when a wavelength of light generated in the active layer is λ, a thickness of the first insulating layer 200 is preferably an integer multiple of $\lambda/4$. Thus, reflection of light may be performed on the surface of the first insulating layer 200, and constructive interference may occur.

[132] For example, when the wavelength of light generated in the active layer 120 has a

center wavelength of about 450 nm, the first insulating layer 200 is preferably formed to a thickness of about 8000 Å to about 9000 Å. Also, the thickness of the second insulating layer 220 is preferably smaller than the thickness of the first insulating layer 200.

[133] In addition, when a flip-chip-type LED module is applied to a PCB, a side surface of the substrate 100 preferably has a rough structure using a sawing or laser cutting process. Light generated in the active layer 120 is easily emitted to the outside through the substrate 100 having the side surface with the rough structure.

[134] In an LED module formed using the above-described processes, pads are formed on a patterned pad region. Thus, local current crowding may be prevented. Also, diffusion of a metal is prevented by the reflection barrier layer provided between the conductive reflection layer 210 and the pads. For instance, a metal forming the conductive reflection layer 210 is prevented from moving to the second pad 240 and increasing the resistivity of the second pad 240. Also, the second semiconductor layer 130 is electrically connected to the first pad 230. A pad barrier layer is formed on each of the pads. The pad barrier layer prevents diffusion of a generated metal during a bonding or soldering process so that the first pad 230 or the second pad 240 can have a high conductivity and be in electrical contact with the outside.

[135]

[136] Embodiment 3

[137] FIG. 19 is a cross-sectional view of an LED package according to a third exemplary embodiment of the present invention.

[138] Referring to FIG. 19, after a final resultant structure described with reference to FIGS. 17 and 18 is separated into respective unit modules, a phosphor layer 300 is formed on side and rear surfaces of each of the unit modules. The formation of the phosphor layer 300 includes re-arranging a plurality of separated unit modules such that the substrate 100 faces upward, and coating a phosphor slurry on the substrate 100. In this case, the phosphor slurry may also be coated on side surfaces of the modules. Subsequently, the phosphor slurry is cured and separation into respective modules is performed.

[139] Meanwhile, a package substrate 400 is provided. A first bonding pad 430 and a second bonding pad 440 may be disposed on the package substrate 400 and spaced apart from one another. A solder resist layer 420 having an opening exposing partial upper regions of the bonding pads 430 and 440 may be disposed on the bonding pads 430 and 440.

[140] The module having the phosphor layer 300 is disposed on the package substrate 400. Thereafter, a first pad 230 and a second pad 240 of the module are electrically connected to the first bonding pad 430 and the second bonding pad 440 using

conductive adhesives 430 and 450.

[141] Furthermore, in the present embodiment, the phosphor layer 300 absorbs light generated in the active layer 120 and generates light having a different wavelength. The phosphor layer 300 may be a single layer or a multi-layered structure. For example, the phosphor layer 300 having wavelength conversion characteristics may have a stack structure of a first phosphor layer (not shown) and a second phosphor layer (not shown). For instance, the first phosphor layer may have a rough shape, and the second phosphor layer may be formed to fill grooves of the first phosphor layer.

[142] In addition, when the phosphor layer 300 has a plurality of wavelength conversion characteristics, the first phosphor layer may be formed of a different material from the second phosphor layer. Alternatively, the first and second phosphor layers may be formed of the same kind of phosphor at different concentrations.

[143] The phosphor layer 300 may be coated or formed of a molding resin using a dispenser. In addition, the phosphor layer 300 may be formed using a spraying process, a molding process, or a printing process or formed using a filling process in vacuum.

[144] While the invention has been shown and described with reference to m certain exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

[145] *Description of Major Symbols in the above Figures

[146] 100: Substrate 110: First semiconductor layer

[147] 120: Active layer 130: Second semiconductor layer

[148] 140: Reflection pattern 141: Ohmic contact layer

[149] 142: Reflection metal layer 143: Stress relaxation layer

[150] 144: Conductive barrier layer 150: Mesa region

[151] 200: First insulating layer 210: Conductive reflection layer

[152] 220: Second insulating layer 230: First pad

[153] 240: Second pad

Claims

[Claim 1] A light emitting diode (LED) module comprising:
an LED having a first semiconductor layer, an active layer, a second semiconductor layer, and a reflection pattern formed on a substrate, and including a mesa region formed to expose the first semiconductor layer;
a first insulating layer formed on the mesa region exposing a portion of a surface of the first semiconductor layer, patterned on the reflection pattern and configured to form a first pad region;
a conductive reflection layer formed on the first insulating layer and the first semiconductor layer exposed in the mesa region;
a second insulating layer formed on the conductive reflection layer and configured to form a second pad region exposing a portion of the conductive reflection layer;
a first pad formed on the first pad region; and
a second pad formed on the second pad region.

[Claim 2] The LED module of claim 1, wherein the first pad region exposes a portion of the reflection pattern through the patterned first insulating layer.

[Claim 3] The LED module of claim 2, wherein the second pad region exposes the portion of the conductive reflection layer through the patterned second insulating layer.

[Claim 4] The LED module of claim 3, wherein an area of the exposed reflection pattern is greater than an area of the exposed conductive reflection layer.

[Claim 5] The LED module of claim 3, wherein the number of holes formed in the first insulating layer formed on the reflection pattern and patterned is equal to or greater than the number of holes formed in the second insulating layer exposing the portion of the conductive reflection layer.

[Claim 6] The LED module of claim 3, wherein an area of the first pad is greater than an area of the second pad.

[Claim 7] The LED module of claim 1, wherein, when a wavelength of light generated in the active layer is λ, a thickness of the first insulating layer is an integer multiple of $\lambda/4$.

[Claim 8] The LED module of claim 1, wherein the reflection pattern comprises:
a reflective metal layer formed on the second semiconductor layer and configured to reflect light; and
a conductive barrier layer configured to shield the reflective metal layer

and continuously extend on the second semiconductor layer.

[Claim 9] The LED module of claim 8, wherein the conductive barrier layer has a different thickness according to an underlying layer.

[Claim 10] The LED module of claim 8, wherein a side surface of the reflective metal layer has an inclination angle of about 5° to about 45° with respect to a surface of the second semiconductor layer.

[Claim 11] A method of manufacturing a light emitting diode (LED) module, comprising:

coating a first insulating layer on a structure in which a first semiconductor layer, an active layer, a second semiconductor layer, and a reflection pattern are formed on a substrate, forming a first pad region by exposing a portion of the reflection pattern, and exposing the first semiconductor layer disposed on a mesa region;

forming a conductive reflection layer on the first insulating layer, electrically connecting the conductive reflection layer to the exposed first semiconductor layer, and maintaining the first pad region in an opened state;

coating a second insulating layer on the conductive reflection layer to expose the reflection pattern disposed in the first pad region, and forming a second pad region exposing a portion of the conductive reflection layer electrically connected to the first semiconductor layer; and

forming a first pad on the first pad region and forming a second pad on the second pad region.

[Claim 12] The method of claim 11, wherein the forming of the structure in which the first semiconductor layer, the active layer, the second semiconductor layer, and the reflection pattern are formed comprises:

sequentially forming the first semiconductor layer, the active layer, and the second semiconductor layer on the substrate;

etching the second semiconductor layer and the active layer to form a mesa region exposing a surface of the first semiconductor layer;

forming a photoresist pattern having an overhang structure on the mesa region, and forming a reflective metal layer on a surface of the second semiconductor layer exposed through a space between photoresist patterns; and

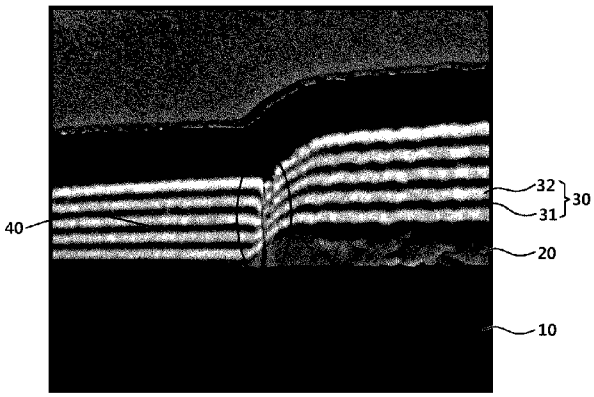
forming a conductive barrier layer on the reflective metal layer,

wherein the conductive barrier layer is continuously formed on the reflective metal layer and the surface of the second semiconductor layer.

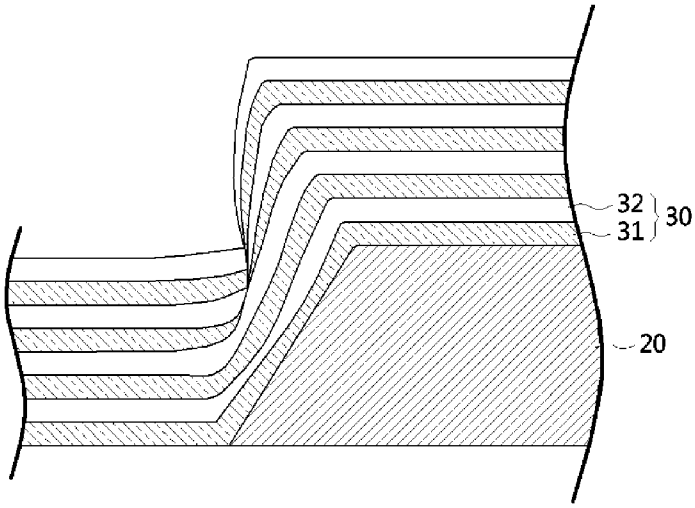
[Claim 13] The method of claim 11, wherein an area of the reflection pattern exposed through the first pad region is greater than an area of the conductive reflection layer exposed through the second pad region.

[Claim 14] The method of claim 11, wherein, when a wavelength of light generated in the active layer is λ, a thickness of the first insulating layer formed on a side surface of the LED module is an integer multiple of λ/4.

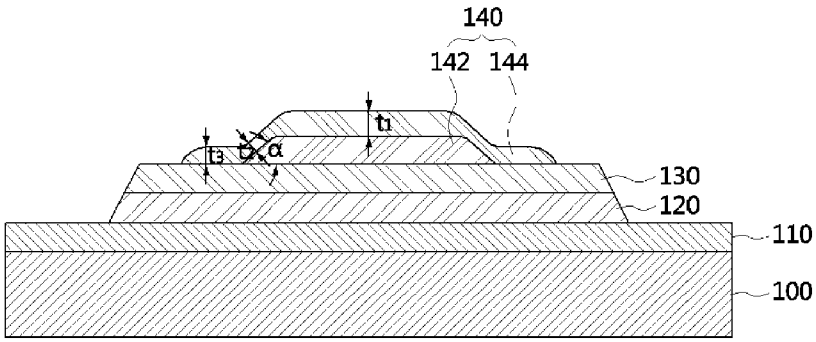
[Fig. 1]



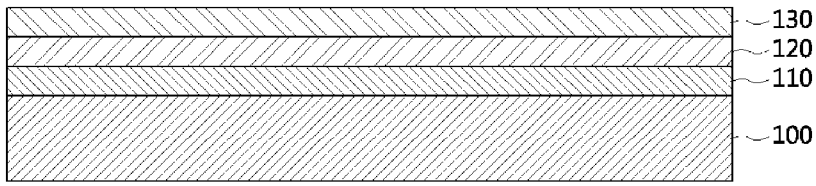
[Fig. 2]



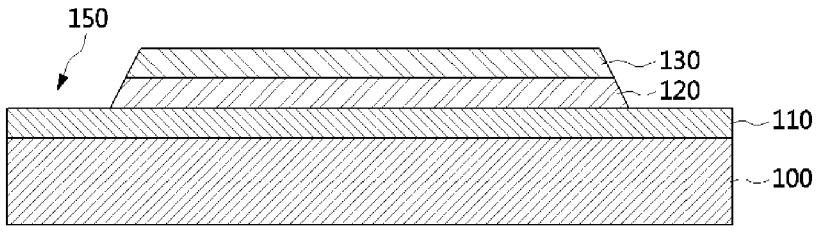
[Fig. 3]



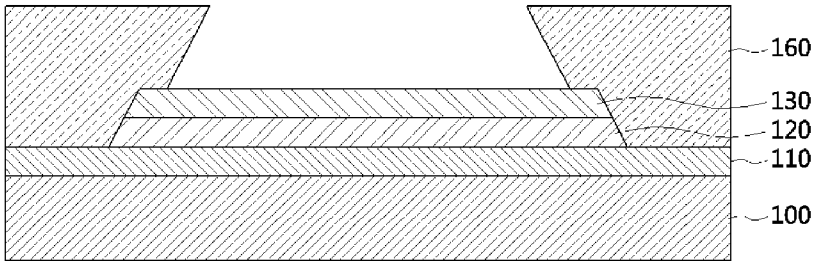
[Fig. 4]



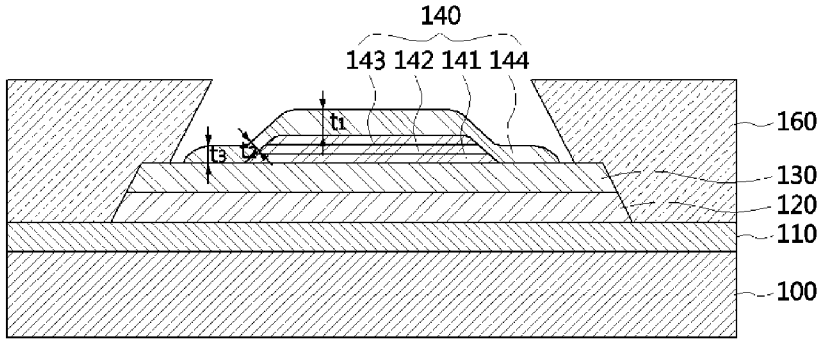
[Fig. 5]



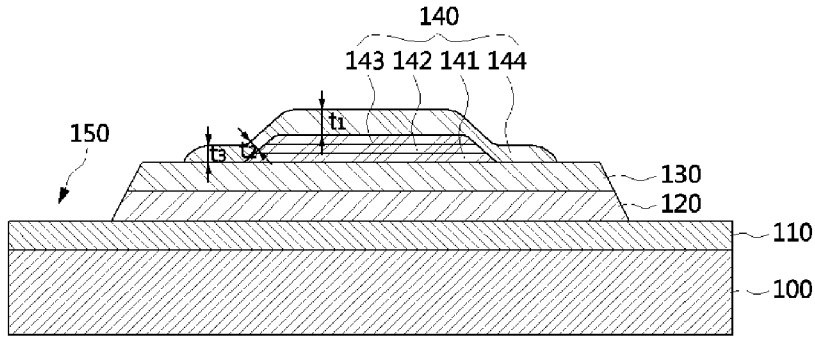
[Fig. 6]



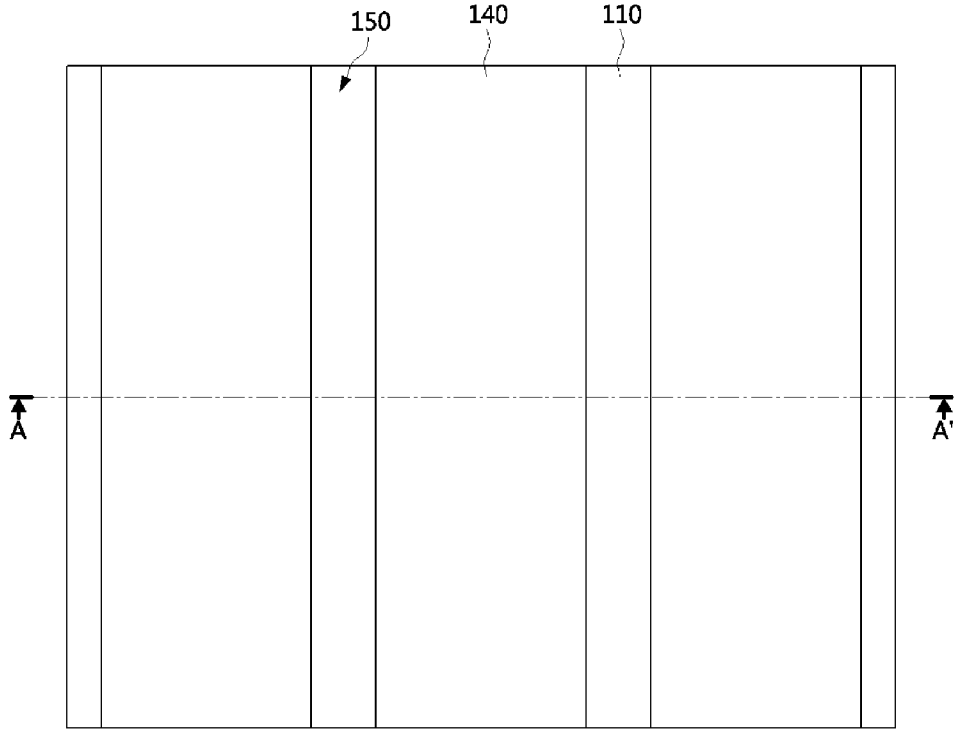
[Fig. 7]



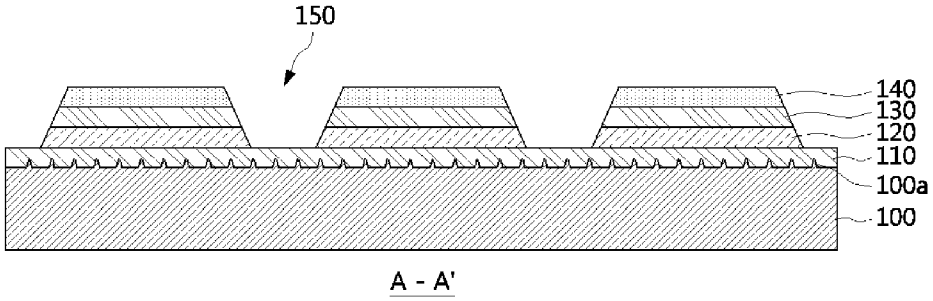
[Fig. 8]



[Fig. 9]

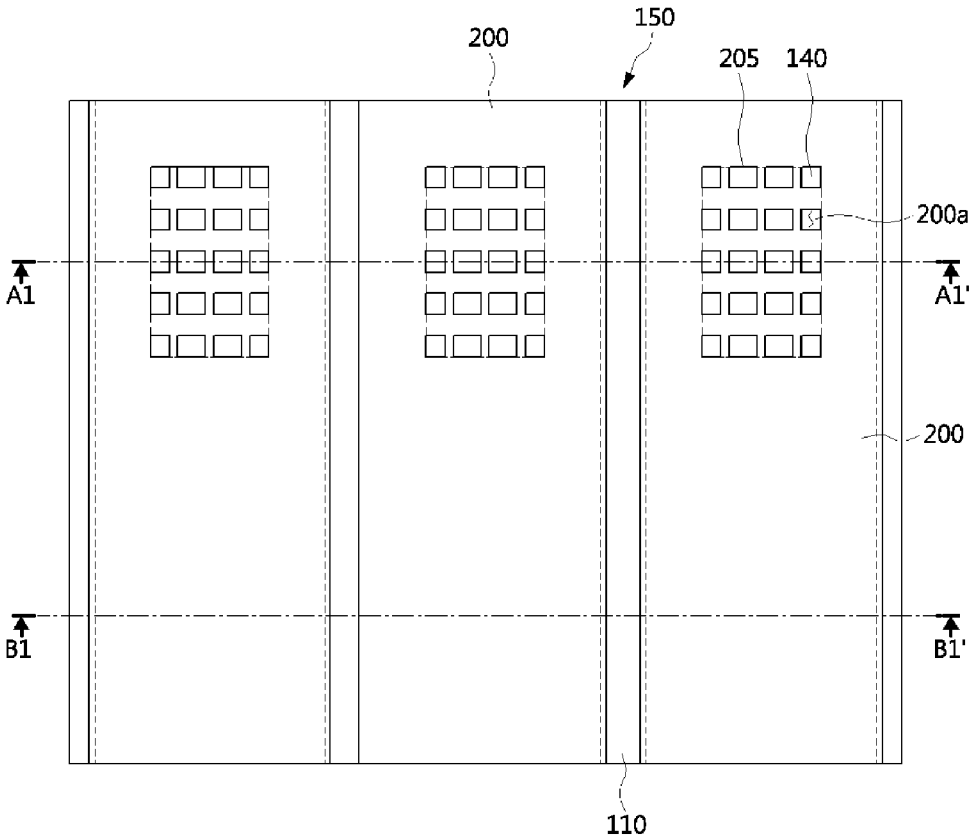


[Fig. 10]

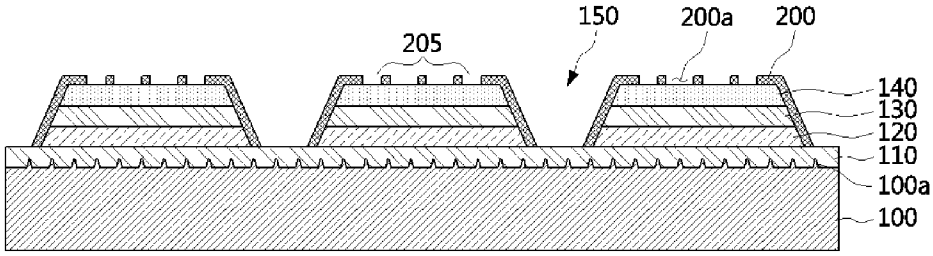


A - A'

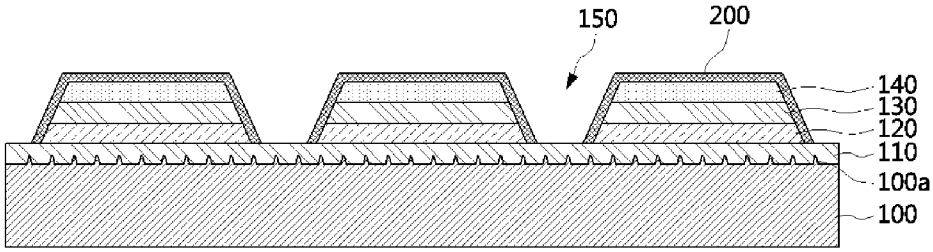
[Fig. 11]



[Fig. 12]

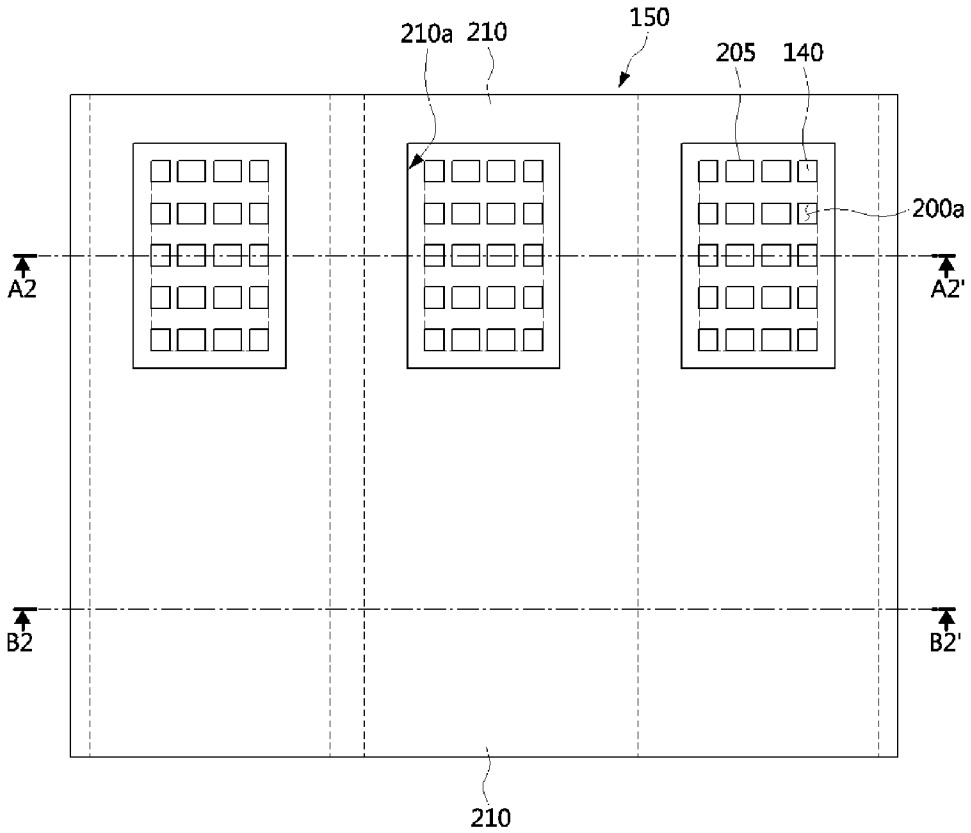


A1 - A1'

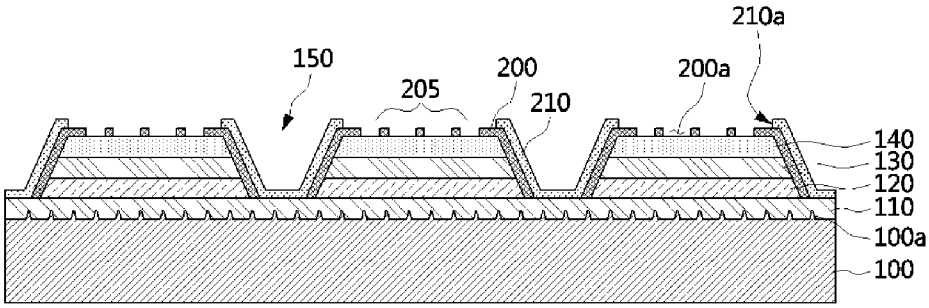


B1 - B1'

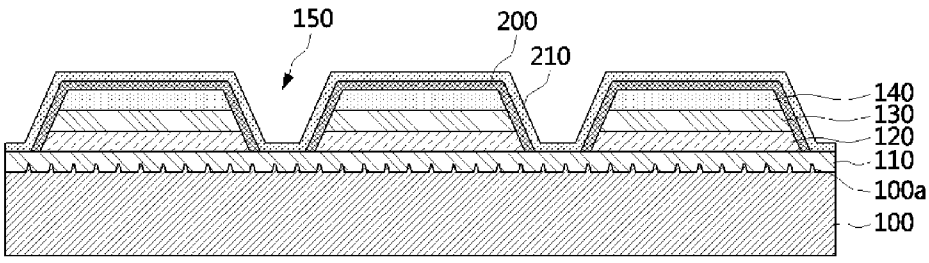
[Fig. 13]



[Fig. 14]

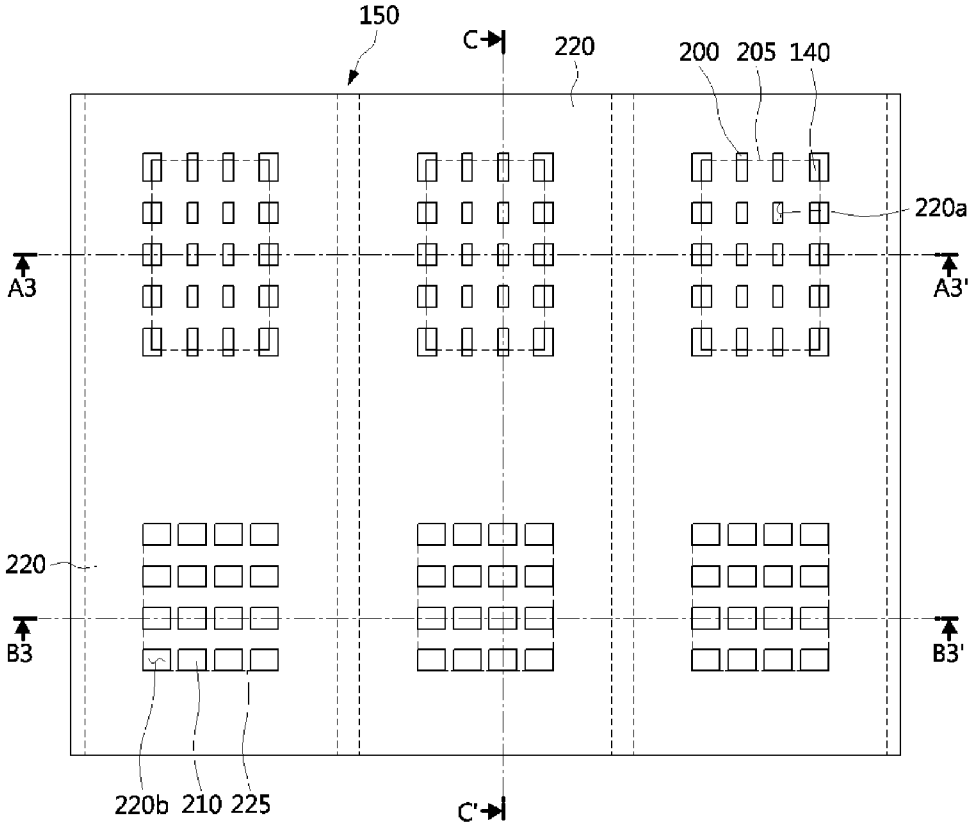


A2 - A2'

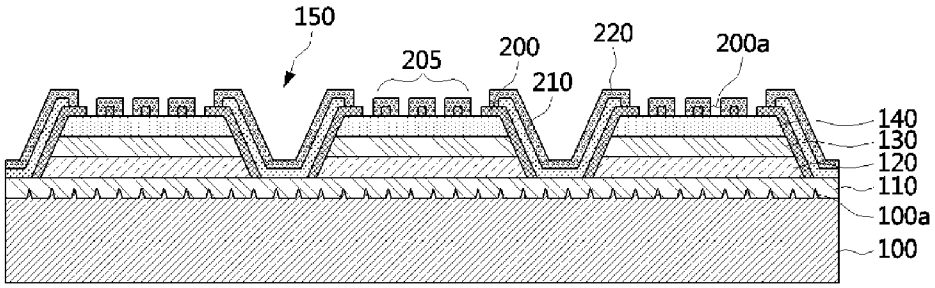


B2 - B2'

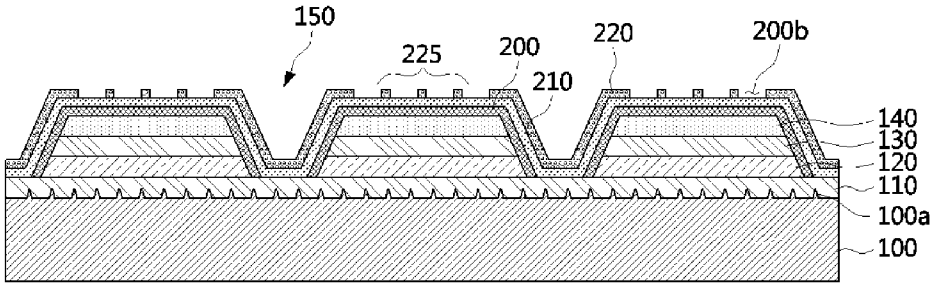
[Fig. 15]



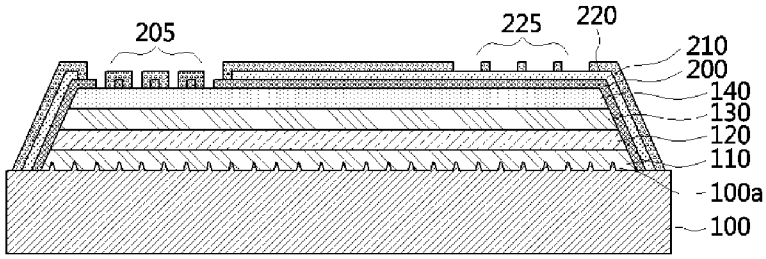
[Fig. 16]



A3 - A3'

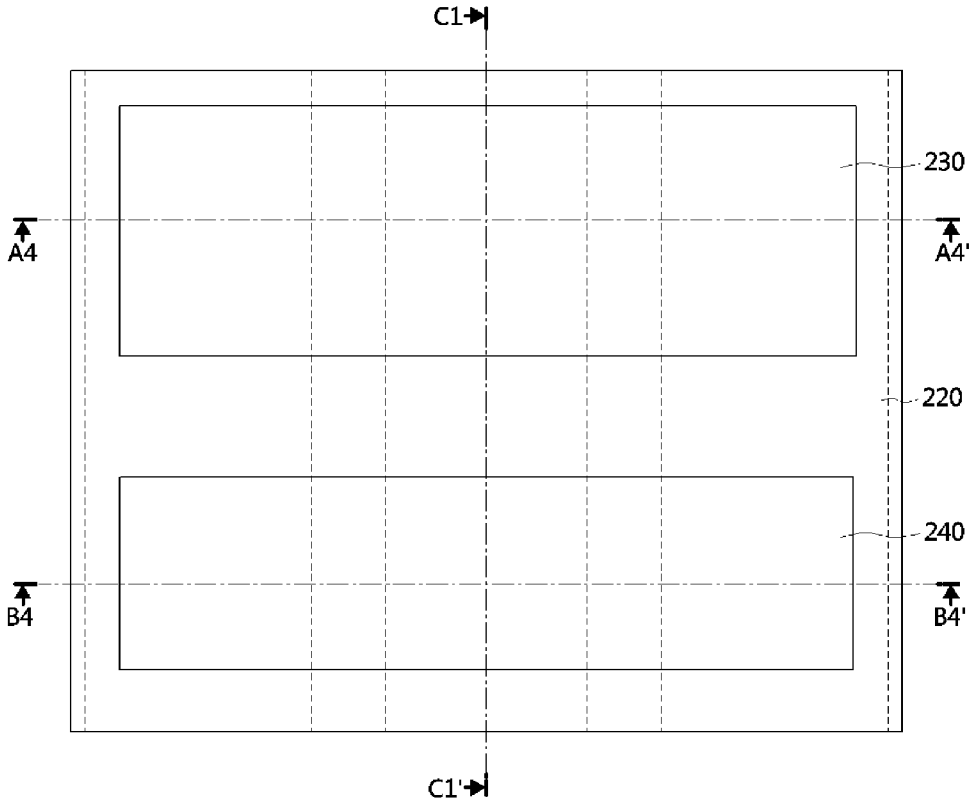


B3 - B3'

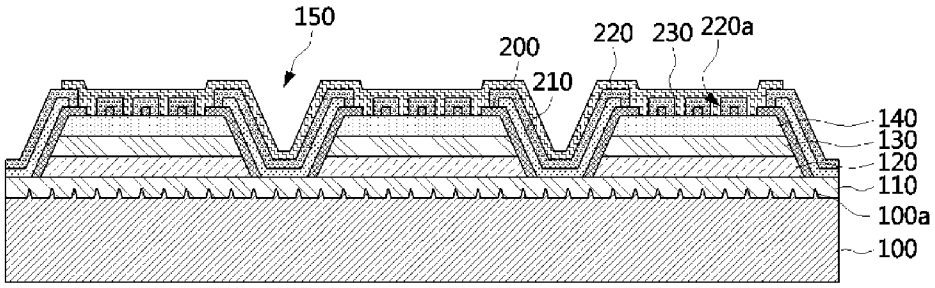


C - C'

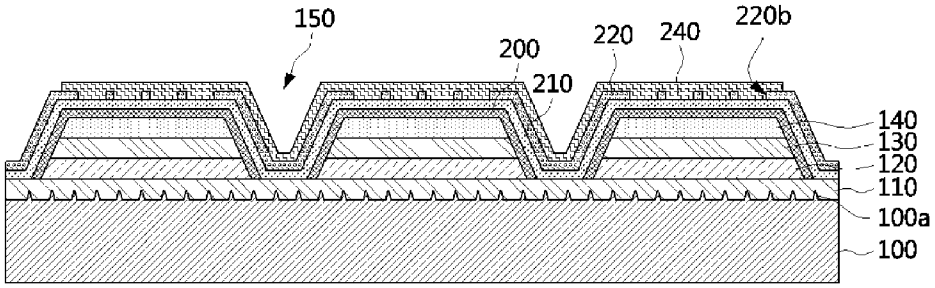
[Fig. 17]



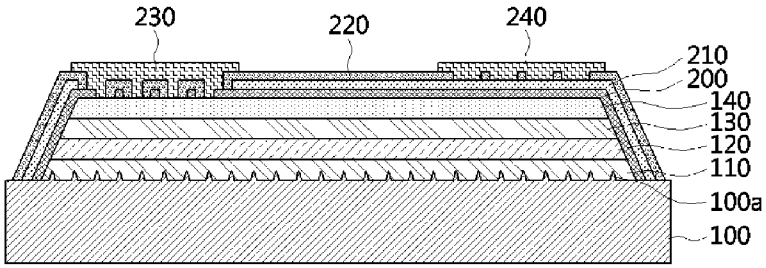
[Fig. 18]



A4 - A4'

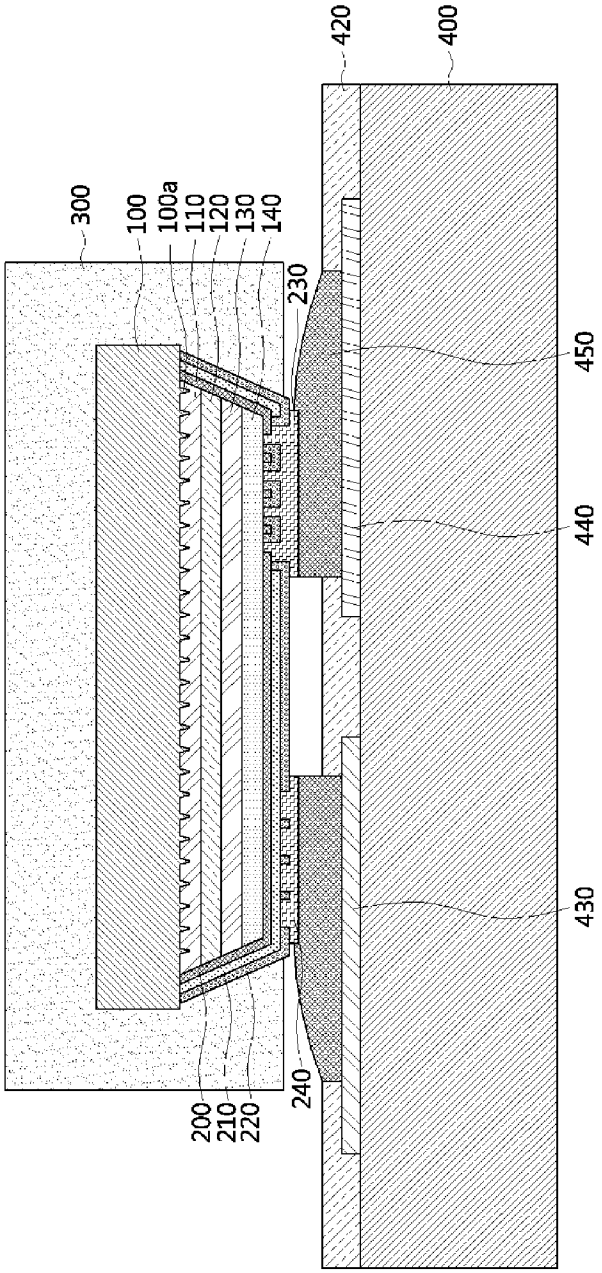


B4 - B4'



C1 - C1'

[Fig. 19]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INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2013/005557

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/46(2010.01)i, H01L 33/44(2010.01)i, H01L 33/62(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 33/46; H01L 21/28; H01L 33/00; H01L 33/60; H01L 33/44; H01L 33/62

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: LED, reflection layer, mesa structure, pad, insulating layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2009-188422 A (STANLEY ELECTRIC CO., LTD.) 20 August 2009 See paragraphs [0020]-[0040], [0055], [0072], claims 1-2 and figures 1A, 12A.	1-3,7,11,14
Y		8,12
A		4-6,9-10,13
Y	JP 2007-080899 A (SHOWA DENKO K.K.) 29 March 2007 See paragraphs [0018]-[0020], figure 1 and claim 1.	8,12
A		1-7,9-11,13-14
A	US 2012-0049219 A1 (MASAO KAMIYA et al.) 01 March 2012 See abstract, paragraphs [0036]-[0053] and figures 1-2B.	1-14
A	US 2007-0262338 A1 (KAZUSHI HIGASHI et al.) 15 November 2007 See paragraphs [0107]-[0111] and figures 9-11.	1-14
A	JP 2006-108161 A (TOYODA GOSEI CO., LTD.) 20 April 2006 See paragraphs [0030]-[0031] and figure 1.	1-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 September 2013 (23.09.2013)	**25 September 2013 (25.09.2013)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2013/005557

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