United States Patent [19]

Weber

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[54] **ANTI-THEFT APPARATUS INCLUDING TURNOVER MODE OF OPERATION**

[75] Inventor: **John A. Weber,** Franklin, Wis.

[73] Assignee: **General Motors Corporation,** Detroit, Mich.

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[21] Appl. No.: **271,141**

[52] **U.S. Cl.** ..... **307/10 AT,** 180/114, 317/134

[51] **Int. Cl.** **B60r 25/00**

[58] **Field of Search** ..... 307/10 AT; 317/134; 340/63; 180/114

[56] **References Cited**

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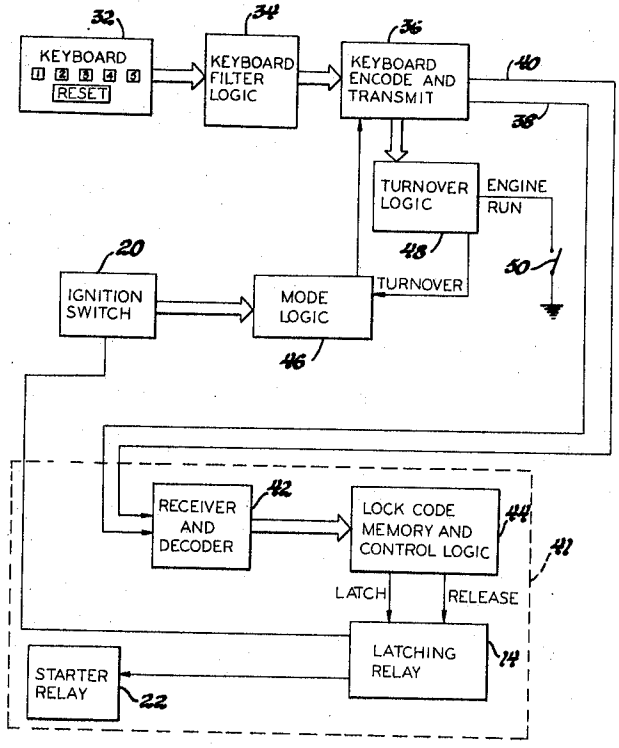
Primary Examiner—J. R. Scott
Assistant Examiner—M. Ginsburg
Attorney—Eugene W. Christen et al.

[57] **ABSTRACT**

Starting of a motor vehicle is controlled from electronic combination lock circuitry which may be placed in a turnover mode of operation after the engine has been started to thereafter permit a predetermined number of engine starts without the entering of the lock combination.

2 Claims, 8 Drawing Figures



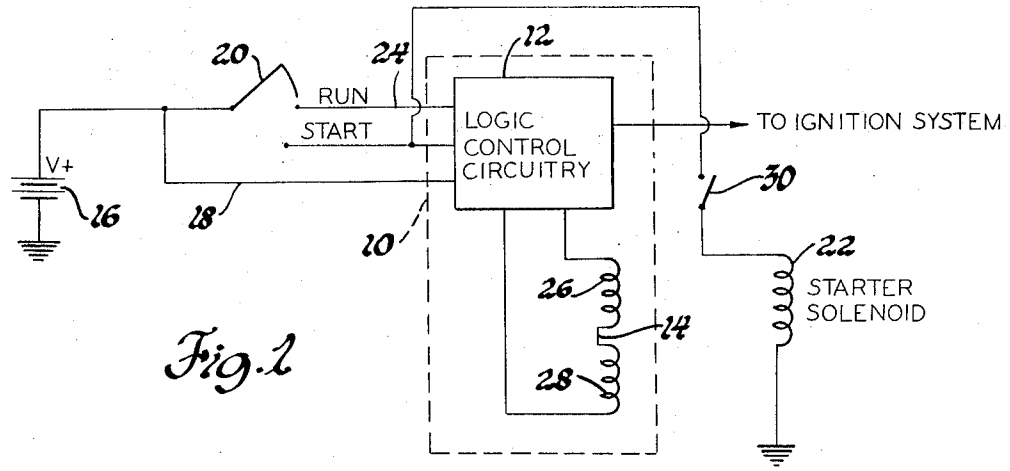

20
24
12
RUN
START
LOGIC
CONTROL
CIRCUITRY
TO IGNITION SYSTEM
V+
16
18
10
30
22
26
14
28
STARTER
SOLENOID

Fig. 1

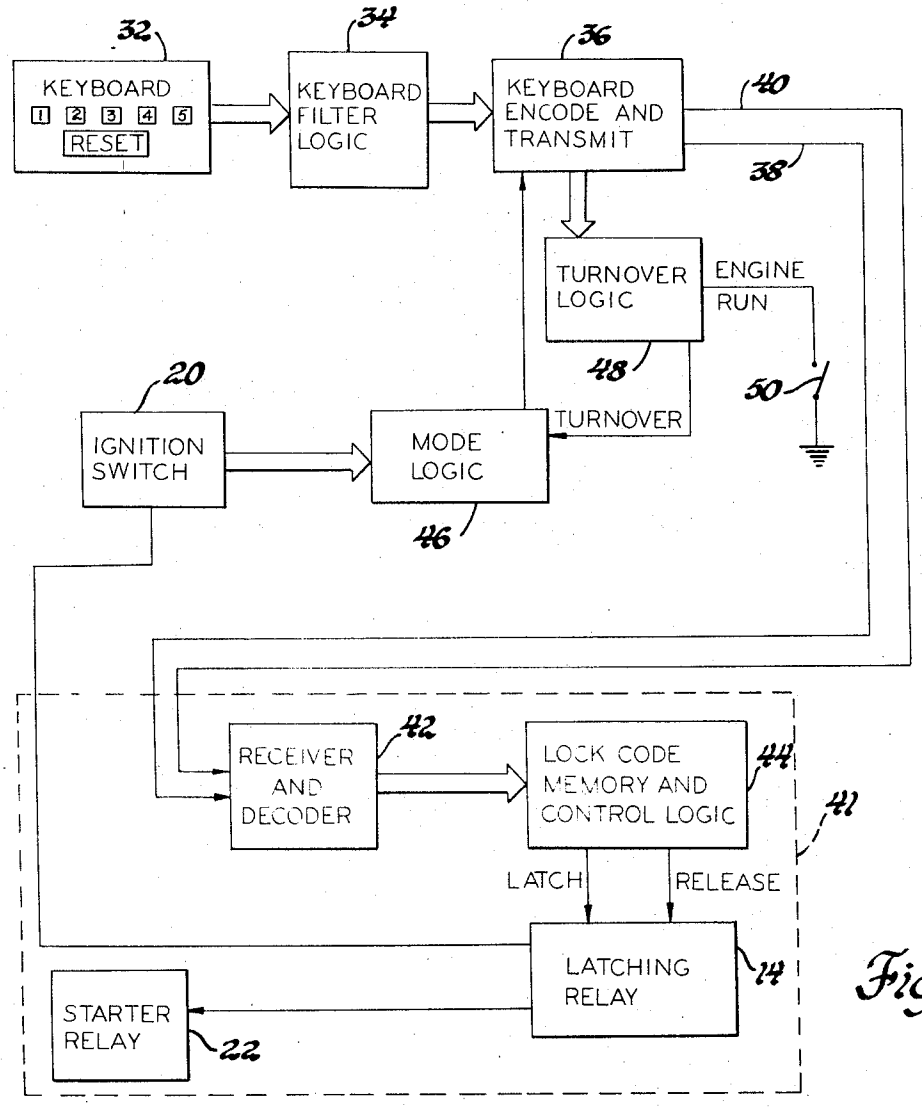

32
34
36
40
KEYBOARD
1 2 3 4 5
RESET
KEYBOARD
FILTER
LOGIC
KEYBOARD
ENCODE AND
TRANSMIT
38
TURNOVER
LOGIC
ENGINE
RUN
48
50
20
IGNITION
SWITCH
MODE
LOGIC
TURNOVER
46
RECEIVER
AND
DECODER
42
LOCK CODE
MEMORY AND
CONTROL LOGIC
44
41
LATCH
RELEASE
LATCHING
RELAY
14
STARTER
RELAY
22

Fig. 2

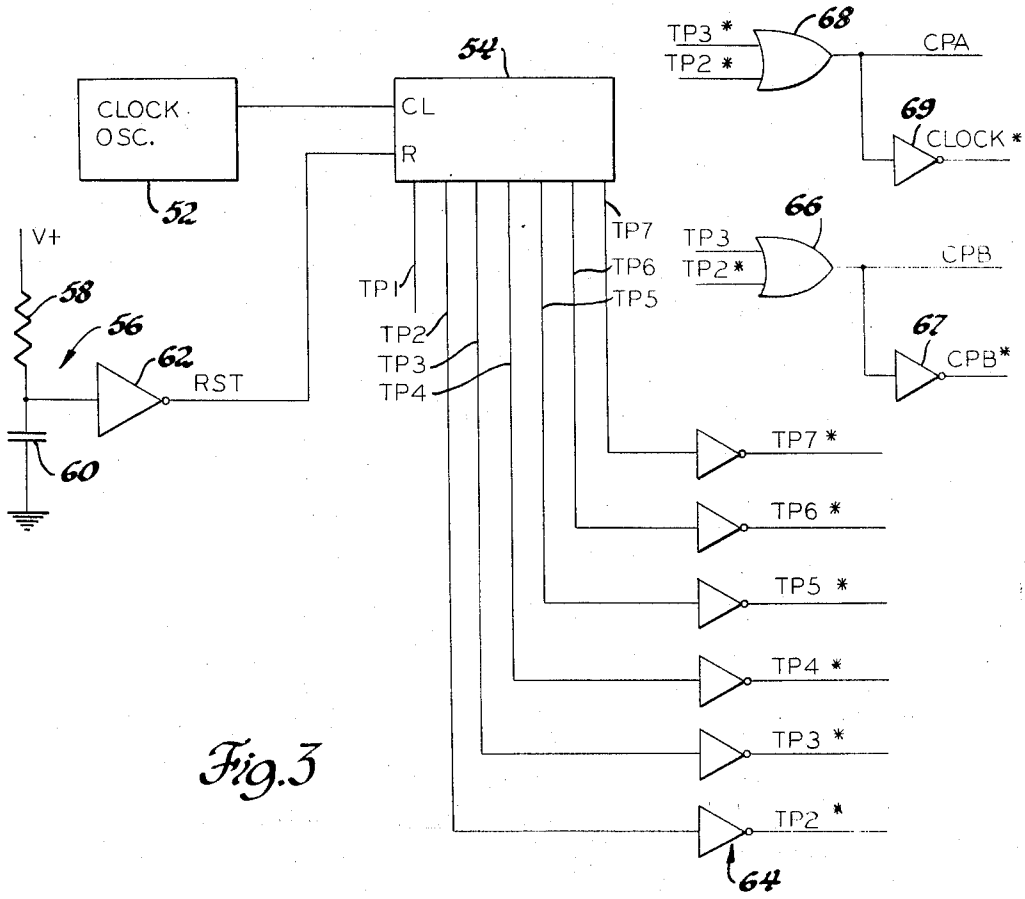

CLOCK OSC.
52
54
CL
R
V+
58
56
62
RST
60
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP3 *
TP2 *
68
CPA
69
CLOCK *
66
TP3
TP2 *
CPB
67
CPB*
TP7 *
TP6 *
TP5 *
TP4 *
TP3 *
TP2 *
64

Fig. 3

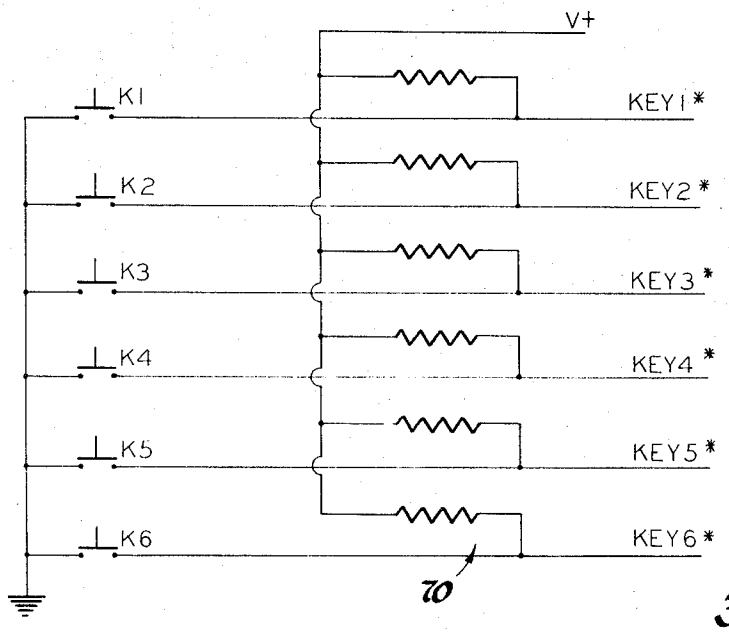

V+
K1
K2
K3
K4
K5
K6
KEY1 *
KEY2 *
KEY3 *
KEY4 *
KEY5 *
KEY6 *
70

Fig. 4

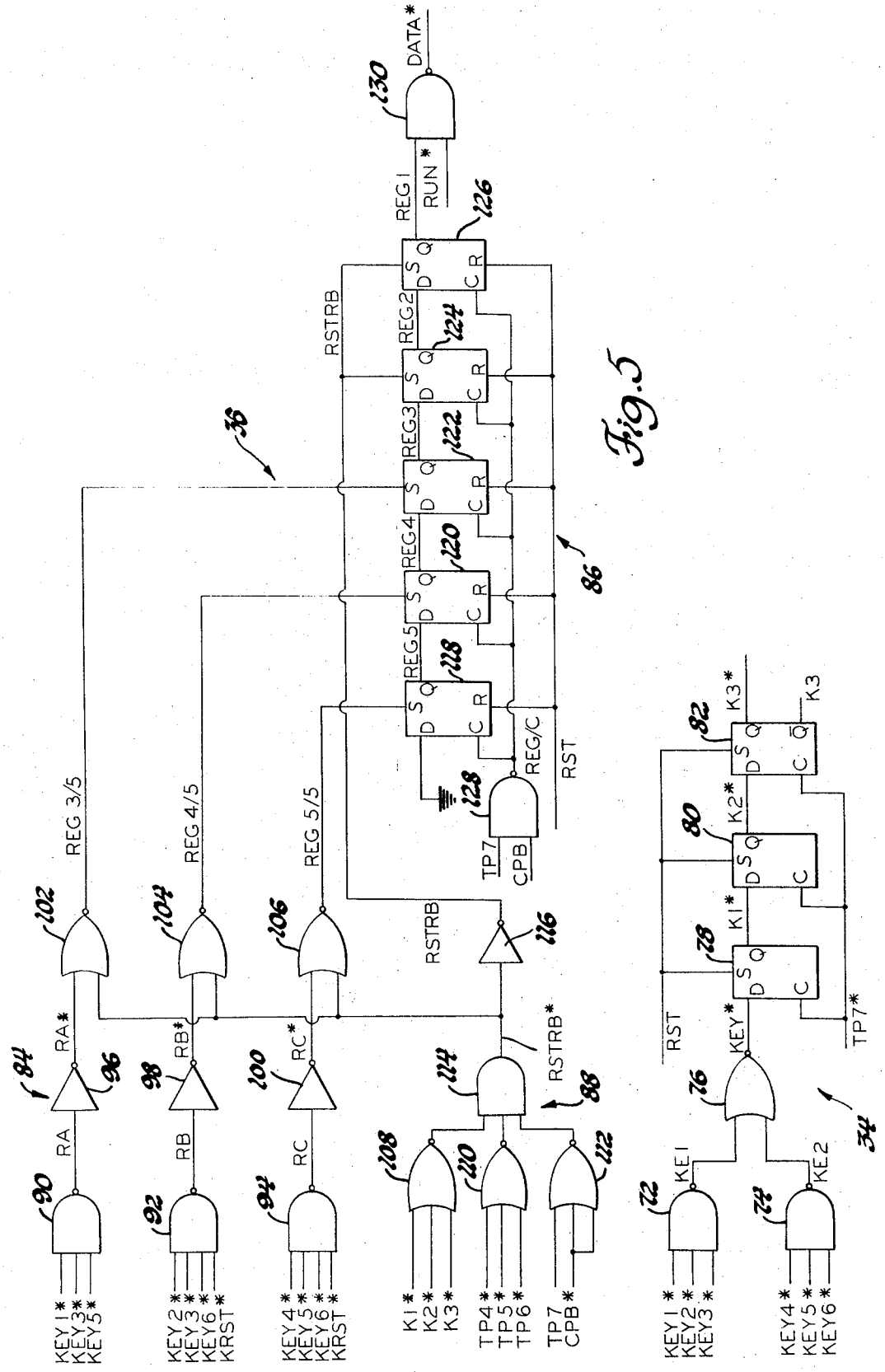

KEY1*
KEY3*
KEY5*
RA
RA*
REG 3/5
KEY2*
KEY3*
KEY6*
KRST*
RB
RB*
REG 4/5
KEY4*
KEY5*
KEY6*
KRST
RC
RC*
REG 5/5
K1*
K2*
K3*
TP4*
TP5*
TP6*
TP7
CPB*
RSTRB
RSTRB*
REG5
REG4
REG3
REG2
REG1
RUN*
DATA*
TP7
CPB
REG/C
RST
K1*
K2*
K3*
KEY*
KE1
KE2
TP7*
36
84
86
88
90
92
94
96
98
100
102
104
106
108
110
112
114
116
118
120
122
124
126
128
130
72
74
76
78
80
82
34

Fig. 5

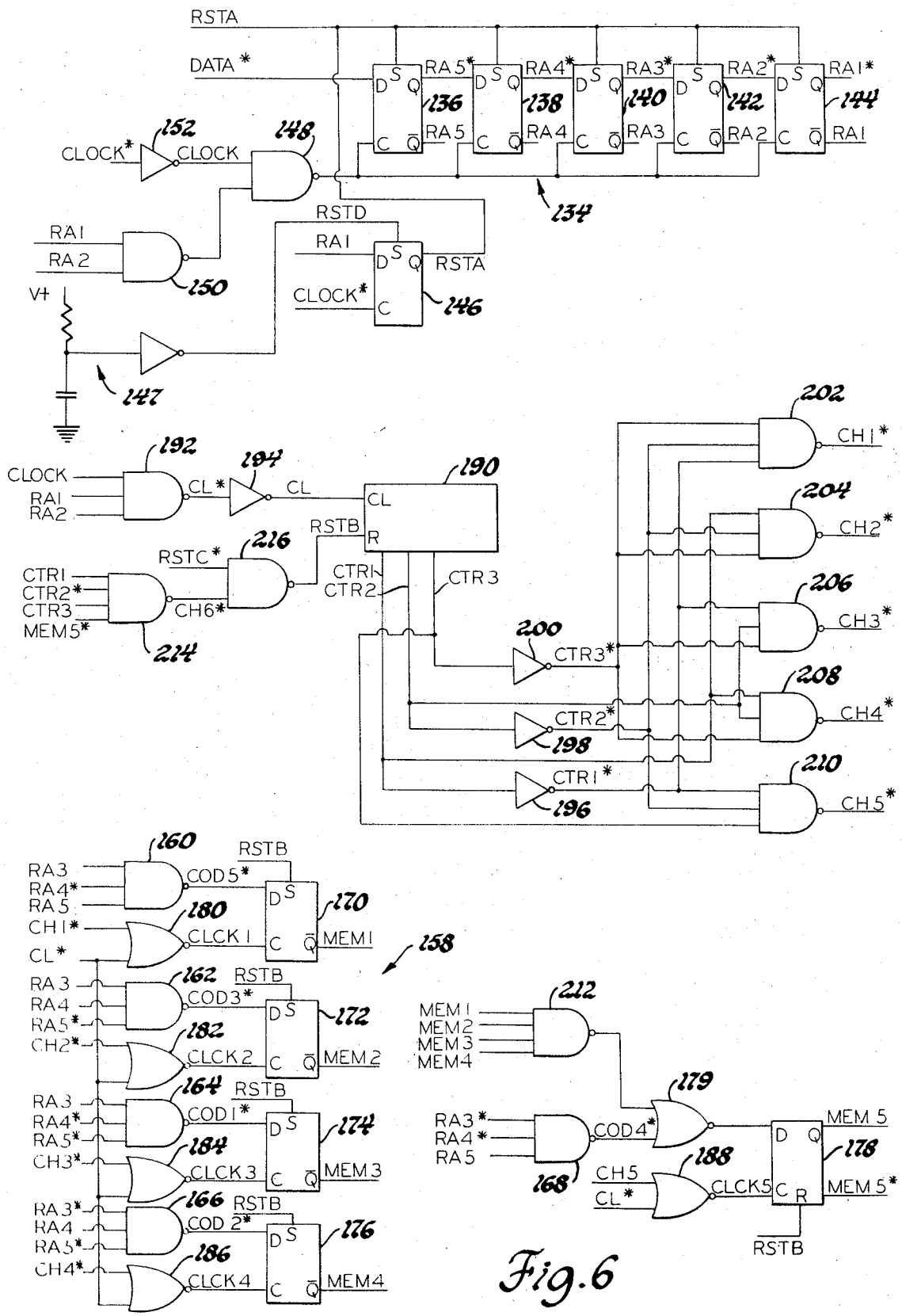

RSTA
DATA*
RA5*
RA4*
RA3*
RA2*
RA1*
136
138
140
142
144
RA5
RA4
RA3
RA2
RA1
CLOCK*
CLOCK
152
148
134
RSTD
RA1
RA2
150
V+
RA1
CLOCK*
RSTA
146
147
202
CH1*
192
194
190
CLOCK
RA1
RA2
CL*
CL
CL
R
RSTB
204
CH2*
RSTC*
216
CTR1
CTR2*
CTR3
MEM5*
CH6*
CTR1
CTR2
CTR3
206
CH3*
200
CTR3*
214
208
CH4*
CTR2*
198
CTR1*
196
210
CH5*
160
RSTB
RA3
RA4*
RA5
COD5*
170
CH1*
180
CLCK1
MEM1
158
CL*
162
RSTB
RA3
RA4
RA5*
COD3*
172
CH2*
182
CLCK2
MEM2
164
RSTB
RA3
RA4*
RA5*
COD1*
174
CH3*
184
CLCK3
MEM3
166
RSTB
RA3*
RA4
RA5*
COD2*
176
CH4*
186
CLCK4
MEM4
212
MEM1
MEM2
MEM3
MEM4
179
RA3*
RA4*
RA5
COD4*
MEM5
178
168
CH5
CL*
188
CLCK5
MEM5*
RSTB

Fig. 6

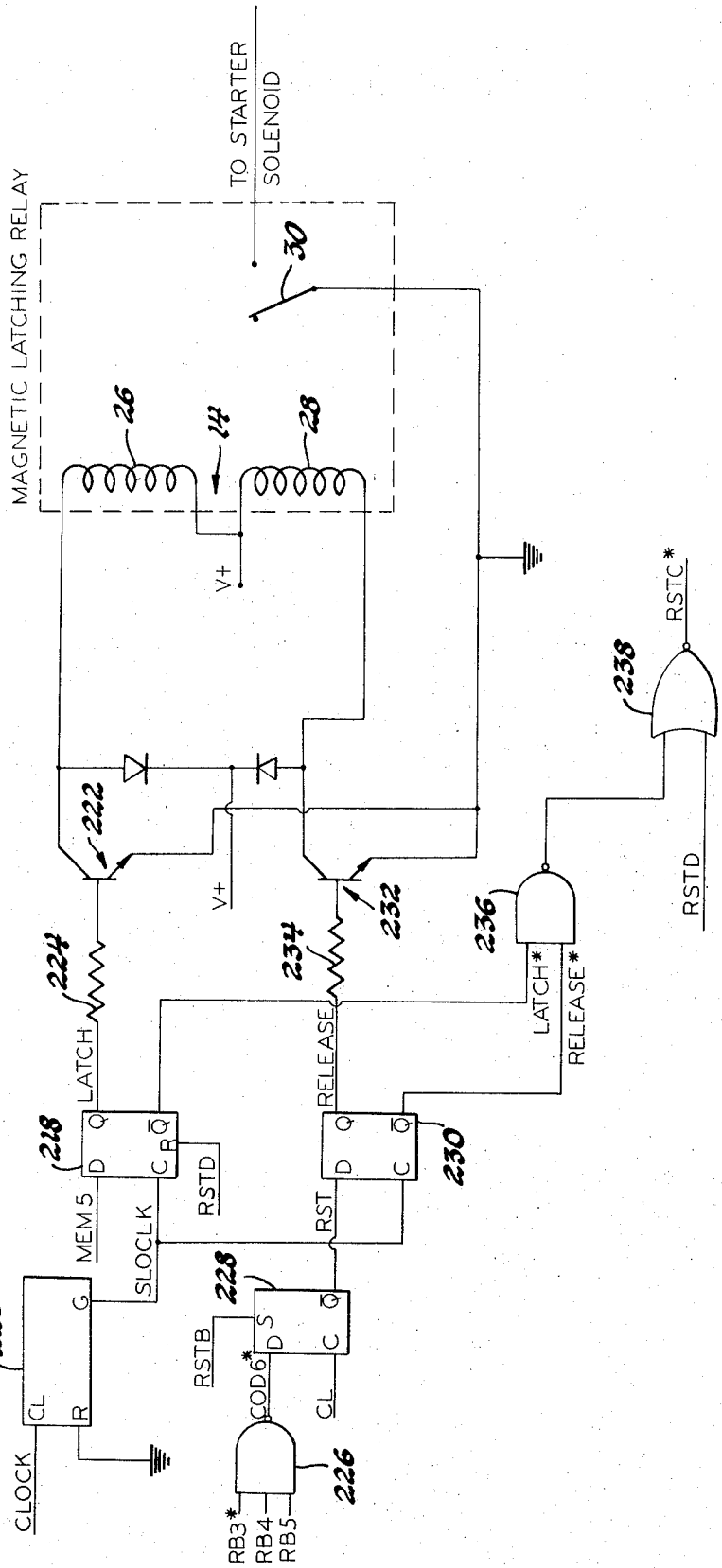

MAGNETIC LATCHING RELAY
TO STARTER SOLENOID
30
26
14
28
V+
V+
222
232
224
234
236
238
RSTC*
RSTD
LATCH*
RELEASE*
LATCH
RELEASE
218
230
D
Q
C
R
MEM 5
SLOCLK
RSTD
RST
220
228
CLOCK
CL
R
G
S
RSTB
COD6*
CL
226
RB3*
RB4
RB5

Fig. 7

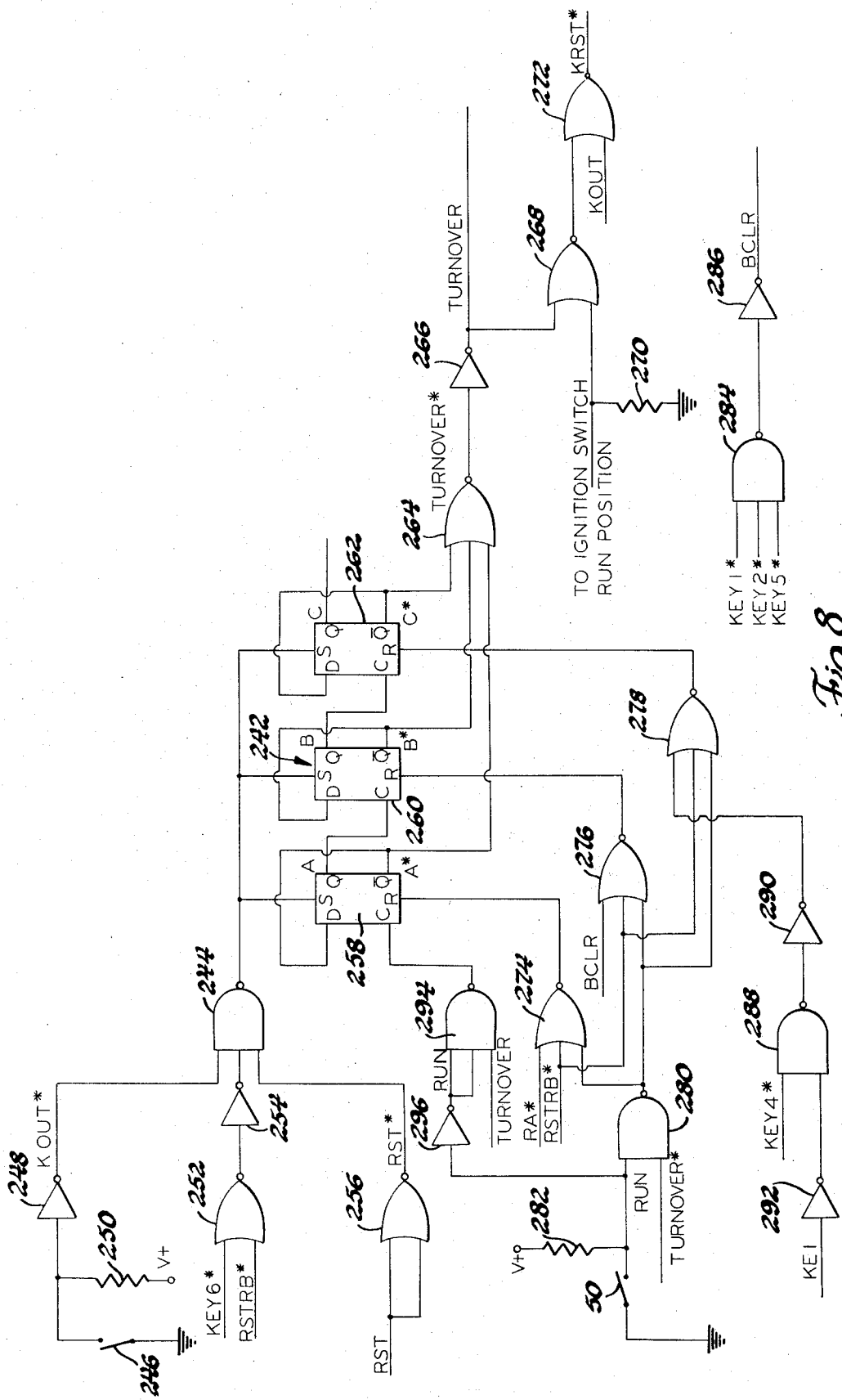

K OUT*
248
250
V+
246
KEY6*
RSTRB*
252
254
RST*
256
RST
244
A
A*
258
B
B*
242
260
C
C*
262
D S Q C R Q
TURNOVER*
264
266
TURNOVER
268
KRST*
272
KOUT
TO IGNITION SWITCH
RUN POSITION
270
BCLR
286
KEY1*
KEY2*
KEY5*
284
278
276
BCLR
274
RA*
RSTRB*
294
RUN
TURNOVER
296
280
RUN
TURNOVER*
282
V+
50
290
KEY4*
288
KEI
292

Fig. 8

ANTI-THEFT APPARATUS INCLUDING TURNOVER MODE OF OPERATION

This invention relates to a system for inhibiting motor vehicle operation by unauthorized persons and more particularly to a system for preventing starting of a motor vehicle until the operator has entered a predetermined code into the system.

It is an object of the present invention to provide an improved anti-theft system for preventing unauthorized operation of a motor vehicle.

It is another object of the present invention to provide such a system wherein knowledge of a particular code is normally required to start the motor vehicle but wherein one who has knowledge of the code may permit others a limited number of starts of the vehicle engine without the necessity for disclosing the code.

It is another object of the present invention to provide electronic combination lock circuitry including a turnover mode of operation which permits another operator a limited number of engine starts as selected by the owner of the vehicle without the necessity for disclosing the code and wherein the turnover mode is terminated in response to removal of the ignition key.

It is a further object of the present invention to provide an anti-theft system including a keyboard unit for entering a particular combination of numbers and means for serially transmitting the data entered to a receiver unit located in a comparatively inaccessible location of the vehicle to thereby render difficult and time consuming any attempt to defeat the system.

It is another object of the present invention to provide electronic combination lock circuitry requiring the entering of a particular code in order to start the vehicle but which permits restarting of the vehicle without the necessity for entering the code as long as the ignition switch remains in the On position.

In accordance with the present invention the ground path of the starter solenoid circuit on the motor vehicle is controlled by a latching relay which is latched, to close the solenoid circuit, by combination lock circuitry responsive to operator actuation of a plurality of pushbuttons in a predetermined sequence. The lock circuitry includes a keyboard unit through which the combination code number may be entered. The digits of the number are encoded and serially transmitted to a receiver and decoder located in a relatively inaccessible part of the vehicle. If the correct code number is transmitted the latching relay is latched to permit starting of the vehicle. If the code number is not entered correctly the latching relay is released or if after the correct code is entered the ignition key is turned off the latching relay is released. If while the engine is running the operator actuates one of the numbered pushbuttons the system is placed in a turnover mode which permits the vehicle to be restarted for a number of times corresponding to the pushbutton depressed. If at any time while the vehicle is in the turnover mode the ignition key is removed, the latching relay is released to return the system to the normal mode of operation.

Other objects and advantages of the present invention will be apparent from the following detailed description which should be taken in conjunction with the drawings in which:

FIG. 1 is a schematic diagram of the system of the present invention;

FIG. 2 is a block diagram of the combination lock circuitry of the present invention; and

FIGS. 3 through 8 are more detailed logic diagrams of the lock circuitry of FIG. 2.

Referring now to the drawings and initially to FIG. 1, the anti-theft system of the present invention is generally designated **10** and comprises logic control circuitry **12** and a latching relay **14.** The control circuitry **12** is connected with a source of direct current potential such as the vehicle battery **16** through a conductor **18.** The conventional vehicle ignition switch generally designated **20** has one side connected with the battery **16** and is movable from a normally open position as shown to engage a Run contact connecting the ignition system with the battery **16** and is further movable to engage a Start contact connecting the starter solenoid **22** of the vehicle to the battery **16** while maintaining engagement with the Run contact. As usual, the ignition switch **20** is biased to return from the Start position to the Run position. The position of the ignition switch **20** is sensed by the control circuitry **12** through a conductor **24.** The latching relay **14** includes a latch winding **26** and a release winding **28** which controls a relay contact **30** to respectively close and open the starter solenoid circuit.

Referring now to FIG. 2, the anti-theft system **10** is shown in block diagram form and includes a master unit located within the vehicle compartment, preferably on the dashboard and a remote unit located in a relatively inaccessible area such as within the starter motor enclosure. The master unit comprises a keyboard unit **32** having a plurality of operator actuable pushbuttons bearing the numerals **1** through **5** and the legend RESET. The particular combination code number is entered by the operator through the keyboard unit **32.** The six pushbuttons on the keyboard unit **32** are connected with keyboard filter logic **34** which is in turn connected with a keyboard encode and transmit block **36** which encodes the digits entered through the keyboard unit **32** and serially transmits such data through a conductor **38** along with a clock signal through a conductor **40** to the remote unit generally designated **41.** The remote unit **41** includes a receive and decode block **42** where the data is received and decoded and fed to a lock code memory and control logic block **44** which provides either the latch or a release signal to the latching relay **14.** The starter solenoid **22** is energizable from the ignition switch **20** and controls the usual engine starter motor (not shown) of the vehicle. The master unit further includes mode logic generally designated **46** which senses the position of the ignition switch **20** as well as whether the ignition key is inserted in or has been removed from the usual ignition lock on the vehicle. A turnover logic block generally designated **48** receives an input from a condition responsive switch **50** which responds, for example, to engine manifold vacuum so as to be indicative of whether the engine is running or not. The logic block **48** also receives inputs from the keyboard encode and transmit block **36** and provides an output designated TURNOVER to the mode logic **46.** The logic **48** when placed in the TURNOVER mode by the vehicle owner permits the starter relay **22** to be energized from the ignition switch **20** through the mode logic **46** for a particular number of starts without the necessity for entering the particular combination code number through the keyboard unit **32.** The mode logic **46** provides a reset output to the keyboard encode and transmit unit **36** whenever the number of starts in the turnover mode have

been completed or whenever the ignition switch **20** is removed from the ignition lock.

Referring now to FIG. **3**, the overall timing for the system of FIG. **2** is provided from a basic clock oscillator **52** which produces, for example, a 20 KHZ square wave output signal to the clock input of a counter **54**. A reset input, designated RST, to the counter **54** is provided from an initialization circuit generally designated **56** which produces a reset pulse upon connection of the logic control circuitry with the battery **16**. The circuit **56** comprises a resistor **58** and capacitor **60** with an inverter **62** connected to the junction between the resistor **58** and capacitor **60** so that a pulse with a positive going leading edge is generated upon connection with the battery **16**. RST will then go low upon charging of the capacitor **60** above the threshold of the inverter **62**. The counter **54** is a divide-by-**128** counter producing seven successively lower frequency outputs designated TP1 through TP7. TP2 through TP7 go low upon charging of the capacitor **60** above the threshold of the inverter **62**, and are inverted by the inverters generally designated **64** to produce the outputs TP2* through TP7*. TP3 and TP2* provide inputs to a NOR gate **66** which produces an output designated CPB which is inverted by an inverter **67** to produce an output designated CPB*. TP3* and TP2* provide inputs to a NOR gate **68** which produces an output designated CPA which is inverted by inverter **69** to produce the output designated CLOCK*.

Referring now to FIG. **4**, the individual pushbuttons **1** through **5** and RESET of the keyboard unit **32** control switches designated K1 through K6 respectively, each of which had one side grounded and the other side connected to V+ through pull-up resistors generally designated **70**. The high side of the switches K1 through K6 respectively, are designated Key **1*** through Key **6*** and are connected with the keyboard filter logic **34**. Referring now to FIG. **5**, the filter logic **34** comprises NAND gates **72** and **74** and a NOR gate **76** which produces an output designated Key* which is normally high but goes low in response to actuation of any of the switches K1 through K6 and returns high upon release of the switch. Key* is connected with the D input on the first stage of a three stage counter comprising D type flip-flops **78, 80** and **82**. The Q outputs of the flip-flops **78** and **80** designated K1* and K2* are connected with the D inputs of the flip-flops **80** and **82** respectively. The flip-flops **78, 80** and **82** are set from the initialization circuit **56** so that K1*, K2* and K3* are high. The flip-flops **78** through **80** and **82** are clocked from the TP7* output of the counter **54**.

The keyboard encode and transmit unit **36** comprises binary encoding circuitry generally designated **84** the output of which is strobed into a register generally designated **86** under the control of strobe circuitry generally designated **88**. The binary encoding circuitry **84** includes NAND gates **90, 92** and **94** which are connected with the pushbutton switches K1 through K6 as indicated. The output of each of the gates **90** through **94** is inverted by inverters **96, 98** and **100** and provide one input to NOR gates **102, 104** and **106**. The other input to the gates **102** through **106** is provided from the strobe circuitry **88** which comprises NOR gates **108, 110** and **112** connected with the three stage counter and with the timing circuitry of FIG. **3** as indicated. The outputs of the NOR gates **108** through **112** provide inputs to a NAND gate **114** the output of which is designated RSTRB* which provides the other input to the NOR gates **102** through **106**. The output of the gates **102** through **106** are connected with the set inputs of the first three stages of the register **86** while the output of the gate **114** is inverted by an inverter **116** and applied to the set input of the last two stages of the register **86**. The register **86** comprises D type flip-flops **118** through **126** which are clocked from the output, designated REG/C, of a NAND gate **128** having its inputs connected to TP7 and CPB. The flip-flops **118** through **126** are reset to an initial condition from RST wherein their Q outputs REG1 through REG5 are low. The output of the flip-flop **126** provides one input to a NAND gate **130**, the other input of which is designated Run* and is high to open the gate **130** whenever the engine is not running. The output of the gate **130** is designated Data*.

Briefly, the operation of the circuitry thus far described is as follows: Depression of one of the switches K1 through K6 causes the binary equivalent of the corresponding digit to be entered in the flip-flops **118, 120** and **122** of the register **86** when RSTRB* goes low. At the time the flip-flops **124** and **126** of the register **86** are set high from RSTRB. Consequently, as the data is shifted out of the register **86** by the clock pulses REG/C the data is always preceded by two logic "1's" for identification purposes.

Referring now to FIG. **6**, the receive and decode logic block **42** comprises a data register generally designated **134** which includes D type flip-flops **136** through **144**. The flip-flops **136** through **144** are set so that their Q outputs are high by a reset signal designated RSTA. RSTA is derived from the Q output of a flip-flop **146** which is initially set high from an initialization circuit **147** which is identical to the circuit **56**. The circuit **147** produces a pulse designated RSTD when the logic circuitry is first connected with the vehicle battery. Thereafter, the flip-flop **146** is toggled and the register **134** is set by the rising edge of CLOCK* whenever the $\overline{Q}$ output of the flip-flop **144**, designated RA1, is high. The data is shifted into the register **134** by a NAND gate **148** having its output connected to the clock input of each of the flip-flops **136** through **144**. One input to the gate **148** is from a NAND gate **150** which has inputs connected to the $\overline{Q}$ outputs of the flip-flops **142** and **144**, designated RA2 and RA1 respectively, which go low when the register **134** is set. The other input to the gate **148** is from CLOCK* which is inverted by an inverter **152** the output of which is designated CLOCK. The gate **148** is open whenever the register **134** is set so that the data is shifted into the register on the following edge of CLOCK until the first two bits, which are logic "1's," are entered in the flip-flops **142** and **144**, whereupon RA1 and RA2 go high and the gate **148** is closed.

The register **134** stores the data for a one CLOCK pulse interval and thereafter the register **134** is set from the flip-flop **146**. During this one CLOCK pulse interval the data stored in the register **134** is decoded.

The outputs of the flip-flops **136** through **144** in the register **134** are connected with decode logic generally designated **158** which comprises NAND gates **160** through **168** connected with the outputs of the flip-flops **136** through **144** in the register **134** as indicated. The decode logic **158** is hard wired with the register **134** to decode the particular combination code number which in the example shown is **53124**. The outputs of

the gates **160** through **166** are connected with the D input of flip-flops **170** through **176** respectively while the output of the gate **168** is connected to the D input of flip-flop **178** through a NOR gate **179.** The flip-flops **170** through **178** are clocked through NOR gates **180** through **188** which are open in sequence to insure that the five numbers of the code are inserted in the keyboard unit **32** in the proper sequence. The $\overline{Q}$ outputs of the flip-flops **170** through **176** and the Q output of the flip-flop **178** are designated MEM1 through MEM **5** respectively. The $\overline{Q}$ output of the flip-flop **178** is designated MEM **5***. The sequential control of the gates **180** through **188** is controlled from a BCD counter **190** which is advanced on the rising edge of CLOCK through a NAND gate **192** and an inverter **194.** The other inputs to the gate **192** besides CLOCK are RA1 and RA2 so that the gate **192** is opened for the CLOCK pulse interval following the entering of the binary data in the register **134.** In other words, after CLOCK goes low to enter the most signficant bit in flip-flop **136,** the gate **148** is closed and the gate **192** is opened. On the following rising edge of CLOCK, CL* goes low and CL goes high and the counter **190** is incremented and on the following falling edge of CLOCK, i.e. CLOCK* goes high, the flip-flop **146** is toggled causing RSTA to go high and reset the register **134.** When the register **134** is reset the gate **148** is opened and the gate **192** is closed. The outputs of the counter **190** designated CTR1 through CTR3 are inverted by inverters **196, 198** and **200** to provide the outputs designated CTR1* through CTR3* respectively. CTR1 through CTR3 and CTR1* through CTR3* are connected with NAND gates **202** through **210** as indicated. The outputs of the gates **202** through **210** are designated CH1* through CH5* respectively. The counter **190** is reset from RSTC* through a NAND gate **216,** the output of which is designated RSTB, or from a NAND gate **214.** The input to the gate **214** is the CTR1, CTR2*, CTR3 outputs of counter **190** and the MEM **5*** output of the flip-flop **178.** The RSTC* input to gate **216,** as will be shown hereinafter, goes low and RSTB goes high when RSTD goes high to initially reset the counter **190.** When RSTB goes high the flip-flops **170** through **176** are set to drive MEM1 through MEM4 low and the flip-flop **178** is reset to drive MEM5 low and MEM5* high. With the counter **190** reset CH1* is low and CH2* through CH5* are high. Accordingly, when CL* goes low, just prior to incrementing the counter **190,** the flip-flop **170** will be toggled to cause MEM1 to go high if the pushbutton switch K5 had been depressed since in that event RA3, RA4* and RA5 would be high. As the counter **190** is incremented CH2* goes low and the next binary coded number entered through the keyboard unit **32** is decoded by the gate **162.** If the number 3 is entered MEM2 is toggled high on the falling edge of CL*. Similarly, MEM3 and MEM4 go high if the pushbutton switches K1 and K2 are successfully depressed. The four outputs of the flip-flops **170** through **176** are inputs to a NAND gate **212,** the output of which is connected with the NOR gate **179** so that if the first four numbers of the code are entered and in the proper sequence and the pushbutton switch K4 is thereafter depressed, the outputs of the flip-flop **178** designated MEM5 is toggled high end MEM5* is toggled low.

Referring now to FIG. **7,** MEM5 is connected to the D input of a flip-flop **218** which is initially reset from the RSTD output of the initialization circuit **147.** The flip-flop **218** is clocked from the output of a BCD counter **220,** designated SLOCLK, which is driven from and is at a frequency of, for example, 20 Hz. as compared with the CLOCK frequency of, for example, 2KHz. When the flip-flop **218** is clocked while MEM5 is high its Q output designated LATCH goes high. The Q output of the flip-flop **218** is connected with the base of a transistor **222** through a resistor **224.** The emitter electrode of the transistor **222** is grounded while its collector is connected to V+ through the latch winding **26** of the latching relay **14.** Accordingly, if the correct combination is entered through the keyboard unit **32** the latch winding **26** is energized and its contact **30** is moved from the position shown to provide a ground path for the starter **22** solenoid.

If the reset button K6 of FIG. **4** is depressed the binary equivalent of the numeral **6** is transmitted to the register **134** causing the inputs to a NAND gate **226** to go high and the output thereof designated COD6* to go low. The output of the NAND gate **226** is connected to the D input of a D type flip-flop **228** which is toggled from CL. Accordingly, on the rising edge of CL (FIG. **6**) following depression of the reset pushbutton switch K6, the $\overline{Q}$ output of the flip-flop **228** designated RST goes high. RST is connected with the D input of a D type flip-flop **230** which is clocked from SLOCLK and has its Q output designated RELEASE connected to the base of a transistor **232** through a resistor **234.** The emitter of the transistor **232** is grounded while the collector is connected to V+ through the release winding **28** of the latching relay **14.** Accordingly, the release winding **28** may be energized to open the ground path of the starter solenoid **22** by actuating the reset pushbutton switch K6. The $\overline{Q}$ outputs of the flip-flops **218** and **230** designated LATCH* and RELEASE* respectively are inputs to a NAND gate **236** the output of which is connected with a NOR gate **238.** The other input to the NOR gate **238** is RSTD from the initialization circuit **147.** The output of the gate **238** is the previously mentioned RSTC* which provides the other input to gate **216** of FIG. **6.** Thus, whenever the latching relay **14** is either latched or released RSTC* goes low to reset the counter **190** and the flip-flops **178** and set the flip-flops **170** to **176** and **228.**

If the code number is incorrectly entered MEM5* will remain high and after the fifth pushbutton switch has been actuated CTR1, CTR2* and CTR3 will be high so the output of the gate **214** will go low and RSTB will go high to reset the counter **190** and the memory flip-flops and release the latching relay **14.**

Referring now to FIG. **8,** the turnover logic **48** is disclosed in greater detail. The turnover logic **48** permits the owner of the vehicle or anyone else having knowledge of the combination to turn over limited use of the vehicle to one not having knowledge of the combination without the necessity of disclosing the combination. Use is limited by the operator prescribing the number of vehicle starts to be permitted. The logic **48** comprises a three stage counter **242** which is set through a NAND gate **244** which performs an OR function. One input to the gate **244** is K OUT* which is derived from a switch **246** which closes when the ignition key is placed in the ignition lock and opens when the ignition key is removed from the ignition lock. One side of the switch **246** is grounded while the other side is connected with an inverter **248** which is tied to V+

through a pull-up resistor 250. Another input to the gate 244 is from the reset pushbutton switch K6 and the accompanying RSTRB* through a NOR gate 252 and an inverter 254. The other input to the NAND gate 244 is from the initialization circuit 56 through a NOR gate 256. The counter 242 comprises flip-flops 258, 260 and 262. The flip-flops 258, 260 and 262 are initially set from RST so that their Q outputs are high and their $\overline{Q}$ outputs are low. The $\overline{Q}$ outputs of the flip-flops 258 through 262 provide inputs to a NOR gate 264, the output of which is designated TURNOVER*, which is inverted by an inverter 266 to provide the output designated TURNOVER. Thus, initially the output of the gate 264 is high and the output of the inverter 266 is low indicating that the vehicle is not in the turnover mode. If at any time the ignition key is removed from the ignition lock or the reset pushbutton switch K6 is actuated the counter 242 is set so that the output of the inverter 266 goes low. The output of the inverter 266 provides one input to a NOR gate 268. The other input to the NOR gate 268 is tied to ground through a pull down resistor 270 and is also connected with the Run position of the ignition switch 20. The output of the gate 268 provides one input to a NOR gate 272 the other input of which is K OUT. The output of the gate 272 is designated KRST* and provides one input to the gates 92 and 94 of the encoding circuitry 84 (FIG. 5). Thus, if KRST* goes low the binary equivalent of the reset pushbutton switch K6 is transmitted to the receive and decode unit 42 to release the latching relay 14. KRST* will go low if the ignition key is removed from the ignition lock or, if the vehicle is not in the turnover mode and the ignition switch is turned off. The flip-flops 258, 260 and 262 are programmed by encoding logic comprising NOR gates 274, 276 and 278. The NOR gates 274, 276 and 278 are each controlled from a NAND gate 280. One input to the gate 280 is TURNOVER*. The other input to the gate 280 is from the engine manifold vacuum switch 50 or other appropriate engine run conditioning sensor and also to V+ through a pull up resistor 282. Thus, the gates 274, 276 and 278 are closed if the engine is not running or the system is in the turnover mode. In other words, the counter 242 can be programmed for a particular number of free starts only if the engine is running and the system is not already in the turnover mode. The second input to each of the gates 274, 276 and 278 is from RSTRB* which goes low in response to actuation of any of the pushbutton switches K1 through K6. The third input to the gate 274 is from RA* (FIG. 5) which goes low in response to actuation of either of the pushbutton switches K1, K3 or K5. The third input to NOR gate 276 is designated BCLR and is derived from the output of a NAND gate 284 through an inverter 286. The inputs to the gate 284 are KEY1*, KEY2*, and KEY5*. Accordingly, BCLR goes low if either of the pushbutton switches K1, K2 or K5 is actuated. The third input to the NOR gate 278 is derived from a NAND gate 288 through an inverter 290. The inputs to the NAND gate 288 are KEY4*, and KEY1 (FIG. 5) through an inverter 292. Accordingly, the output of the inverter 290 goes low if either of the pushbutton switches K1, K2, K3 or K4 is actuated. Thus, the $\overline{Q}$ outputs of the flip-flops 258, 260 and 262 will be reset to the binary equivalent of any pushbutton switch depressed while the vehicle is running and the vehicle is not in the turnover mode. For example, if the register 242 is set so that TURNOVER* is high and if the engine is running and the driver depresses the pushbutton switch K4, the $\overline{Q}$ output of the flip-flop 262 will be reset high and the $\overline{Q}$ outputs of the flip-flops 258 and 260 will remain low. When the $\overline{Q}$ output of the flip-flop 262 goes high TURNOVER* goes low closing the gate 280. TURNOVER* will remain low until the counter 242 has been toggled four times. The counter 242 is toggled through a NAND gate 294 and inverter 296 each time the switch 50 opens while TURNOVER is high. Thus, each time the engine is started during the turnover mode the counter 242 is toggled so that after four starts, all inputs to the gate 264 are low and TURNOVER goes low. Accordingly, when the ignition switch 20 is turned off after the fourth start the output of the gate 268 goes high and KRST* goes low to generate the reset number 6 and interrupt the circuit to the starter solenoid 22.

Having thus described my invention what I claim is:

1. In a motor vehicle provided with starter motor control means for controlling starting of the vehicle engine, including an ignition switch operable by an ignition key, apparatus for preventing unauthorized starting of said vehicle comprising:

a keyboard unit including a plurality of operator actuable switch means,

latch means for enabling said starter motor control means,

latch control means responsive to actuation of said switch means in a predetermined sequence for energizing said latch means to enable said starting motor control means,

said latch control means responsive to actuation of said ignition switch to an off position for releasing said latch means to disable said starter motor control means,

override means for overriding said ignition switch and thereby prevent releasing of said latch means, said override means including counter means, means responsive to actuation of one of said switch means while said vehicle engine is running to program said counter means to a predetermined number of ignition switch actuations, said counter means being advanced each time said engine is started after said counter means is programmed whereby the override condition is terminated after said engine has been started said predetermined number of times,

and means responsive to removal of said ignition key for resetting said counter means.

2. In a motor vehicle provided with an electrical load device for controlling usage of the vehicle, apparatus for preventing unauthorized usage of said vehicle comprising:

input means including a plurality of operator actuable switch means,

latch means for enabling said load device,

latch control means responsive to actuation of said switch means in a predetermined sequence for energizing said latch means to enable said load device,

an additional operator actuable switch means,

said latch control means responsive to actuation of said additional switch means for releasing said latch means to disable said load device,

override means for overriding said additional operator actuable switch means and thereby preventing release of said latch means, said override means in-

cluding counter means, means responsive to actuation to one of said plurality of operator actuable switch means while said load device is enabled to program said counter means to a predetermined number of actuations of said additional operator-actuable switch means, said counter means being advanced each time said additional switch means is actuated after said counter means is programmed whereby the override condition is terminated after said additional switch means has been actuated said predetermined number of actuations.

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