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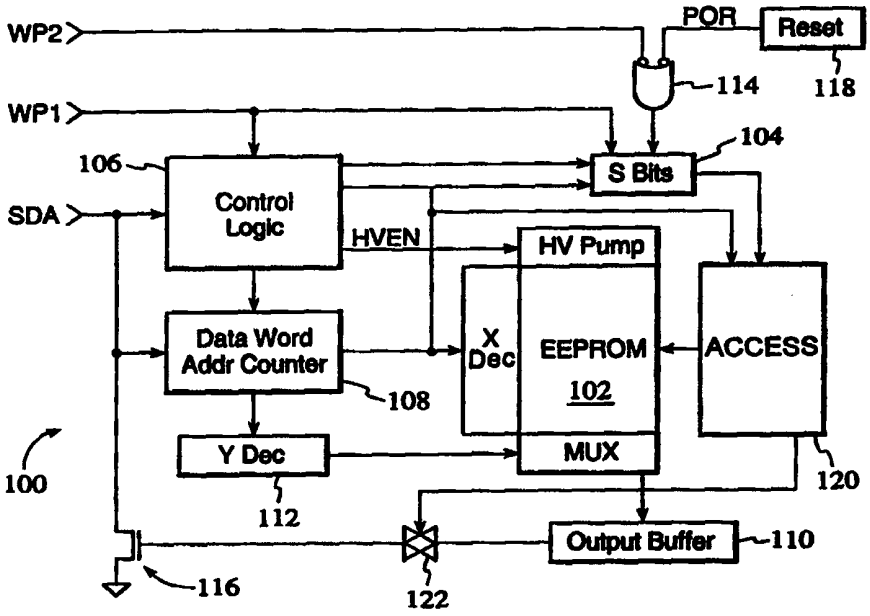

(57) Abstract

A memory device (100) comprises a memory array (102) having corresponding first access control bits (202, 204) to control access thereto. A second set of access control bits (104) is provided to control write access to the first access control bits. The memory array is divided into memory blocks, each block having a corresponding access control bit. At least one such block (BLK0) is further subdivided into pages, each page having a corresponding control bit.

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Description

PROGRAMMABLE ACCESS PROTECTION IN A FLASH MEMORY DEVICE

TECHNICAL FIELD

The present invention relates generally to memory devices, and more specifically to providing access protection in such memory devices.

BACKGROUND ART

Electrically erasable and programmable read-only memories (EEPROM) are used wherever reprogrammable nonvolatile memory is required. Typically, writing to such devices requires asserting a write enable signal to the chip at the same time the write operation takes place. This prevents inadvertent writing of the memory.

Data contained in an EEPROM, however, is susceptible to various sources of corruption. For example, transients due to powering up and powering down an EEPROM present an opportunity for data corruption. EEPROMs typically find application in harsh industrial environments, thus exposing the devices to noise spikes on the control lines. It is therefore desirable to provide enhanced protection against inadvertent writes, in addition to the simple write enable signaling presently used.

EEPROMs also find use in situations where controlled read access is desirable. For example, smart cards incorporate EEPROM-type memory which require some form of protection against unauthorized access. Such cards are used in personal banking applications, health delivery services, and so on where privacy of the information contained in the card is fundamental.

EEPROMs can be found in radio frequency identification devices (RFIDs), where the memory device is used to store information identifying the object to which an RFID tag is attached. Typically, RFID tags can be

written in order to store information in addition to an identifier. RFID tags usually have some sort of write protection capability and read access control. Such read access control is currently implemented by providing password mechanisms which gate access to the memory incorporated in the tag, resulting in a bulky device.

What is needed is a strategy which prohibits reading some or all of the information contained in a memory device, as well as write access to the memory. It is desirable to avoid having additional circuitry to implement such capability, thus permitting smaller and more compact applications which require read access protection.

SUMMARY OF THE INVENTION

In accordance with the present invention a memory device comprises a memory array and access logic to control access to the memory array. A first bit store provides access information which determines the accessibility of the memory array. In a preferred embodiment of the invention, the memory array is divided into a plurality of memory blocks, each block having corresponding access information for access thereto. A second bit store contains access control information to control access to the first bit store. A write protect pin sets the second bit store to a first logic level. Write access to the first bit store is permitted when the corresponding bit in the second bit store is at a second logic level. Further in accordance with the present invention, at least one memory block is subdivided into pages. A third bit store is provided to control access to each such page.

In a first variation of the preferred embodiment, the present invention is configured as a serial memory device. In a second variation, the memory device is adapted with a parallel interface. In yet a third variation, the present invention includes a radio frequency interface to provide radio frequency signaling

for use in RFID applications. The RFID interface can operate with either a serial type memory device or a parallel type memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the memory architecture of the present invention.

Figs. 2A and 2B depict the access control logic shown in Fig. 1.

Fig. 3 illustrates the access logic for memory block 0.

Fig. 4 shows a memory map of the access protection page.

Fig. 5 shows the present invention in an RFID application.

BEST MODE OF CARRYING OUT THE INVENTION

Referring to Fig. 1, a preferred embodiment of the memory device 100 in accordance with the present invention includes an electrically erasable programmable read only memory store (EEPROM) 102. A serial interface is provided to access the EEPROM, comprising a serial input/output data pin SDA for receiving op-codes to operate the memory device and for receiving data to be stored in the memory device. The serial data pin feeds into device control logic 106 which produces control signals to operate the memory device in accordance with received op-codes. Serial data pin SDA also feeds into a data store 108 which serves to hold data to be written into EEPROM 102, and to hold addresses for accessing the EEPROM. Memory addresses are decoded by the X decoder and the Y decoder, the latter serving as a selector input to an output MUX of EEPROM 102. The serial data pin also serves as an output pin. An output buffer 110 drives data onto serial data pin SDA via transmission gate 122 and output transistor 116. Transmission gate 122 is operated under the control of access control logic 120.

The serial interface of the memory device further comprises two write protect pins WP1, WP2, which feed into the device control logic 106 and a set of sticky bits 104. Write protect pin WP1 is a conventional write protection mechanism which prohibits writing to memory whenever the pin is asserted. Control logic 106 disables the high voltage pump of EEPROM 102 so that programming of the EEPROM is prevented when WP1 is asserted. Similarly, writes to the sticky bits 104 are disabled when WP1 is asserted.

The sticky bits are set to logic '1' when WP2 is asserted LO. The sticky bits are also set to logic '1' at power up as the power-on reset signal goes LO when the memory device becomes fully powered. In accordance with the principles of operation of the invention, a logic '0' can only be written to the sticky bits. Thus, once a logic '0' is written to a sticky bit by a user, that sticky bit cannot be subsequently reset to logic '1' except by cycling the power or by asserting WP2 LO. As will be explained below, the sticky bits feed into access control logic of EEPROM 102 in order to provide controlled access to the memory.

Turn now to Fig. 2A for a discussion of the access control logic 120 shown in Fig. 1. As can be seen in the schematic representation of Fig. 2A, EEPROM 102 is divided into eight memory blocks BLK0 - BLK7. EEPROM 102 also includes an amount of memory known as the access protection page APP. Protection bit store 202 (PB0 - PB7) contains access control information for read and write access to each block in EEPROM 102. Protection bit store 204 (PB/AP) contains access control information for the APP portion of the EEPROM. In the preferred embodiment, the protection bits 202, 204 reside in the access protection page APP .

Functionally, access control logic 120 comprises AND gates 201a - 201h through which the bits in protection bit store 202 are fed, so that a determination can be made as to whether write access to memory blocks

BLK0 - BLK7 is permitted via serial pin SDA. Thus, protection bits PB0 control write access to block BLK0 of EEPROM 102, protection bits PB1 control write access to block BLK1, and so on. Similarly, protection bit PB/AP controls write access to access protection page APP through AND gate 203.

Access control logic 120 further comprises AND gates 205a - 205h and 207. As can be seen in Fig. 2A, the sticky bits 104 provide write access control over protection bit stores 203, 204 by coupling serial data pin SDA to the protection bits through AND gates 205a - 205h and 207. More specifically, a protection bit can be written only if its corresponding sticky bit is set to logic '1'. In this way, for example, sticky bit SB0 controls whether protection bit PB0 may be written.

As noted above, an aspect of the invention is that the sticky bits can only be written via the serial data pin SDA to store logic '0'. Once written to logic '0', the sticky bits can only be reset to logic '1' by asserting a LO on write protect pin WP2 or as the POR line to goes LO when the device is powered up. Thus, OR gate 114, via its inverted inputs, signals the sticky bit memory store 104 to reset to logic '1' when either of these two conditions occurs.

Also as noted above with respect to Fig. 1, write protect pin WP1 prohibits writing to EEPROM 102 by disabling the high voltage pump needed to program the memory cells of the EEPROM. In accordance with the present invention, asserting write protect pin WP1 also prohibits writing the sticky bit memory store 104, as indicated in Fig. 2A where WP1 feeds into the sticky bit memory store through AND gates 209a - 209h and 211.

Fig. 2B illustrates that protection bits PB0 - PB7 provide control over read access of memory blocks BLK0 - BLK7, in addition to providing write control over the memory blocks. Thus, access control logic 120 (Fig. 1) includes additional logic, e.g. AND gates 213a - 213h,

into which the protection bits and the output of the memory blocks feed.

Turning now to Fig. 3, an additional level of write access protection is shown provided for memory block BLK0. Memory block BLK0 is further divided into eight pages PG0 - PG7 that can be individually protected against a write operation. A set of write-protect bits 302 is combined with protection bit PB0 for the memory block via additional logic, such as AND gates 301a - 301h, contained in the access control logic 120. Thus, a page in memory block BLK0 requires first that the protection bits PB0 are set to permit writing to the memory block and second that the corresponding write-protect bit is set to permit writing to the page.

The memory map shown in Fig. 4 illustrates the address mapping of the access protection page APP. The memory comprises sixteen addressable bytes, addressed from byte0 - byte15. The first eight bytes contain the protection bits PB0 - PB7 and the sticky bits SB0 - SB7. The protection bits for a given memory block are organized in the following manner. They comprise two bits: a most significant bit (MSB) and a least significant bit (LSB), resulting in four possible combinations.

If the protection bits are set to (0,0) or (0,1), then the corresponding memory block can neither be read nor written; i.e. no access to the memory block is permitted. If the protection bits are set to (1,0), then read-only access is permitted. If the protection bits are set to (1,1), then full access (read and write) is permitted on the memory block. Thus, the protection bits each occupy two bits of each of bytes 0 - 7 in access protection page APP.

In the preferred embodiment, all the bits comprising the APP, except for the sticky bits, are stored in EEPROM 102. Thus when power to the device is cycled, the information contained in that portion of the APP remains intact and unaffected. The sticky bits,

although they share the same address space as the APP, are stored in a memory separate from EEPROM 102. In the preferred embodiment, the sticky bits are stored in registers, such as those formed by D-type flip-flops. By so doing, the content of the sticky bits can be initialized to contain logic '1' upon power up of the memory device. In addition, the registers are coupled to the WP2 pin such that asserting the pin results in resetting the registers to contain logic '1'.

The foregoing discussion has been based on a memory device having a serial interface. It is noted that the access protection aspects of the memory device can be used in parallel memories without departing from the spirit and scope of the invention. Similarly, radio frequency interface circuitry can be used to communicate with the memory device. Thus, RFID devices can be constructed with minimum size and yet still have the benefits of a secure memory which the present invention provides.

Referring to Fig. 5, a typical RFID 500 comprises an interrogator 502 and a tag 504. The tag comprises a pick-up coil L_t, which together with capacitor C_t, forms a tank circuit 520. Coupled across the tank circuit are a voltage clamp 522, a load modulation circuit 524, and a full-wave bridge rectifier 526.

The bridge rectifier 526 charges a small supply capacitor C_f to provide the supply voltage V_{dd}. The supply voltage provides power to the memory device 100 of the present invention. In addition to providing internal power to the tag 504, the bridge circuit 526 also provides a clock signal, based on the incoming signal from the interrogator 502, to a clock generator 536.

The modulation circuit 524, varies a load placed across the tank circuit, which varies the Q factor of the tank circuit 520. The modulation circuit operates under the control of a controller 534 to vary the Q of the tank circuit in accordance with the data to be conveyed to the interrogator 502. Data is "transmitted"

when the interrogator 502 detects corresponding changes in the reflected signal. Conversely, demodulation circuit 538 demodulates an incoming data signal and feeds it into the controller 534. Typically, the data signal includes command bits and/or data bits to be written into memory device 100.

Claims

1. A memory device comprising:

a memory array (102);

first control means (120), coupled to the memory array, for controlling access to the memory array;

first storage means (202, 204) for receiving and storing memory access control information, the first control means (120) adapted to provide access to the memory array on the basis of the content of the first storage means;

second control means (205a-205h, 207), coupled to the first storage means, for controlling write access to the first storage means (202, 204);

second storage means (104) for receiving and storing modification control information, the second control means (205a-205h, 207) adapted to provide write access to the first storage means (202, 204) on the basis of the logic state of the second storage means;

first pin means (WP2) for receiving an external signal, coupled to set the second storage means (104) to a first logic state in response to receiving an external signal; and

second pin means (WP1) for receiving an external signal, coupled to inhibit all write access to the memory array (102) in response to receiving an external signal.

2. The memory device of claim 1 wherein the first storage means (120) is a bit store and the second storage means is a bit store having a bit corresponding to each bit in the first storage means (202, 204) and the second control means is adapted for permitting write access to a bit in the first storage means only if the corresponding bit in the second storage means (104) is at a second logic level.

3. The memory device of claim 1 wherein the memory array (102) comprises a plurality of memory blocks, each memory block having corresponding memory access control information to control access thereto.

4. The memory device of claim 3 wherein the memory access control information comprises a plurality of protection bits, each protection bit being associated with a memory block.

5. The memory device of claim 4 wherein the second storage means (104) comprises a plurality of sticky bits, each sticky bit corresponding to a protection bit.

6. The memory device of claim 1 further including means for generating a power-on-reset signal (118), coupled to set the second storage means to the first logic state upon powering up the memory device.

7. The memory device of claim 1 further including a high voltage pump means for providing a voltage to program the memory array, the second pin means (WP1) being coupled to enable and disable (106) the high voltage pump in response to a received external signal.

8. The memory device of claim 1 further having either a serial interface or a parallel interface.

9. The memory device of claim 8 further including a radio frequency interface, in order to communicate with the memory device via radio frequency signalling.

10. A memory device comprising:

a memory array (102) organized as a plurality of memory blocks;

access control logic (120) coupled to the memory array to control read and write access thereto;

a first bit store (202) coupled to the access control logic, the first bit store having access enable bits corresponding to each of the memory blocks, the access control logic adapted to enable and disable read and write operations to a selected memory block based on the logic levels of the access enable bits corresponding to the selected memory block;

write control logic (205a-205n) coupled to the first bit store to write externally provided access enable information into the access enable bits;

a second bit store (104) coupled to the write control logic, the second bit store having a plurality of bits, each bit corresponding to one of the access enable bits, the write control logic adapted to enable writing to the first bit store based on the logic levels of the plurality of bits; and

a first write protect pin (WP1) coupled to the memory array to prohibit write access to the memory array when the first write protect pin is asserted.

11. The memory device of claim 10 wherein the first bit store (202) is addressable and the address space of the first bit store is a subset of the address space of the memory array.

12. The memory device of claim 10 wherein the write control logic (205a-205n) is further adapted to enable writing to the first bit store (202) only when the corresponding bit in the second bit store (104) is equal to a first logic level.

13. The memory device of claim 12 further including a second write protect pin (WP2) coupled to the second bit store, the bits of the second bit store being set to the first logic level when the second write protect pin is asserted LO.

14. The memory device of claim 10 wherein at least one of the memory blocks (BLK0) is subdivided into N pages, and wherein the memory device further includes a third bit store (302) having N page enable bits, each page enable bit corresponding to one of the N pages, the access control logic further adapted to enable and disable read and write operations to a selected page based on the logic level of the page enable bit corresponding to the selected page.

15. The memory device of claim 10 further including a radio frequency interface (520) for communication with the memory device using radio frequency signalling.

16. A method of operating a memory device, the method comprising:

in response to a read request, detecting the logic state of permission bits associated with the memory location specified in the read request and carrying out the read request if the result of the detecting step indicates that the read request is permitted;

in response to a write request, detecting the logic state of permission bits associated with the memory location specified in the write request and carrying out the write request if the result of the detecting step indicates that the write request is permitted;

updating the permission bits, including detecting the logic states of access information associated with the permission bits and carrying out the step of updating only if the access information is at a first logic state;

updating the access information, including allowing only updates wherein the access information is changed from the first logic state to a second logic state;

setting the logic state of the access information to the first logic state upon receiving a power-on-reset signal or upon asserting an access protection pin.

17. The method as claimed in claim 16 further including dividing the memory array into a plurality of memory blocks, associating non-volatile permission bits with each of the memory blocks, and carrying out read and write requests on a per memory block basis.

18. The method as claimed in claim 16 further including allocating a portion of the memory array to store the access information.

19. The method as claimed in claim 16 further including subdividing one of the memory blocks into a plurality of pages, and in response to either a read or a write request to a page, detecting the logic state of non-volatile page permission bits associated with the page specified in the request and carrying out the operation if the result of the detecting step indicates that the request is permitted.

20. The method as claimed in claim 16 further including communicating read and write requests via radio frequency signalling.

AMENDED CLAIMS

[received by the International Bureau on 23 March 1999 (23.03.99);
original claims 2, 17 and 19 cancelled; original claims 1, 10 and 16 amended;
remaining claims unchanged (6 pages)]

1. A memory device comprising:

a memory array (102);

first control means (120), coupled to the memory array, for controlling access to the memory array;

first storage means (202, 204) for receiving and storing memory access control information, the first control means (120) adapted to provide access to the memory array on the basis of the content of the first storage means;

second control means (205a, 205h, 207), coupled to the first storage means, for controlling write access to the first storage means (202, 204);

second storage means (104) for receiving and storing modification control information, the second control means (205a, 205h, 207) adapted to provide write access to the first storage means (202, 204) on the basis of the logic state of the second storage means;

first pin means (WP2) for receiving an external signal, coupled to set the second storage means (104) to a first logic state in response to receiving an external signal; and

second pin means (WP1) for receiving an external signal, coupled to inhibit all write access to the memory array (102) in response to receiving an external signal; and

wherein the first storage means (120) is a bit store and the second storage means is a bit store having a bit corresponding to each bit in the first storage means (202, 204) and the second control means is adapted for permitting write access to a bit in the first storage means only if the corresponding bit in the second storage means (104) is at a second logic state.

2. (Cancelled)

3. The memory device of claim 1 wherein the memory array (102) comprises a plurality of memory blocks, each memory block having corresponding memory access control information to control access thereto.

4. The memory device of claim 3 wherein the memory access control information comprises a plurality of protection bits, each protection bit being associated with a memory block.

5. The memory device of claim 4 wherein the second storage means (104) comprises a plurality of sticky bits, each sticky bit corresponding to a protection bit.

6. The memory device of claim 1 further including means for generating a power-on-reset signal (118), coupled to set the second storage means to the first logic state upon powering up the memory device.

7. The memory device of claim 1 further including a high voltage pump means for providing a voltage to program the memory array, the second pin means (WP1) being coupled to enable and disable (106) the high voltage pump in response to a received external signal.

8. The memory device of claim 1 further having either a serial interface or a parallel interface.

9. The memory device of claim 8 further including a radio frequency interface, in order to communicate with the memory device via radio frequency signalling.

10. A memory device comprising:

a memory array (102) organized as a plurality of memory blocks;

access control logic (120) coupled to the memory array to control read and write access thereto;

a first bit store (202) coupled to the access control logic, the first bit store having access enable bits corresponding to each of the memory blocks, the access control logic adapted to enable and disable read and write operations to a selected memory block based on the logic levels of the access enable bits corresponding to the selected memory block;

write control logic (205a-205n) coupled to the first bit store to write externally provided access enable information into the access enable bits;

a second bit store (104) coupled to the write control logic, the second bit store having a plurality of bits, each bit corresponding to one of the access enable bits, the write control logic adapted to enable writing to the first bit store only when the corresponding bit in the second bit store (104) is equal to a first logic state; and

a first write protect pin (WP1) coupled to the memory array to prohibit write access to the memory array when the first write protect pin is asserted to set the second bit store (104) to a second logic state in response to receiving an external signal.

11. The memory device of claim 10 wherein the first bit store (202) is addressable and the address space of the first bit store is a subset of the address space of the memory array.

12. The memory device of claim 10 wherein the write control logic (205a-205n) is further adapted to enable writing to the first bit store (202) only when the corresponding bit in the second bit store (104) is equal to a first logic level.

13. The memory device of claim 12 further including a second write protect pin (WP2) coupled to the second bit store, the bits of the second bit store being set to the first logic level when the second write protect pin is asserted LO.

14. The memory device of claim 10 wherein at least one of the memory blocks (BLKϕ) is subdivided into N pages, and wherein the memory device further includes a third bit store (302) having N page enable bits, each page enable bit corresponding to one of the N pages, the access control logic further adapted to enable and disable read and write operations to a selected page based on the logic level of the page enable bit corresponding to the selected page.

15. The memory device of claim 10 further including a radio frequency interface (520) for communication with the memory device using radio frequency signalling.

16. A method of operating a memory device, the method comprising:

in response to a read request, detecting the logic state of permission bits associated with the memory location specified in the read request and carrying out the read request if the result of the detecting step indicates that the read request is permitted;

in response to a write request, detecting the logic state of permission bits associated with the memory location specified in the write request and carrying out the write request if the result of the detecting step indicates that the write request is permitted;

dividing the memory array into a plurality of memory blocks, associating non-volatile permission bits with each of the memory blocks, and carrying out read and write requests on a per memory block basis;

updating the permission bits, including detecting the logic states of access information associated with the permission bits and carrying out the step of updating only if the access information is at a first logic state;

updating the access information, including allowing only updates wherein the access information is changed from the first logic state to a second logic state;

setting the logic state of the access information to the first logic state upon receiving a power-on-reset signal or upon asserting an access protection pin;

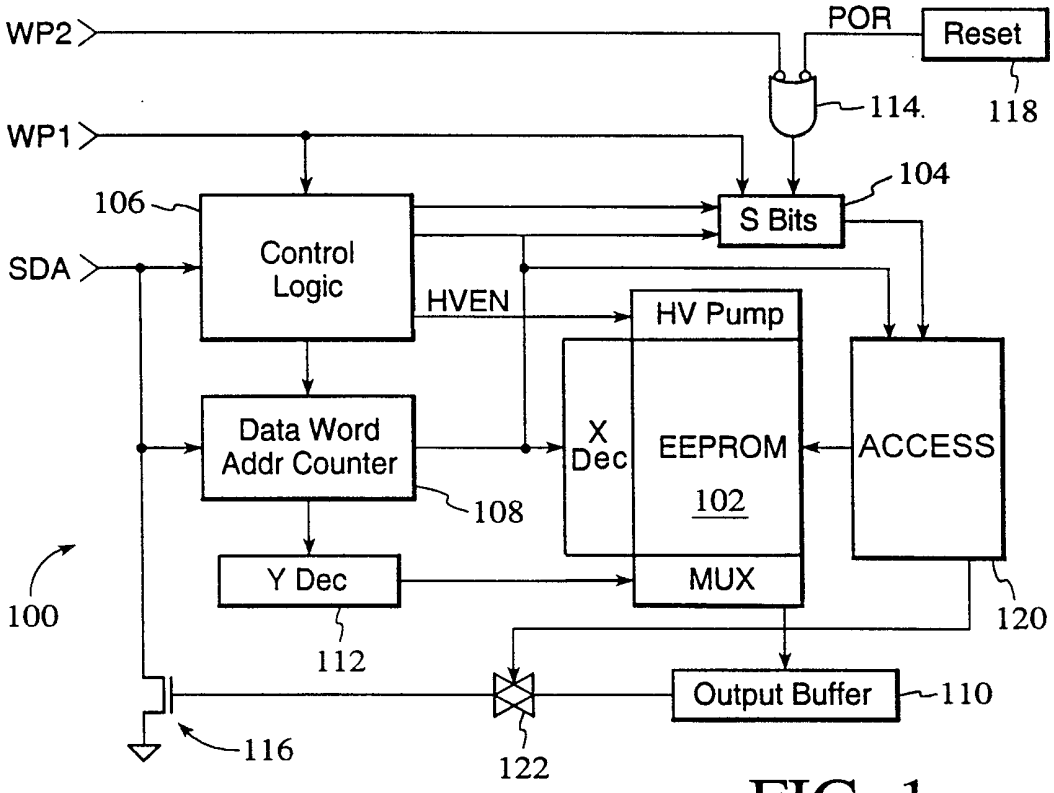
subdividing one of the memory blocks into a plurality of pages, and in response to either a read or a write request to a page, detecting the logic state of non-volatile page permission bits associated with the page specified in the request and carrying out the operation if the result of the detecting step indicates that the request is permitted.

17. (Cancelled)

18. The method as claimed in claim 16 further including allocating a portion of the memory array to store the access information.

19. (Cancelled)

20. The method as claimed in claim 16 further including communicating read and write requests via radio frequency signalling.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WP1
SDA
POR
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118
114
104
106
Control Logic
S Bits
HVEN
HV Pump
Data Word Addr Counter
108
X Dec
EEPROM
102
ACCESS
Y Dec
MUX
120
100
112
Output Buffer
110
116
122

FIG. 1

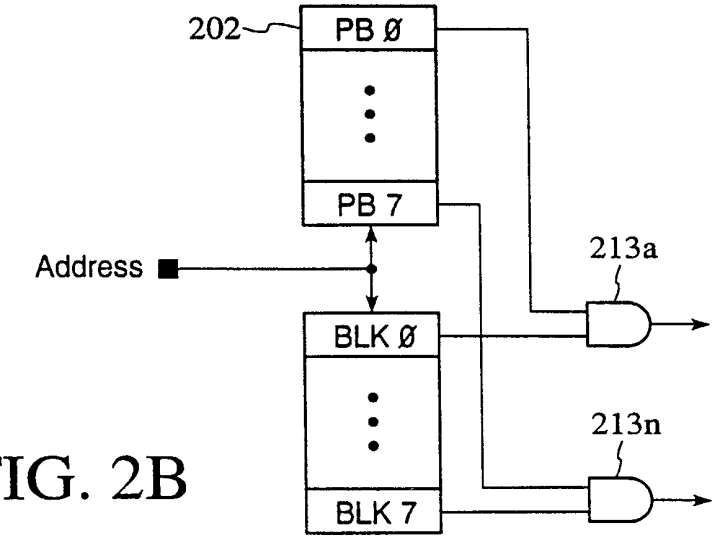
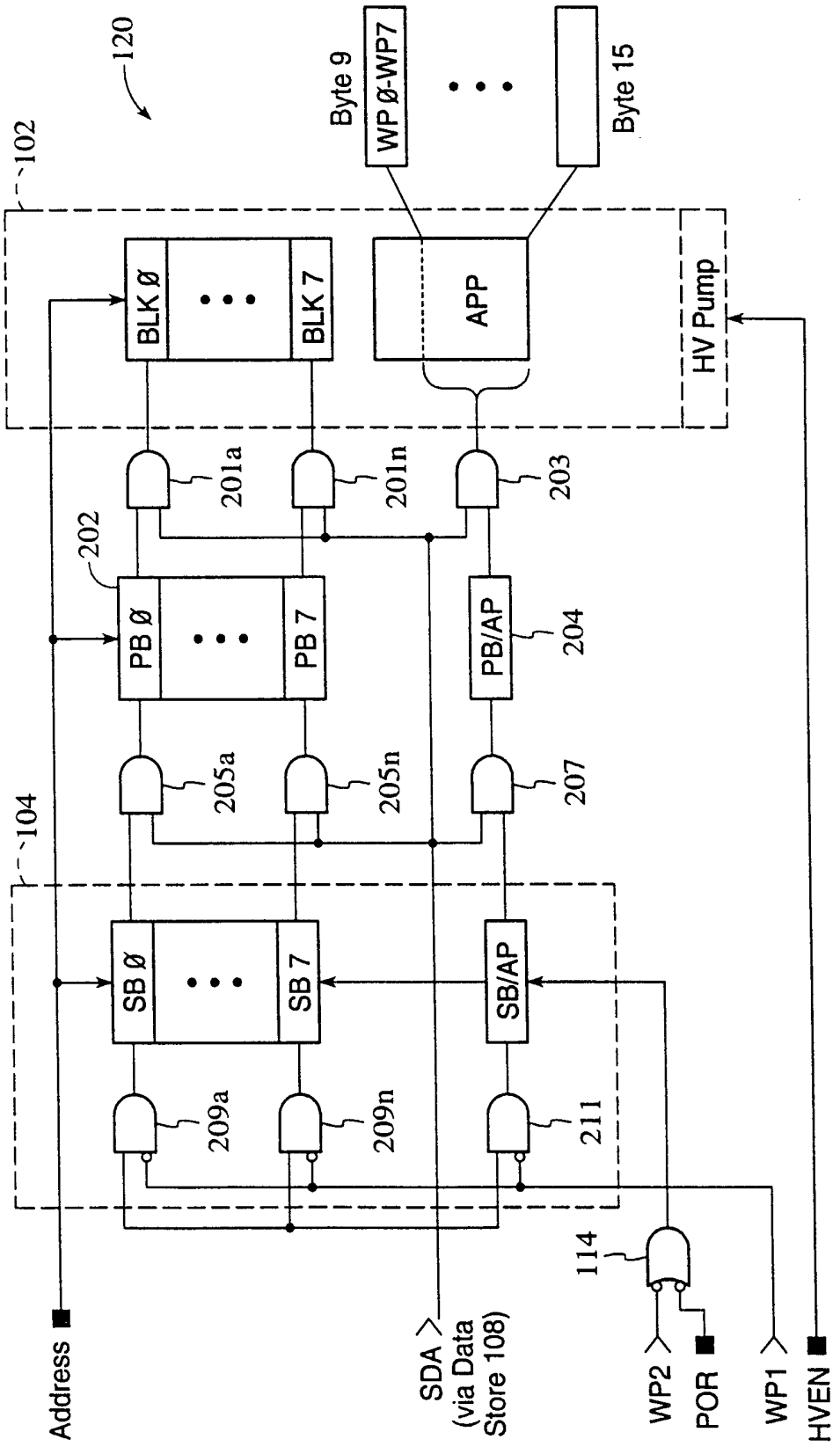

202
PB Ø
PB 7
Address
213a
BLK Ø
213n
BLK 7

FIG. 2B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102
Byte 9
WP Ø-WP7
Byte 15
BLK Ø
BLK 7
APP
HV Pump
201a
201n
203
202
PB Ø
PB 7
PB/AP
204
205a
205n
207
104
SB Ø
SB 7
SB/AP
209a
209n
211
114
Address
SDA
(via Data
Store 108)
WP2
POR
WP1
HVEN
External Signal
Internal Signal

FIG. 2A

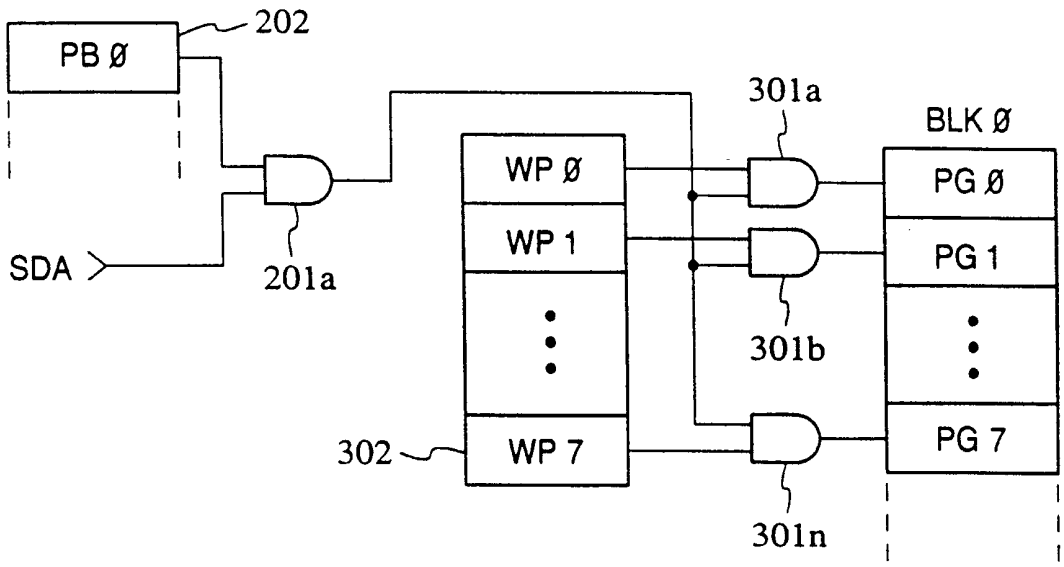

FIG. 3

Access Protection Page (APP)

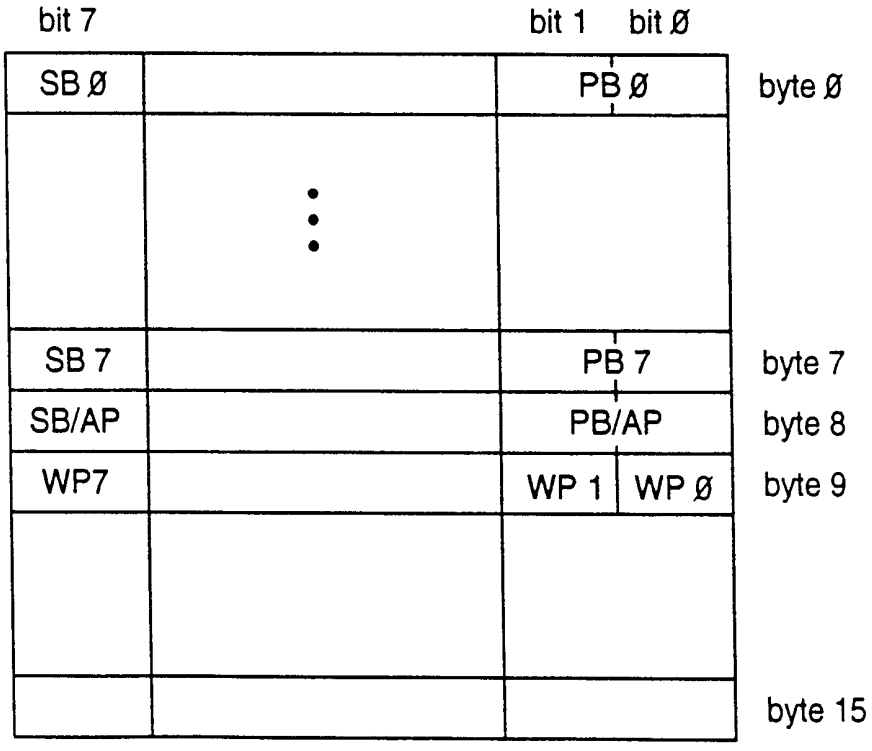

FIG. 4

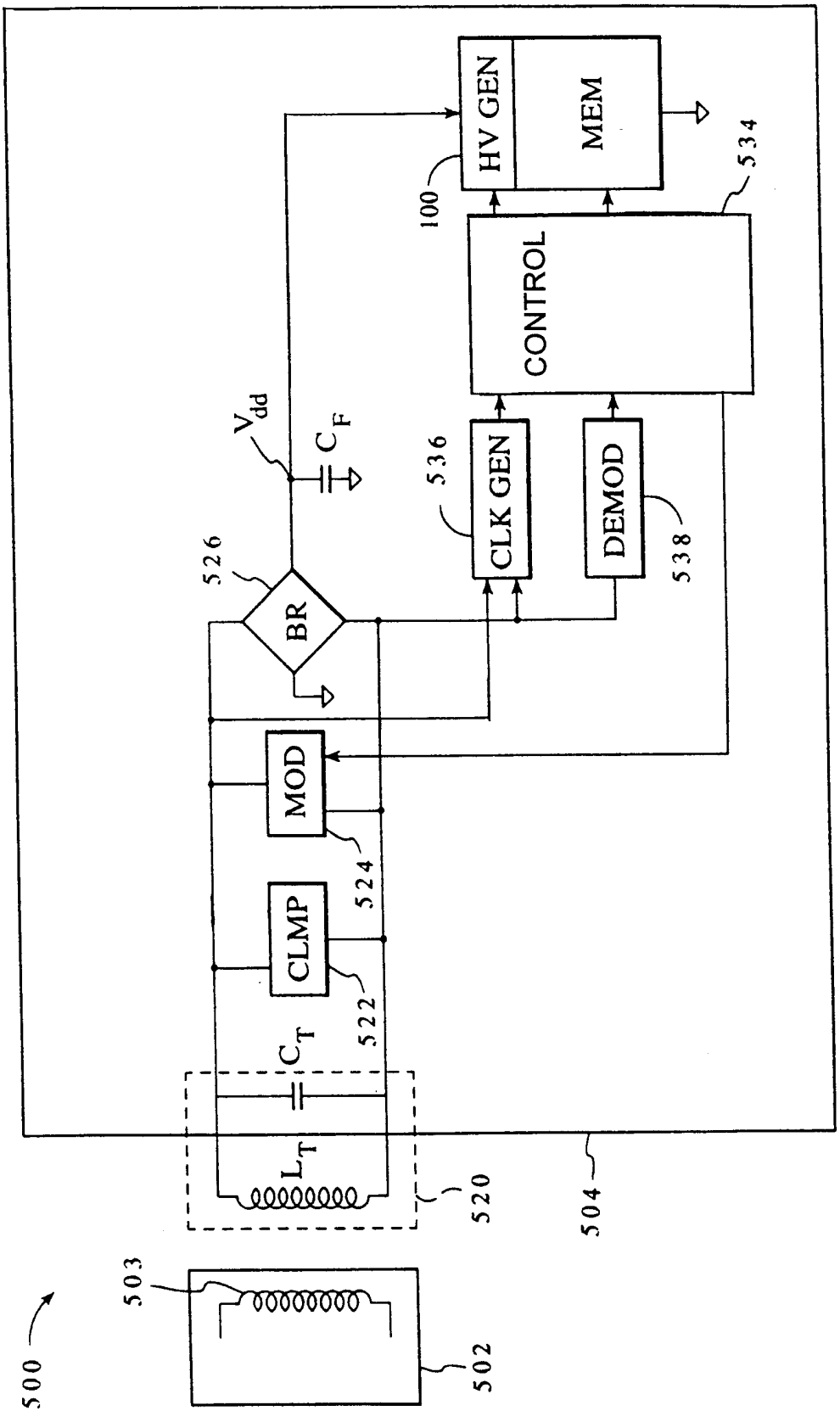
500
503
502
520
504
L_T
C_T
522
CLMP
524
MOD
526
BR
V_{dd}
C_F
536
CLK GEN
538
DEMOD
CONTROL
534
100
HV GEN
MEM

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/23525

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G11C 16/04; G06F 7/00, 12/00

US CL : 711/103, 154; 365/120, 189.05, 222

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 711/103, 154; 365/120, 189.05, 222

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, EPOABS, JPOABS, DIALOG, PROQUEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,548,741 A (WATANABE) 20 August 1996, column 4, lines 23 et seq.; column 5, lines 51 et seq.; column 6, lines 1 et seq.; column 1, line 32; column 11, lines 42-43);	1, 3, 6-8, 10-12, 14, 16-18
X,P	US 5,862,075 A (LECONTE et al) Jan 19, 1999; abstract; column 4, lines 3-64;	2, 4, 5, 9, 13, 15, 19-20
A	US 5,386,539 A (NISHI) 31 January 1995; (entire document)	1-20
A	US 5,210,854 A (BEAVERTON et al.) 11 May 1993; (entire document)	1-20
A	US 4,905,140 A (SAKAKIBARA et al.) 27 February 1990; (entire document);	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
04 FEBRUARY 1999	04 MAR 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer TUAN V. THAI Telephone No. (703) 305-3842

Form PCT/ISA/210 (second sheet)(July 1992)★