Jan. 2, 1962 B. LIPPEL 3,015,814

CATHODE RAY CODING TUBE AND CIRCUIT

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FIG. 1

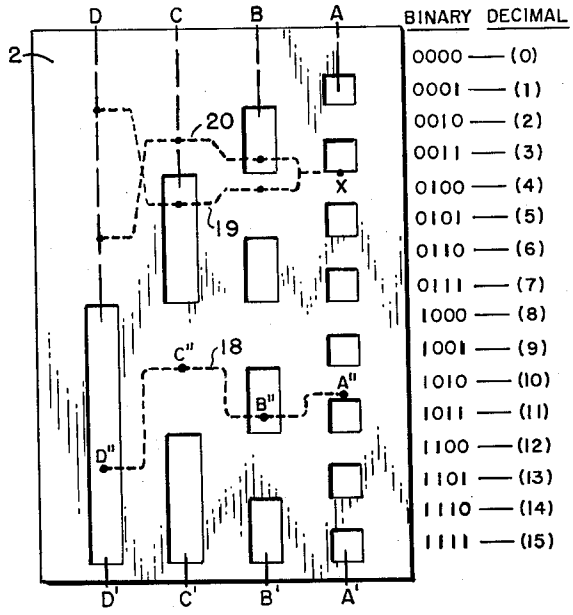


FIG. 2

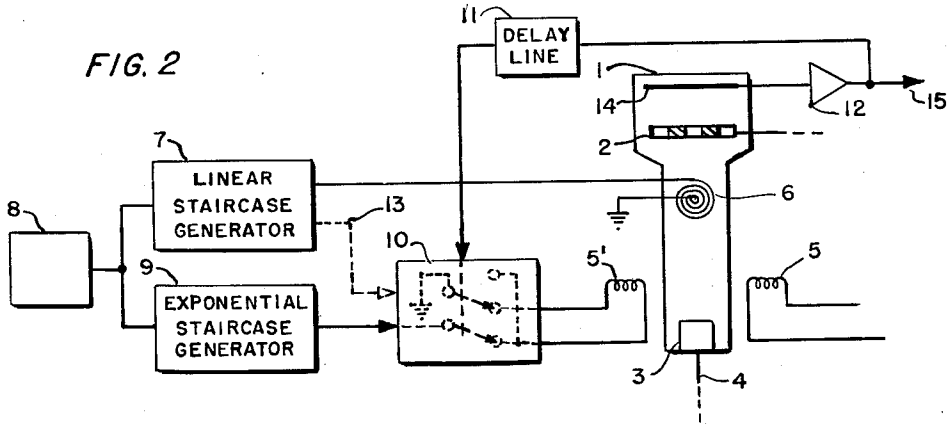


FIG. 3

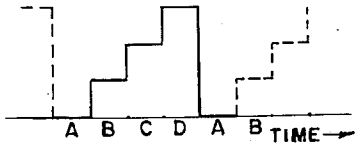
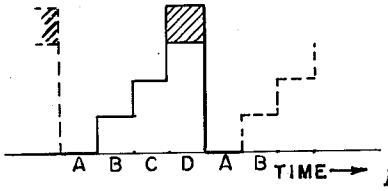


FIG. 4



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FIG. 5

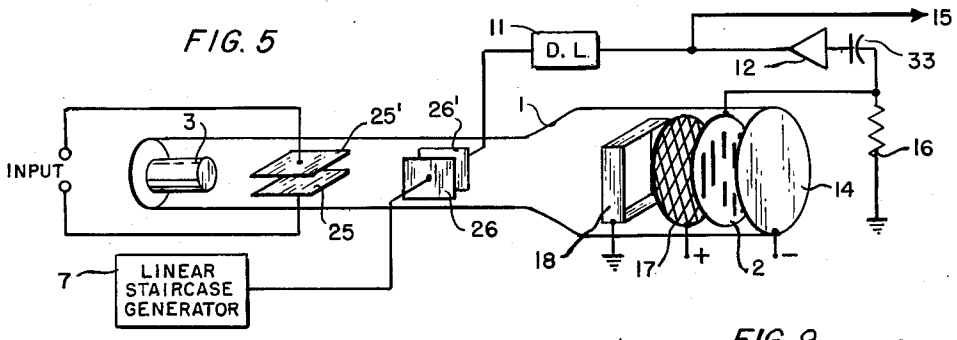


FIG. 9

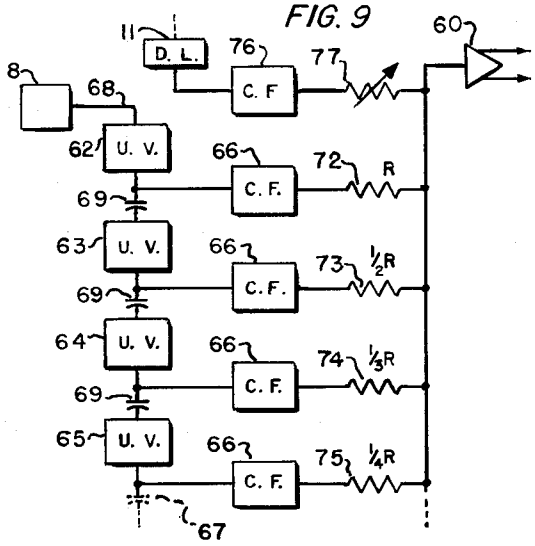


FIG. 13

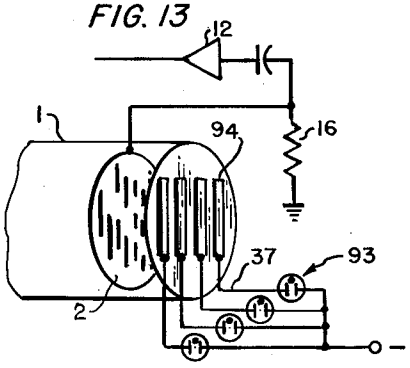
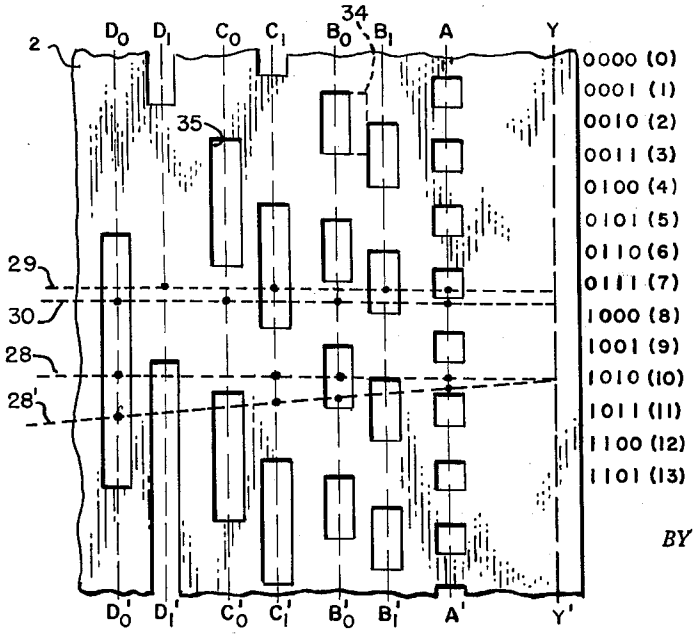


FIG. 6



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FIG. 7

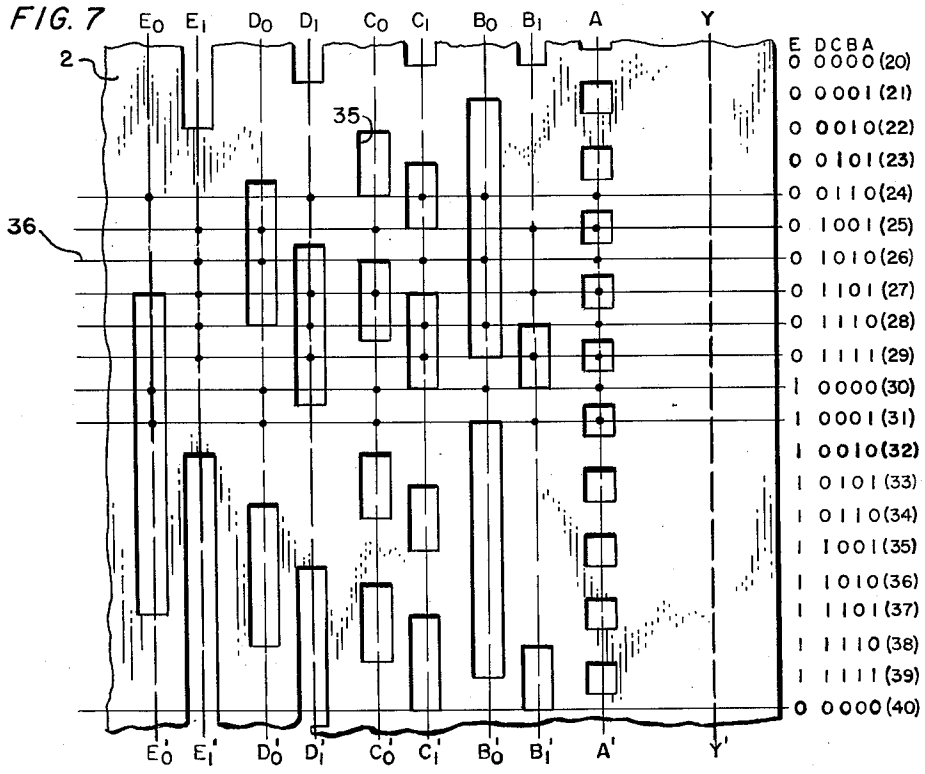


FIG. 10

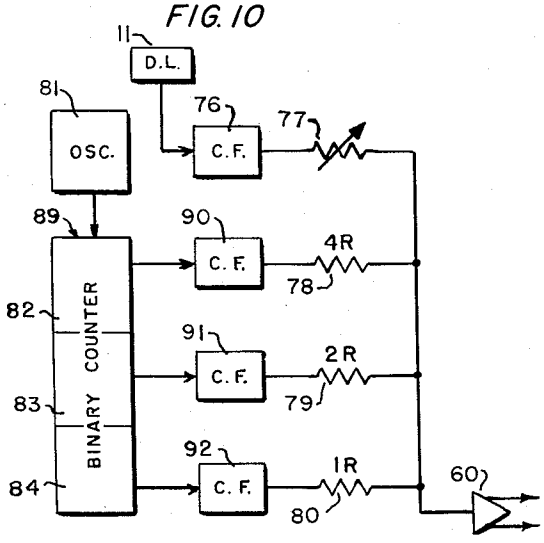
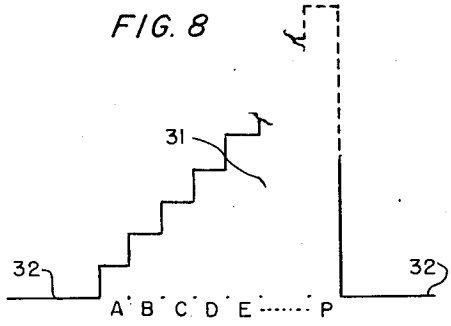


FIG. 8



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FIG. 11

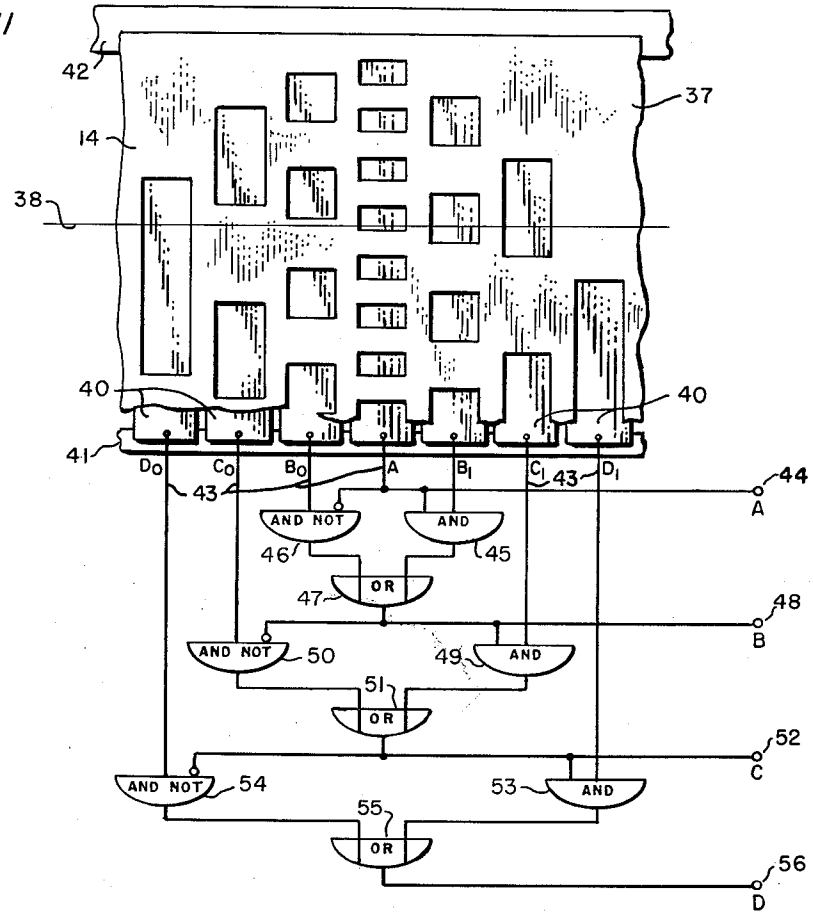
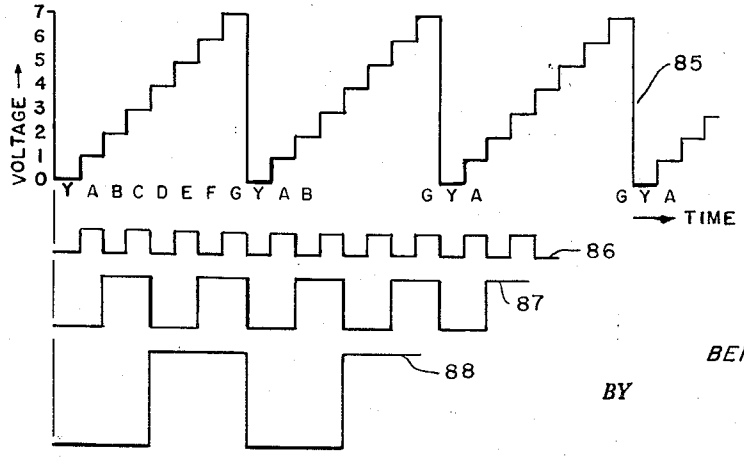


FIG. 12



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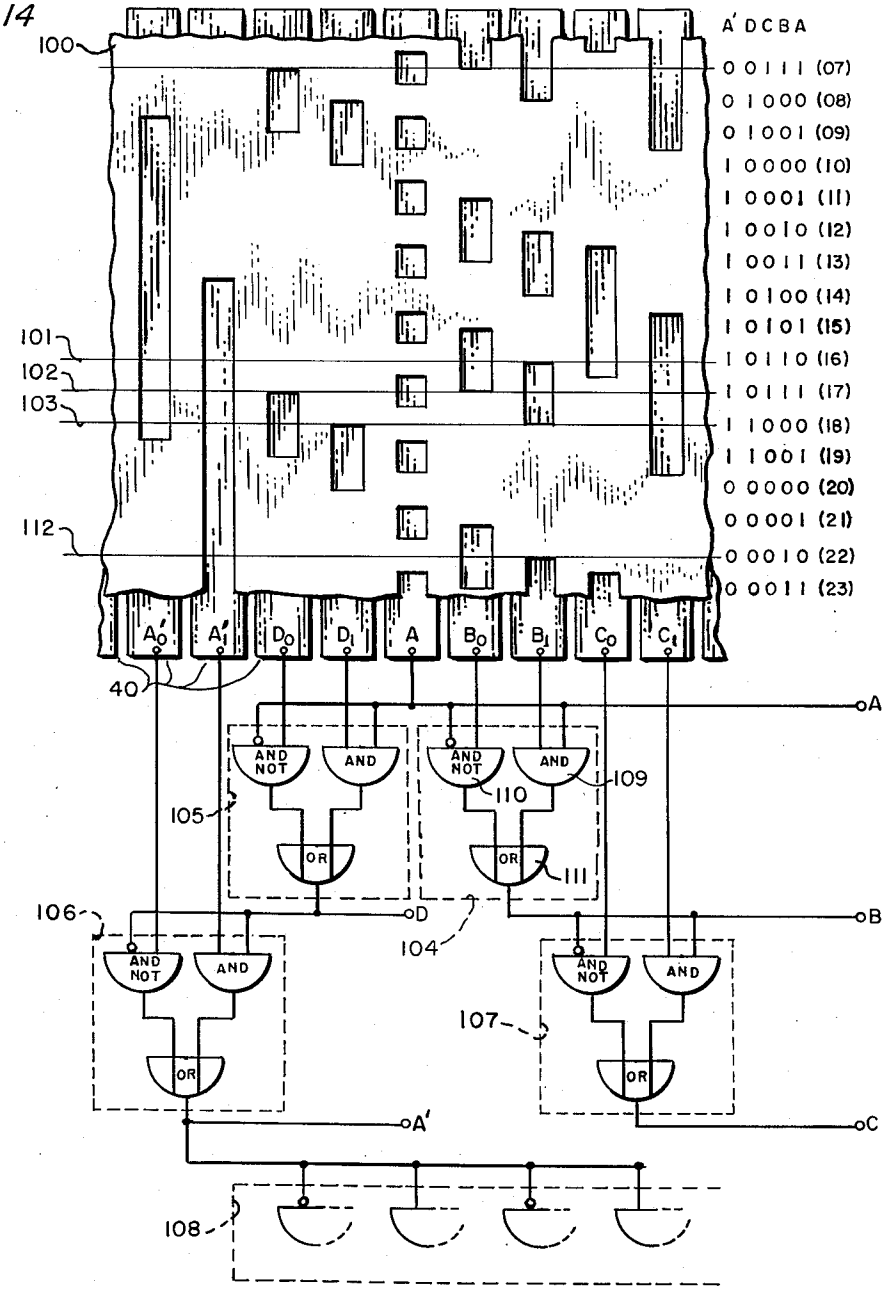
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FIG. 14



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United States Patent Office 3,015,814 Patented Jan. 2, 1962

3,015,814

CATHODE RAY CODING TUBE AND CIRCUIT

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Filed Mar. 2, 1959, Ser. No. 796,712
6 Claims. (Cl. 340—347)
(Granted under Title 35, U.S. Code (1952), sec. 266)

The invention described herein may be manufactured and used by or for the Government for governmental purposes without the payment of any royalty thereon.

This invention relates to analog to digital conversion, also called coding, encoding, and digitizing. It is illustrated entirely in relation to cathode ray coding tubes and circuits although not necessarily limited to cathode ray coding.

The broad background for this invention may be found in "Notes on Analog-Digital Conversion Techniques," edited by Alfred K. Susskind, Technology Press or John Wiley, 1957, particularly pages 5–60 and 61 on "Coding Tubes" and pages 6–40 to 72 on "Coded Patterns."

Cathode ray coding tubes are designed to furnish digital number representations of the strength of certain input current or voltage signals and ordinarily include an electron gun to form an electron beam; a generally rectangular code pattern upon which the beam may be focused; and deflection means responsive to the input current or voltage to so displace the beam that one of its coordinates represents the analog of the input, corresponding in direction and distance to its polarity and magnitude. The other rectangular coordinate of the beam regularly has a plurality of values due to scanning motion as a function of time, or use of a long line focus, to fall upon appropriate portions of the code pattern, coding the output in a manner depending on the particular tube and system associated therewith. These may be considered as the analog input and coding output coordinates.

Many variations in apparatus details, some not specifically shown in Susskind or other are to be mentioned below, will be familiar to those skilled in the art, such as the alternative use of: electrostatic or electromagnetic deflection or combinations of both; predominantly current or voltage phenomena; output from a coded pattern target, an anode behind it, a secondary emission responsive means, other electrode, or even a phosphor and photocell associated with an optical pattern (particularly useful for preliminary testing of patterns and techniques before construction of special tubes); serial or parallel reading of patterns; digitizing based on binary, binary coded decimal, or other binary coded radix representations; digitizing according to linear, exponential, trigonometric, or other scale (Susskind, page 6–69). Some of these alternatives are illustrated in various species of the present invention; where such alternatives involve a special interrelation to the invention, rather than a substantial equivalent, this will be specifically mentioned.

In a serial reading tube the beam scans the code pattern by progressively varying the coding coordinate, to produce in a single output circuit successive pulse signals at times depending on the code pattern and the scanning schedule. In a parallel reading tube a long line focus or its equivalent is used to provide the multi-valued coding coordinate, producing in separate output circuits signals depending on the code pattern. It is well known that a maximum 2^n different degrees of deflection can be indicated with a tube providing n possible output signals, or "bits," each of which can be represented by two conditions. The commonly-used abbreviation "bit" will henceforth be employed interchangeably with the term "binary digit," especially to distinguish from digits of other number bases. The term "two-valued" may also be used to further emphasize the quantitative significance of the code elements.

As described generally above, the outputs of cathode ray coding devices are serial or parallel combinations of binary signals. A binary signal ideally has only two recognized values (for example, "zero volt" and "one volt," or "minus one volt" and "plus ten volts"); one of these states is by convention designated with the written symbol or digit "0," the second by the digit "1." Every combination of binary outputs similar to that produced by a digitizer can thereby be represented by a written sequence of 0's and/or 1's which is called a "binary-coded number." Although the operating principle of the aforementioned cathode ray devices can readily be extended to provide combinations of outputs each of which assumes three states (ternary-coded outputs) or more than three states, it is well known that binary-coded digital representations are preferred in most electronic digital equipments and systems.

For many applications it is preferred that the binary-coded numbering system employed shall be the conventional binary code (also called the natural binary code), which is related in construction to the Arabic system of numbering with decimal digits. Specifically, in the Arabic (natural decimal) system a number whose value is N is written $a_n a_{n-1} \ldots a_2 a_1 a_0$, according to the relation

$$N = a_n 10^n + a_{n-1} 10^{n-1} + \ldots + a_2 10^2 + a_1 10^1 + a_0 10^0 \quad (1)$$

and, in the natural binary system, N is written

$$b_m b_{m-1} \ldots b_2 b_1 b_0$$

according to the relation

$$N = b_m 2^m + b_{m-1} 2^{m-1} \ldots + b_2 2^2 + b_1 2^1 + b_0 2^0 \quad (2)$$

Each symbol a_k is a specific digit chosen from 0, 1, 2, 3, 4, 5, 6, 7, 8 or 9, and, likewise, each symbol b_k is either 0 or 1.

On the other hand, there are other applications (as when numbers are presented to human beings), where the common decimal system is desirable.

Although based on the use of ten different symbols, decimal numbers can nevertheless be binary-coded by replacing each of the decimal digits 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9 with a unique combination of four or more binary digits. Such numbers are referred to as binary-coded decimal numbers or bit-coded decimal numbers. The latter term minimizes any implication that decimal code must be derived directly from conventional (natural) binary weighted code by using only values 0 to 9, omitting 10 to 15, as ordinarily assumed from the term "binary coded decimal," whereas a wide variety of codes (even arbitrary) may be assumed from the term "bit-coded decimal." The Baudot Teletype code is a binary coding system for both Arabic numerals and letters of the alphabet; the example of the Teletype printer illustrates one arrangement whereby binary-coded decimal numerals are decoded so that Arabic numerals are displayed.

Accordingly there is requirement for digitizers with outputs as pure binary numbers (preferably the conventional or natural binary numbering system), and also for digitizers giving binary-coded decimal numbers.

The cathode ray voltage or current coder is a so-called "reading-type" digitizer, akin to coded-commutator-and-brush devices and optical code wheels used for coding of position. Any reading-type digitizer has two characteristics of interest, viz:

(1) It has a pattern element (e.g., coded commutator or pattern mask) and a reading element (e.g., brush assembly or focused electron beam and deflection system).

(2) Special means—called "quantizing" means—provided to prevent erroneous output readings when the input is midway between properly encoded values (called "quantum levels").

For proper operation, it is necessary that both the pattern element and the reading element be constructed

accurately relative to one another, in dimension and in other geometrical relationships. The accuracy and precision of the output is in practice limited by departures from perfect constructional and operational accuracy of the components.

For positions coders of the reading type three different quantizing means are in practical use, viz:

(1) A mechanical click or detent is used to force the digitizable input to the central region of a quantizing level, thereby avoiding transitions.

(2) A unit-distance code (exemplified by the "Gray" or "reflected binary" code) is employed; such codes are free from erroneous readings because only one binary digit changes at each transition. Digit outputs provided directly with such codes do not follow the natural numbering system exemplified by Equations 1 and 2 (or desirable LSD-first order) and for most purposes must be processed in translator equipment to provide natural numbers.

(3) A system of logical selection between dual encoding means for each output bit is employed, wherein each choice depends upon previous bit outputs.

The last two means especially are widely and competitively used in coders for angular or linear displacement, so that there is no obvious superiority of one over the other. Optical code wheels for very accurate angle measurement have been disclosed for both systems, of which the unit-distance-code type at least is commercially manufactured.

In the case of cathode-ray-tube digitizers, tubes employing wire grids or holes for indexing, in a manner comparable with mechanical clicks or detents, have been disclosed by Sears (Bell System Technical Journal, vol. 27, January 1948, pages 44–57) and by Goodall (U.S. Patent No. 2,616,060). The use of unit-distance codes (particularly Gray code) has been disclosed by Goodall (Bell System Technical Journal, vol. 30, January 1951, pages 38–40) and numerous others, but the prior art use of logical selection techniques in a coding tube is not commonly known.

Although presently marketed code wheel angle digitizers quantized with unit-distance codes are better than one-tenth as accurate as the best manually-read theodolites, it is believed that prior art coding tubes (also employing unit-distance coding) have been at most between one and two percent as accurate as the best voltage-measuring devices, and only about one-tenth as accurate as non-reading type digitizers which are inherently slower in operation.

I have analyzed the sources of error in cathode ray coders, and also the reading-type position coders, and have concluded that a principal limitation on the accuracy of prior art coding tubes is the inability to provide and maintain a more accurate geometric configuration in the reading element. Specifically, the pattern element in a coding tube (the pattern mask) can be machined or otherwise fabricated with relatively accurate dimensions and configuration, and being a rigid body, holds the dimensions and configurations; in this respect it is like the pattern element provided in an angle coder or the like; the "reading element" in the coding tube, however, is a locus of impingement of electrons during the generation or reading of a complete number output (specifically, in prior art a line in the coding scan direction). The dimensions and configuration of such locus of impingement are basically defined by electron sources, electron lenses and lens apertures, deflection means, electrical power sources, and the like; such an electronic reading element cannot in practice be made as accurate as mechanical reading elements such as brush assemblies or optical slits or as accurate as its cooperating pattern element; furthermore, extraneous influences, such as external electric or magnetic fields, variations in supply voltages, or variation of electrical signal input during scan may introduce dimension changes in the reading element or distort its configuration, a problem which does not ordinarily arise with position coders. In particular, configuration errors in an electron-beam reading element correspond to movement of brushes relative to one another in a brush-and-commutator device or bending of slits in an optical coder; and variations of the sharpness of focus when the beam is deflected over the surface of the mask corresponds to variability in the width of brushes or reading slits; and the situation whereby the accuracy of a cathode ray tube coder is limited by errors in the reading element, long before it is limited by practical tolerance errors in the pattern mask, is not found with other reading-type coders. Although the use of logical selection has been little known for cathode ray coders, I have noticed that this method offers marked advantage because it tolerates configuration errors to a much larger extent than the quantizing means hitherto employed for cathode ray digitizers. The advantage does not have a comparable significance for position coders, wherein configuration errors do not play such a part owing to the mechanical construction of both pattern element and reading element. Furthermore, this advantage has apparently been little known to prior inventors and has therefore not been used to provide better cathode ray digitizers than have hitherto been available.

Logical-selection quantizing for conventional binary outputs is ordinarily done with dual brushes in a commutator device or by optical equivalents, and a single chain of selection is used, operative in the same manner on each bit in succession except an initial bit (see Susskind, FIGS. 6–22). The pattern element may be exactly the same as when clicks or detents are used for conventional binary coding.

Broadly similar means, whereby binary-coded decimal (or other radix) output numbers may be generated are shown by Ziserman, IRE Transactions on Instrumentation, vol. 5, pp. 215–218 and in his Patent No. 2,873,-442; by Lippel, IRE Transactions on Electronic Computers, vol. EC–4, No. 4, pp. 158, 159, and in Susskind, pp. 6–68, 69, but in all such cases bit choices cannot be made by simple chain selection. It can, in fact be demonstrated that the specific interconnection circuit of brushes shown in Susskind, FIGS. 6–22 suffices only for number bases which are integral powers of two.

The cathode ray coder system shown in my FIG. 2 below, which uses the pattern mask shown in FIG. 1, is the most direct combination of the usual system of logical selection with a cathode ray tube coder. Although it demonstrates aforementioned benefits from such combination, which are not apparent in prior art, the system is limited to conventional binary code outputs for the same reason as brushes interconnected by analogous logic circuits.

The use of split columns as in FIG. 6 has been shown by R. H. Barker in his article, "Measurement of Angle Using the Binary Digital Scale" (see A. Tustin, "Automatic and Manual Control," Academic Press, Inc., New York, pp. 561–566; 1952), and in his British patent specification 650,913, published Mar. 7, 1951 wherein he points out that the upward and downward displacement of each half column is substantially equivalent to displacement of the reading means as shown in FIG. 1. Barker does not consider the dual columns in any other way and does not show the reading of other than conventional binary numbers. Neither is any other use of split patterns for encoding with a variety of number bases known.

In my study of the split-column system I have noted that (besides the system operating advantages disclosed by Barker and incorporated in some versions of my invention) the use of two columns in place of one permits storage of more information. Consequently, I have concluded that by use of dual columns the selection of successive bits can be chain controlled in a manner that provides variation of selection logic from quantum level to quantum level and from column to column in FIG. 1.

In have in fact found the means for utilizing the split columns to provide the effect of such flexible selection rules. I have thereby expanded the areas of application and increased the usefulness of my cathode ray digitizers by providing natural number outputs in a variety of radixes, using the same control circuits as for simple binary numbers.

I have also found that the split-column feature permits logical selection schemes of either simple or complicated structure to be conveniently and straight-forwardly used in a parallel reading cathode ray digitizer, where the problem of configurational errors in the beam is especially important, for which purpose the analog offsetting arrangement of FIG. 1 is less suitable or even impossible.

The object of my invention includes the generation by simple logical selection of codes previously considered either entirely unsuited thereto or suited only to a more complex form of logical selection.

The invention will be analyzed and described in connection with the accompanying drawings, in which:

FIG. 1 represents a conventional binary code pattern illustrating one manner in which the invention may be applied in a prior art serial reading cathode ray coding tube;

FIG. 2 illustrates a circuit diagram for a cathode ray tube incorporating a code pattern such as that of FIG. 1;

FIGS. 3 and 4 illustrate staircase waveforms involved in the operation of the circuit of FIG. 2;

FIG. 5 illustrates a circuit diagram similar to that in FIG. 2 for a variation of the invention involving a different type of code pattern;

FIG. 6 illustrates a modified pattern for conventional binary code applicable to the circuit diagram of FIG. 5;

FIG. 7 illustrates the same general type of code pattern as in FIG. 6 for binary coded decimal members;

FIG. 8 illustrates a staircase waveform involved in the operation of the circuit of FIG. 5;

FIG. 9 illustrates a suitable waveform generator for the type of waveforms illustrated in FIG. 8;

FIG. 10 illustrates a suitable waveform generator for the type of waveforms illustrated in FIG. 12.

FIG. 11 illustrates a modified pattern for conventional binary code especially suited to a parallel reading cathode ray coding tube and logic circuits for applying the invention;

FIG. 12 illustrates the combining of waveforms by the circuits of FIG. 10 to generate a staircase waveform;

FIG. 13 illustrates a parallel-reading output circuit supplementing the normal output circuit of a serial cathode ray coding tube; and

FIG. 14 illustrates a modified pattern for decimal numbers the digits of which are represented by conventional binary code, especially suited to a parallel reading cathode ray coding tube.

Although I mostly prefer to use other arrangements for reasons which will become clear later, the arrangement of FIG. 2 will be described first as an aid to orderly exposition. FIG. 2 shows schematically a serial type cathode ray coding tube **1**, which includes the pattern mask **2**. FIG. 1 shows said mask in detail as it would be arranged for generating 4-bit conventional binary numbers to permit sixteen different values of current flow to be measured and represented digitally. Ordinarily, a larger number of vertical columns will, of course, be used to generate more than four binary digits, and thus to measure with more precision. The cathode ray tube **1** of FIG. 2 has an electron gun **3** which may be of conventional design and conventionally supplied with heating current and various electrode potentials by means of leads shown collectively as **4**, as required to form a pencil beam of electrons coming to a focus on the plane of the mask **2**.

It may happen that there are imperfections in the design and construction of the electron-optical system, which make it impossible to adjust fixed potentials on the leads **4** to provide equally sharp focusing over the whole of the pattern area of the mask **2**. In such case, the focus should be adjusted so that a line trace AA', obtained by scanning in the direction of analog deflection and passing centrally through the pattern column with the finest perforations is brought into the best possible focus, even though the trace may now become sensibly defocussed when moved to the opposite side of the mask.

Paying attention now to FIG. 1, the tube may be adjusted so that with no current flowing in the scanning deflection means **6**, the cathode ray beam focused into a spot, falls somewhere on the line AA' which traverses the first column of perforations. More particularly, the quiescent position of the focused electron beam will be a point A'' on the line AA', where the distance AA'' is the analog deflection, resulting from a certain strength of input current flowing in the input coil **5**.

Suppose that the input current flowing in the coil **5** of FIG. 2 has strength of ten units. Then the point A'' will be at a level marked 1010 on the scale labelled with both binary and decimal numbers on the right of FIG. 1. Assume for the present that the input current does not vary, so that the deflection AA'' is fixed. It is required that the serial coding tube shown shall generate and transmit in succession the binary digits 0, 1, 0, and 1, which is the serial mode of transmission of the binary number 1010 with the right-hand, or least-significant, digit sent first.

Returning to FIG. 2, the staircase generator **7** generates uniformly increasing steps of current, as shown in FIG. 3, commencing with zero current during the time interval A; it provides unit current during time interval B, two units of current during the next time interval C, and three units during D, a different step of current being provided for each column of perforations in the mask **2**. It returns to zero after the last step, which corresponds to the last column of perforations and which is shown as D in FIG. 3. The exponential staircase generator **9**, operates synchronously with the generator **7** to produce current steps as shown in FIG. 4. In FIG. 4 it is seen that the output is zero during time interval A, one unit during interval B, two units during C, and preferably four units during D. When more than four columns are provided in the code pattern of mask **2**, succeeding steps preferably have amplitudes of 8 units, 16 units, etc., increasing as integral powers of two. Although growth of steps in proportion to integral powers of two provides optimum operation, it can be proven that a linear growth as shown under the shaded area of FIG. 4, or any intermediate curve of increase, is almost as effective.

The two staircase generators may be triggered by a common interrogating source **8**, whereupon each proceeds to generate one full cycle of steps, A through D and back to A, as shown with solid lines in FIGS. 3 and 4. Alternatively, the two generators may continuously recycle, automatically repeating the steps in synchronism with each other, as shown dotted in FIGS. 3 and 4. In the former case a binary number will be generated once after each interrogation signal, and in the latter case it will be continuously regenerated and transmitted out anew, changing only when the input current changes perceptibly. In the discussion which follows, it is immaterial which kind of step operation is provided for the step generators.

Referring to FIGS. 1 and 2, the cathode ray beam comes to a focus upon the surface of the mask **2** at the point A'', which is shown to be on a solid portion of the A column. The entire beam current is therefore intercepted by the mask **2**, so that the collector **14**, the amplifier **12**, the input to delay unit **11** and the device output **15** receive no electrical signal. It is by convention understood that the bit "0" is thereby indicated at the output **15**. At the same time, because the expo-

nential generator provides null output during the initial step A, no current flows through the supplemental coil 5′ to deflect the cathode ray spot away from A″. A short time later the two step generators progress simultaneously to step B. The linear generator 7 provides a current increment through the coils 6 which causes the spot to jump from line AA′ to line BB′ and the exponential staircase generator puts out a unit of current. The delay line 11 delays the output signal by an interval of time equal to the duration of each step; for the duration of step B, the electronic polarity switch 10 is therefore provided with a signal from the delay unit indicating that a "0" was generated during step A. The switch is so arranged that, in the presence of a "0" from the delay line, the current through coil 5 augments the analog deflection in the manner of a larger current input, but in the presence of a "1," the direction of current flow in the coil 5′ is reversed, so that the analog deflection is diminished an equal amount. In the case illustrated, therefore, the analog deflection is augmented during step B so that the beam focus is at B″. The increase in distance BB″ over AA″ is ideally adjusted to be one-fourth the distance between centers of the perforations in the AA′ column (equivalent to one-half quantum), but the adjustment is not critical. It will be seen on FIG. 1 that the focussed beam now passes through a perforation to impinge on the collector 14 of FIG. 2 so that the second bit generated is "1." It follows that a negative increment is added to the basic deflection AA″ during the next step C of the two step generators, inasmuch as the polarity switch now acts in accordance with a delayed "1." The magnitude of the increment CC″ minus AA″ is a full quantum for the reason that the generator 9 provides twice as much output during C. C″ will be seen to fall upon the solid metal of mask 2 so that another "0" is put out for the third binary digit, resulting in a positive increment during the generation of step D, so that the beam falls on a hole at D″, resulting in a "1" for the fourth digit. The sequence of bits A, B, C, D is therefore seen to be 0, 1, 0, 1 which is the manner in which the binary number 1010 is transmitted serially fine-digit-first.

The incremental deflection of the beam in accordance with previously generated digits serves to confine lines of scan to interior portions of the code pattern, that is to say to the central portions of perforations or to the central portions of the metallic bridges between perforations, so that the line of scan never touches edges of B, C, or D perforations. However, in the digitizers of my invention, the first reading locus A″ may be permitted to straddle a pattern boundary, so long as the amplifier 12 is constructed to provide only either of two outputs, the input will be encoded properly for one of the two adjacent encodable values. For example, on FIG. 1, suppose that three and one-half units of current are measured, so that the initial reading locus is X on the boundary between quantum level 0011 (three) and 0100 (four). If the amplifier 15 puts out a "1" during the A step the beam will be deflected upward on FIG. 1 for reading of column BB′ and the line of scan 20 will be followed. This line of scan avoids boundaries in the remaining portions of the pattern and generates the binary number 0011. On the other hand, if the output 15 is a "0," the line of scan 19, which equally avoids pattern boundaries, will be followed, and the binary number 0100 will be generated. Either binary number, 0011 or 0100, is a proper representative for three and one-half rounded-off to the nearest integer. On the other hand, it is well known that a perfectly horizontal line of scan (as when the coil 5′ is removed) might generate incorrect numbers (for example, 0111, seven).

It will be noted that in the mask shown in FIG. 1, which is designed for the conventional binary code, the size and spacing of the perforations increase rapidly, going from the column AA′ to the opposite column DD′; it will also be noted that reading loci (for example, A″, B″, C″ and D″) tend to be well inside of pattern elements (perforations, or bridges between perforations) everywhere but in the AA′ column; it is therefore tolerable for the beam to become gradually defocussed at the surface of the mask to a degree which increases with the distance from AA′, or for the pattern elements to be constructed with errors in edge location increasing in proportion to the perforation size, or for the coils 6 to be misaligned so that the direction of scan is not quite perpendicular to AA′; or for the analog deflection AA″ to vary in the course of the scan so that the scan direction departs slightly from the horizontal. This feature, which confines the requirement for full accuracy of construction and electrical operation to only one column of pattern elements and permits gradually increasing tolerances for other pattern elements spaced away from said one column, is a characteristic feature of all forms of my invention from which many of its advantages derive.

The embodiment shown is a primitive embodiment which can be readily reduced to practice, and which moreover could be simplified by eliminating the exponential step generator 9, using instead the output of the linear generator 7 as by the dotted connection 13. However, I shall not describe this form of my invention in greater detail, for the reason that I ordinarily prefer alternative forms, which cannot be used with the mask design shown in FIG. 1 but which have other advantages.

FIG. 5 illustrates a preferred arrangement for the serial form of my invention, which employs simpler control circuits than the arrangement of FIG. 1, and which furthermore lends itself better to generation of natural decimal (as well as natural binary) number outputs, or natural number outputs based on radixes other than two or ten. For convenience and clarity a radix other than an integral power of two may also be defined as a radix having an odd factor. Thus the radices 6 (or 12) and 10 would have factors 3 and 5; angle or time radices might have more than one odd factor as for 60 minutes, 90 degrees, etc. In accordance with usual mathematical practice, unity is not considered as a factor, especially since including unity would so broaden the expression "having an odd factor" as to be meaningless.

The provision of decimal outputs is particularly important and will be illustrated in detail. For such outputs the decimal digits 0, 1, 2, 3, 4, 5, 6, 7, 8 or 9 must be indicated at the output 15. Every one of the ten decimal digits is therefore associated with a unique combination of four or more bits which can be generated serially to indicate that particular decimal digit, i.e., the decimal digits are binary-coded. Conventional positional notation is used and decimal digits are generated in the order of increasing sgnificance; thus, when the value of an input to the digitizer is one-hundred and twenty-three units, the output is the binary-coded representation for the digit 3, followed by the binary-coded representation for 2, followed by the code for 1.

The radix with which a digitizer encodes, and the binary-coding language for digits is determined by the code pattern placed on the mask 2. Any one of a very large number of binary-coded systems can be used on the mask.

FIG. 6 shows a fragment of a mask whose coding pattern provides conventional binary numbers, and, likewise, FIG. 7 shows a portion of one variety of coding mask designed for decimal digitizing. The binary code with which the FIG. 7 mask represents decimal digits is a well-known code described as a 4, 2, 2, 1 weighted code. A typical perforation is labelled 35 on either mask.

Directing our attention now to FIG. 5, the tube 1 has analog deflection plates 25 and 25′ and scanning plates 26 and 26′. The electron gun 3 forms a pencil beam

of electrons which comes to a focus in the plane of the perforated mask 2, and in particular forms a sharp focus when it falls on the line AA', shown on the detailed drawing, FIG. 6. The focus of the electron beam scans horizontally across the pattern of FIG. 6 in response to a deflection signal from the linear staircase generator 7 of FIG. 5. The beam position vertically depends upon the electrical potential difference between the analog deflection plates 25 and 25', which in turn is a measure of the input. The horizontal traces labelled 28, 29 and 30 on FIG. 6 are scanning loci, corresponding to three different values of analog deflection. To the right of the mask the binary number 0111 is written on a line with trace 29, to indicate that the binary number to be generated for this deflection ends with the four least-significant binary digits 0111. Inasmuch as the binary number 0111 has value seven, the decimal number 7 is also, for convenience, written in parentheses. It should be understood that in a seven bit coder (128 levels) the pattern for the four bits (16 levels) as shown (double columns except for units bit) would repeat 8 times and a trace identical to the showing of trace 29 would occur not only in generating the binary number 0000111 (7) but also in generating 0010111 (23) 1110111 (119), etc. The principle of my invention which insures that the digits 1, 1, 1, and 0 are the first four digits to be generated serially insures proper encoding in the remaining digit places, regardless of the digits there to be generated.

Returning now to mask 2 shown in FIG. 6, a column of perforations AA' (shown near the right) generates the first, or least significant, bit. Two columns of perforations B_0B_0' and B_1B_1' are provided for the second bit, and dual columns, likewise identified by 0 and 1 subscripts, are provided for the third (C) and fourth (D) bits, as well as for the succeeding bits which may be generated by portions of the mask pattern not shown. The spacing horizontally between AA' and B_0B_0' is the same as the spacing between B_0B_0 and C_0C_0' or between any other pair of successive columns with subscript 0.

The staircase generator 7 of FIG. 5 provides a uniformly increasing staircase output, similar to that shown in FIG. 3 but preferably having at least as many steps or levels additional to the quiescent level as there are bits to be generated. The generator and the cathode ray tube deflection system are preadjusted so that, with the output of amplifier 12 held at the "0" signal level, the focussed spot scanning from right to left in response to the signal from the staircase generator, comes to rest on the columns of perforations denoted AA', B_0B_0', C_0C_0', D_0D_0' and so on, jumping quickly across all columns labelled with 1 subscripts; and with the output of amplifier 12 held at the "1" signal level, an additional voltage bias superimposed by means of the deflection plate 26' shifts the entire staircase scan rightward, so that the focussed beam now alights on all columns with "1" subscripts and on none of the columns with "0" subscripts or the AA' column.

The AA' column of FIG. 6 corresponds to the AA' column of FIG. 1. The B_0B_0' column is similar to BB' of FIG. 1 but it is displaced upward one-half quantum, so that scanning in said column is equivalent to scanning with the analog deflection augmented by one-half quantum (as at B'' of FIG. 1). Likewise B_1B_1' of FIG. 6 is displaced downward with respect to BB' of FIG. 1, so that reading in B_1B_1 is equivalent to diminishing the analog deflection. Likewise C_0C_0' is displaced upwards by a full quantum, D_0D_0' by two quanta, E_0E_0' four quanta, etc. The displacement doubles from column to column, to correspond with the optimum exponentially increasing downward offsets of the scan provided by the exponential scan generator 9 of FIG. 1. In a like manner, C_1C_1' is displaced downward one full quantum, D_1D_1' is displaced downward two quanta, etc., to provide the equivalent of exponentially increasing upward offsets. The term "quantum" when applied to distances refers to the unit of analog deflection which the digitizer effectively counts; perforations in the AA' column are separated by two quanta of distance.

In the system of FIG. 5, the staircase generator 7 may (as in the case of the system of FIG. 2 already described) be either of the single-sweep type, or the continuously recyling type. Assume for the moment that a single-sweep generator is provided. FIG. 8 shows the output of such a generator as a function of time. During its rest periods, the generator puts out a quiescent signal, labelled 32, at a constant voltage level which shall for convenience be considered zero voltage. On receipt of a triggering signal from the interrogating source 8 (not shown in FIG. 5), the generator 7 steps through a sequence of phases, denoted A, B, C . . . P, during which the voltage output increases stepwise with equal increments, as shown by the staircase portion 31 of FIG. 8.

The cathode-ray tube deflection circuits are initially adjusted so that the quiescent beam falls somewhere on a vertical line YY' which is shown in FIG. 6 to be on the body of the mask, parallel to AA', at a distance to the right equal to the separation of AA' from B_0B_0'. When the beam falls upon YY' all of the beam current is intercepted by the mask and electrons flow to ground through the resistor 16, developing a constant negative voltage across the resistor. The constant voltage may be blocked by a capacitor 33 so that the input and output of amplifier 12 are at zero voltage level so long as the beam continues to strike the mask. Any short-lived stoppage of the flow of electrons, as by momentarily deflecting the electron beam to cause it to pass through a hole 35, will then result in a positive voltage input signal to the amplifier 12. The amplifier output for a positive input has the same polarity as the step increments of voltage produced by the staircase generator 7.

On receipt of a synchronizing signal the staircase generator jumps from the quiescent level 32 in FIG. 8, to a succession of linearly increasing voltage levels (A, B, C, D, E, . . . P) which deflect the beam progressively leftward on FIG. 6 to a succession of rest positions, examples of which are denoted by dots on the traces 28, 29, and 30.

Suppose the analog deflection corresponds to the scan line labelled 28: Initially, the beam is at rest on the right-hand dot which marks the intersection of 28 with YY' and the amplified signal appearing at the output 15 and the input to delay unit 11 is zero volt. Unit 11 is a delay line of conventional design which delays the signal by substantially the duration of one step, or phase, of the staircase generator 7. After the interrogation signal is received, the staircase generator enters phase A. Throughout phase A, the delayed signal on plate 26' remains zero volt, but the signal from the step generator on plate 26 has deflected the beam along line 28 to column AA' of the pattern mask, where it resides at the point (marked by a second dot) which happenes not to be inside a perforation. The electron beam current therefore continues to flow from the mask 2 through resistor 16, and the output 15 is "0" for the first bit (denoted A) of the binary number. When the generator 7 enters phase B, the voltage impressed upon the deflection plate doubles, as shown in FIG. 8 and meanwhile the voltage on plate 26', corresponding to output bit A, remains zero. The cathode ray beam therefore moves further along trace 28 to column B_0B_0', which is twice as far from YY' as is AA'. The intersection of 28 with B_0B_0' again marked with a dot, will be seen to take place within a perforation. The electron current through resistor 16 is now greatly reduced, resulting in an a "1" output for bit B. During phase B, the voltage which denotes "1" is also applied to the input of delay unit 11; owing to the time delay of one step interval, a potential of voltage V will appear on the deflection plate 26', during substantially the whole of the next generator phase C.

During the next phase C, the generator 7 has increased

its output by the same increment as in previous steps. However, the voltage on 26', having the same polarity as the staircase signal, reduces the difference of potential between 26 and 26' so that the leftward travel of the beam is insufficient to reach C_0C_0'; it resides at C_1C_1' instead. It will be understood that the voltage actually impressed on plate 26' must be preadjusted in relation to the spacing between B_0B_0' and B_1B_1', just as the actual voltage increment between steps is preadjusted for the spacing between columns with zero subscripts. The beam now strikes the metal body of the mask at C_1C_1', generating a "0" output for bit C. It follows then, that because bit C is a "0," the voltage on 26' during phase D is zero, whereby the beam rests next at the perforated intersection of 28 with DD'. The first four bits generated are therefore 0, 1, 0, 1, in that order, and additional bits can be likewise generated by means of additional columns of perforations. It should be noted that (as with the system of FIG. 2) the beam always rests, as indicated by dots, well in the interior of all pattern elements ,whether perforations or the metallic bridges between perforations, except in column AA'. The horizontal edges of perforations in FIG. 6 are therefore not utilized except in column AA'. This fact permits accurate encoding with a pattern whose edges are imperfectly fabricated. Furthermore, suppose that the scan line 28 is not perfectly horizontal, but is inclined as shown by 28': It will be seen that substantial departures from the ideal scan line can be tolerated, without altering the binary number generated, so long as the A digit is read properly. Such variation of the scan direction may in practice come about because of change of the input signal during scan, because of interaction between analog and scan deflection systems, because of external magnetic or electrical fields, or for other reasons. In a similar way, the beam may be permitted to become gradually defocussed as it moves further and further away from AA', and the full beam current may nevertheless strike either the mask 2 or the collector 14. If the signal varies within allowable (and very liberal) limits during the scan, it is encoded for the value it has at the moment the AA' column is scanned; i.e., it is, in effect, sample during phase A.

To study the effect of scanning with such a value of analog deflection that the beam comes to rest near the edge of a perforation in column AA', we examine scan lines 29 and 30 of FIG. 6. Line 29 traverses column AA' just inside a perforation and 30 traverses just outside the same perforation, but the two lines lie close together and every one of the larger perforations that is traversed by one line is also traversed by the other; therefore, distinction between the two by the coding mechanism can only occur in column AA'. In the case of line 29, the A bit becomes "1." Therefore B_1B_1' is utilized and the B bit becomes "1"; whereupon C_1C_1' is utilized giving a "1" for the C bit, and D_1D_1' is utilized for the D bit, which turns out to be "0." On the other hand, because trace 30 gives a "0" for the A bit, B_0B_0' is next utilized, instead of B_1B_1'. This results in another "0" for the B bit, and, in like manner, "0" and "1" are generated for the C and D bits. Therefore the combination CDBA which is 0111 when read with scan line 29, becomes 1000 when read with scan line 30, all four binary digits changing. As shown on FIG. 6, 0111 is the conventional binary code representation for seven and 1000 signifies eight; therefore this is proper operation. It will be evident that, even when the beam falls on the very edge of a perforation in such a manner that the electron current divides evenly between the mask 2 and the collector 14, it is only necessary to have in the amplifier 12 a bistable element (which makes a definite choice for bit A even if it depends on chance) to insure that either 0111 or 1000, but no improper bit combination, will be generated. Without a bistable amplifier, it is not possible to insure that the least significant digit will always be consistent with the remaining digits. However, the remaining digits will all be correct, provided that either the B_0B_0' perforations or the B_1B_1' perforations are increased in width (as shown by the perforation 34 of FIG. 6) to accommodate partial signals on deflection plate 36'.

I have found that the self-same arrangement of control apparatus shown in FIG. 5 provides binary-coded decimal output, as well as purely binary outputs, so long as the binary-decimal code satisfies certain rules which will presently be stated. Therefore, I ordinarily prefer one of the large number of satisfactory codes which permit use of the simple and otherwise beneficial FIG. 5 arrangement. However, many other codes can be provided when appropriate modifications are made to the system of FIG. 5 (as, for example, by providing a plurality of delay lines). The form of my invention which generates parallel bits output lends itself particularly well to a much greater variety of binary representational schemes for the decimal digits.

A representative example of a preferred code is the well known "4, 2, 2, 1" weighted code which is indicated at the right of FIG. 7; it is noted that the same code in columns A, B, C, and D applies consistently for any value of the units decimal digit. Very briefly, the properties characterizing the preferred codes are as follows: The bit denoted generally as A (which the serial digitizer generates first) always changes between successive decimal digits, as between 6=1010 and 7=1101 in FIG. 7. The next bit, B, may also change (as between 6 and 7) or it may be the same; but, when B does not change, neither C nor D change (as in 8 and 9). It may happen that B changes, but not C (as in the 7–8 transition of the example), in which case D does not change. If more than four binary places are used, similar rules apply to the remaining bits of the decimal digit.

To generate more than one decimal place it is also necessary that binary combinations be assigned in relation to the decimal digits such that all the bits change at the 9–0 transition. Inasmuch as in the common decimal numbering system the tens digit changes only when the units digits progresses from 9 to 0 (or retrogresses from 0 to 9), the hundreds digit changes only when tens and units go between 99 and 00, and like relations hold for higher decimal places, the characteristic rules of bit change then hold true, not only for the binary numbers which represent individual decimal digits, but also for the larger groups of binary digits which represent many-place decimal numbers.

Most serial decimal digitizing requirements can be satisfied by 4-bit codes which adhere to the aforementioned rules, although more than four bits can also be provided. Included in the large class of satisfactory 4-bit codes are the so-called "excess-3" code and numerous weighted codes such as a 4, 4, 2, 1 and a 4, 2, 2, 1 code. Many of these codes are also self-complementing, avoid 0000 and 1111 combinations, and/or have other desirable properties.

I have disclosed in detail the theory and technique for finding all codes with the properties described above, and illustrated several more examples, in the IRE Transactions on Instrumentation, vol. I–7, No. 1 (pp. 33, 34 and 37). Briefly, the techniques for finding these codes, which I there call "V-scannable codes," are similar to those used to find unit-distance decimal codes (see Susskind, p. 3–15 and his references). In fact, one such code is associated with every closed unit-distance decimal code and its code tabulation can be written by converting each binary number of the unit-distance table in the manner used for translating a Gray code (reflected binary) number into conventional binary code.

Reference is now made to FIG. 7, which is similar to FIG. 6 and is similarly labelled but shows a mask designed to provide decimal numbers in a 4, 2, 2, 1 decimal code indicated in the table at the right. FIG. 7 shows a pertinent part of the mask for input values between 20 and 40 units. As in FIG. 6, YY' is the quiescent

locus, AA' is a single column of perforations which generates the earliest serial bit, and the remaining columns are double columns labelled with letters in alphabetical sequence according to the order of generation of bits. Columns with 0 subscripts are active when the previously generated bit is "0," and columns with 1 subscripts are brought into play following "1" generation by bias of the scan rightward exactly as previously described for purely binary numbers. The portion of the mask shown in FIG. 7 contains pattern columns AA', B_1B_1', B_0B_0', C_1C_1' D_1D_1' and D_0D_0', which produce a sequence of four bits to signify the units-place decimal digit, and columns E_1E_1' and E_0E_0' which generate the earliest bit (corresponding to A) of the tens-place decimal digit.

All five bits to be generated by the nine columns of perforations are listed on the right in FIG. 7. The four right-hand bits which specify the units digit are grouped together and the decimal values are shown in parentheses with two decimal digits given.

Suppose now, that the input to analog deflection plates 25 and 25' of FIG. 5 is of strength corresponding to twenty-six units: Then the quiescent beam will reside initially on the intersection of trace 36 with the quiescent locus YY'. Upon receipt of a signal from an interrogating source, the generator 7 puts out voltage step A and the electron beam moves to column AA' on trace 36 where it strikes the mask at the point denoted by a dot and generates a "0." During step B the beam therefore moves to the B_0B_0' column as denoted by the dot on trace 36. The beam traverses a perforation, impinging upon the collector 14 instead of the mask, and a positive signal is developed across resistor 16, and into amplifier 12, whereby a "1" is put out at point 15 and into delay line 11. During phase C, the "1" generated in phase B and delayed by 11, acts to bias the new beam position rightward, so that C_1C_1' is used, resulting in a "0." The D bit is therefore read in the D_0D_0' column and is found to be "1." Subsequently, inasmuch as D is "1," E is read on the E_1E_1' column and is found to be "0." The digits generated therefore agree with the number 0,1010 shown for trace 36. A drawing illustrating additional columns to the right could be made showing, in like manner, the generation of further bits to produce the complete binary coded decimal number 0010,1010 (equivalent to 26), and additional bits pertaining to the hundreds place could likewise be generated.

The reading loci for eight uniformly spaced analog deflections corresponding to integral values 24 through 31 are shown in FIG. 7 by means of dots drawn on the lines of scan, in the manner detailed for scan line 36. It will be evident that the electron beam comes to rest well inside a pattern element, except, possibly, for the earliest bit of the units digit.

The minimum clearance between reading loci and the horizontal edges of perforations tends to increase monotonically as the beam scans progressively from right to left; furthermore, clearances for corresponding bits of the decimal code increase ten-fold for each advance in the decimal place. Consequently, maximum pattern accuracy is required only in the AA' column, and may deteriorate leftward in proportion to the decimal digit weight; scanning deflection may be misaligned; etc., in a manner resembling that described for purely binary coding tubes.

The split-column binary pattern shown in FIG. 6 may be derived from the single-column binary pattern of FIG. 1 by upward and downward displacement of the component columns and is simply related to the binary code tabulation, but no equally simple relation applies to binary-coded decimal masks like FIG. 7. With the aid of FIG. 7, one simple procedure will therefore be described for design of any such masks when the control circuitry and code are given: To the left of the mask, write the binary-coded form of the decimal number at each quantum level, using a preferred code. Construct the AA' pattern (holes at odd levels in FIG. 7) and draw a scan line, like 36, through each pattern element (hole or bridge) of AA'. Now draw the center lines of all the remaining columns, B_0B_0', B_1B_1' . . . P_0P_0', P_1P_1', whose relative placement the control circuits define. Starting with bit B, copy the binary number for each scan line writing each "0" and "1" in either a 0-subscript or a 1-subscript column, according to whether preceding bit was "0" or "1." In FIG. 7, therefore, each of the dots will be replaced by either a "0" or a "1." Now draw perforation boundaries in the blank column spaces, preferably placing them equidistant between continuous flights of 0's and 1's to maximize tolerances. A boundary occurs only when a flight of 0's changes to 1's or vice versa. For example, B_1B_1' in FIG. 7 is "0" at level 27, "1" at level 29 and "0" again at level 31. Therefore, boundaries are placed at levels 28 and 30; C_0C_0' changes from "1" at level 27 to "0" at level 30, so a boundary is placed midway, at level 28.5.

FIG. 5 also illustrates certain optional details of the construction and operation of the cathode-ray coding tube which have been found convenient in practice. In the cathode-ray tube 1 the electron gun 3 forms an electron beam focussed on a mask 2 through a coarse-mesh fine-wire screen 17, which serves to collect secondary electrons emitted from the mask. Between the deflection plates and the screen 17 is placed a short tubular grounded electrostatic shield 18. The end face of the tube 1 is coated internally with a phosphor layer as in oscilloscope tubes, and the phosphor in turn is covered by a thin conductive coating which allows it to serve as the final collector electrode 14. The conductive coat on the phosphor is preferably made negative in potential relative to the mask. The load resistor 16 is preferably connected between mask and ground, but alternatively, a reversed-polarity signal can be obtained by connecting between the collector 14 and its source of potential.

The phosphor is not essential for proper operation, but it has been provided as a convenience, to assist in adjustment of the scanning circuits. It also serves to display directly the various bit combinations generated. The phosphor output display is particularly effective when the staircase generator recycles continually, whereupon the pattern of dots is repeatedly re-excited and the visual display persists. It will be seen that such display is in addition to the serial output on lead 15.

Staircase generators, also known as step generators, are well-known to the art in a variety of forms. The linear staircase generator 7 shown in FIGS. 2 and 5 may be of any suitable type, for example, of the type described on pp. 5–2 through 5–6 of the referenced book of Susskind or the novel staircase generators mentioned in Proc. IRE, January 1959, p. 44, et seq. Especially advantageous staircase generator arrangements for the invention are shown in FIGS. 9 and 10. The basic system of FIG. 9 may be connected to provide either single-scan operation or repetitive scanning, or simultaneous linear and exponential staircase outputs. FIG. 10 shows an arrangement for a recycling type linear staircase generator, which requires fewer component parts when the number of steps is appreciable. Although these varieties of staircase generators have been found useful and convenient, the manner of staircase generation is not critical to the functioning of my invention.

FIG. 9, for simplicity, shows only four steps, but it will be obvious as we go on that the number of steps may be increased indefinitely. A chain of similarly constructed one-shot multivibrators (henceforth termed univibrators) 62–65, of conventional design and equal in number to the number of bits to be generated, are connected in series through differentiating capacitors 69 and fire in sequence. An input signal having specified polarity and sufficient amplitude is required to fire any of the similar univibrators. Such a signal is furnished by the

source 8 to univibrator 62. When vibrator 62 fires, it puts out a rectangular pulse whose duration is determined by the circuit values provided and whose polarity is opposite to that of the firing pulse. The sharp pulse, received by the next univibrator stage 63 through the small differentiating capacitor 69 when stage 62 fires, is therefore of the wrong polarity to fire 63 at that time. However, when 62 returns to its original state, the pulse, resulting from differentiation of the trailing edge of the rectangular pulse put out by 62, is of the required polarity to fire 63. Stage 63 therefore fires almost at the precise moment when 62 becomes inactive again. In a like manner the unit 63 fires 64 and so on, so that the chain of univibrators delivers rectangular output pulses, each stage in its turn.

The rectangular pulse from each univibrator stage also goes to an individual cathode follower 66. The cathode followers therefore also deliver rectangular pulses, each in its turn and one at a time. It is preferred that all of the univibrator and cathode follower stages be matched or adjusted to provide rectangular pulses substantially equal in duration voltage level and amplitude, and uniformly spaced in time. Cathode followers associated with the univibrator stages 62–65 deliver their respective outputs to resistors 72–75 which are joined at their further ends to each other and to the input of an amplifier 60 as shown. The output impedance of each cathode follower is always small compared to any of the resistors 72–75 and may therefore be neglected. The instantaneous action of the univibrators and cathode followers is therefore to impress a voltage upon the input of each resistor in turn, in the manner of a group of relays each of which switches one resistor terminal between the two terminals of a low-impedance battery. It is known that, in such a circuit, the fraction of the battery potential which appears at the common junction of the various resistors is inversely proportional to the resistance of the energized resistor 66. (This has been shown in the specification of Patent No. 2,685,084 issued to Lippel and Buegler). The resistors 72–75 are therefore chosen to have respective resistances proportional to R, ½R, ⅓R, and ¼R, as shown in FIG. 9, whereupon voltage steps of one, two, three and four units, then back to zero are produced in succession at the input to amplifier 60. The amplifier is of conventional design and, if used with electrostatic deflection means it preferably has high impedance push-pull outputs; for electromagnetic deflection, it provides current flow in the deflection coils proportional to the input voltage.

Although only four stages are shown in FIG. 9, it will ordinarily be necessary to provide additional stages of univibrators and cathode followers, and a like number of additional resistors to provide as many steps of voltage as there are bits to be generated. In general, the calibrated resistor for a Kth stage should have a resistance of R/K in the arrangement of FIG. 9.

It will be evident that if a similar network, comprised of a second set of resistors, in which the resistance varies as $R/2^K$, is meanwhile connected to the various cathode follower stages so that its input is in parallel with the network of resistors shown in FIG. 10, the output at the second junction point provided by the second set of resistors will be an exponentially rising staircase voltage, synchronized with the linear staircase provided at the input to amplifier 60 and doubling from step to step. Likewise, by adjusting the individual resistors to have a sequence of resistances reciprocal in value to other sequences of step amplitudes, other step functions can be provided.

Means are well known which permit one to connect the differentiated output from the last univibrator stage back to the first stage input 68, so that the chain of univibrators is converted into a ring multivibrator, having continuous recirculation of one pulse and giving continuous repetition of the staircase output. A preferable method is to employ a pulse generator with constant repetition rate as the triggering source 8.

It will also be clear to those skilled in the art how delay lines can be substituted for the chain of univibrators 62–65 in FIG. 9, and how special beam switching vacuum tubes, used in counters and electronic commutators, can likewise be employed.

It will be observed that when the staircase is automatically and continually regenerated there is no need for the quiescent beam position YY′ shown in FIGS. 6 and 7. The voltage corresponding to the quiescent output or zero level of a single scan generator can therefore serve as one of the reading steps in repetitive scan, permitting the omission of one cathode follower and one resistor. However, it is necessary to insure that when the final bit of the generated number is a "1," there will be no rightward deflection when the A bit is generated during the next scan. Although there are other ways of preventing such malfunction (e.g., by limiting the scan deflection amplifier output to prevent deflection right ward of AA′ or by providing two zero level steps in sequence), a convenient arrangement is to scan from YY′ to the extreme left, using $n+1$ steps to generate n bits. The YY′ reading is therefore offset after a "1," but the electron beam nevertheless strikes the body by the mask so that the subsequent A-bit is nevertheless generated properly. (The extra scan position can as well be located at the extreme left margin of the mask, instead of at YY′.)

FIG. 10 illustrates another generator circuit for a recycling staircase output as grasped in FIG. 12. The number of step levels provided by the circuit in its simplest form is an integral power of two, for example eight or sixteen, but means whereby recycling after any other desired numbers of steps may be obtained will be apparent to all those familiar with electronic counters and digital-to-analog converters.

FIG. 12 shows eight stepped levels of output voltage, 85, running from zero to seven potential units during successive cyclic time phases labelled Y, A, B, C, D, E, F, and G. The system of FIG. 10 which provides the output shown in FIG. 12 therefore suffices for a cathode ray digitizer encoding with eight or fewer bits, and is particularly convenient for seven or fewer.

The oscillator 81 of FIG. 10 provides uniformly spaced pulses to a 3-stage binary counter 89 having counting stages 82, 83 and 84. A simple 3-stage binary counter counts modulo eight; therefore the count output furnished in parallel to cathode followers 90, 91 and 92 increases by units from zero (binary 000) through seven (binary 111), then reverts to zero and repeats indefinitely.

A graph of the numerical count as a function of the total number of input pulses will be seen to be shaped precisely like the staircase curve 85 of FIG. 12. To obtain a signal output from the amplifier 60 which is precisely the staircase signal 85, we therefore interpose a digital-to-voltage converter between the counter 89 and the amplifier 60. Such a converter is provided by means of the resistors 78, 79 and 80, each connected at one end to the amplifier input and at the other end to the cathode followers 90, 91, and 92 respectively, as shown in FIG. 10. Since 90 receives the least significant bit and 92 the most significant bit, the resistors 78, 79 and 80 have resistance values in the ratios of 4 to 2 to 1, in accordance with the teachings of the aforementioned specification of U.S. Patent No. 2,685,084, issued to Lippel and Buegler.

Further understanding of the action of this staircase generator is gained by noting that counter stage 82 delivers to the cathode follower 90 a square-wave signal which the resistor 78 converts to the unit-amplitude voltage wave 86 of FIG. 12. Stage 83 meanwhile provides a square-wave signal with exactly half the repetition frequency of 86; resistor 79, having only one-half the resistance of 78, converts this signal to the voltage wave 87 with twice the amplitude of 86. Likewise the square-wave signal 88 is produced by counter stage 84, cathode

follower **92**, and resistor **80** which has one-fourth the resistance of **78**; and this square-wave signal has one-fourth the repetition frequency but four times the amplitude of the wave **86**.

Each of the resistors **78**, **79** and **80** act in the same manner as the resistors **72–75** of FIG. 9 to produce the illustrated square-wave signals at the input of amplifier **60**. Moreover, in accordance with the well-known superposition theorem of electrical engineering the instantaneous voltage effects are additive. Therefore the three waves combine linearly to provide the staircase signal **85**, whose amplitude will at any instant be seen to be the sum of the amplitudes of **86**, **87** and **88**.

From the foregoing explanation, it will be obvious that it is not essential for the resistor network **78**, **79** and **80** to receive input signals which are actually generated by an oscillator **81** and counter **89**, but that any circuit arrangement whatsoever which provides three additive square-wave signals having the frequency, amplitude and phase relationships shown for **86**, **87** and **88** of FIG. 12 will result in the staircase output **85**.

For clarity, FIG. 5 shows the signal from the staircase generator **7** applied to a single deflection plate **26** while the delayed output pulse is applied to the opposite plate **26'** so that the signals subtract algebraically. In order that a delayed "1" shall cause the beam to move a lesser amount than it would in the case of a delayed "0," the polarity of the "1" signal relative to a "0" signal must be the same as the unit step increments to the staircase. It will, of course, be obvious that the patterns of FIGS. 6 and 7 can also be modified so that reversed polarity may be used for the signals on plate **26'**.

In practice, it may not be desirable or convenient to connect to individual deflection plates to accomplish the subtractive operation schematized in FIG. 5.

A preferred arrangement for producing an additive component of deflection, as required to select between the 0-subscript columns and the 1-subscript columns of FIGS. 6 and 7, is shown in FIG. 9 and also in FIG. 10. The amplified output **15** of FIG. 5 is transmitted through the delay line **11** of conventional design, to the cathode follower **76**. A calibrated resistor **77** (which may be variable as shown to aid calibration) is connected to the cathode follower **77** and to the junction of resistors at the input to amplifier **60**. The cathode follower **77** and resistor **76** function exactly like the cathode followers **90–92** and resistors **78–80** of FIG. 10, to increase or decrease the voltage at the input to amplifier **60** according to the nature of the delayed output bit signal received by the cathode follower **77**. The polarity of stepped deflection increments must be so related to the polarity of a "1" signal from the delay line relative to a "0" signal that the shift due to receipt of a "1" is rightward in the case of FIGS. 6 and 7; likewise the value of resistor **76** should be adjusted so that the deflection difference due to a delayed "1," rather than a delayed zero, is substantially the distance between B_1B_1' and B_0B_0', C_1C_1' and C_0C_0', and the remaining component pairs.

It is frequently necessary to provide parallel bit signals for numerical display, or to actuate electromechanical devices such as typewriters or punches. Although such output is inherently provided by the parallel version of my invention to be described below, parallel signals can also be obtained, employing the serial coders previously described, and synchronous decommutation of the serial output, preferably with high-frequency scanning. For such operation, the staircase generator of FIG. 9 using a constant-frequency pulse generator for the trigger source **8** is convenient inasmuch as the cathode followers **66** then receive signals one at a time, which permits decommutation with the aid of simple "and" gates. For equivalent operation with a staircase generator of the FIG. 10 type, a switching matrix or switching tree is required.

The need for external decommutation is entirely removed if the serial cathode ray coding tube **1** is constructed as in FIG. 13. FIG. 13 shows the end face of a coding tube substantially like that of FIG. 5 in all respects except that the final collector **14**, which in FIG. 5 covers the whole face of the tube and receives electrons traversing all parts of the mask **2**, is replaced by a multiplicity of strip collectors. Each strip **94** is insulated from every other strip and is connected to an output lead **37** which emerges separately through the tube envelope. One such strip receives the electrons which traverse any perforations in the AA' column, but not electrons from any other column. A second such strip receives electrons which traverse holes in either B_0B_0' or B_1B_1', but no other column. A third backs up C_0C_0', and so on, with a strip, as exemplified by **94**, and an output lead, exemplified by **37**, for every bit of the encoded number. The number may be purely binary, binary-coded decimal, or in any other binary-coded radix, and there will be as many output leads as there are bits generated.

When a repetitive-scan staircase generator repeatedly scans the mask **2**, preferably with a rapid rate of repetition, it will be evident that bits are automatically distributed to different output leads, according to their positions in the binary-coded number. Whenever the output to a lead, e.g., **37** is a "1," the signal thereon will consist of pulses of negative current, a pulse for each staircase scan; such a signal has a low frequency or "D.C." component, which can be made evident by a small glow tube **93**, and which moreover, can be amplified and delivered to electromechanical equipment and the like. When the output is a "0," the pulses and low frequency are absent. Serial code output may simultaneously be obtained from the amplifier as in FIG. 5, and it operates the column selection circuits.

A symmetrically constructed mask (e.g. that of FIG. 11) for conventional binary code or any other V-scannable code can also be used for serial reading, with some benefit in increased coding tube constructional tolerances over the generally preferred unsymmetrical masks exemplified in FIGS. 5, 6 and 7. For this purpose the polarity of each step of the staircase must be selected according to the delayed bit signal, rather than the voltage amplitude. This may be done with a scanning circuit similar to FIG. 2, but with the exponential generator **9** and the coil **5'** omitted and the electronic reversing switch **10** operating on the signal from generator **7** to deflection means **6**.

This invention applies to the parallel type of cathode ray coder as well as to the serial type. For the parallel type of coder, the gun **3** of FIG. 2 and FIG. 5 is modified so as to form a long line focus of electrons, instead of a pencil, which extends across all columns of perforations, substantially perpendicular to the columns and to the direction of analog deflection. The construction and operation of the beam forming and focussing arrangement may be similar to that disclosed for a prior art parallel coding tube by Goodall in U.S. Patent No. 2,616,060. However, this invention will operate satisfactorily with less perfect beam forming than must be provided for prior art devices. A pattern mast, **37** of FIG. 11, is placed inside the tube envelope in the manner shown by Goodall, so that the electrons come to a focus along a line extending across the entire pattern of perforations; for example, the focus of the beam may be the line **38** shown in FIG. 11. No scanning deflection means is required. The focussing controls operative on tubes of this invention should be adjusted to give best focus for the central part of the line of electrons, namely, the part which crosses the central column of perforations, regardless of whether the adjustment provides sharpest focus for the entire line of impingement.

FIG. 11 represents a perforated mask **37**, behind which is placed collector means comprising a plurality of conductive strips **40**, riveted or otherwise fastened to strips **41** and **42** of insulating material which function to separate

and support the strips **40** parallel to each other, with each one directly behind one column of mask perforations.

The mask **37** is made of material, preferably metal, opaque to transmission of electrons and is provided with parallel columns of perforations, or transparencies through the mask arranged in a suitable pattern for effecting a prescribed coded output. In FIG. 11, the pattern is such that it will effect conventional binary code output.

The pattern **37** has one column, marked A, which is similar to AA′ of FIG. 6 but which is centered on the mask as shown. Likewise FIG. 11 has two columns of perforations, B_0 and B_1, which correspond to B_0B_0' and B_1B_1' of FIG. 6, respectively; but B_0 is placed to the left of A, and B_1 on the right. Likewise C_0 (which corresponds to C_0C_0' of FIG. 6) is beyond B_0 on the left, and C_1 is beyond B_1 on the right; and so on for the remaining columns, as shown in FIG. 11. Any arrangement or permutation of the columns is workable, but the symmetrical arrangement illustrated is believed most suitable.

As further illustrated in FIG. 11, the collector strips **40** are connected to separate output leads **43** which go to logical gating circuits. Column A has a lead connecting it directly to output terminal **44**, to one input of the "and" gate **45**, and also to the "inhibit" terminal "and not" gate **46**. The other input terminal of the "and" gate **45** is connected to the collector strip B_1 and the other terminal of the "and not" gate is connected to the collector strip B_0. The outputs of gate **45** and gate **46** are the inputs of the "or" gate **47**. The output of the "or" gate **47** is connected to the output terminal **48**, to one input of the "and" gate **49** and to the "inhibit" input of "and not" gate **50**. The other inputs of the "and" gate **49** and "and not" gate **50** are respectively connected to the collector strips C_1 and C_0. The outputs of gate **49** and gate **50** are connected to the input of the "or" gate **51**. The output of the "or" gate **51** is likewise connected to the terminal **52**, to an input of the "and" gate **53**, and to the inhibit input of "and not" gate **54**. The other inputs of the gates **53** and **54** are respectively connected to the collector strips D_1 and D_0. The outputs of gate **53** and gate **54** are connected to the "or" gate **55** which is connected at its output to the terminal **56**.

FIG. 11 shows the perforation pattern for only the four least significant bits of a conventional binary number. Ordinarily additional columns of perforations, on either side of those of the drawing and additional pattern elements at the top and/or bottom will be provided to generate more than four bits, and the manner of construction of the pattern and interconnection of the outputs will be obvious by extension of the drawing and the description.

When the input signal to the digitizer is such that the sheet of electrons impinges upon the mask **37** of FIG. 11 along the straight line marked **38**, signals are obtained from the strips **40**; a strip is charged negatively to indicate a "1."

The "and", "and not" and "or" gates are conventional logical gates, which should be designed to operate with negative "1" signals for direct connection as shown. The "and" gate produces an output "1" only when two 1's are put into it; otherwise it delivers "0." The "and not" gate or inhibitor puts out a "1" only when the "inhibit" input is "0" and the other input is "1." The "inhibit" input is identified with a small circle, according to convention. The "or" gate puts out a "1" so long as both inputs are not "0."

As seen in FIG. 11, the line of impingement **38** extends transversely of the mask intersecting all columns, and where it intersects an aperture it impinges on a collector strip beyond the mask. As illustrated, the line intersects column A in the region of a perforation or transparency. Therefore a "1" signal will appear at the output terminal **44**, at an input of "and" gate **45** and at the inhibit input to **46**. The "1" input to the "and" gate **45** activates it and that to the "and not" gate inhibits it so that only the "and" gate **45** can be conductive. The "and" gate **45** is connected to the strip B_1 which is also shown impinged upon by the electron beam. The "1" voltage thus impress on collector B_1 is transmitted through "and" gate **45** and the "or" gate **47** to the output terminal **48**. The output voltage from "or" gate **47** is also applied to "and" gate **49** and "and not" gate **50** so as to activate the "and" gate **49** and to inhibit the "and not" gate **50**. The "and" gate **49** transmits the voltage condition of the collector strip C_1 throught he "or" gate **51** to the terminal **52**. As illustrated, the electron beam pierces the transparency in column C_1, so a "1" also appears at terminal **52**. The output from the "or" gate **51** is also applied to the "and" gate "and not" gates **53** and **54** so as to activate the "and" gate **53** to inhibit the "and not" gate **54**. The bit signal on the collector strip D_1, and not the signal on D_0, will be transmitted through the "or" gate **55** to the terminal **56**. In the example illustrated the line of impingement of the electron beam on the column D_1 is in an opaque area and therefore there will be a "0" signal strip D_1 and the terminal **56** will register 0111, which is the representation of the numerical value "seven" in conventional binary code.

Although the line of impingement of the electron beam is shown straight and sharp in the figure, it will be seen that the allowances for deviation of the line of impingement from the illustrated straight line increase in each direction away from the column A, for reasons similar to those which pertain to deviations in the serial coder. This also allows for greater tolerances in the location and dimensioning of the apertures.

Variations in the construction of the mask **37** which do not depart from the spirit of my invention will readily suggest themselves to persons skilled in the art. Thus the collector **40** can be constructed in one piece, and the mask **37** sectionalized instead; or both mask and collector may be divided so that electrons impinging on one represent 0's while electrons coming to the other represent 1's.

The action of the network of gates, shown in FIG. 11 to be connected to the group of collector strips **40**, can be expressed as follows, using Boolean algebra notation for switching functions as used in the computer art (as explained in Richards, "Arithmetic Operations in Digital Computers," Van Nostrand, 1955, chapter 2):

$$\begin{aligned} A&=A \\ B&=B_0\overline{A}+B_1A \\ C&=C_0\overline{B}+C_1B \\ &\cdots \\ K&=K_0\overline{J}+K_1J \\ &\cdots \end{aligned} \qquad \text{(Equations 3)}$$

It will be evident to all persons skilled in the art that the particular arrangement of logical gates or switches diagrammed in FIG. 11 may be replaced by any circuit, network, device, computer or data processor which selects output signals in accordance with Equation 3 (or any mathematic equivalent thereof) without departing from the spirit of my invention.

It will now be evident to those skilled in the art that the purely binary code mask **37** of FIG. 11 may be replaced with masks designed for any of certain other codes, in particular, one of the "preferred decimal codes," without change in the external selection. Thus the mask pattern of FIG. 7 may be incorporated in the parallel coder of my invention, although I ordinarily prefer to rearrange the order of the columns, in the symmetrical fashion illustrated by FIG. 11, placing AA′ in the center.

When the serial version of my invention is used, various decimal codes, other than those termed "preferred codes," can be provided, but relatively major (and generally inconvenient) changes must be made in the opera-

tion of the system shown in FIG. 5, according to the particular special code desired. On the other hand, although the output selection means illustrated in FIG. 11 and characterized generally by Equations 3 likewise operates properly only for preferred codes, the modifications which must be made to provide numerous other decimal (or other non-binary-radix) codes are relatively simple and convenient.

An example of the parallel generation of decimal outputs coded in a non-"preferred" code is shown in FIG. 14. The mask **100** of the figure is designed for a much-used code, known as the "8, 4, 2, 1 code" which is indicated at the right of the figure. This is the code commonly designated binary-coded decimal as previously mentioned. To be able to discuss more than one decimal place of a number, we indicate the tens-place decimal digit and its bit components by $N'=D'C'B'A'$ and the units digit and its bits by $N=DCBA$.

The 8, 4, 2, 1 code is not "preferred" inasmuch as only A and D, and not B and C, change state at the 9–0 transition. The processing described by Equations 3 does not therefore suffice for the outputs of the collector strips **40** shown in FIG. 14; in its place, however, the following scheme of logical selection may be used:

$$\begin{aligned} A &= A \\ B &= B_0\overline{A}+B_1A \\ C &= C_0\overline{B}+C_1B \\ D &= D_0\overline{A}+D_1A \\ A' &= A'_0\overline{D}+A'_1D \\ B' &= B'_0\overline{A'}+B_1A \\ C' &= C_0'\overline{B'}+C'_1B, \text{ etc.} \end{aligned} \qquad (4)$$

It is seen that Equations 4, like Equations 3 provide that every output bit is selected by means of an iterative process to depend ultimately on the value of A. A change of state in A can, if necessary, change every bit of the output without changes in the signals on other collector strips. Any such iterative selection process I call "logical detenting." Equations 3 describe a simple kind of logical detenting in which the same selection rule, or Boolean equation, applies between every pair of successive bits, while (4) indicates different rules for different bit places.

The code pattern fragment shown in FIG. 14 encompasses vertically approximately fifteen quanta (i.e., successive numbers), running from 07 to 22, and the width of the fragment is such as to show the columns and collector strips, labelled A, B_0, B_1, C_0, C_1, D_0 and D_1, which generate the units decimal digit, and also A'_0 and A'_1 which provide the first bit of the tens-place number. As in FIG. 7, all four bits of the units place and the first bit (A') of the tens place are tabulated on the right hand side of the figure, and the decimal equivalent is written in parentheses, for sensibly different analog deflections.

The interconnected gates shown on the lower half of FIG. 14 perform a function analogous to that of the network of gates in FIG. 11. Specifically, they select n output bits from the $2n-1$ collector strips in accordance with Equations 4, and it will, of course, be understood that any equivalent selection means may be substituted.

Four identical switching groups, each consisting of an "and gate," an "and not (inhibitor) gate," and an "or gate" are labelled **104–107** in FIG. 14. These are also identical with like switching groups within the network of gates shown in FIG. 11, and operate in the same manner. Thus, the inhibitor gate **110** of network **104** corresponds in every respect with **46** of FIG. 11, "and" gate **109** corresponds to **45**, and "or" gate **111** is equivalent to **47**. The leads to gates **109** and **110** are furthermore connected to collector strips labelled A, B and B_0 in exactly the same way as the leads to **45** and **46** are connected to correspondingly labelled strips. Consequently, the combination **104** of FIG. 14, like the identical combination of gates shown in FIG. 12, acts as a transfer switch to transmit B_0 to the output B when A is 0, and to transmit B_1 when A is 1. In exactly the same manner, transfer switch **105** selects between D_0 or D_1 according to whether A is 0 or 1, transfer switch **106** selects A'_0 or A'_1 according to whether output D is 0 or 1, and transfer switch **107** selects either C_0 or C_1 according to the state of output B. The output A' goes to further iterations of the gating network which are indicated generally as **108** and which selects additional output bits, including B', C', D' and higher-order decimal digit representations, from collector strips not shown in the drawing.

We now fix our attention upon the trace line **101** which is the focus of a sheet beam of electrons deflected by an input signal with sixteen units strength. Electrons impinge on the trace line, and wherever said trace traverses a perforation (as in column A'_0) electrons strike a collector strip placed behind the mask, inducing a voltage signal which signifies a "1"; where the mask **100** shields the collector (as in column D_0) the absence of a voltage signal signifies a "0." It will be seen that the focussed beam alighting on trace **101** induces the following signals on the group of collector strip **40**:

$$A=0,\ B_0=1,\ B_1=?,\ C_0=1,\ C_1=1,\ D_0=0,\ D_1=0,\ A'_0=1,\ A'_1=1$$

(The trace falls on the boundary of a perforation in the B_1 column, producing an indefinite, or unreliable signal shown as "?.")

Because $A=0$, the transfer switch network **104** selects $B=B_0=1$; the indefinite B_1 output is not utilized. With B selected to be 1 switch network **107** selects $C=C_1=1$. At the same time, the $A=0$ signal also results in selection of D_0 by transfer switch **105**. Therefore $D=D_0=0$. The $D=0$ input to switch **106** results in $A=A'_0=1$ and also the consequent further choice of B'_1 and D'_1 which is not shown in FIG. 14.

It is seen therefore that when the focus falls on line **101** the output A', DCBA is 1,0110 which is correct for an analog deflection of 16 units.

Likewise, when the beam falls on trace **102**, the collector strip signals are:

$$A=1,\ B_0=?,\ B_1=1,\ C_0=0,\ C_1=1,\ D_0=?,\ D_1=0,\ A'_0=1,\ A=1$$

Therefore $A=1$ and $B=B_1=1$, $C=C_1=1$
$D=D_1=0$, $A'=A'_0=1$

It is therefore seen that trace **102** results in

$$A'DCBA=1,0111$$

which is correct for 17 units of deflection.

In the same way trace **103** will be seen to result in the output 1,1000, the five least significant bits of the number 18 coded in 8, 4, 2, 1 decimal code; and trace **112** yields 0,0010, or 22.

Other binary codes for decimal and other high-radix numbers may be generated with my inventions especially in the parallel output version, using still different logical detenting processes. Two additional examples of 4-bit decimal codes and the processing equations for each will now be given, to illustrate more fully the scope and versatility of the invention:

$P=DCBA$	$Q=DCBA$
0=0000	0=0110
1=0001	1=0111
2=0010	2=0100
3=0011	3=0101
4=0110	4=0000
5=0111	5=1001
6=1100	6=1000
7=1101	7=1011
8=1000	8=1010
9=1001	9=1111

The following logical detenting scheme may be used for either code P or code Q:

$$A=A$$
$$B=B_0\overline{A}+B_1A$$
$$C=C_0\overline{A}+C_1A$$
$$D=D_0\overline{A}+D_1A$$
$$A'=A'_0\overline{D}_0+A'_1D$$
$$B'=B'_0\overline{A}'+B'_1A'$$
$$C'=C'_0\overline{A}'+C'_1A', \text{ etc.}$$

Code Q is peculiar in that all transitions in B, C, or D columns are accompanied by identical (i.e. 0–1 or 1–0) transitions in A. This alternatively permits a simplified scheme as follows, for Q only:

$$A=A$$
$$B=B_0+B_1A$$
$$C=C_0+C_1A$$
$$D=D_0+D_1A$$
$$A'=A_0\overline{D}+A_1D$$
$$B'=B'_0+B'_1A', \text{ etc.}$$

It is seen, therefore, that for other than purely binary numbering, the individual bits may be processed in a single chain or sequence; or alternatively branch processing, whereby one bit may control the selection of two or more subsequent bits, may be used. However, it is preferred that all of the bits which represent a single decimal digit (or a digit of some other base) shall be directly or indirectly controlled by no more than one component bit of the decimal digit of next lower significance, and thus, ultimately by a corresponding component bit of the units place.

Owing to the iterative selection, it becomes possible to construct the coding masks with variable accuracy inversely proportional to the weight of the decimal, binary, or other digit generated, so that only a small central part of the mask pattern (related to the units digit) must be fully accurate, and the electron-optical and deflection systems needed to be fully accurate only in a correspondingly small part of the deflection field. The binary coding scheme for digits of a higher radix and the physical layout of the mask pattern may be chosen such that the constructional and operational tolerances, even for the successive bits of one digit place, are significantly increased over the tolerance requirements of prior art.

It will be obvious to those skilled in the art, how coding tubes of my invention can be constructed to change from one binary coding system for the decimal digits to another, for different digit positions of a number, or how mixed radixes may be provided.

Certain obvious extensions of my invention can be made to eliminate single bit control in the units place. For example, a unit-distance binary code for the decimal numbers may be employed, in which case all bits of the units decimal place may be generated without selection, but any bit of the higher decimal places will be logically selected in accordance with one units-place bit. This is shown for analogous interconnection of counter decades in Susskind, pp. 6–68, 69.

In the counting sequence for natural numbers all less-significant digits change whenever a digit changes. Consequently changes in the bit components of a binary-coded *n*-ary number are always accompanied by at least one bit change in the next less significant digit, even when no other bits of the same digit change.

Persons skilled in the art will therefore have no difficulty in establishing logical selection schemes suitable for any binary-coded natural numbering system and sophisticated selection schemes can be found by noting that the bits involved in any component selection chain of a branching system (e.g., A, D, A', D', A'', B'', and C'' when Equations 4 apply) cooperate exactly like the bits of "preferred" code (viz., C'' is accompanied by changes in A, D, A', D', A'', and B'').

A split column code pattern can be designed, after the code tabulation and the selection logic have been determined, by distributing the written code tabulation in dual columns. One writes the master controlling bit (A in all my examples) normally, in a single column, but writes each subsequent 0 or 1 in whichever one of the two alternative columns is required by the selection scheme. Thus, when K controls L and K is 0, L is written 0 or 1 in the L_0 column; but if K is 1, L is written in the L_1 column. It will be evident that wherever K is 0 the L_1 column is empty and wherever K is 1, the L_0 column is empty. A pattern boundary is placed within the L_1 empty space whenever the L_1 bits above and below it are different and likewise with L_0; if the contiguous digits are alike, the boundary is omitted. Boundaries obviously cannot occur at the same level in both L_1 and L_2 columns. Although the order of pattern columns may be changed about somewhat, the arrangement exemplified by FIG. 7, is preferred for serial coding with a preferred code; and for parallel coding, it is preferred that the columns be arranged with a view to maximizing the allowable configuration errors.

What is claimed is:

1. In a digitizer for bit-coding plural digits, having a reading element and a geometrical code pattern made up of elemental areas defined by analog and coding coordinates and providing either 0 or 1 readings for each code bit, including controlled bits each read at one of two coding coordinates designed as the "0" or "1" coding coordinates selected in accordance with the 0 or 1 reading of a controlling bit, variation of the analog coordinate near certain transitions of the controlling bit corresponding to opposite readings of the controlled bit at its two coding coordinates, whereby transitions in the actual controlled bit readings are always obtained by change between "0" and "1" coding coordinates in synchronism with change in the controlling bit: a pattern suitable for digits of a radix having an odd factor, wherein said certain transitions of the controlling bit involve a change from 0 to 1 at one analog coordinate level and from 1 to 0 at another analog coordinate level with unidirectional variation of the analog coordinate.

2. In a digitizer for bit-coding plural digits, having a reading element and a geometrical code pattern made up of elemental areas defined by analog and coding coordinates and providing either 0 or 1 readings for each code bit, including controlled bits each read at one of two coding coordinates designated as the "0" or "1" coding coordinates selected in accordance with the 0 or 1 reading of a controlling bit, variation of the analog coordinate near certain transitions of the controlling bit corresponding to opposite readings of the controlled bit at its two coding coordinates, whereby transitions in the actual controlled bit readings are always obtained by change between "0" and "1" coding coordinates in synchronism with change in the controlling bit: a pattern suitable for digits of a radix having an odd factor, wherein the patterns at two coding coordinates of a controlled bit are geometrically dissimilar.

3. In a digitizer for bit-coding plural digits, having a reading element and a geometrical code pattern made up of elemental areas defined by analog and coding coordinates and providing either 0 or 1 readings for each code bit, including controlled bits each read at one of two coding coordinates designated as the "0" or "1" coding coordinates selected in accordance with the 0 or 1 reading of a controlling bit, variation of the analog coordinate near certain transitions of the controlling bit corresponding to opposite readings of the controlled bit at its two coding coordinates, whereby transitions in the actual controlled bit readings are always obtained by change between "0" and "1" coding coordinates in synchronism with change in the controlling bit: a pattern suitable for digits of a radix having an odd factor, wherein the patterns at two coding coordinates of a con-

trolled bit are geometrically dissimilar and each controlled bit is also the controlling bit for only one further controlled bit.

4. In a digitizer for bit-coding plural digits, having a reading element and a geometrical code pattern made up of elemental areas defined by analog and coding coordinates and providing either 0 or 1 readings for each code bit, including controlled bits each read at one of two coding coordinates designated as the "0" or "1" coding coordinates selected in accordance with the 0 or 1 reading of a controlling bit, variation of the analog coordinate near certain transitions of the controlling bit corresponding to opposite readings of the controlled bit at its two coding coordinates, whereby transitions in the actual controlled bit readings are always obtained by change between "0" and "1" coding coordinates in synchronism with change in the controlling bit and for any such certain transition the closest of avoided pattern transitions along the analog coordinate for a controlled bit at one coding coordinates corresponds to an increase of the analog coordinate and at the other coding coordinate to a decrease: a pattern, suitable for digits of a radix having an odd factor, wherein for one said certain transition said closest pattern transititon for a controlled bit at said one coding coordinate corresponds to an increase and for said other coding coordinate to a decrease, whereas for another such certain transition said closest pattern transition for said same one coding coordinate corresponds to a decrease and for said same other coding coordinate to an increase.

5. An analog to digital converter providing number outputs coded in terms of two-valued signal bits, comprising a code pattern and a reading element, said code pattern having areas for providing in conjunction with said reading element different sequencies of successive bits for a plurality of digits at each of a plurality of analog input values, each bit except a first being derived alternatively from either one of a corresponding pair of columns of the pattern, the output bits including said first bit, a second bit derived from that one of its corresponding pair of columns selected by said first bit, and further successive bits each derived from that one of its corresponding said pair of columns selected by a previous said bit, wherein the radix of said number outputs involves an odd factor and successive changes in the value of a particular said output bit correspond sometimes to an odd and sometimes to an even number of changes in the value of an output bit previous to said particular bit and so selecting that one of the pair of columns corresponding to said particular bit.

6. An analog to digital converter providing number outputs coded in terms of two-valued signal bits, comprising a code pattern and a reading element, said code pattern having areas for providing in conjunction with said reading element different sequencies of successive bits for a plurality of digits at each of a plurality of analog input values, each bit except a first being derived alternatively from either one of a corresponding pair of columns of the pattern, said first bit being an output bit and also selecting the proper one of the pair of columns from which a second output bit is derived to avoid ambiguity at transitions in digital values with change in analog values, one of said output bits also selecting the proper one of the pair of columns from which a further similar output bit is similarly derived, wherein the radix of said number outputs involves an odd factor and successive changes in the value of a particular said output bit correspond sometimes to an odd and sometimes to an even number of changes in the value of an output bit previous to said particular bit and so selecting that one of the pair of columns corresponding to said particular bit.

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