



US 20090072375A1

(19) **United States**

(12) **Patent Application Publication**
Song et al.

(10) **Pub. No.: US 2009/0072375 A1**

(43) **Pub. Date: Mar. 19, 2009**

(54) **INTEGRATED CIRCUIT PACKAGE SYSTEM WITH MULTI-CHIP MODULE**

Publication Classification

(51) **Int. Cl.**
H01L 23/02 (2006.01)
(52) **U.S. Cl.** **257/686**

(76) Inventors: **Sungmin Song**, Incheon (KR);
SeungYun Ahn, Ichon-si (KR);
JoHyun Bae, Seoul (KR);
Jong-Woo Ha, Seoul (KR)

(57) **ABSTRACT**

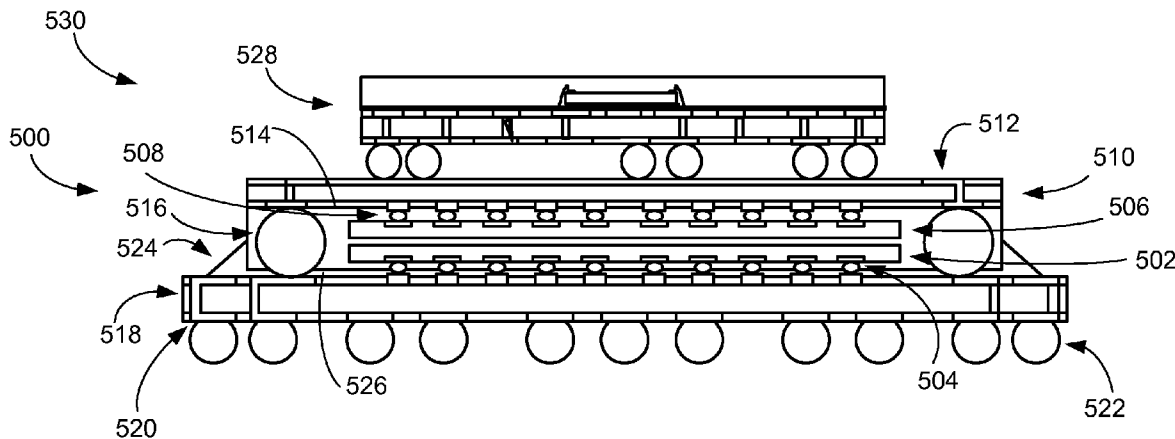
An integrated circuit package system with multi-chip module is provided including: providing an upper substrate having an upper chip thereon; positioning a lower chip under the upper chip, the lower chip having bottom interconnects thereon; encapsulating the upper chip and the lower chip with a chip encapsulant on the upper substrate with the bottom interconnects exposed; mounting the lower chip over a lower substrate with a gap between the chip encapsulant and the lower substrate; and filling the gap with a package encapsulant or chip attach adhesive.

Correspondence Address:

LAW OFFICES OF MIKIO ISHIMARU
333 W. EL CAMINO REAL, SUITE 330
SUNNYVALE, CA 94087 (US)

(21) Appl. No.: **11/857,188**

(22) Filed: **Sep. 18, 2007**



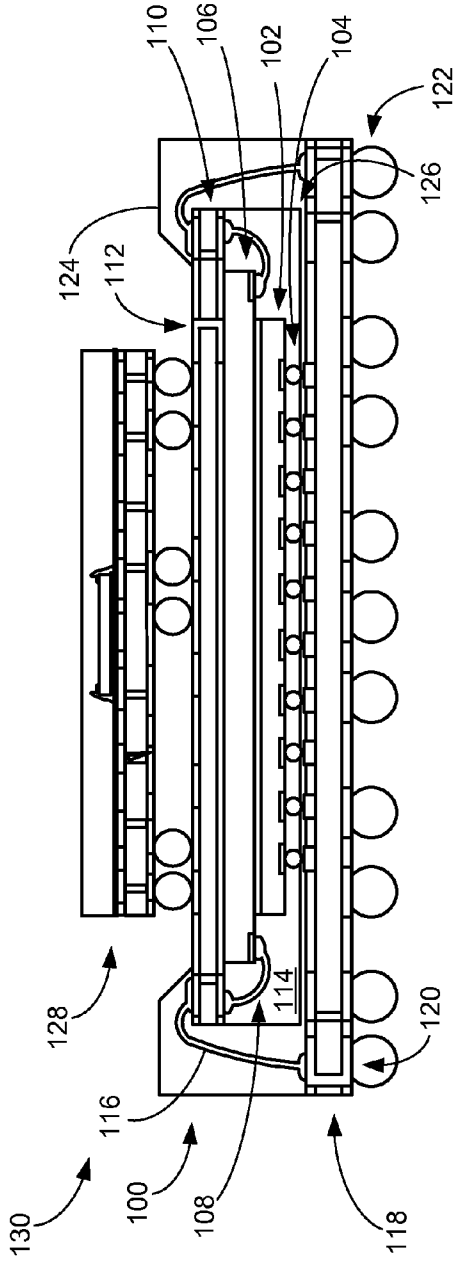


FIG. 1

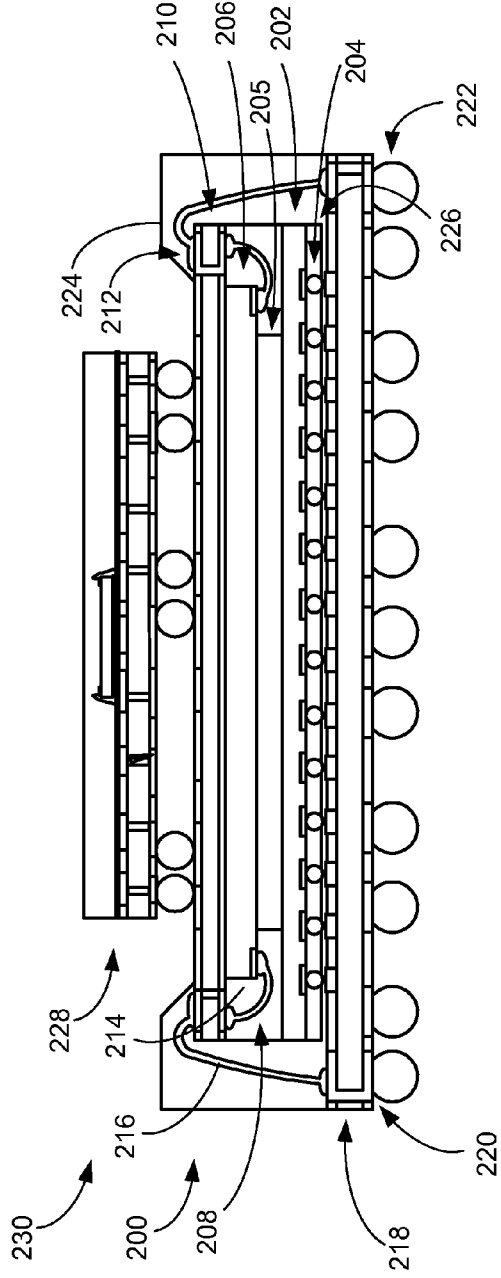


FIG. 2

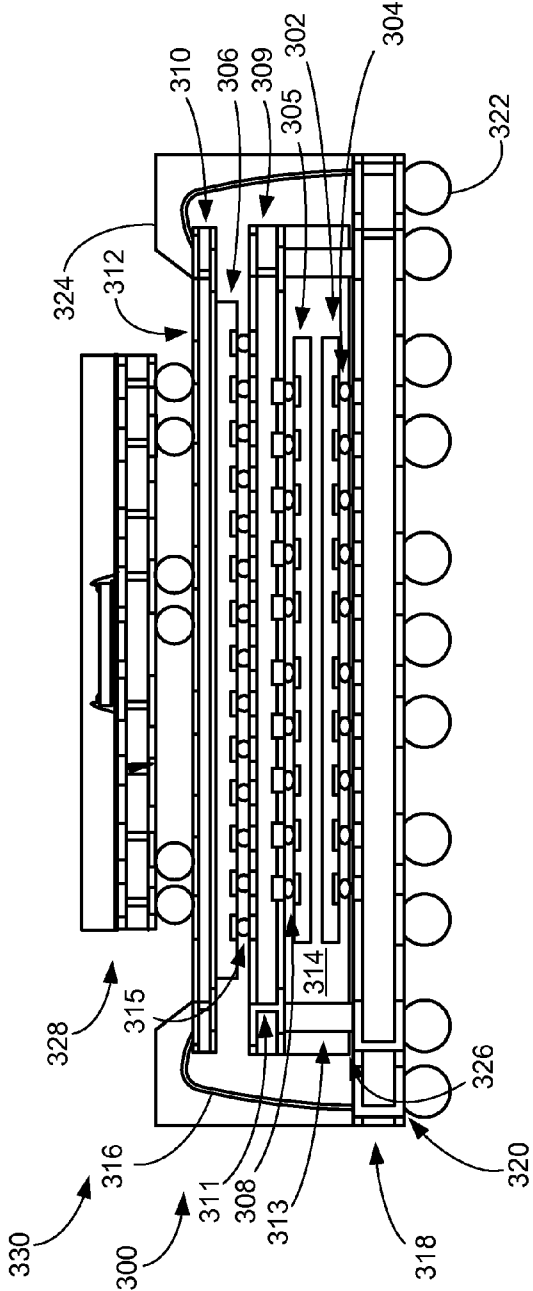


FIG. 3

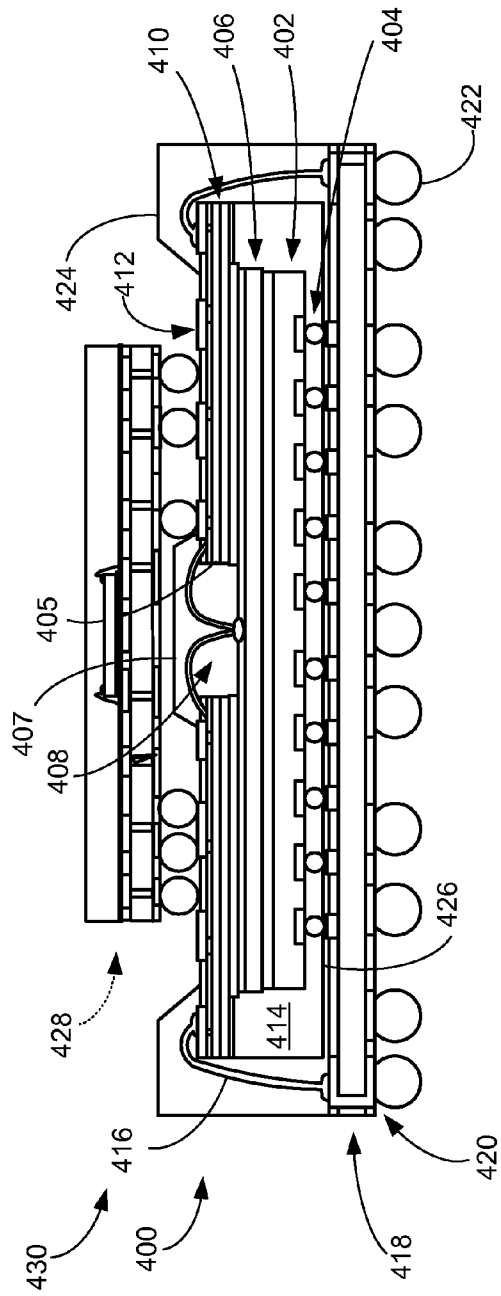


FIG. 4

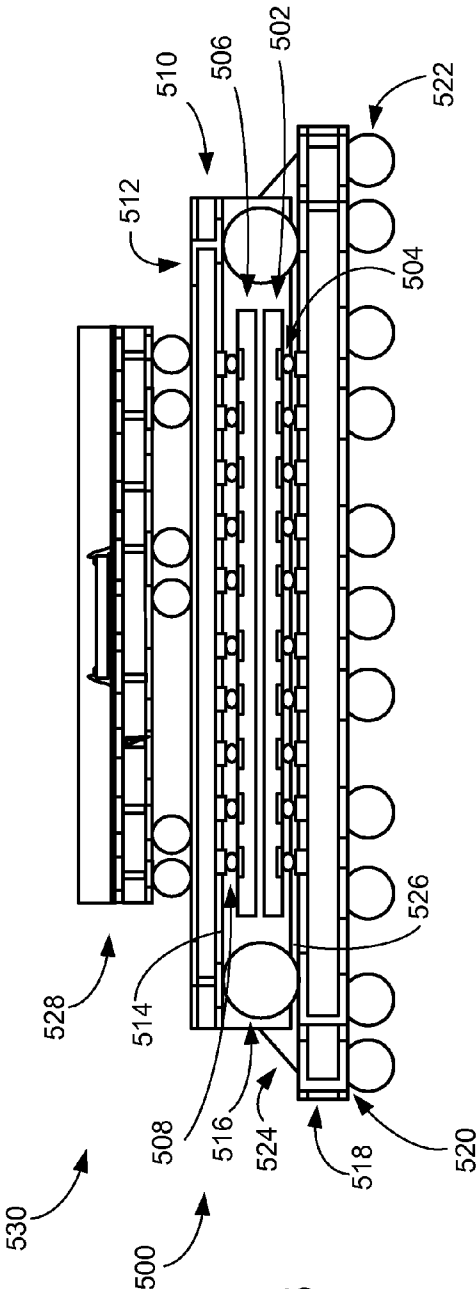


FIG. 5

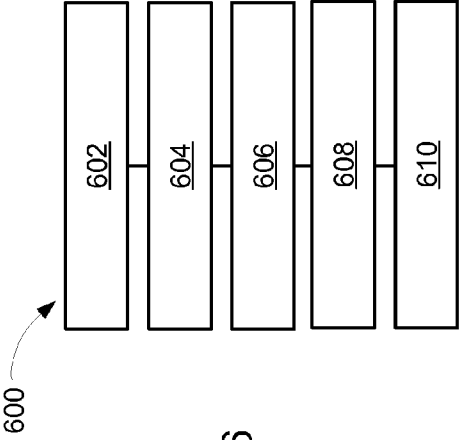


FIG. 6

INTEGRATED CIRCUIT PACKAGE SYSTEM WITH MULTI-CHIP MODULE

TECHNICAL FIELD

[0001] The present invention relates generally to package-on-package integrated circuit package systems, and more particularly to an integrated circuit package system with a package module over a substrate.

BACKGROUND ART

[0002] Integrated circuit packaging technology has seen an increase in the number of integrated circuits mounted on a single circuit board or substrate. The new packaging designs are more compact in form factors, such as the physical size and shape of an integrated circuit, and providing a significant increase in overall integrated circuit density. However, integrated circuit density continues to be limited by the “real estate” available for mounting individual integrated circuits on a substrate. Even larger form factor systems, such as personal computers, compute servers, and storage servers, need more integrated circuits in the same or smaller “real estate”. Particularly acute, the needs for portable personal electronics, such as cell phones, digital cameras, music players, and location-based devices, have further driven the need for integrated circuit density.

[0003] This increased integrated circuit density, has led to the development of multi-chip packages in which more than one integrated circuit can be packaged. Each package provides mechanical support for the individual integrated circuits and one or more layers of interconnect lines that enable the integrated circuits to be connected electrically to surrounding circuitry. Current multi-chip packages, also commonly referred to as multi-chip modules, typically consist of a printed circuit board substrate onto which a set of separate integrated circuit components are attached. Such multi-chip packages have been found to increase integrated circuit density and miniaturization, improve signal propagation speed, reduce overall integrated circuit size and weight, improve performance, and lower costs—all primary goals of the computer industry.

[0004] Multi-chip packages whether vertically or horizontally arranged, can also present problems because they usually must be pre-assembled before the integrated circuit and integrated circuit connections can be tested. Thus, when integrated circuits are mounted and connected in a multi-chip module, the individual integrated circuits and connections cannot be tested individually, and it is not possible to identify known-good-die (“KGD”) before being assembled into larger circuits. Consequently, conventional multi-chip packages lead to assembly process yield problems. This fabrication process, which does not identify KGD, is therefore less reliable and more prone to assembly defects.

[0005] Moreover, vertically stacked integrated circuits in typical multi-chip packages can present problems beyond those of horizontally arranged integrated circuit packages, further complicating the manufacturing process. It is more difficult to test and thus determine the actual failure mode of the individual integrated circuits. The substrate and integrated circuit are often damaged during assembly or testing, complicating the manufacturing process and increasing costs. The vertically stacked integrated circuit problems can be greater than the benefits.

[0006] In addition, multi-chip packages generally provide higher density of integrated circuits but present yet other challenges. Additional structures, such as printed circuit boards, middle substrates, or flexible wiring, must be currently used to connect the integrated circuits in the multi-chip package. These additional structures add cost, manufacturing complexity, potential failure areas, and potential reliability problems.

[0007] The conventional fan in package-on-package integrated circuit system has a wire bonded bottom tie and an internal stacking module (ISM) stacked on top with an exposed surface after molding to allow mounting other devices.

[0008] The difficulty with such devices is that delamination often occurs between the wire bonded bond die spacer and the inverted ISM.

[0009] The conventional package-on-package design requires many process steps, which require a long time for assembly and makes the end product expensive.

[0010] Further, package warpage between the packages may result in defective solder joints leading to open circuits.

[0011] Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

DISCLOSURE OF THE INVENTION

[0012] The present invention provides an integrated circuit package system with multi-chip module including: providing an upper substrate having an upper chip thereon; positioning a lower chip under the upper chip, the lower chip having bottom interconnects thereon; encapsulating the upper chip and the lower chip with a chip encapsulant on the upper substrate with the bottom interconnects exposed; mounting the lower chip over a lower substrate with a gap between the chip encapsulant and the lower substrate; and filling the gap with a package encapsulant or chip attach adhesive.

[0013] Certain embodiments of the invention have other aspects in addition to or in place of those mentioned above. The aspects will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a view of a multi-chip module in accordance with a first embodiment of the present invention;

[0015] FIG. 2 is a view of a multi-chip module in accordance with a second embodiment of the present invention;

[0016] FIG. 3 is a view of a multi-chip module in accordance with a third embodiment of the present invention;

[0017] FIG. 4 is a view of a multi-chip module in accordance with a fourth embodiment of the present invention;

[0018] FIG. 5 is a view of a multi-chip module in accordance with a fifth embodiment of the present invention; and

[0019] FIG. 6 is a flow chart for an integrated circuit package system for manufacturing the integrated circuit package system of FIG. 1.

BEST MODE FOR CARRYING OUT THE INVENTION

[0020] The following embodiments are described in sufficient detail to enable those skilled in the art to make and use the invention. It is to be understood that other embodiments

would be evident based on the present disclosure, and that system, process, or mechanical changes may be made without departing from the scope of the present invention.

[0021] In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known circuits, system configurations, and process steps are not disclosed in detail. Likewise, the drawings showing embodiments of the system are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the drawing FIGS.

[0022] Similarly, although the views in the drawings for ease of description generally show similar orientations, this depiction in the FIGS. is arbitrary for the most part. Generally, the invention can be operated in any orientation. Also, where multiple embodiments are disclosed and described having some features in common, for clarity and ease of illustration, description, and comprehension thereof, similar and like features one to another will ordinarily be described with similar reference numerals.

[0023] For expository purposes, the term “horizontal” as used herein is defined as a plane parallel to the plane or surface of the semiconductor chip, regardless of its orientation. The term “vertical” refers to a direction perpendicular to the horizontal as just defined. Terms, such as “above”, “below”, “bottom”, “top”, “side” (as in “sidewall”), “higher”, “lower”, “upper”, “over”, and “under”, are defined with respect to the horizontal plane. The term “on” means that there is direct contact among elements and the term “over” means that there is no such direct contact. The term “system” means the method and the apparatus of the present invention as will be apparent from context. The term “processing” as used herein includes stamping, forging, patterning, exposure, development, etching, cleaning, and/or removal of material or laser trimming as required in forming a described structure.

[0024] Referring now to FIG. 1, therein is shown a multi-chip module 100 in accordance with a first embodiment of the present invention.

[0025] The multi-chip module 100 includes a lower chip 102 having interconnects 104, such as solder bumps. The lower chip 102 is attached to an upper chip 106 having interconnects 108, such as bond wires. The upper chip 106 is attached to an upper substrate 110 having vias and wires 112 therein for attachment of other packages or devices 128. The interconnects 108 connect the upper chip 106 electrically to the vias and wires 112 of the upper substrate 110.

[0026] The lower chip 102, the upper chip 106, and the interconnects 108 are encapsulated in a chip encapsulant 114, which forms a package over the lower substrate 118. The chip encapsulant 114 also encapsulates the interconnects 104 but leaves them exposed for interconnection at the bottoms thereof.

[0027] Interconnects 116, such as bond wires, connect the upper substrate 110 to a lower substrate 118 having vias and wires 120. The vias and wires 120 interconnect the interconnects 116 to main interconnects 122, such as a ball grid array (BGA). The vias and wires 120 further connect the interconnects 104 to the main interconnects 122.

[0028] A module encapsulant 124 encapsulates the perimeter of the upper substrate 110, the interconnects 116, the interconnects 104, and the chip encapsulant 114 over the lower substrate 118. The module encapsulant 124 fills a gap

126 between the chip encapsulant 114 and the lower substrate 118. It has been discovered that filling the gap 126 in this way eliminates the possibility of delamination between the lower chip 102 and the lower substrate 118.

[0029] The multi-chip module 100 is part of a package-on-package configuration, which means that the module encapsulant 124 encapsulates the perimeter of the upper substrate 110 to allow another known-good package 128 to be attached to the vias and wires 112 of the upper substrate 110. The combination of the multi-chip module 100 and the known-good package 128 makes up an integrated package system 130.

[0030] Referring now to FIG. 2, therein is shown a multi-chip module 200 in accordance with a second embodiment of the present invention.

[0031] The multi-chip module 200 includes a lower chip 202 having interconnects 204, such as solder bumps. The lower chip 202 is attached to a dielectric spacer 205, which is attached to an upper chip 206 having interconnects 208, such as bond wires. The upper chip 206 is attached to an upper substrate 210 having vias and wires 212 therein for attachment of other packages or devices 228. The interconnects 208 connect the upper chip 206 electrically to the vias and wires 212 of the upper substrate 210.

[0032] The lower chip 202, the dielectric spacer 205, the upper chip 206, and the interconnects 208 are encapsulated in a chip encapsulant 214, which forms a package over the lower substrate 218. The spacer 205 protects the interconnects 208 from contact with the upper chip 206. The chip encapsulant 214 also encapsulates the interconnects 204 but leaves them exposed for interconnection at the bottoms thereof to the lower substrate 218.

[0033] Interconnects 216, such as bond wires, connect the upper substrate 210 to a lower substrate 218 having vias and wires 220. The vias and wires 220 interconnect the interconnects 216 to main interconnects 222, such as a ball grid array (BGA). The vias and wires 220 further connect the interconnects 204 to the main interconnects 222.

[0034] A module encapsulant 224 encapsulates the perimeter of the upper substrate 210, the interconnects 216, and the interconnects 204 over the lower substrate 218. The module encapsulant 224 fills a gap 226 between the chip encapsulant 214 and the lower substrate 218. It has been discovered that filling the gap 226 in this way eliminates the possibility of delamination between the lower chip 202 and the lower substrate 218.

[0035] The multi-chip module 200 is part of a package-on-package configuration, which means that the module encapsulant 224 encapsulates the perimeter of the upper substrate 210 to allow another known-good package 228 to be attached to the vias and wires 212 of the upper substrate 210. The combination of the multi-chip module 200 and the known-good package 228 makes up an integrated package system 230.

[0036] Referring now to FIG. 3, therein is shown a multi-chip module 300 in accordance with a third embodiment of the present invention.

[0037] The multi-chip module 300 includes a lower chip 302 having interconnects 304, such as solder bumps. The lower chip 302 is spaced from a middle chip 305 having interconnects 308, such as solder bumps. The middle chip 305 is attached to a middle substrate 309 having vias and wires

311. Interconnects **313**, such as studs or columns, connect the vias and wires **311** on the middle substrate **309** to a lower substrate **318**.

[0038] An upper chip **306** is attached to the middle substrate **309** by interconnects **315**, such as solder bumps. The upper chip **306** is attached to an upper substrate **310** having vias and wires **312** therein for attachment of other packages or devices **328**.

[0039] The lower chip **302**, the middle chip **305**, and the interconnects **308** are encapsulated in a chip encapsulant **314**, which forms a package over the lower substrate **318**. The chip encapsulant **314** also encapsulates the interconnects **304** but leaves them exposed for interconnection at the bottoms thereof.

[0040] Upper substrate interconnects **316**, such as bond wires, connect the upper substrate **310** to the lower substrate **318** having vias and wires **320**. The vias and wires **320** interconnect the upper substrate interconnects **316** to main interconnects **322**, such as a ball grid array (BGA). The vias and wires **320** further connect the interconnects **304** to the main interconnects **322**.

[0041] A module encapsulant **324** encapsulates the perimeter of the upper substrate **310**, the interconnects **316**, and the interconnects **304** over the lower substrate **318**. The module encapsulant **324** fills a gap **326** between the chip encapsulant **314** and the lower substrate **318**. It has been discovered that filling the gap **326** in this way eliminates the possibility of delamination between the lower chip **302** and the lower substrate **318**.

[0042] The multi-chip module **300** is part of a package-on-package configuration, which means that the module encapsulant **324** encapsulates the perimeter of the upper substrate **310** to allow another known-good package **328** to be attached to the vias and wires **312** of the upper substrate **310**. The combination of the multi-chip module **300** and the known-good package **328** makes up an integrated package system **330**.

[0043] Referring now to FIG. 4, therein is shown a multi-chip module **400** in accordance with a fourth embodiment of the present invention.

[0044] The multi-chip module **400** includes a lower chip **402** having interconnects **404**, such as solder bumps. The lower chip **402** is attached to an upper chip **406** having interconnects **408**, such as bond wires. The upper chip **406** is attached to an upper substrate **410** having vias and wires **412** therein for attachment of other packages or devices **428**. The interconnects **408** extend through an opening **405** in the upper substrate **410** and are encapsulated in an interconnect encapsulant **407**. The interconnects **408** connect the top of the upper chip **406** electrically to the vias and wires **412** of the top of the upper substrate **410**.

[0045] The lower chip **402** and the upper chip **406** are encapsulated in a chip encapsulant **414**, which forms a package over the lower substrate **418**. The chip encapsulant **414** also encapsulates the interconnects **404** but leaves them exposed for interconnection at the bottoms thereof.

[0046] Interconnects **416**, such as bond wires, connect the upper substrate **410** to a lower substrate **418** having vias and wires **420**. The vias and wires **420** interconnect the interconnects **416** to main interconnects **422**, such as a ball grid array (BGA). The vias and wires **420** further connect the interconnects **404** to the main interconnects **422**.

[0047] A module encapsulant **424** encapsulates the perimeter of the upper substrate **410**, the interconnects **416**, and the

interconnects **404** over the lower substrate **418**. The module encapsulant **424** fills a gap **426** between the chip encapsulant **414** and the lower substrate **418**. It has been discovered that filling the gap **426** in this way eliminates the possibility of delamination between the lower chip **402** and the lower substrate **418**.

[0048] The multi-chip module **400** is part of a package-on-package configuration, which means that the module encapsulant **424** encapsulates the perimeter of the upper substrate **410** to allow another known-good package **428** to be attached to the vias and wires **412** of the top of the upper substrate **410**. The combination of the multi-chip module **400** and the known-good package **428** makes up an integrated package system **430**.

[0049] Referring now to FIG. 5, therein is shown a multi-chip module **500** in accordance with a fifth embodiment of the present invention.

[0050] The multi-chip module **500** includes a lower chip **502** having interconnects **504**, such as solder bumps. The lower chip **502** is spaced from an upper chip **506** having interconnects **508**, such as solder bumps. The upper chip **506** is attached to an upper substrate **510** having vias and wires **512** therein for attachment of other packages or devices **528**. The interconnects **508** connect the upper chip **506** electrically to the vias and wires **512** of the upper substrate **510**.

[0051] The lower chip **502**, the upper chip **506**, and the interconnects **508** are encapsulated in a chip encapsulant **514**, which forms a package over the lower substrate **518**. The chip encapsulant **514** also encapsulates the interconnects **504** but leaves them exposed for interconnection at the bottoms thereof.

[0052] Interconnects **516**, such as solder balls, connect the upper substrate **510** to a lower substrate **518** having vias and wires **520**. The vias and wires **520** interconnect the interconnects **516** to main interconnects **522**, such as a ball grid array (BGA). The vias and wires **520** further connect the interconnects **504** to the main interconnects **522**.

[0053] A chip attach adhesive **524** encapsulates the perimeter of the chip encapsulant **514** and the interconnects **504** on the lower substrate **518**. The chip attach adhesive **524** fills a gap **526** between the chip encapsulant **514** and the lower substrate **518**. It has been discovered that filling the gap **526** in this way eliminates the possibility of delamination between the lower chip **502** and the lower substrate **518**.

[0054] The multi-chip module **500** is part of a package-on-package configuration, which means that the upper substrate **110** allows another known-good package **528** to be attached to the vias and wires **512** of the upper substrate **510**. The combination of the multi-chip module **500** and the known-good package **528** makes up an integrated package system **530**.

[0055] Referring now to FIG. 6, therein is shown a flow chart for an integrated circuit package system **600** for manufacturing the integrated circuit package system **130**. The integrated circuit package system **600** includes: providing an upper substrate having an upper chip thereon in a block **602**; positioning a lower chip under the upper chip, the lower chip having bottom interconnects thereon in a block **604**; encapsulating the upper chip and the lower chip with a chip encapsulant on the upper substrate with the bottom interconnects exposed in a block **606**; mounting the lower chip over a lower substrate with a gap between the chip encapsulant and the lower substrate in a block **608**; and filling the gap with a package encapsulant or chip attach adhesive in a block **610**.

[0056] While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the scope of the included claims. All matters hitherto set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

What is claimed is:

1. An integrated circuit package system with multi-chip module comprising:

providing an upper substrate having an upper chip thereon; positioning a lower chip under the upper chip, the lower chip having bottom interconnects thereon; encapsulating the upper chip and the lower chip with a chip encapsulant on the upper substrate with the bottom interconnects exposed; mounting the lower chip over a lower substrate with a gap between the chip encapsulant and the lower substrate; and filling the gap with a package encapsulant or chip attach adhesive.

2. The system as claimed in claim **1** further comprising interconnecting the upper chip and the upper substrate.

3. The system as claimed in claim **1** further comprising spacing the upper chip from the lower chip to prevent contact between interconnections between the upper chip and the upper substrate, and the lower chip.

4. The system as claimed in claim **1** wherein positioning the lower chip positions a lower chip larger than the upper chip.

5. The system as claimed in claim **1** further comprising: providing a middle substrate having a middle chip thereon; connecting the upper chip to the middle substrate; and connecting the middle substrate to the lower substrate.

6. The system as claimed in claim **1** wherein: providing the upper substrate provides the upper substrate with an opening provided therein; and interconnecting the upper chip and the upper substrate through the opening.

7. The system as claimed in claim **1** further comprising connecting a second package to the upper substrate.

8. An integrated circuit package system with multi-chip module comprising:

providing an upper substrate having an upper chip thereon and having interconnects therebetween; positioning a lower chip under the upper chip, the lower chip having bottom interconnects thereon; encapsulating the upper chip and the lower chip with a chip encapsulant on the upper substrate with the bottom interconnects exposed; mounting the lower chip over a lower substrate with a gap between the chip encapsulant and the lower substrate; interconnecting the upper substrate and the lower substrate; and filling the gap with a package encapsulant or chip attach adhesive.

9. The system as claimed in claim **8** further comprising interconnecting the upper chip and the upper substrate by solder bumps or bond wires.

10. The system as claimed in claim **8** further comprising spacing the upper chip from the lower chip to prevent contact

between interconnections between the upper chip and the upper substrate, and the lower chip wherein the interconnections are bond wires.

11. The system as claimed in claim **8** wherein positioning the lower chip positions a lower chip larger than the upper chip and having a spacer therebetween.

12. The system as claimed in claim **8** further comprising: providing a middle substrate having a middle chip thereon and having interconnects therebetween; connecting the upper chip to the middle substrate by interconnects therebetween; and connecting the middle substrate to the lower substrate by a stud or solder ball in the chip encapsulant.

13. The system as claimed in claim **8** wherein: providing the upper substrate provides the upper substrate with an opening provided therein; and interconnecting the upper chip and the upper substrate through the opening using bond wires.

14. The system as claimed in claim **8** wherein: filling the gap with package encapsulant leaves the upper substrate exposed; and connecting a known-good package to the exposed upper substrate.

15. An integrated circuit package system with multi-chip module comprising:

an upper substrate; an upper chip on the upper substrate; a lower chip under the upper chip, the lower chip having bottom interconnects thereon; a chip encapsulant encapsulating the upper chip and the lower chip on the upper substrate with the bottom interconnects exposed, the lower chip over a lower substrate with a gap between the chip encapsulant and the lower substrate; and a package encapsulant or chip attach adhesive filling the gap.

16. The system as claimed in claim **15** further comprising interconnecting between the upper chip and the upper substrate.

17. The system as claimed in claim **15** further comprising: interconnections between the upper chip and the upper substrate; and

a spacer between the upper chip and the lower chip to prevent contact between the interconnections between the upper chip and the upper substrate, and the lower chip.

18. The system as claimed in claim **15** wherein the lower chip is larger than the upper chip.

19. The system as claimed in claim **15** further comprising: a middle substrate; a middle chip on the middle substrate; upper chip interconnects between the upper chip and the middle substrate; and middle substrate interconnects between the middle substrate and the lower substrate.

20. The system as claimed in claim **15** wherein: the upper substrate has an opening provided therein; and upper chip interconnects connect the upper chip and the upper substrate through the opening.

21. The system as claimed in claim **15** further comprising: a second package attached to the upper substrate.

22. The system as claimed in claim **15** further comprising: upper chip interconnects between the upper chip and the upper substrate; and

substrate interconnects interconnecting the upper substrate and the lower substrate.

23. The system as claimed in claim **22** further comprising upper chip interconnects connecting the upper chip and the upper substrate wherein the upper chip interconnects are solder bumps or bond wires.

24. The system as claimed in claim **22** further comprising a spacer spacing the upper chip from the lower chip for preventing contact between interconnections between the upper chip and the upper substrate, and the lower chip wherein the interconnections are bond wires.

25. The system as claimed in claim **22** wherein:

the lower chip is larger than the upper chip; and
a spacer between the upper chip and the lower chip.

26. The system as claimed in claim **22** further comprising:
a middle substrate;
a middle chip on the middle substrate;
middle chip interconnects between the middle substrate
and the middle chip;

chip interconnects for connecting the upper chip to the middle substrate; and

substrate interconnects for connecting the middle substrate to the lower substrate wherein the substrate interconnects are studs or solder balls in the chip encapsulant.

27. The system as claimed in claim **22** wherein:

the upper substrate has an opening provided therein; and
upper chip interconnects for connecting the upper chip and the upper substrate through the opening wherein the upper chip interconnects are bond wires.

28. The system as claimed in claim **22** wherein:

the package encapsulant and chip attach adhesive leave the upper substrate exposed;

and

a known-good package is connected to the exposed upper substrate.

* * * * *