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(54) Title: CACHE FILTER

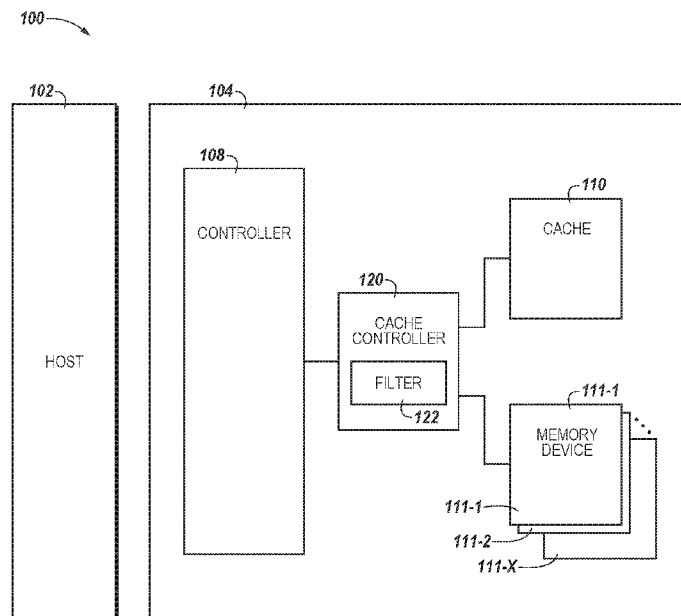


Fig. 1

(57) Abstract: The present disclosure includes apparatuses and methods related to a memory system including a filter. An example apparatus can include a filter to store a number flags, wherein each of the number of flags corresponds to a cache entry and each of the number of flags identifies a portion of the memory device where data of a corresponding cache entry is stored in the memory device.

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CACHE FILTER

Technical Field

[0001] The present disclosure relates generally to memory systems, and more particularly, to apparatuses and methods with memory system having a filter.

Background

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuits in computing devices or other electronic devices. There are many different types of memory including volatile and non-volatile memory. Volatile memory can require power to maintain its data (e.g., user data, error data, etc.) and includes random-access memory (RAM), dynamic random access memory (DRAM), and synchronous dynamic random access memory (SDRAM), among others. Non-volatile memory can provide persistent data by retaining stored data when not powered and can include NAND flash memory, NOR flash memory, read only memory (ROM), Electrically Erasable Programmable ROM (EEPROM), Erasable Programmable ROM (EPROM), and resistance variable memory such as phase change random access memory (PCRAM), resistive random access memory (RRAM), and magnetoresistive random access memory (MRAM), among others.

[0003] A memory system can include a cache memory that may be smaller and/or faster than other memory of the system (e.g., DRAM, NAND, disk storage, solid state drives (SSD), etc., which may be referred to as main memory). As an example, cache memory may comprise DRAM memory. A memory system can cache data to improve performance of the memory system. Therefore providing cache memory that delivers improved performance for the memory system is desirable. Improving the latency and hit rate of the cache memory are performance characteristics that can provide improved performance of the memory system.

Brief Description of the Drawings

[0004] Figure 1 is a block diagram of a computing system including an apparatus in the form of a host and an apparatus in the form of memory system in accordance with one or more embodiments of the present disclosure.

[0005] Figure 2 is a block diagram of an apparatus in the form of a memory system in accordance with a number of embodiments of the present disclosure.

[0006] Figure 3 is a block diagram of an apparatus in the form of a cache controller including a filter in accordance with a number of embodiments of the present disclosure.

[0007] Figures 4-5 are diagrams illustrating a flag in a filter of cache controller in accordance with a number of embodiments of the present disclosure.

Detailed Description

[0008] The present disclosure includes apparatuses and methods related to a memory system including a filter. An example apparatus can include a filter to store a number flags, wherein each of the number of flags corresponds to a cache entry and each of the number of flags identifies a portion of the memory device where data of a corresponding cache entry is stored in the memory device.

[0009] In a number of embodiments, a filter on a cache and/or cache controller can be used to predict whether the cache controller should service a request to read and/or write data to a memory system using the cache memory and/or a memory device (e.g., backing store). For example, a filter can include a number of flags, where each of the number of flags can have a corresponding cache entry (e.g. cache line) in the cache memory and identify a portion of a memory device where data of a corresponding cache entry is stored in the memory device. The cache controller can use information from a request and the flags in the filter to determine whether the request may be serviced using data in the cache or whether the request is be serviced using data in the memory device.

[0010] In a number of embodiments, the flags can include a number of bits that identify a portion of a memory device where data of a corresponding cache entry is stored in the memory device. The number of bits can also indicate if data of a corresponding cache entry is valid or invalid and/or dirty or not dirty. For example, a memory device can include 16 regions of a particular size and a cache can be the size of one of the regions of the memory device. A filter can include a first bit that can be used to predict whether data of a corresponding cache entry is in a first portion of the memory device, the first 8 regions of the memory device in this example, or in a second portion of the memory device, the last 8 regions of the memory device in this example. A filter can include a first bit and a second bit that can be used to predict whether data of a corresponding cache entry is in a first portion of the memory device which corresponds to the first 4 regions of the memory device in this example, in a second portion of the memory device which corresponds to the second 4 regions of the memory device in this example, in a third portion of the memory device which corresponds to the third 4 regions of the memory device in this example, or in a fourth portion of the memory device which corresponds to the last 4 regions of the memory device in this example. The filter can also include a bit that indicates whether the data in an associated cache entry is valid or invalid and a bit that indicates whether data in an associated cache entry is dirty or not dirty.

[0011] A cache controller can receive a request with information, such as address information. The information in the request can indicate which flag in the filter is associated with the request, which cache entry in the cache is associated with request, and where data associated with the request is and/or will be located in a memory device. The cache controller can locate the flag associated with request and compare the information about where data associated with the request is and/or will be located in a memory device to the bits (e.g. settings) in the flag that identifies a portion of the memory device where data of a corresponding cache entry is stored in the memory device. If the location where data associated with the request is and/or will be located in a memory device is in the portion of the memory device where data of a corresponding cache entry is stored in the memory device as identified by the flag, then the cache controller can attempt to service the request using cache by querying the cache to determine if the data associated with the request is located

in the cache. If the location where data associated with the request is and/or will be located in a memory device is not in the portion of the memory device where data of a corresponding cache entry is stored in the memory device as identified by the flag, then the cache controller can service the request using the memory device.

[0012] In a number of embodiments, a filter can be used to reduce latency of a memory system with cache by determining whether or not to attempt to service a request for data using a cache. The filter can indicate whether there is no chance or a chance that the request can be serviced using data in the cache. If the filter indicates that the request will be a cache miss, the cache controller can skip attempting to service the request with data that is in the cache (e.g., skip searching the cache for data associated with the request), thus decreasing the latency associated with the request and reducing the load on the cache.

[0013] In the following detailed description of the present disclosure, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration how one or more embodiments of the disclosure may be practiced. These embodiments are described in sufficient detail to enable those of ordinary skill in the art to practice the embodiments of this disclosure, and it is to be understood that other embodiments may be utilized and that process, electrical, and/or structural changes may be made without departing from the scope of the present disclosure. As used herein, the designators “M”, “N”, and “X”, particularly with respect to reference numerals in the drawings, indicates that a number of the particular feature so designated can be included. As used herein, “a number of” a particular thing can refer to one or more of such things (e.g., a number of memory devices can refer to one or more memory devices).

[0014] The figures herein follow a numbering convention in which the first digit or digits correspond to the drawing figure number and the remaining digits identify an element or component in the drawing. Similar elements or components between different figures may be identified by the use of similar digits. For example, 120 may reference element “20” in Figure 1, and a similar element may be referenced as 220 in Figure 2. As will be appreciated, elements shown in the various embodiments herein can be added, exchanged, and/or

eliminated so as to provide a number of additional embodiments of the present disclosure.

[0015] Figure 1 is a functional block diagram of a computing system 100 including an apparatus in the form of a host 102 and an apparatus in the form of memory system 104, in accordance with one or more embodiments of the present disclosure. As used herein, an “apparatus” can refer to, but is not limited to, any of a variety of structures or combinations of structures, such as a circuit or circuitry, a die or dice, a module or modules, a device or devices, or a system or systems, for example. In the embodiment illustrated in Figure 1A, memory system 104 can include a controller 108, a cache controller 120, cache 110, and a number of memory devices 111-1, . . . , 111-X. The cache 120 and/or memory devices 111-1, . . . , 111-X can include volatile memory and/or non-volatile memory.

[0016] As illustrated in Figure 1, host 102 can be coupled to the memory system 104. In a number of embodiments, memory system 104 can be coupled to host 102 via a channel. Host 102 can be a laptop computer, personal computers, digital camera, digital recording and playback device, mobile telephone, PDA, memory card reader, interface hub, among other host systems, and can include a memory access device, e.g., a processor. One of ordinary skill in the art will appreciate that “a processor” can intend one or more processors, such as a parallel processing system, a number of coprocessors, etc.

[0017] Host 102 can include a host controller to communicate with memory system 104. The host 102 can send commands to the memory system 104 via a channel. The host 102 can communicate with memory system 104 and/or the controller 108 on memory system 104 to read, write, and erase data, among other operations. A physical host interface can provide an interface for passing control, address, data, and other signals between the memory system 104 and host 102 having compatible receptors for the physical host interface. The signals can be communicated between host 102 and memory system 104 on a number of buses, such as a data bus and/or an address bus, for example, via channels.

[0018] Controller 108, a host controller, a controller on cache 110, and/or a controller on cache memory can include control circuitry, e.g., hardware, firmware, and/or software. In one or more embodiments, controller

108, a host controller, a controller on cache 110, and/or a controller on cache memory can be an application specific integrated circuit (ASIC) coupled to a printed circuit board including a physical interface. Memory system 104 can include cache controller 120 and cache 110. Cache controller 120 and cache 110 can be used to buffer and/or cache data that is used during execution of read commands and/or write commands.

[0019] Cache controller 120 can include a buffer with filter 122. A buffer can include a number of arrays of volatile memory (e.g., SRAM) that can act as filter 122. A buffer on the cache controller can be configured to store signals, address signals (e.g., read and/or write commands), and/or data (e.g., metadata and/or write data). The buffer can temporarily store signals and/or data while commands are executed. Cache 110 can include arrays of memory cells (e.g., DRAM memory cells) that are used as cache and can be configured to store data that is also stored in a memory device. The data stored in cache and in the memory device is addressed by the controller and can be located in cache and/or the memory device during execution of a command.

[0020] Memory devices 111-1, . . . , 111-X can provide main memory for the memory system or could be used as additional memory or storage throughout the memory system 104. Each memory device 111-1, . . . , 111-X can include one or more arrays of memory cells, e.g., non-volatile and/or volatile memory cells. The arrays can be flash arrays with a NAND architecture, for example. Embodiments are not limited to a particular type of memory device. For instance, the memory device can include RAM, ROM, DRAM, SDRAM, PCRAM, RRAM, and flash memory, among others.

[0021] The embodiment of Figure 1 can include additional circuitry that is not illustrated so as not to obscure embodiments of the present disclosure. For example, the memory system 104 can include address circuitry to latch address signals provided over I/O connections through I/O circuitry. Address signals can be received and decoded by a row decoder and a column decoder to access the memory devices 111-1, . . . , 111-X. It will be appreciated by those skilled in the art that the number of address input connections can depend on the density and architecture of the memory devices 111-1, . . . , 111-X.

[0022] Figure 2 is a block diagram of an apparatus in the form of a memory system in accordance with a number of embodiments of the present

disclosure. In Figure 2, the memory system can be configured to cache data and service requests from a host and/or memory system controller. The memory system can include cache controller 220 with a buffer including filter 222. The buffer can include SRAM memory, for example. A buffer can include information about the data in cache 210, including metadata and/or address information for the data in the cache. The memory system can include a memory device 211 coupled to the cache controller 220. Memory device 211 can include non-volatile memory arrays and/or volatile memory arrays and can serve as the backing store for the memory system.

[0023] Memory device 211 can include a controller and/or control circuitry (e.g., hardware, firmware, and/or software) which can be used to execute commands on the memory device 211. The control circuitry can receive commands from a memory system controller and or cache controller 220. The control circuitry can be configured to execute commands to read and/or write data in the memory device 211.

[0024] Figure 3 is a block diagram of an apparatus in the form of a cache controller including a filter in accordance with a number of embodiments of the present disclosure. In Figure 3, filter 322 can be included on a cache controller, such as cache controller 120 in Figure 1, for example. Filter 322 can include a number of entries (e.g., flags 324-1, ..., 324-X). Each of the flags 324-1, ..., 324-X can correspond to entries (e.g., cache lines) in a cache, such as cache 110 in Figure 1. For example, flag 324-1 in filter 322 can correspond to a first entry in a cache, flag 324-2 in filter 322 can correspond to a second entry in a cache, flag 324-X in filter 322 can correspond to an Xth entry in a cache, and so on. Each of the flags 324-1, ..., 324-X can include number of bits 326-0, ..., 236-Y.

[0025] In a number of embodiments, the number of bits 326-0, ..., 236-Y in a flag can identify a portion of a memory device, such as memory 111 in Figure 1, where data of a corresponding cache entry is stored in the memory device. A cache controller can receive a request and locate a flag in filter 322 based on information in the request. The request can include address information that can identify a flag in the filter 322 and also a cache entry in the cache, such as cache 110 in Figure, where data associated with the request may be located. The cache controller can locate the flag identified by the request and

determine if the number of bits of the flag identify a portion of a memory device where data of a corresponding cache entry is stored in the memory device.

[0026] If the address information of the request includes an address for a portion of a memory device where the data of a corresponding cache entry is stored in the memory device as indicated by the number of bits of the flag, then the cache controller can check in the corresponding cache entry in the cache for the data associated with the request. The flag can be used by the cache controller to determine whether to check the cache for data associated with the request. The flag can indicate and/or predict that the data associated with the request may be located in the cache and the cache controller can proceed to check the cache to determine if the data associated with the request is a hit or miss in the cache. If the address information of the request does not include an address for a portion of a memory device where data of a corresponding cache entry is stored in the memory device as indicated by the number of bits of the flag, then the cache controller can retrieve the data associated with the request from the memory device.

[0027] Figures 4-5 are diagrams illustrating a flag in a filter of cache controller in accordance with a number of embodiments of the present disclosure. In Figure 4, flag 424 can be on a filter on a cache controller and correspond to an entry (e.g., cache line) of a cache. Flag 424 can be used to determine if data associated with a request may be in cache or if it is not in cache. In Figure 4, flag 424 can include bits 426-0, 426-1, 426-2, and 426-3. In a number of embodiments, flag 424 can include any number of bits. The bits can correspond to at least a portion of an address where data in a corresponding cache entry is stored in a memory device. The cache controller can determine if data associated with a request may be located in a corresponding cache entry by comparing the address information in the request to the bits in the flag. If there is a match between the address information in the request and the bits in the flag, the cache controller can check the cache to determine if the data associated with the request is in the cache. If there is not a match between the address information in the request and the bits in the flag, the cache controller can locate and/or retrieve the data associated with the request from a memory device.

[0028] In a number of embodiments, bits 426-0, 426-1, 426-2, and 426-3 of flag 324 can be set to logical values 1 or 0, where a logical value of 0

indicates data in a corresponding cache entry is in a first portion of a memory device and a logical value of 1 indicates data in a corresponding cache entry is in a second portion of a memory device.

[0029] In a number of embodiments, flag 424 can include one bit, bit 426-0. When bit 426-0 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 432-1 of a memory device that includes regions 430-0, ..., 430-7 of a memory device. When bit 426-0 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 432-2 of a memory device that includes regions 430-8, ..., 430-15 of a memory device.

[0030] In a number of embodiments, flag 424 can include two bits, bits 426-0 and 426-1. When bit 426-0 is set to logical value 0 and bit 426-1 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 434-1 of a memory device that includes regions 430-0, ..., 430-3 of a memory device. When bit 426-0 is set to logical value 0 and bit 426-1 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 434-2 of a memory device that includes regions 430-4, ..., 430-7 of a memory device. When bit 426-0 is set to logical value 1 and bit 426-1 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 434-3 of a memory device that includes regions 430-8, ..., 430-11 of a memory device. When bit 426-0 is set to logical value 1 and bit 426-1 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 434-4 of a memory device that includes regions 430-12, ..., 430-15 of a memory device.

[0031] In a number of embodiments, flag 424 can include three bits, bits 426-0, 426-1, and 426-2. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, and bit 426-2 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 436-1 of a memory device that includes regions 430-0, ..., 430-1 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, and bit 426-2 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 436-2 of a memory device that includes regions 430-2, ..., 430-3 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 1, and bit 426-2 is set to logical value 0, flag 424 can indicate data in a

corresponding cache entry is in portion 436-3 of a memory device that includes regions 430-4, ..., 430-5 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 1, and bit 426-2 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 436-4 of a memory device that includes regions 430-6, ..., 430-7 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, and bit 426-2 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 436-5 of a memory device that includes regions 430-8, ..., 430-9 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 0, and bit 426-2 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 436-6 of a memory device that includes regions 430-10, ..., 430-11 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 1, and bit 426-2 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 436-7 of a memory device that includes regions 430-12, ..., 430-13 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 1, and bit 426-2 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 436-8 of a memory device that includes regions 430-14, ..., 430-15 of a memory device.

[0032] In a number of embodiments, flag 424 can include four bits, bits 426-0, 426-1, 426-3, and 426-4. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 0, and bit 426-3 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-1 of a memory device that includes region 430-0 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 0, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 438-2 of a memory device that includes region 430-1 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-3 of a memory device that includes region 430-2 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding

cache entry is in portion 438-4 of a memory device that includes region 430-3 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 0, and bit 426-4 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-5 of a memory device that includes region 430-4 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 0, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 438-6 of a memory device that includes region 430-5 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-7 of a memory device that includes region 430-6 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 438-8 of a memory device that includes region 430-7 of a memory device. When bit 426-0 is set to logical value 0, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 0, and bit 426-4 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-9 of a memory device that includes region 430-8 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 0, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 438-10 of a memory device that includes region 430-9 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-11 of a memory device that includes region 430-10 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 0, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 438-12 of a memory device that includes region 430-11 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 0, and bit 426-4 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-13 of a memory

device that includes region 430-12 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 0, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 438-14 of a memory device that includes region 430-13 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 0, flag 424 can indicate data in a corresponding cache entry is in portion 438-15 of a memory device that includes region 430-14 of a memory device. When bit 426-0 is set to logical value 1, bit 426-1 is set to logical value 1, bit 426-2 is set to logical value 1, and bit 426-4 is set to logical value 1, flag 424 can indicate data in a corresponding cache entry is in portion 438-16 of a memory device that includes region 430-15 of a memory device.

[0033] In Figure 5, flag 524 can be on a filter on a cache controller and correspond to an entry (e.g., cache line) of a cache. Flag 524 can be used to determine if data associated with a request may be in cache or if it is not in cache. In Figure 5, flag 524 can include bits 526-0, ..., 526-15. In a number of embodiments, flag 524 can include any number of bits. Bits 526-0, ..., 526-15 can correspond to a portion of a memory device where data in a corresponding cache entry is stored in a memory device. The cache controller can determine if data associated with a request may be located in a corresponding cache entry by comparing the address information in the request to the bits in the flag. If there is a match between the address information in the request and the bits in the flag, the cache controller can check the cache to determine if the data associated with the request is in the cache. If there is not a match between the address information in the request and the bits in the flag, the cache controller can locate and/or retrieve the data associated with the request from a memory device.

[0034] In Figure 5, a memory device includes 16 regions, regions 530-0, ..., 530-15 and each of the bits 526-0, ..., 526-15 can correspond to a particular region. Bit 526-0 can correspond to region 530-0, bit 526-1 can correspond to region 530-1, bit 526-2 can correspond to region 530-2, bit 526-3 can correspond to region 530-3, bit 526-4 can correspond to region 530-4, bit 526-5 can correspond to region 530-5, bit 526-6 can correspond to region 530-6, bit 526-7 can correspond to region 530-7, bit 526-8 can correspond to region 530-8, bit 526-9 can correspond to region 530-9, bit 526-10 can correspond to region

530-10, bit 526-11 can correspond to region 530-11, bit 526-12 can correspond to region 530-12, bit 526-13 can correspond to region 530-13, bit 526-14 can correspond to region 530-14, and bit 526-15 can correspond to region 530-15. Bits 526-0, ..., 526-15 can be set to logical values 1 or 0. A bit set to logical value 1 indicates data in a corresponding cache entry is located in the region of the memory device corresponding to the bit. A bit set to logical value 0 indicates data in a corresponding cache entry is not located in the region of the memory device corresponding to the bit.

[0035] Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of various embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the various embodiments of the present disclosure includes other applications in which the above structures and methods are used. Therefore, the scope of various embodiments of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

[0036] In the foregoing Detailed Description, various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosed embodiments of the present disclosure have to use more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. An apparatus, comprising:
a cache controller; and
a cache and a memory device coupled to the cache controller, wherein the cache controller includes a filter configured to:
store a number flags, wherein each of the number of flags corresponds to a cache entry and each of the number of flags identifies a portion of the memory device where data of a corresponding cache entry is stored in the memory device.
2. The apparatus of claim 1, wherein the memory device is a non-volatile memory device and the cache is a DRAM memory device configured to store a portion of the data stored in the memory device.
3. The apparatus of claim 1, wherein the number of flags indicate a portion of the memory device where data corresponding to a request is located.
4. The apparatus of any one of claims 1-3, wherein a setting of the number of flags indicate whether the cache is storing valid data corresponding to a request.
5. The apparatus of any one of claims 1-3, wherein each of the number of flags identifies at least a partial location of data stored in the memory device of a corresponding cache entry.
6. An apparatus, comprising:
a cache controller; and
a cache and a memory device coupled to the cache controller, wherein the cache controller includes a filter, wherein the filter includes a number of flags that correspond to a number of cache entries in the cache and wherein the cache controller is configured to determine whether to search the cache for data corresponding to a request based on the number of flags.

7. The apparatus of claim 6, wherein the cache controller is configured to locate data in the cache corresponding to the request in response to one of the number of flags indicating the data corresponding to the request is in the cache.
8. The apparatus of claim 6, wherein the cache controller is configured to locate data in the memory device corresponding to the request in response to one of the number of flags indicating the data corresponding to the request is not in the cache.
9. The apparatus of any one of claims 6-8, wherein a first bit of the number of flags indicate whether a cache entry corresponding to the request is storing data from a first or a second portion of the memory device and wherein a second bit of the number of flags indicate whether a cache entry corresponding to the request is storing data from a first, second, third, or fourth portion of the memory device.
10. An apparatus, comprising:
 - a controller; and
 - a memory device coupled to the controller via cache controller that includes a filter;wherein the controller is configured to receive a number of requests for data; and query the cache controller to determine whether the data corresponding to the number of requests for data is located in the cache; and
 - wherein the cache controller is configured to determine whether data corresponding to the number of requests for data is located in the cache based on a number of entries in the filter that identify a location of data stored in the memory device of a corresponding cache entry.
11. The apparatus of claim 10, wherein the number of requests for data include an indication of a location in the memory device where the data corresponding to a particular request is located.
12. The apparatus of claim 10, wherein the filter is SRAM on the cache controller and includes an entry for each cache entry of the cache used to

determine whether the cache is accessed to locate data corresponding to the number of requests for data.

13. The apparatus of any one of claims 10-12, wherein the number of flags identify a portion of the memory device that corresponds to the data stored in a particular cache entry.

14. A method, comprising:
receiving a request for data at a cache controller;
locating an entry in a filter on the cache controller based on information in the request;
determining that data associated with the request may be located in a cache based upon the information in the request matching a flag of the entry in the filter; and
determining that data associated with the request is not located in the cache based upon the information in the request not matching the entry in the filter.

15. The method of claim 14, wherein determining that data associated with the request may be located in the cache includes matching a portion of address information associated with the request with the flag of the entry in the filter that identifies a portion of the cache where data associated with the request may be located.

16. The method of claim 14, further including searching for the data associated with the request in the cache in response to determining that data associated with the request may be located in the cache.

17. The method of claim 14, wherein determining that data associated with the request is not located in the cache includes matching a portion of address information associated with the request with the flag of the entry in the filter.

18. The method of claim 14, wherein determining that data associated with the request is not located in the cache includes locating an indication in the entry that a cache entry associated with the request is invalid.

19. A method, comprising:
receiving a request for data at a cache controller; and
determining whether data associated with the request may be in a cache based on a flag in a filter on the cache controller, wherein the flag identifies a portion of a memory device where data of a corresponding cache entry is stored in the memory device.

20. The method of claim 19, further including servicing the request by querying the cache to determine if the data associated with the request is located in the cache.

21. The method of claim 19, further including servicing the request using the memory device and not querying the cache to determine if the data associated with the request is located in the cache.

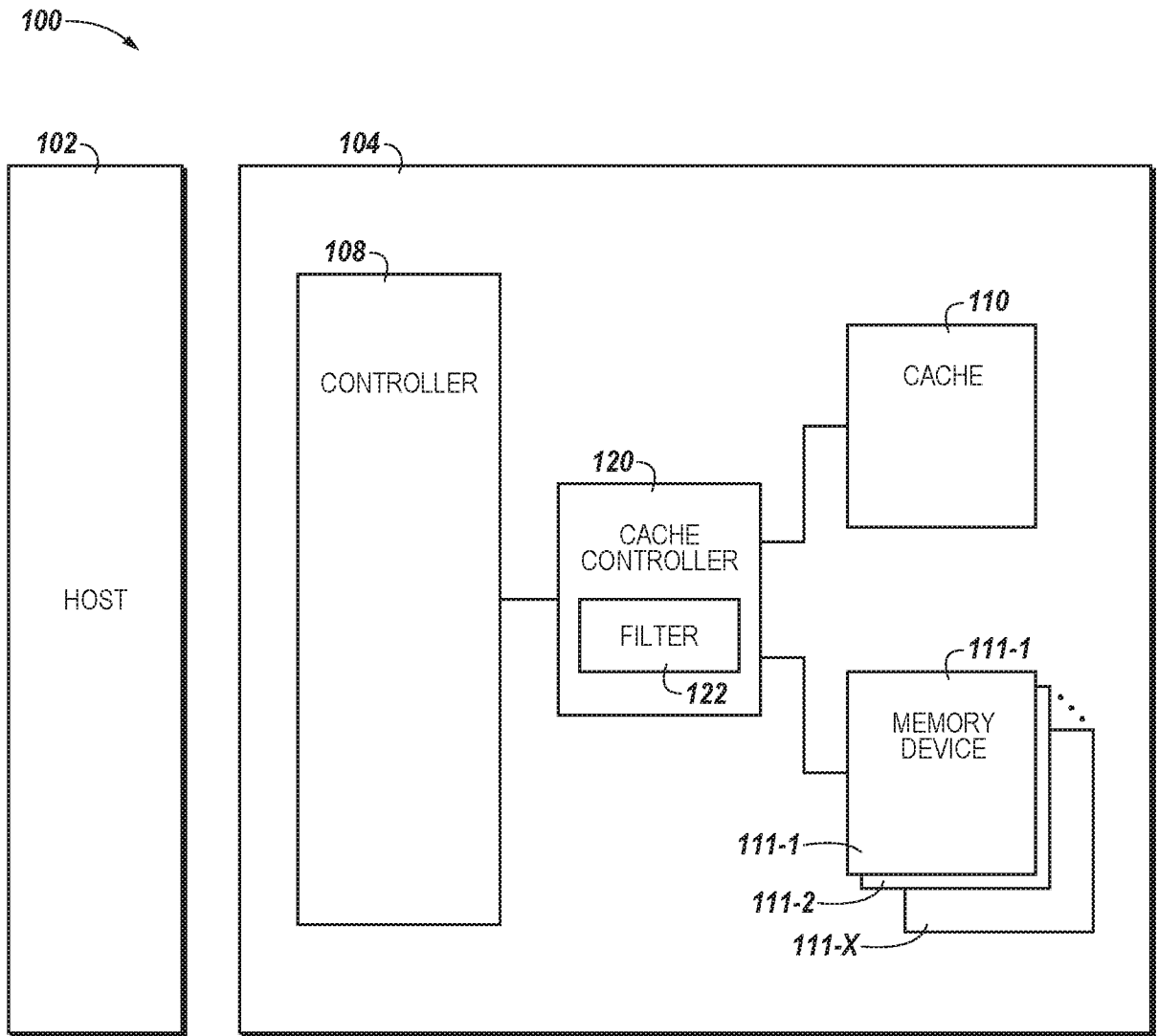


Fig. 1

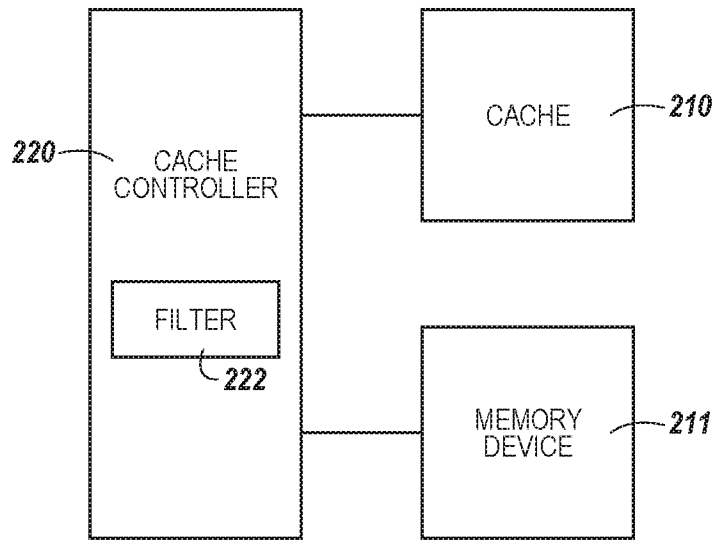


Fig. 2

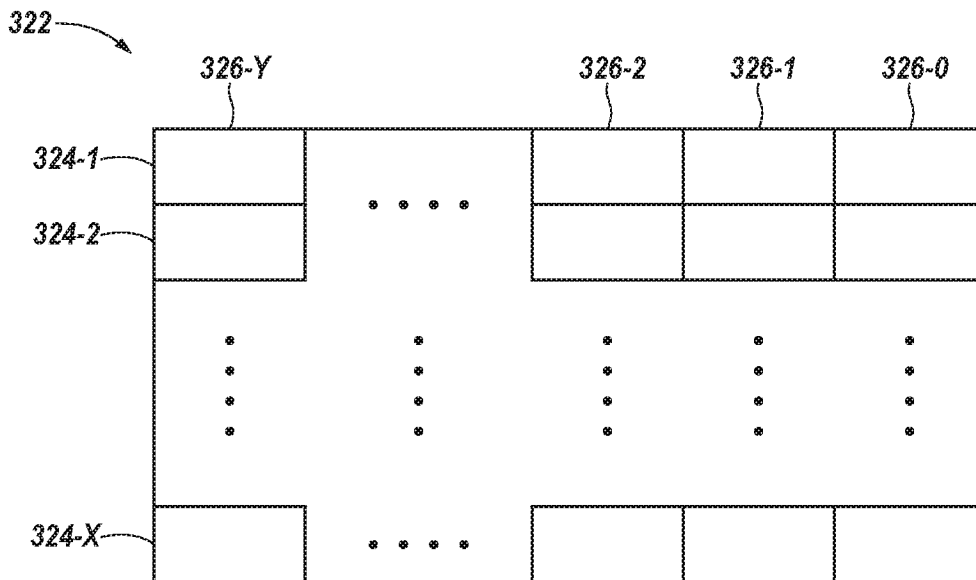


Fig. 3

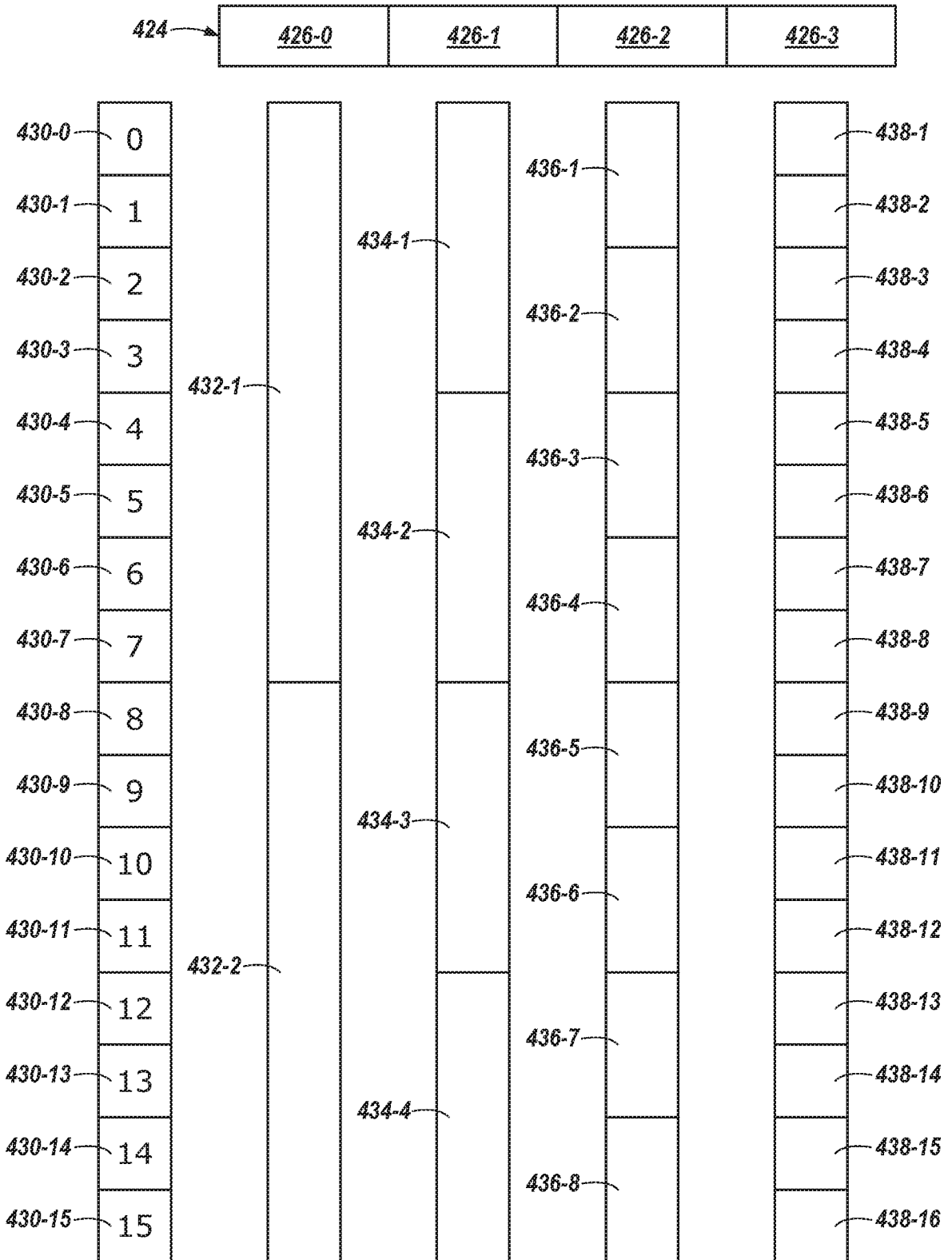


Fig. 4

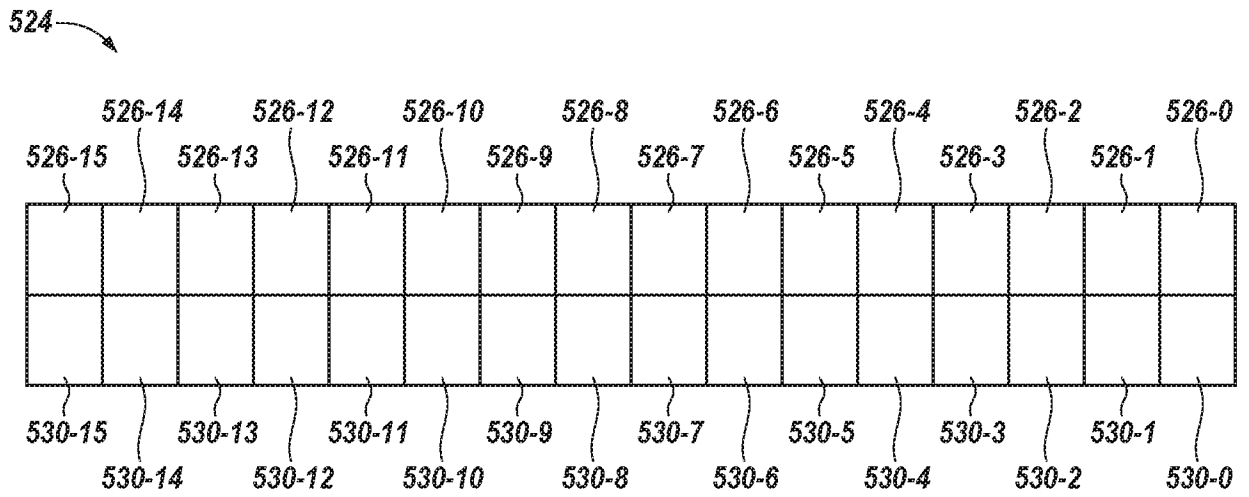


Fig. 5

A. CLASSIFICATION OF SUBJECT MATTER**G06F 12/0888(2016.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 12/0888; G06F 12/08; G06F 12/10; G06F 12/12; G06F 13/28; G06F 3/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: memory, cache, access, request, identify, filter, flag, address, hit, miss, determine

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013-0138894 A1 (GABRIEL H. LOH et al.) 30 May 2013 See paragraphs [0008]-[0010], [0034], [0040]-[0041], [0045]-[0052], [0062], [0071]-[0075], [0083]; and figure 8.	1-21
Y	US 2017-0097909 A1 (AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE, LTD.) 06 April 2017 See paragraphs [0027], [0047]; and figure 2.	1-21
A	US 2004-0148464 A1 (HO-RANG JANG) 29 July 2004 See paragraphs [0017], [0046]-[0047]; and figure 3.	1-21
A	US 2014-0173244 A1 (ADVANCED MICRO DEVICES, INC.) 19 June 2014 See paragraphs [0021], [0034]; and figure 1.	1-21
A	EP 2622485 B1 (ADVANCED MICRO DEVICES INC.) 26 October 2016 See paragraphs [0012], [0027]; and figure 1.	1-21

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/044726

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0138894 A1	30/05/2013	US 8868843 B2 WO 2013-081937 A1	21/10/2014 06/06/2013
US 2017-0097909 A1	06/04/2017	US 9910798 B2	06/03/2018
US 2004-0148464 A1	29/07/2004	DE 102004004248 A1 FR 2850179 A1 FR 2850179 B1 KR 10-0532417 B1 KR 10-2004-0067063 A	09/09/2004 23/07/2004 08/12/2006 30/11/2005 30/07/2004
US 2014-0173244 A1	19/06/2014	US 9104593 B2	11/08/2015
EP 2622485 B1	26/10/2016	CN 103221930 A CN 103221930 B EP 2622485 A1 JP 2013-542511 A JP 5913324 B2 KR 10-1731006 B1 KR 10-2013-0113440 A US 2012-0079205 A1 US 8478942 B2 WO 2012-047526 A1	24/07/2013 07/09/2016 07/08/2013 21/11/2013 27/04/2016 27/04/2017 15/10/2013 29/03/2012 02/07/2013 12/04/2012