PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :		(11) International Publication Number:	WO 99/26353
H04B 1/40, H03D 7/16	A1	(43) International Publication Date:	27 May 1999 (27.05.99)

(21) International Application Number: PCT/US98/23216

(22) International Filing Date: 3 November 1998 (03.11.98)

(30) Priority Data:

08/974,227	19 November 1997 (19.11.97)	US
09/042,554	17 March 1998 (17.03.98)	US

(71) Applicant: ERICSSON, INC. [US/US]; 7001 Development Drive, Research Triangle Park, NC 2709 (US).

(72) Inventors: SCHLANG, Jeffrey; 8301 Old Well Lane, Raleigh, NC 27615 (US). BEOSCH, Ron; 106 Fentress Court, Morrisville, NC 27560 (US). GORE, Charles; 5202 Brookstone Drive, Durham, NC 27713 (US). HADJICHRISTOS, Aristotle; 104 Northcote Drive, Apex, NC 27502 (US).

(74) Agents: GRUDZIECKI, Ronald, L. et al.; Burns, Doane, Swecker & Mathis, L.L.P., P.O. Box 1404, Alexandria, VA 22313–1404 (US).

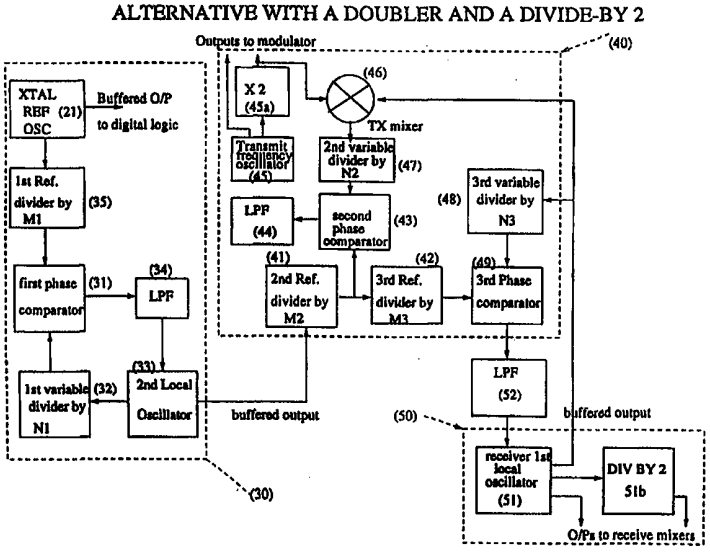
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: TRANSCEIVER ARCHITECTURE IN A DUAL BAND MOBILE PHONE



(57) Abstract

According to a second embodiment of the invention, a mobile phone receiver comprises a first down converter using a first local oscillator frequency which can be tuned in frequency steps by a programmable digital frequency synthesizer (PLL) which is locked to a reference frequency. The first down converter converts received signals to a first (IF) for filtering. A second down converter using a second local oscillator converts first (IF) signals to a second IF. The second local oscillator frequency is generated using a second digital frequency synthesizer (PLL) which locks the second oscillator to the reference frequency. A third down converter mixes the transmit frequency with the first local oscillator frequency to produce a lock frequency. A third digital frequency synthesizer (PLL) compares the lock frequency and the reference frequency to control generation of the transmit frequency.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

TRANSCEIVER ARCHITECTURE IN A DUAL BAND MOBILE PHONE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a Continuation-in-part of a U.S. Patent Application entitled "Simplified Reference Frequency Distribution in a Mobile Phone", filed November 19, 1997, in the names of Charles Gore, Rodney A. Dolman, and Paul W. Dent.

FIELD OF THE INVENTION

The invention relates to transceiver architecture in a mobile phone. More particularly, this invention relates to on-channel transceiver architecture in a dual band mobile phone.

BACKGROUND OF THE INVENTION

It is well known in the art of mobile radiotelephones to employ a receiver for receiving a receive frequency signal while a transmitter simultaneously transmits a transmit frequency signal in the other direction, the transmit frequency being separated from the receive frequency by a constant offset known as the duplex spacing.

Although the duplex spacing is nominally a constant, it can be a different constant depending on the frequency band in which the mobile phone is operating. Complications can then arise in constructing mobile phones that operate in more than one frequency band. Various approaches have been proposed for handling these complications.

One approach is to employ two separate and independent receiver-transmitter chains for each band of interest. This has the advantage of inherent redundancy for enhanced operation reliability and power control. However, the separate receiver-transmitter chains require extra space, resulting in a more

expensive and bulkier mobile phone product. As the market demand shifts toward smaller, less expensive phones with more embedded features, this approach becomes less suitable.

U.S. Patent Application Serial No. 08/795,930 entitled "Transmit Signal Generation with the Aid of Receiver" (Dolman) describes the use of the second local oscillator of the receiver as a reference frequency against which a transmit frequency is controlled relative to a receive frequency to achieve either a first or a second duplex spacing. The Dolman application is hereby incorporated by reference.

It is also known in the prior art, when packaging two synthesizer PLL circuits into a common integrated circuit, to synchronize or otherwise relate the reference dividers of the two PLLs so that their phase comparators do not mutually interfere. The Philips UM1005 and 8026 dual synthesizer integrated circuits available on the open market use this technique. These circuits include the use of fractional-N dividers and programmable loop bandwidth, such as described in U.S. Patents 5,095,288 and 5,180,993, which are hereby incorporated by reference. Novel ways to employ such synthesizers in dual mode satellite/cellular telephones in order to achieve different tuning step sizes in different frequency bands are described in U.S. Patent Nos. 5,535,432 and 5,610,559 which are also hereby incorporated by reference.

Another approach is to employ an offset voltage controlled oscillator (VCO) to mix up or down the receiver local oscillator frequency to generate the transmitter frequency. This approach is disclosed, for example, in commonly assigned U.S. Patent Applications No. 08/675,171 and 08/823,068.

U.S. Patent Application No. 08/675,171, entitled "Dual Band Transceiver", describes the use of common radio components for dual bands. Sharing a common receiver local oscillator synthesizer, transmitter offset oscillator loop, transmitter UHF VCO, IF filter, and receiver IF circuit greatly reduces the number of components for a dual band mobile phone. However, the

transmitter offset frequency is fixed for both bands. Thus, one band has to jog the main channel stepper to put the transmitter on frequency, i.e., one band has to change frequency for transmission. The band that must do the hop cannot, therefore, be used in full duplex mode, which is required for CDMA and multi-rate TDMA mobile phones.

U.S. Patent Application No. 08/823,068, entitled "Dual Band Mobile Station", also describes the sharing of similar common radio components between bands but enables duplex operation in both bands. However, as with all offset schemes, generation of the transmitter carrier is inherently troublesome because of the spurious performance of the transmitter. This is because mixing the synthesized VHF signal up with the receiver local oscillator frequency to the desired transmit band spawns up-conversion products which have to be filtered. These products may add a filtering burden to meet the transmitter output spectral mask requirements.

Continuous advances in electronics allow for smaller mobile phones complying with a variety of national and international protocols. The international mobile phone standard known as GSM in Europe and as PCS 1900 in the USA operates with a transmit/receive duplex spacing of 45MHz in the European 900MHz band; 95MHz in the European 1800MHz band, and 80MHz in the U.S. 1900MHz PCS band. The channel spacing is 200KHz (13MHz/65) and the transmitted symbol rate is 13MHz/48. All timing in this standard is related to a 13MHz clock, as is well known. The U.S. IS 136 system known as DAMPS operates with a 45MHz duplex spacing in the US 800MHz cellular band, and with an 80.4MHz duplex spacing in the U.S. 1900MHz PCS band, with a tuning step size of 30KHz and a transmitted symbol rate of 24.3 Kilosymbols/sec. In IS 136, as is well known, the tuning step sizes and symbol rates and internal timing are all derivable from a 19.44MHz clock. Yet another U.S. standard known as IS95 uses Code Division Multiple Access at a transmitted chip rate of 1228.8MHz, with a duplex spacing of 45MHz combined with tuning steps of 30KHz in the 800MHz

band, alternatively 50KHz steps combined with 80MHz duplex spacing in the 1900MHz band. In IS95, the chip rate and frequency step sizes are not easily derivable from the same crystal oscillator.

U.S. Patent No. 5,471,652 discloses an arrangement including a multiplier which permits the operating point of a VCO in a single band phone to be adjusted for various bands. This patent does not discuss application to a dual band phone. In addition, according to this patent, a synthesized VHF signal (80-400MHz) must be up-converted to the transmitter channel for digital (non-FM) operation. In the FM mode, the UHF oscillator is directly modulated and bled through the mixer.

It may be easily understood that combining two or more of the various abovementioned protocols in the same handheld unit is hindered by the variety of tuning step sizes, duplex spacings and symbol rates that must be synthesized. Consequently, there exists a need for an improved radio architecture to facilitate such combination.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a transceiver which supports full duplex operation in dual bands. It is a further object of the present invention to minimize the generation of spurs, thereby reducing the filtering design requirements of the transmitter. It is still a further objection of the present invention to provide a dual band transceiver that can accommodate multiple standards within the same handset.

According to a first embodiment of the invention, a mobile phone receiver comprises a first superheterodyne down conversion means using a first local oscillator frequency which can be tuned in frequency steps by a programmable digital frequency synthesizer phase lock loop (PLL). The first down conversion means converts received signals to a first intermediate frequency (IF) for filtering. A second down conversion means using a second local oscillator converts first IF signals to a second IF or to the complex baseband for further filtering and

processing. The second local oscillator is generated using a second digital frequency synthesizer PLL which locks the second oscillator to a crystal reference oscillator. The crystal reference oscillator provides a buffered clock output signal from which digital logic derives transmit symbol rates and receiver processing sampling rates.

According to a first aspect of the invention, the second local oscillator provides a buffered output signal at the second local oscillator frequency. The buffered output signal is used as the reference frequency for the first local oscillator's synthesizer PLL, thus eliminating the need to distribute the crystal oscillator signal to the first oscillator's PLL circuit. According to a second aspect of the invention, the first oscillator PLL comprises a phase comparator to compare the divided down first local oscillator signal with the divided down reference frequency signal from the second local oscillator, the divided down frequencies being equal to the desired receiver frequency tuning steps or a multiple thereof. It should be appreciated that this frequency would not have been available by dividing down the crystal frequency in an integral ratio without practicing this aspect of the invention.

According to a third aspect of the invention, a third digital frequency synthesizer PLL controls the transmitter frequency to be equal to the first local oscillator frequency plus or minus a transmit offset frequency. The transmit frequency can for example be heterodyned with the first local oscillator frequency to produce a transmit offset frequency signal; the transmit offset frequency signal is then divided down in a digital divider and compared with a phase reference frequency which is also derived by dividing the second local oscillator frequency by an integer factor.

Since according to the third aspect of the invention, the transmit offset synthesizer PLL and the first local oscillator PLL both utilize the second local oscillator as a common frequency reference, they can furthermore be packaged in a common integrated circuit and can share at least part of the reference divider

which divides the second local oscillator frequency to produce a first and second phase comparator reference frequency signal for the two PLLs respectively. The two PLLs' respective phase comparators are arranged to respond to opposite polarities of a signal at a lowest common multiple frequency of their respective first and second phase comparator reference signals in order to minimize mutual interference between the two PLLs.

According to a second embodiment of the invention, a mobile phone receiver comprises a first down conversion means using a first local oscillator frequency which can be tuned in frequency steps by a digital frequency synthesizer PLL which is locked to a reference frequency. The first down conversion means converts received signals to a first IF for filtering. A second down conversion means using a second local oscillator converts first IF signals to a second IF. The second local oscillator frequency is generated using a second digital frequency synthesizer PLL which locks the second oscillator to the reference frequency. A third down conversion means mixes the transmit frequency with the first local oscillator frequency to produce a lock frequency. A third digital frequency synthesizer PLL compares the lock frequency and the reference frequency to control generation of the transmit frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood upon reading the following description with reference to the accompanying drawings, in which:

FIG. 1 illustrates prior art reference frequency distribution;

FIG. 2 illustrates another prior art scheme;

FIG. 3 illustrates the improved system described in the incorporated Dolman reference;

FIG. 4 illustrates a reference distribution scheme according to a first embodiment;

FIG. 5 illustrates more detail of the inventive frequency synthesis scheme according to the first embodiment;

FIG. 6 illustrates an inventive dual band scheme using frequency doublers according to the first embodiment;

FIG. 7 illustrates an inventive dual band scheme using frequency halvers according to the first embodiment;

FIG. 8 illustrates an inventive scheme using one frequency halver and one frequency doubler according to the first embodiment;

FIG. 9 illustrates an inventive scheme in which the frequency halver and the frequency doubler are switched in position according to the first embodiment;

FIG. 10 illustrates an inventive scheme in which a frequency doubler can be powered down for AMPS reception according to the first embodiment;

FIG. 11 is a modification of figure 10, using frequency halvers;

FIG. 12 illustrates an alternative reference frequency distribution for dual-mode radios according to the first embodiment;

FIG. 13 illustrates divider ratios for the dual-mode radio of FIG. 12;

FIG. 14 illustrates a dual-mode radio using I.F. Homodyne for a PCS1900 mode according to the first embodiment;

FIG. 15 illustrates a dual-mode radio using a single crystal according to the first embodiment;

FIG. 16 illustrates divider ratios for the dual-mode radio of FIG. 15;

FIG. 17 illustrates a dual-mode radio using two reference crystals according to the first embodiment;

FIG. 18 illustrates divider ratios for the dual-mode radio of FIG. 17;

FIG. 19 illustrates divider ratios to eliminate the second crystal of FIG. 17;

FIG. 20 illustrates a skip-counter for generating 194.4KHz from 19.5MHz according to the first embodiment;

FIG. 21 illustrates a dual band scheme according to a second embodiment of the present invention;

FIG. 22 illustrates more detail of the inventive dual band scheme using a filter according to the second embodiment;

FIG. 23 illustrates an inventive dual band scheme using narrow band modulators according to the second embodiment;

FIG. 24 illustrates an inventive dual band scheme using a frequency divider according to the second embodiment;

FIG. 25 illustrates an inventive dual band scheme using various frequency multipliers/dividers according to the second embodiment; and

FIG. 26 illustrates an inventive dual band scheme using an alternative arrangement of variable gain amplifiers according to the second embodiment.

DETAILED DESCRIPTION

Referring now to FIG. 1, a prior art cellular phone comprises an antenna (10) connected to a receiver and a transmitter by means of a transmit/receive duplexor (11). When simultaneous transmit and receive (frequency duplex) is used, as in the analog FM AMPS standard or the IS95 CDMA standard, the duplexor (11) is a duplexing filter. Alternatively, for a TDMA system such as GSM/PCS1900 or D-AMPS/IS136 that employs time-duplex, the duplexor can be a T/R switch. For dual band phones employing frequency duplex in one band and time duplex in another band, duplexor (11) can be a dual-band duplexor having both a switch and a duplexing filter. When frequency duplex is used in both bands, duplexor (11) could comprise duplexing filters for both bands, and when time duplex is used in both bands, a single T/R switch might serve for both bands.

The duplexor allows the transmitter to be connected to the antenna without affecting receiver sensitivity. The receiver comprises a low noise amplifier and downconvertor known as "the front end", (12). The front end can be fabricated in a single integrated circuit comprising a low-noise amplifier, a downconverting and possibly image-rejecting mixer and a first local oscillator, for each of two or more different frequency bands (such as the 800MHz and 1900MHz bands).

The first local oscillator mixes with the desired receive frequency signal to produce a first intermediate frequency signal. Filtering can take place with a fixed frequency bandpass filter, IF filter (15). The desired receive frequency is selected by tuning the local oscillator to a frequency equal to the sum or the difference of the desired receive frequency and the first IF, by means of first local oscillator synthesizer phase lock loop (14). The 1st LO PLL tunes the 1st LO to a programmable integer multiple of a basic tuning step size, which is derived from a crystal reference oscillator (21) by dividing the crystal frequency by another integer to get the step size. For small step sizes, the synthesizer may alternatively derive a greater step size from crystal oscillator (21) by dividing by a smaller integer, and then interpolate between these larger steps to get the desired smaller steps using the technique of fractional-N synthesis described in the above-incorporated references. First LO PLL circuit (14) compares the 1st LO frequency to the crystal reference signal and generates an error signal. The error signal is filtered and integrated in Loop Filter (24) to produce a control signal to control the oscillator frequency until the frequency is exactly as intended.

The receiver amplifies the filtered 1st IF signal and then customarily performs a second frequency down conversion using a second heterodyne mixer and second local oscillator. The IF amplifiers, second local oscillator and second mixer are all contained in a conventional second integrated circuit (16). After downconverting a second time to a second or final Intermediate frequency, further amplification may take place at the final IF and a detector circuit can be employed to produce a Radio Signal Strength Indication (RSSI) related to the strength of the received signal. The second IF amplifier may be hardlimiting, and then outputs a hardlimited final IF signal to digital signal processing (20) where phase information is extracted and digitized using the second IF signal simultaneously with digitizing the RSSI signal, as described in U.S. Patent No. 5,048,059 entitled "Log-polar signal processing", which is hereby incorporated by reference herein. The second local oscillator part of IF amplifier circuit (16) is also controlled to the

desired frequency by means of a synthesizer PLL circuit (17) and loop filter (23). The 2nd LO frequency is compared with the crystal oscillator (21) and an error signal produced as before. Thus both synthesizer circuits (14) and (17) use the crystal as the frequency reference or standard of accuracy for controlling both the first and second LO. The digital signal processing logic (20) can also require an accurate frequency standard for producing receiver sampling and processing rates and transmit symbol rates, and so is also fed with an output from crystal oscillator (21).

The transmitter comprises transmit frequency generation circuit (19) for producing a signal offset from the receive frequency by the fixed duplex spacing. The transmit frequency is thus offset from the 1st LO frequency by the duplex spacing combined with the first intermediate frequency, which nevertheless is still a constant offset. The constant transmit offset is either equal to the first IF minus the duplex spacing or the first IF plus the duplex spacing, depending on whether the 1st LO is lower or higher than the receive and transmit frequencies.

The transmit frequency signal is then modulated with information from digital signal processor (20) using modulator (18), which is for example a quadrature modulator having I and Q input signals. The modulated signal is then amplified to a transmit power level using power amplifier (13), which may be a dual-band power amplifier in a dual-band phone.

Transmit offset PLL forms the difference between the transmit and 1st LO frequencies and tests to see if it equals the desired offset, by comparing the offset with the crystal reference. The TX offset PLL thus also has need of a crystal reference frequency signal from oscillator (21), making four places to which the oscillator signals must be distributed.

The four separate outputs from oscillator (21) must be sufficiently isolated from one another by buffer amplifiers and conditioned to drive copper tracks on the printed circuit motherboard. This consumes battery power and presents a radiated interference hazard. Often, to save battery power during standby, outputs

which are momentarily not required, such as that feeding the transmit offset PLL, may be turned off by control signals from a control processor (part of digital signal processing 20), which is a further complication. It is thus desirable to reduce the distribution of the crystal reference signal by means of printed circuit board tracks to multiple destinations.

A first step in this direction is already taken in prior art products sold by Ericsson in the USA. By combining the first and second LO PLLs in a single chip, such as the Philips UM1005 or 8026 part, a single input for the crystal reference may be used, since both use the crystal as the reference. Further, by combining crystal oscillator (21) into a transmit signal generator chip together with TX offset PLL and modulator (18), no external output connection between oscillator (21) and offset PLL (19) is needed.

Thus, referring to FIG. 2, the number of crystal reference signal outputs required is reduced to two, one feeding dual synthesizer circuit (14+17) and the other feeding digital signal processing (20).

In U.S. patent application Serial No. 08/795,930 to Dolman, incorporated above, it is explained that all PLLs desirably operate by dividing the crystal reference frequency by the smallest possible integer for comparison with the frequency of the oscillator they are controlling, which is also divided by the smallest possible integer. Expressing this another way, it is desired to have the largest possible common factors between the controlled oscillator frequencies and the reference frequency. Dolman discloses that this is facilitated when the transmit offset frequency is generated using the 2nd LO as the reference frequency rather than the crystal (22). Dolman's inventive arrangement is shown in FIG. 3.

The second LO provides a first output signal to its controlling PLL (17) and a second output to TX offset PLL (19). Since the crystal oscillator is now not used for any purpose in transmit circuits (18,19) oscillator (21) is shown once more as a separate circuit (21), having two buffered outputs. The total number of radio frequency signal outputs has however increased, as has the number of

separate integrated circuit chips. The radio frequency signals distributed on the printed circuit board are as follows:

1) 1st LO signal from frontend (12) to PLL (14);
2) 1st LO signal from frontend (12) to TX offset PLL (19);
3) Crystal reference frequency from oscillator (21) to PLL (14+17);
4) Crystal reference frequency from oscillator (21) to processing (20);
5) 2nd LO from IF chip (16) to controlling PLL (17); and
6) 2nd LO from IF chip (16) to TX offset PLL (19).

It is an object of the current invention to reduce the number of RF distribution tracks from the six enumerated above.

FIG. 4 shows one implementation of the invention. The two places to which the 1st LO signal is routed, that is the first LO PLL (14) and the TX offset PLL (19) are colocated with modulator circuit (18) in first (transmit) integrated circuit. Thus there is only a single 1st LO output connection from front end chip (12) to transmit chip (14,18,19).

However, when two synthesizer PLLs are colocated on the same chip, they should produce output pulses at different times. This is difficult or impossible to arrange if the two phase comparators have independent reference frequency sources, such as when the second LO is used for the TX offset PLL reference and the crystal is used as the first LO reference. Therefore, according to this invention the second LO is also used as the reference for the first LO synthesizer PLL. Moreover, as will be shown below, there are numerical advantages in using the second LO as the reference source for the first LO, particularly when it is desired to construct dual-band/dual-mode radios. Thus, a single reference input from 2nd LO part of IF chip (16) is provided for both PLLs (14) and (19).

Crystal oscillator circuit (21) is now combined with 2nd LO PLL and IF circuit (16) so that the reference signal from oscillator (21) to PLL (17) is an internal connection only. Likewise, the 2nd LO signal to its controlling PLL (17)

is an internal signal only. The only remaining external signal is from reference oscillator (21) to digital processing (20).

The radio frequency oscillator signal distribution has now been reduced to the following signals:

1) 1st LO signal from frontend (12) to PLLs (14 & 19);

2) Crystal reference frequency from oscillator (21) to processing (20); and

3) 2nd LO from IF chip (16) to TX offset PLLs (14 & 19).

It would have been equally conceivable to place crystal oscillator (21) into digital processing chip (20), however, the oscillator (21) is more logically associated with other analog/RF circuits that use the same integrated circuit fabrication processes, and is therefore envisioned to be preferably integrated with IF chip (16,17,21). It is possible that in some applications a Very High Frequency (VHF) crystal, such as an overtone crystal, could be used directly to control the frequency of the second local oscillator without the use of a digital frequency synthesizer PLL circuit; however, VHF overtone crystals are more difficult to adjust to a desired oscillation frequency than fundamental-mode crystals, so a fundamental-mode crystal reference oscillator with a digital PLL is preferred.

FIG. 5 gives more details of the reference frequency distribution and frequency synthesis arrangements according to the inventive block diagram of FIG. 4.

The basic source of an accurate frequency reference in the apparatus is quartz crystal resonator (22) of FIGs. 1-4, connected to oscillator circuit (21). Even a quartz crystal cannot provide the necessary accuracy required for cellular phones operating in the 2GHz region of the radio spectrum, and therefore means contained within digital processing (20) determine the receiver frequency error relative to signals received from land-based network stations or satellite relays, which error is ascribed to crystal (22), and an adjusting signal is sent to frequency

adjustment components (such as a varactor diode for example) connected to crystal (22) so as to annul the error.

In FIG. 5, the oscillator circuit (21) is incorporated in IF chip (30) along with second local oscillator (33) and its control PLL comprising reference divider (35), first variable divider (32), phase comparator (31) and loop filter (34). The crystal oscillator signal is divided in frequency by counter/divider (35) which divides by a first integer Ml to produce a phase comparison frequency $F_{ref}/M1$, where F_{ref} is the crystal frequency. The second local oscillator signal is divided in frequency by an integer Nl in first variable divider (32), to produce a second phase comparison signal, which is compared with the phase comparison frequency signal from divide-by-M1 circuit (35) to produce a phase and frequency error signal from first phase comparator (31). The phase error signal is filtered and integrated using loop filter (34) to produce a frequency control signal to 2nd local oscillator (33) free of comparison frequency ripple. The higher the comparison frequency from divider (35), the easier it is for loop filter (34) to eliminate this unwanted ripple while otherwise maintaining a fast speed of response to correct unwanted fluctuations of the 2nd LO's frequency due to noise or vibration, for example. Therefore an objective of the invention is to obtain a high comparison frequency, that is a low reference divide ratio M1. The second local oscillator frequency is thus accurately controlled to equal $F_{ref}.N1/M1$.

According to Dolman's prior invention and the current invention, a buffered second local oscillator signal is output from 2nd LO (33) to be used as a reference for other frequency generation, in particular the transmit offset frequency (according to Dolman's prior application referenced above) and now also the first local oscillator frequency according to this invention. Since both the TX offset and 1st LO synthesizer PLL circuits are to be colocated in transmit signal generation chip (40) in order to reduce distribution of the second LO signal to a single cross-board connection, it is desirable that the phase comparators of the respective PLLs should pulse at different times separated as far as possible within

some longest common period. This ensures that when one charge-pump phase comparator receives a current pulse from the supply, the other charge pump is in its tristate, that is, a high impedance state or open circuit output, with no current flowing to its respective loop filter. This minimizes the risk of interference from one charge pump to the other. The design and operation of charge pump phase detectors is described more fully in above-incorporated U.S. Patent No. 5,095,288.

In order to provide the preferred out-of-phase relationship between the charge pumps (43,49), internal frequency plans are sought in which the phase comparison frequency for the TX offset loop is an integer multiple M3 of the phase comparison frequency for the first LO. Since the second LO frequency is also, according to Dolman's incorporated application, an integer M2 times the TX offset reference, the first LO comparison frequency must now be related to the second LO frequency divided by M2.M3.

Thus the second LO frequency signal is input from IF chip (30) to TX chip (40) and divided by integer M2 in a second reference divider (41) to obtain the phase reference to TX offset phase comparator (43) according to Dolman as

$$F_{LO2}/M2 = F_{ref}.N1/(M1.M2)$$

This frequency is then further divided in third reference divider (42) by integer M3 in order to obtain the phase comparison frequency for first LO phase comparator (49). Moreover, divider M3 and phase comparator (43) are arranged to respond to opposite edges of the output of divider M2, for example one responding to a rising edge (low voltage or '0' state transitioning to high voltage or '1' state) while the other responds to a falling edge (1 to 0 transition). This ensures that they respond one half cycle apart in time of their lowest common multiple frequency at the output of divider (41).

The phase comparison rate for charge pump phase comparator (49) is thus

$$F_{ref}.N1/(M1.M2.M3).$$

This frequency is compared with the 1st LO frequency from first LO (51) divided down by a factor N3 in third variable divider (48), to produce a frequency and phase error signal from comparator (49) which is filtered in loop filter (52) to obtain a feedback control signal to control oscillator (51) to the desired 1st LO frequency

$$F_{ref}.N3.N1/(M1.M2.M3)$$

Preferably, N3 is not an integer factor but comprises a whole part and a fractional part, the components (48,49 and 52) of the first LO PLL forming a fractional-N synthesizer according to above-incorporated Patent No. 5,180,993. Optionally, both M3 and N3 can be varied in a pattern generated by a fractional-(N,M) controller according to U.S. patent application no. _____entitled "Frequency Synthesis by Sequential Fraction Approximations" (Dent, filed _____) which is hereby incorporated by reference. Both the fractional-N and the fractional-(N,M) techniques have the desirable effect of allowing the 1st LO phase comparison frequency to be higher than the desired tuning step size, thus making it easier for the loop filter (52) to filter out unwanted comparison frequency ripple while otherwise maintaining a fast control loop response to correct errors.

The transmitter frequency signal, when transmission is required, is generated by transmit frequency oscillator (45). A transmit frequency signal from oscillator (45) is mixed in TX mixer (46) with a first LO signal from first LO (51). The first LO signal preferably comes from receive chip (12) via a single cross board connection to minimize RF tracks. A single cross board connection for any of the interchip signals mentioned can nevertheless be a balanced connection comprising two tracks driven in antiphase, as balanced connections to and from RF chips at high frequencies reduce unwanted stray coupling and radiation effects.

TX mixer (46) mixes the transmit frequency and the 1st LO frequency to produce a difference frequency signal at the TX offset frequency F_{txoff}. The difference frequency signal output from mixer (46) may be low-pass filtered to

ensure the original, higher input frequencies are removed, and then drives second variable divider (47) which divides by a factor N2. The output signal at frequency $F_{txoff}/N2$ is then compared in second phase comparator (43) with the phase reference from divider (41) to produce a frequency and phase error signal. The error signal from comparator (43) is filtered and integrated in loop filter (44) to produce a control signal which controls TX oscillator (45) until the desired TX-offset frequency is accurately achieved. Thus the TX offset frequency is given by

$$F_{txoff}/N2 = F_{ref}.N1/(M1.M2), \text{ or } F_{txoff} = F_{ref}.N2.N1/(M2.M1)$$

It is possible for the TX offset PLL comprising components (41,43,44,45,46,47) also to be a fractional-N synthesizer, however fractional-N synthesizers are more complex than integer synthesizers and thus it is desired to avoid having more than one in the apparatus. Thus, factor N2 is preferably an integer.

Obtaining the highest possible phase comparison frequencies for phase comparators (31,43,49) is rarely a problem in single-band radios having a single duplex spacing between transmit and receive frequency channels. It is more difficult first in the context of two-band radios that must operate with more than one duplex spacing. Therefore two-band radio designs according to the invention will now be described with the aid of FIGs. 6,7,8 and 9.

A two-band radio according to FIG. 6 would comprise a transmit frequency oscillator (45) for generating transmit frequencies in the lower of the two possible transmit frequency bands, A frequency doubler (45a) is then used to double the frequency when operation in the higher of the two frequency bands is desired, the lower and higher bands being approximately one octave apart. An output from the oscillator (45) directly is used to drive the modulator when lower-band operation is required while an output from the doubler (45a) is used when operation at the higher band is desired. However, as indicated in FIG. 6, the lower frequency direct from oscillator (45) enters TX mixer (46).

Likewise, first local oscillator (51) operates on a frequency adapted to the lower of the two-possible receive frequency bands to convert received signals to

the desired first Intermediate Frequency; the signal from first LO (51) is doubled in frequency using doubler (51a) when operation in the higher of the two receive frequency bands is desired, the LO frequency for the higher band being approximately an octave higher than that for the lower band. This approximation can be manipulated to be a close approximation by suitable choice of the first Intermediate frequency and by suitable choice of either high-side or low-side mixing in front-end chip (12).

For example, for low-band receive operation, we have

$F_{lo1}(lo) = F_{rx}(lo) + F_{if1}$ for high-side mixing or

$F_{lo1}(lo) = F_{rx}(lo) - F_{if1}$ for low side mixing, where

$F_{lo1}(lo)$ is the low-band first LO frequency,

$F_{rx}(lo)$ is the low-band receive channel frequency and

F_{if1} is the chosen first intermediate frequency.

Likewise $F_{lo1}(hi) = F_{rx}(hi) + F_{if1}$ for high-side mixing or

$F_{lo1}(hi) = F_{rx}(hi) - F_{if1}$ for low side mixing, where

$F_{lo1}(hi)$ is the high-band first LO frequency,

$F_{rx}(hi)$ is the high-band receive channel frequency and

F_{if1} is the same chosen first intermediate frequency as for low-band.

Thus, for $F_{lo1}(hi)$ to be twice $F_{lo1}(lo)$, we have

$$F_{rx}(hi) \pm F_{if1} = 2 (F_{rx}(lo) \pm F_{if1})$$

giving $F_{if1} = F_{rx}(hi) - 2F_{rx}(lo)$ (for both optional signs '+') ....(1)

or $F_{if1} = (F_{rx}(hi) - F_{rx}(lo))/3$ ('-' in high band and 1+1 in low)..(2)

or $F_{if1} = 2F_{rx}(lo) - F_{rx}(hi)$ (for both optional signs

or $F_{if1} = (2F_{rx}(lo) - F_{rx}(hi))/3$ ('+' in high band and 1-1 in low)

The latter two equations give negative results which is impossible. A possible alternative is to make the first Lo range at high band triple the first LO range at low band, giving

$F_{if1} = (3F_{rx}(lo) - F_{rx}(hi))/2$ (for both optional signs '-') ....(3)

$F_{if1} = (3F_{rx}(lo) - F_{rx}(hi))/4$ (for '+' in high band and in low) ....(4)

Examples of preferred internal frequency plans for a radio according to FIGs. 4 and 5, operating according to the IS54 "D-AMPS" single-band standard, will now be described. A search of frequency plans giving the highest possible phase comparison frequencies at phase comparators (31,43 and 49) yielded, among others, the results:

1ST IF	2ND LO	TXOFFSET	M1	N1	M2	N2	M3	1ST LO	FRAC-N	MODULUS
101.64	101.52	146.64	9	47	9	13	47		8	

The above results provide phase comparison frequencies of

$F_{xtal}/M1 = 19.44/9 = 2.16MHz$ for 2nd LO phase comparator (31);

$F_{lo2}/M2 = 101.52/9 = 11.28MHz$ for TX offset phase comparator (43), and

$F_{lo2}/(M2.M3) = 11.28/47 = 240KHz$ for 1st LO phase comparator (49).

The first LO tuning steps are reduced from the above 240KHz to 30KHz by employing a fractional-N divider for N3 giving steps of 1/8th, i.e. the fractional-N modulus is 8.

The above solution provides a high TX offset phase comparison frequency of 11.28MHz. Other criteria might be to obtain the highest 2nd LO phase comparison frequency. An alternative result for which the 2nd LO is just a harmonic of the crystal is for example:

1ST IF	2ND LO	TXOFFSET	M1	N1	M2	N2	M3	1ST LO	FRAC-N	MODULUS
116.76	116.64	161.76	1	6	243	337	1		16	

The above values result in a 2nd LO phase comparison frequency of 19.44MHz at phase comparator (33), and divider (35) is not necessary because M1=1. The transmit offset and first LO phase comparators (43,49) both operate at 480KHz, and divider (42) may be omitted as M3=1. The first LO tuning steps are reduced from 480KHz to 30KHz by employing a modulus 16 fractional-N divider (48) allowing N3 to be varied in steps of 1/16th.

Attention is now turned to dual-band radios with internal frequency reference distribution according to FIG. 6. The above two exemplary solutions were illustrated because they are also compatible with a dual-band radio operating according to the dual-band D-AMPS standard IS136. Solutions for dual-band radios are given in the tables below for cases where the first local oscillator is on the high side for 800MHz hand operation and on the low side for 1900MHz band operation, and the second IF is fixed at 120KHz.

Table 1 illustrates solutions in which the 2nd LO is a harmonic of the crystal, that is the second LO has the highest possible phase comparison frequency, Ml being equal to unity.

TABLE 1: Dual band 800(1900) solutions with 2nd LO a crystal harmonic

1st IF	2nd LO	TX OFFSET	M1	N1	M2	N2	M3	1st LO modulus
116.76	116.64	161.76(36.72)	1	6	243(54)	337(17)	1 (9 or 3)	16 (8 or 24)
155.64	155.52	200.64(75.6)	1	8	162(72)	209(35)	1 (9 or 3)	32 (8 or 24)
194.52	194.4	239.52(114.48)	1	10	405(90)	499(53)	1 (9 or 3)	16 (8 or 24)
233.4	1233.28	278.4(153.36)	1	12	243(108)	290(71)	1 (9 or 3)	32 (8 or 24)

When using the figures in table 1 above to determine the phase detector comparison frequencies for TX offset phase comparator (43), it must be taken into

account that the arrangement in FIG. 6 controls the TX oscillator (S1) frequency BEFORE doubling to 1900MHz in doubler (51a).

Therefore, phase comparator (43) must operate at half the frequency provided by divider (41) and the indicated value of M2.

Thus, either phase comparator (43) must contain a further divide by two circuit to halve the frequency from divider (41) when operating in the 1900MHz band, or else the value of M2 for 1900MHz must be doubled.

In the latter case, the value of M3 for 1900MHz operation must be halved (which is impossible as M3 is always odd at 1900MHz), or else the fractional modulus for 1900MHz operation must be halved. The latter is preferable and so the preferred fractional-modulus at 1900 MHZ is 4 or 12 combined with an M2 value double that shown in table 1 for 1900MHz operation. The TX offset phase comparison frequency at phase comparator (43) is thus 1080KHz for 1900MHz operation and not 2160KHz as would be obtained by dividing the second LO frequency in table 1 by the indicated values of M2.

Furthermore, note that in FIG. 6 it is always the doubled frequency from doubler (S1a) that is fed to fractional-N first-LO synthesizer loop beginning with variable divider (48) for N3. Since the frequency used for the receiver mixer during 800MHz band operation is half of the synthesized frequency, the synthesizer need only provide 60KHz steps in order to tune the receiver in 30KHz steps. Thus the fractional-N modulus shown in table 1 for 800MHz operation may be halved.

It may be desirable to operate in both bands using the same fractional-N modulus, and this may always be accomplished by use of a modulus which is the lowest common multiple of the 800MHz and 1900MHz moduli, accepting that the frequency steps in one or both bands may then be finer than needed, it being acceptable to exceed the required frequency resolution.

The above issues are one motivation for considering frequency halving circuits (45b,S1b) in FIG. 7 as opposed to frequency doubling circuits (45a,51a)

of FIG. 6. Another motivation is that phase noise is doubled by frequency doubling circuits but halved by frequency halving circuits. Thus there is an expectation of lower unwanted phase noise and ripple when using frequency halving circuits. Yet another motivation is that a frequency doubling circuit requires a filter to remove unwanted leakage of the fundamental, as well as other unwanted higher harmonics; the output of a frequency divide-by-2 circuit is however relatively free of other unwanted spectral components.

Referring now to FIG. 7, it is seen that it is the non-divided output of oscillator (Sl) which is fed to the TX offset synthesizer loop beginning with mixer (46). Therefore the phase comparator for 800MHz band operation must operate at double the frequency implied by table 1, i.e. the value of M2 must be halved, alternatively the value of N2 must be double that shown in table 1 for 800MHz operation. The former is not possible for cases where M2 is odd, but is possible when the first IF is 155.64MHz and M2 = 162. Thus, when table 1 is applied to FIG. 7, the values of N2 for 800MHz should be doubled except in the case of first IF = 155.64MHz, in which case a better option is to halve M2 to 81; then it is necessary to double the value of M3 (to two) for 800MHz operation in order to maintain the same 1st LO phase comparison frequency at phase comparator (49), alternatively to increase the fractional-N modulus from 32 to 64. On the other hand, since the frequency of oscillator (51) is halved before use in the receiver for 800MHz operation, it is sufficient that oscillator (51) be tuned in 60KHz steps, allowing the fractional-N modulus to be halved again back to 32.

The above considerations with respect to FIG. 7 also apply to the arrangement of FIGs. 8 and 9, in which the TX frequency signal and the first LO are always controlled at the higher frequency and halved for 800MHz use.

In choosing between the implementations of FIGs. 6,7,8 and 9, another motivation is power consumption. In FIG. 6, the x2 circuit 51a must be powered up during 800MHz band receive operation, which has most impact on standby time before the battery must be replenished. Still, the x2 circuit 45a need only be

powered up for 1900MHz transmission, thus saving power in 800MHz band transmission. In FIG. 7, divider 51b need only be powered up for 800MHz reception, and may be powered down for 1900MHz reception. Divide by 2 circuit 45b likewise need only be powered up for 800MHz transmission and is not needed for 1900MHz transmission.

In FIG. 8, x2 circuit 45a must be powered up for transmission in either frequency band, but this is of little consequence as the power amplifier (13) dominates transmit power consumption. Divide by 2 circuit 51b may be powered down during 1900MHz receive. In FIGs. 6 and 9, x2 circuit 51a must always be powered up for reception in either frequency band. Therefore this is not as desirable for standby battery life at 1900MHz as FIGs. 7 or 8.

1900MHz D-AMPS operation uses TDMA, which affords much longer standby times due to a low receive duty factor. 800MHz operation however includes the analog FM AMPS mode, in which receive standby duty factor is longer. The 800MHz AMPS operation is therefore the limiting factor for battery life and we are therefore led to consider FIG. 10, in which the first LO is always controlled at the lower frequency, allowing doubler 51A to be powered down during 800MHz reception.

Referring to FIG. 10, the first LO is always controlled at the lower frequency, i.e. before doubling. This allows doubler 51a to be powered down in 800MHz operation. A disadvantage, however, is that the oscillator 51 must be tuned in 15KHz steps in order to provide 30KHz steps at 1900MHz, requiring the fractional-N modulus to be doubled, which is undesirable. Taking into account that a divide-by-2 circuit in present semiconductor technology consumes very little power, and likely less than a frequency doubler circuit, together with the other advantages outlined above for frequency halving rather than frequency doubling, FIG. 7 is likely to be the best practical implementation.

The above Table 1 listed solutions for which the second LO was a harmonic of the crystal, giving the lowest value of unity for divider (35). Table 2

lists solutions in which 2nd LO phase comparator (31) operates at 6.48MHz, which is the crystal frequency divided by 3 (M1=3).

TABLE 2: Dual band 800(1900) with 2nd LO a multiple of crystal/3

1st IF	2nd LO	TX OFFSET	M1	N1	M2	N2	M3	1st LO modulus
90.84	90.72	135.84(10.8)	3	14	189(42)	283(5)	1 (9 or 3)	16 (8 or 24)
103.8	103.68	148.8(23.76)	3	16	108(48)	155(11)	1 (9 or 3)	32 (7 or 24)
129.72	129.6	174.72(49.68)	3	20	1135(60)	182(23)	1 (9 or 3)	32 (8 or 24)
142.68	142.56	187.68(62.64)	3	22	297(66)	391(29)	1 (9 or 3)	16 (8 or 24)
168.6	168.48	213.6(88.56)	3	26	351(78)	445(41)	1 (9 or 3)	16 (8 or 24)
1181.56	181.44	226.56(101.52)	3	28	189(84)	236(47)	1 (9 or 3)	32 (8 or 24)
207.48	207.36	252.48(127.44)	3	32	216(96)	263(59)	1 (9 or 3)	32 (8 or 24)
220.44	220.32	265.44(140.4)	3	34	459(102)	553(65)	1 (9 or 3)	16 (8 or 24)

There are also many solutions with the 2nd local oscillator a multiple of 2.16MHz (crystal/9, i.e. M1=9), or 720KHz (crystal/27 or M1=27), and at least one solution with M1=6. Table 3 below only lists other solutions that have particularly interesting characteristics such as high comparison frequencies for TX offset comparator (43) in either 800MHz or 1900MHz operation.

TABLE 3: Other solutions of particular interest

1st IF	2nd LO	TX OFFSET	M1	N1	M2	N2	M3	1st LO modulus
152.4	152.28	197.4(72.36)	6	47	27(141)	35(67)	47(3)	4(12)
101.64	101.52	146.64(21.6)	9	47	9(47)	13(10)	47 (9 or 3)	8 (8 or 24)
159.96	159.84	204.96(79.92)	9	74	333(2)	427(1)	1 (333 or 111)	16(8 or 24)
203.16	203.04	248.16(123.12)	9	94	9(94)	11(57)	47 (9 or 3)	16 (8 or 24)
106.68	106.56	151.68(26.64)	27	148	111(4)	158(1)	1 (111 or 37)	32 (8 or 24)
213.24	213.12	258.24(133.2)	27	296	222(8)	269(5)	1 (111 or 37)	32 (8 or 24)

The above solutions are remarkable for their relatively low values of (M2,N2) in one or other frequency band, giving very high TX offset phase comparison frequencies in those cases.

As described above, it is of interest that the first local oscillator in the higher frequency range should tune over a range approximately equal to twice the range of frequencies needed for operation in the lower band.

The receive frequency range for the 800MHz cellular band is 869.04 to 893.97MHz, while the receive frequency range of the 1900MHz PCS bands is 1930.08 to 1990.08MHz. Substituting into equations (1),(2),(3) and (4) above gives desirable first intermediate frequencies of 192MHz, 64MHz, 338.52MHz and 169.26MHz respectively. The 64MHZ IF is too low to provide sufficient image rejection when operating over the 60MHz wide 1900MHz receive band. The 338.52MHz IF is difficult to choose because of the unavailability of SAW or crystal filters with a 30KHz bandwidth at that frequency. The solution of equation (1) or equation (4) is therefore preferred.

All the above solutions in tables 1 - 3 were for 1st LO high at 800MHz and low at 1900MHz, i.e. for the solution of equation (2). These can be employed providing the range of the local oscillator (51) is band-switched between 800MHz and 1900MHz operation. It can be undesirable to attempt to cover in one band the entire tuning range that would be required for operation at both 800 and 1900MHz.

A search for solutions for the case of equation (1) yielded the following result with the closest first IF to 192MHz:

1st IF	189.96MHz		
2nd Lo	190.08MHz	= 88/9 x the 19.44MHz crystal	(N1=88, M1= 9)
TX offset (800MHz)	234.96MHz	= 89/72 x 2nd LO	(N2=89, M2=72)
TX offset (1900MHz)	270.00MHz	= 125/88 x 2nd LO	(N2=125,M2=88)

TX offset comparison frequency AT 800MHz = 2640KHz
(actually 5280KHz for the arrangement of figure 7, with N2=89,M2=36)
TX offset comparison frequency at 1900MHz = 2160KHz
2nd LO comparison frequency = 2160KHz
Possible 1st LO fractional-N moduli: 1,2,4,8,11,22,44 or 88 (800MHz)
and: 1,2,3,4,6,8,9,12,18,24,36 or 72 (1900MHz)

The first LO phase comparison frequency is for example 240KHz if a fractional-N modulus of 8 is selected for both bands.

Alternatively, a fractional-N modulus of 24 may be selected to give 720KHz phase comparison frequency at 1900MHz, but the phase comparison frequency will still be 240KHz at 800MHz. The tuning step size at 800MHz will be 10KHz with the same modulus of 24, or even 5KHz for the arrangement of FIG. 7. This is finer than the 30KHz needed, but is acceptable. 240KHz is an adequate comparison frequency for 800MHz operation, and the higher comparison rate of 720KHz is desirable for 1900MHz operation where the oscillator phase noise is double that at 800MHz.

A solution in accordance with equation (4) assumes division of the high-band first local oscillator frequency by 3 for 800MHz operation. In other words, the divider (51b) of FIG. 7 must be changed from a divide-by-2 to a divide-by-3 circuit. It is also necessary then to change divider 45b to a divide by 3 circuit, in order for the transmit frequency steps at 800MHz to be correct. This solution is not investigated further here, as it is not preferred for a dual-band IS136 cellular phone, and in any case is an obvious extension of the disclosed methods.

The invention can be used for dual-band/dual-mode radio telephones in which compatibility with AMPS and IS54 (DAMPS) is desired in the 800MHz band together with compatibility with the PCS1900 (GSM-based) standard.

The problem to be solved is that a radio is normally designed for D-AMPS operation based upon the use of a 19.44MHz crystal as the most convenient common multiple of the 24.3KS/S transmission symbol rate, the 30KHz channel

spacing and the 8KS/S voice digitization. On the other hand, a radio is normally designed for GSM, DCS1800 or PCS1900 operation based upon a 13MHz crystal, which is the lowest common multiple of the transmission bitrate of 270.833KB/S (13MHz/48), the channel spacing of 200KHz (13MHz/65) and the 8KS/S voice digitization rate. This makes it difficult to merely integrate a radio of one design with a radio of the other design, due to the increase in parts count. Therefore it is desired to find internal frequency plans that allow components to be designed that can operate from either crystal frequency, and as another objective it is desired to find reference frequency distribution schemes that will allow operation with the same crystal reference frequency in any of an AMPS mode at 800MHz, a D-AMPS mode at 800 or 1900MHz or a PCS1900 mode at 1900MHz.

FIG. 12 illustrates a solution using both a 13MHz and a 19.44MHz crystal connected to reference oscillator (21), only one of which however is activated at a time via a "select crystal" control signal from digital logic (20).

A single intermediate frequency amplifier chip comprise a dual-crystal reference oscillator (21), second LO and its control PLL (17) and a dual-bandwidth second IF amplifier and second mixer (16). The reference oscillator operates in one mode at 13MHz and the second LO is then controlled to 12 x 13MHz. Alternatively, in a second mode, the reference oscillator operates at 19.44MHz and the second LO is controlled to, for example, 155.52MHz, which is sufficiently close to 156MHz that the same oscillator can be used, while also being a multiple of 19.44MHz (eight times 19.44MHz).

The IF amplifier chip receives a downconverted signal from front end chip (12) which is filtered either using Wideband IF filter (15 WB) or Narrowband IF filter (15 NB). The filter center frequency in the wideband mode is 150MHz, which mixes with the 2nd LO of 156MHz in that mode to produce a second IF of 6MHz, which is fed to digital signal processing (20) along with the RSSI signal. The narrowband first IF filter operates at a center frequency of 120KHz higher than the second LO of 155.52, that is at 155.64MHz, giving a second IF in the

narrowband mode of 120KHz, which is then fed to the signal processing chip (20). The second IF signal at either 120KHz in the narrowband mode or 6MHz in the wideband mode is preferably further filtered in IF amplifier (16) using second IF filters (not shown). In one implementation, the 120KHz second IF filters are integrated active bandpass filters having a passbandwidth of approximately 30KHz, and are fabricated as part of IF amplifier chip (16,17,21). The 6MHz 2nd IF filtering is performed by external ceramic filters (not shown) of approximately 170KHz bandwidth, as used for TV sound IF stages.

When operating in the narrowband AMPS mode at 800MHz, the duplex spacing is 45MHz and so the transmitter frequency is 45 + 155.64MHz below the first LO. The TX offset would therefore be 200.64MHz. However, as shown in FIG. 13, the TX mixer (46) mixes transmit and receiver oscillators (45,51) at double the 800MHz frequency, and so produces an offset of 401.28MHz. This has a highest common factor of 1920KHz with the second LO of 155.52MHz, so divider (47) divides the TX offset from TX mixer (46) by a first integer N2 to obtain a first 1920KHz signal, and divider (41) divides the second LO from IF chip (30) by and integer M2=81 to produce a second 1920KHz signal. The two 1920KHz signals are compared in transmit phase comparator (43) to produce an error signal. The error signal is filtered and integrated in loop filter (44) to produce a control signal for TX oscillator (45) to maintain it at the desired frequency, which, when halved in divider (45b), is the desired 800MHz transmit frequency.

This frequency plan at 800MHz may also be used for the D-AMPS mode in the 800MHz band. For operating in the D-AMPS mode at 1900MHz, the duplex spacing is 80.04MHz, so that the transmit offset is 80.04+155.64MHz = 235.68MHz. This is not simply related to second LO frequency of 155.52MHz; however, since only time-duplex modes are used at 1900MHz such that transmission and reception occur in different timeslots and not simultaneously, the first local oscillator may be sidestepped by the relatively small amount of 240KHz

between transmit and receive so that a TX offset of 235.44MHz may be used instead of 235.68MHz.

The slightly modified TX offset of 235.44MHz shares a common factor of 2160KHz with the second LO of 155.52 MHZ. Thus in the 1900MHz D-AMPS mode, divider (47) divides by an integer N2 reprogrammed to divide 235.44MHz to 2160KHz, while divider (41) is reprogrammed to divide by an M2 of 72 to obtain 2160KHz, the phase comparator (43) now comparing signals at 2160KHz instead of 1920KHz.

Finally, to obtain the PCS1900 mode, where the duplex offset is 80MHz, the transmit offset is 80 + 150MHz, as the first IF is 150MHz in that mode. The 230MHz TX offset shares a common divisor of 2MHz with the second LO that is now 156MHz. This mode is also time duplex, and the first LO could be sidestepped to modify the TX offset from 230MHz to for example 234MHz, which has the much larger common factor of 78MHz with the 2nd LO of 156MHz. Nevertheless, it may be advantageous to keep a phase comparison frequency of 2MHz, which makes all phase comparison frequencies (1920,2160 and 2000KHz) sufficiently close to facilitate the use of a common loop filter (44) and phase comparator (43). Otherwise, if desired to take advantage of a larger common factor such as 78MHz, a different loop filter and even phase comparator may become necessary to provide the desired closed loop characteristics of stability and lock-in time. Thus the arrangement of FIG. 13 has deliberately aimed to maintain roughly the same TX offset loop operational characteristics of loop-bandwidth and lock-in time in all bands and modes.

The dual-mode, dual-band transmitter-receiver of FIGs. 12 and 13 assumes a double superheterodyne receiver is used in all modes. In the narrowband AMPS and D-AMPS modes, the second intermediate frequency is 120KHz and the second IF filters are integrated, on-chip, active filters; in the wideband PCS1900 modes, which can include all GSM voice and data modes, satellite communication modes and GPRS packet data modes, the second IF is 6MHz, and the second IF filters

are more difficult to integrate at that frequency. An alternative receiver architecture for the wideband mode is shown in FIG. 14, in which the second IF in the wideband mode is zero frequency, otherwise known as an "IF Homodyne", as opposed to an RF Homodyne, which converts directly from the frequency received at the antenna to zero frequency in one conversion step. The receiver of FIG. 14 converts from the frequency received at the antenna to zero frequency in two steps, the first step converting to a first Intermediate Frequency of 156MHz and the second step converting from 156MHz to zero frequency by mixing with the 156MHz local oscillator. Since the first IF in FIG. 14 is now 156MHz as opposed to the 150MHz of FIGs. 12 and 13, the TX offset for 1900MHz is now 156+80=236MHz, which still shares a common factor of 2MHz with the 156MHz local oscillator. Thus the only change to FIG. 13 is that the value of N2 for PCS1900 operation would change from 230/2=115 to 236/2 = 118. If desired, a higher common factor of 4MHz could be used by changing N2 to 236/4 = 59 and M2 from 78 to 39, and M3.from 2 to 4 (or alternatively changing the fractional-N modulus of N3 to accept a higher reference frequency for third phase comparator (49).

The implementations of FIGs. 12, 13 and 14 use two different reference crystals, although only one is active at any time. Nevertheless this adds the complication that both crystals must be independently temperature compensated, as every crystal has different individual temperature compensation needs. Temperature compensation is carried out by a "self-learning" technique, whereby the receiver locks to a base station signal and then uses the base station signal frequency as a basis for correcting crystal error. The prevailing temperature is measured using a thermistor, and the correction applied to the crystal is stored in a table against the prevailing temperature in microprocessor memory in digital signal processor (20).

To simplify the temperature compensation as well as eliminating the cost and board area associated with a second crystal, it is therefore of interest to

consider the solutions of FIGs. 15 and 16 using a single crystal. The solution of FIG. 15 is to choose a compromise crystal frequency of 19.5MHz. This is 1.5 times the 13MHz from which PCS1900 bitrates are derived, and the bitrate is still derivable as 19.5MHz/72 as opposed to 13MHz/48. 19.5MHz is also close to the 19.44MHz needed for D-AMPS modes, from which the symbol rate of 24.3KS/S is derived by dividing by 800. When 19.5MHz is used, the error is 0.3%, which would cause a timing drift in the transmitted symbol stream of exactly half a symbol period during transmission of a TDMA burst of 6.667mS or 162 symbols duration. In principle, such an error is no greater than must in any case be anticipated by the receiver due to multipath propagation causing transmission path delay variations of up to one symbol. Nevertheless it is desirable to correct the transmitted signal so that its errors do not compound the imperfections introduced by the propagation path. To a first approximation, the symbol rate error can be reduced by dividing the crystal frequency by 802 to obtain the symbol rate with a residual error of 0.0585%, giving a timing drift of less than one tenth of a symbol over a 162-symbol burst duration. A further refinement can be made by means of a skip-counter, which divides sometimes by 802 and sometimes by 803 in order to create a more accurate approximation to the 24.3KS/S symbol rate. However, in one implementation, the 24.3KS/S modulation is generated digitally at the rate of 8 samples per bit. Several samples per bit are used to represent the curved waveform of a symbol stream that has been filtered using a root-raised-cosine filter frequency response. Thus it is really desired to create an accurate approximation to 8 times the symbol rate, or 194.4 kilosamples per second, by dividing the crystal frequency sometimes by 100 and sometimes by 101. The number of times Nl division by 100 occurs and the number of times N2 that division by 101 occurs will now be derived.

The D-AMPS frame repetition period of 20mS represents 390,000 cycles of a 19.5MHz clock as opposed to 388,800 cycles of a 19.44MHz clock.

A timing generator is thus programmed to divide by 390,000 when a 19.5MHz clock is used as opposed to 388,800 when a 19.44MHz clock is used, in order to create the 20mS repetition period. The D-AMPS TDMA frame is divided into 3 timeslots, and one timeslot is thus 130,000 cycles of a 19.5MHz clock in duration as opposed to 129,600 cycles of a 19.44MHz clock. The first equation for Nl and N2 is therefore that

$$100.N1 + 101.N2 = 130,000$$

In addition, the total number of 1/8th symbol sample periods to be created is 8 x 162 =1296 as before, so the second equation for Nl and N2 is

$$N1 + N2 = 1296$$

Solving these equations gives N2 = 400, N1 = 896.

Thus a skip counter is programmed to divide by 100 a total of 896 times interspersed with dividing by 101 a total of 400 times, creating a total of 1296 1/8th symbol periods with no timing error greater than of the order of half a clock period of the 19.5MHz clock, or 25 nanoseconds. FIG. 20 shows a skip counter design accomplishing the above. A divider (100) is configured to divide either by 100 or by 101 according to a control input from accumulator (101), so that successive output pulses from the divider (100) will be spaced by either 100 cycles of the 19.5MHz clock or by 101 cycles. The accumulator (101) is configured as a modulo-81 accumulator, which means that if after adding an increment, the value in the accumulator is equal to or greater than 81, then 81 is subtracted from the accumulator value and an overflow or carry pulse is generated. The carry pulse output from accumulator (101) is used to cause divider (100) to divide by 101.

If no carry is generated by accumulator (101) upon being caused to increment by the last divider (100) output pulse, then divider (100) counts 100 cycles of the 19.5MHZ clock input to produce the next output sample rate pulse. Else, if upon the last divider output pulse causing the accumulator to increment and overflow, then the accumulator carry output fed back to divider (100) causes

the divider to count 101 cycles of the 19.5MHz clock input before producing the next divider output sample rate pulse.

By setting the accumulator increment equal to 25, the accumulator produces a carry pulse 25/81ths of the time, which is equal to 400/1296ths of the time, this being the proportion of divide-by-101's calculated above needed to produce the exact number 1296 of 8 x symbol rate pulses in a D-AMPS timeslot.

FIG. 16 shows the internal frequency plan using a 19.5MHz crystal. The first IF in D-AMPS mode is changed to 154.32MHz to give high phase comparator frequencies of 1320KHz and 1080KHz for transmit phase comparator (43) in 800 and 1900MHz operation respectively, while also giving a high comparison frequency of 780KHz at 2nd LO phase comparator (31).

Yet another implementation of the invention is shown in FIG. 17, this time using a 13MHz crystal to derive all radio oscillator frequencies, and a 19.44MHz crystal connected to digital chip (20) only to derive bit and digital sampling rates for the AMPS and D-AMPS modes. The frequency plan for this case is shown in FIG. 18, in which substantially the only difference from FIG. 16 is that the second LO phase comparator now operates at 520KHz.

In both FIG. 16 and FIG. 18, the main receiver synthesizer (the first LO) operates as a fractional-N synthesizer with a modulus of 5 (optionally 10 or 20) in PCS1900 mode, and 12 in AMPS and D-AMPS modes.

It is possible to eliminate the 19.44MHz crystal used only for generating digital clocks by using the arrangement of FIG. 19, in which the digital chip (20) creates its own 19.44MHz clock by means of an internal PLL when needed. To facilitate this, dividers (41) and (42) are split into two dividers (41a,41b) and (42a,42b). Divider 41a divides the 2ND LO frequency of 154.44MHz by 117 in D-AMPS mode at 800MHz to obtain 1320KHz at which the transmit phase comparator (43) operates. Selector switch 41c is operated to select the output of divider 41a in this mode. During-this mode, divider 41b operates simultaneously, dividing by 11 to provide a 14.040 MHZ output to the digital chip (20). This

frequency shares a common factor of 1080KHz with the 19.44MHz generated on the digital chip (20) by means of a local PLL when needed. Divider (42a) operates at this time to divide the operation frequency of phase comparator (43) by a further factor of 2 to obtain 660KHz, which is used along with a modulus-11 fractional-N divider (43) to provide 60KHz steps of oscillator (51), which provides 30KHz steps after division by 2 for 800MHz AMPS or D-AMPS operation. For 1900MHz D-AMPS operation switch 41c selects instead the output of divider (42b) which is 14.04MHz divided by 13, that is 1080KHz. This is the desired frequency to provide the duplex offset of 80.04MHz at 1900MHz compared to 45MHz at 800MHz. The selected 1080KHz for phase comparator (43) is then further divided by 3 in divider (42a) reprogrammed to divide by 3, giving a 360KHz phase comparison frequency for phase comparator (49), which, together with the use now of a fractional-N modulus of 12 for divider (48), gives 30KHz tuning steps for oscillator (51) during D-AMPS operation at 1900MHz. For PCS1900 operation, divider (41b) is programmed to divide by 12, dividing the second LO of now 156MHz to provide a 13MHz clock output to the digital chip (20). The 13MHz is divided by 13 in divider (42b) to 1MHz, which is the operating frequency of phase detectors (43,48). Divider (42a) is thus programmed to make M3=1. Using a fractional-N modulus of 5 for divider (48) provides the desired 200KHz steps in this mode.

It has thus been shown above that the invention permits the construction of dual-band, dual-mode transceivers using either a single crystal reference or two crystals in a variety of ways to derive alternative symbol rates of 270.833KB/S and 24.3KS/S, alternative channel spacings of 30KHz or 200KHz, and transmit-receive duplex spacings of 45MHz, 80.04MHz or 80.00MHz.

Moreover, this flexibility is achieved with an improved architecture as compared with the prior art, allowing the radio hardware to be reduced to essentially three integrated circuit chips having a reduced number of RF

interconnections there between, thus minimizing risks of internal interference and reducing power consumption.

An alternative to using a transmit offset frequency to control generation of the transmit frequency, as described above, is using a lock frequency. FIG. 21 illustrates a dual band transceiver employing a lock frequency according to a second embodiment of the present invention.

The dual band transceiver according to the second embodiment includes similar components as the dual band transceiver described above, e.g., a duplexor, a receiver front end, a receiver IF, modulators, and a power amplifier. Although not shown, the dual band transceiver according to the second embodiment also comprises DSP means (20) as described above.

For illustrative purposes, the second embodiment is described with reference to operation according to the PCS and AMPS/DAMPS standards. It will be appreciated, however, that the invention is also applicable to other standards.

Referring to FIG. 21, for frequency duplex operation, the Duplexor (11a) includes a Diplexer or Switch, PCS and AMPS/DAMPS Couplers, a PCS Duplexer or RX/TX switch, and an AMPS/DAMPS Duplexer. A signal received by the antenna 10 is diplexed or switched, to select the band of operation. The PCS and AMPS/DAMPS Couplers detect the power level of the system and communicate with the DSP (20) which ensures that the system is operating at the appropriate power level for the band of interest. The PCS Duplexor or RX/TX Switch and the AMPS/DAMPS Duplexor couple the appropriate input to the receiver front end (12a).

The duplexors can be replaced with a switch or used in conjunction with an isolator or circulator, depending on the requirements for a particular band. Similarly, the switch may be replaced with a duplexer or used in conjunction with an isolator or circulator.

The receiver front end (12a) comprises one or more low-noise amplifiers and downconverting mixers. The receiver front end (12a) may contain separate

amplifiers and mixers for each band, as shown in FIG. 21. Filters for each band may be included in the receiver front end (12a) or implemented as separate components, as shown in FIG. 21. A 1st LO (51) and a frequency doubler (59) may also be included in the front end (12a) or implemented as separate components as shown in FIG. 21.

For low band operation, the 1st LO frequency from the 1st LO (51) is delivered to a mixer in the receiver front end (12a). For high band operation, the 1st LO frequency is doubled in a doubler (59), then delivered to a mixer in the receiver front end (12a). The 1st LO frequency or the doubled 1st LO frequency, depending on the band, is mixed with the desired receive frequency signal to produce a first intermediate frequency signal which is filtered in the IF filter (15). The desired receive frequency is selected by tuning the 1st LO (51) to a frequency equal to the sum or the difference of the desired receive frequency and the first IF, using the 1st LO PLL (14). The 1st LO (51) is a channel stepper which is tuned by the 1st LO PLL (14) to an integer multiple of a basic tuning step size, derived from a reference frequency source, e.g., a crystal frequency oscillator (21,22). The 1st LO (51) operates at a frequency adapted to the lower of the two-possible receive frequency bands to convert received signals to the desired first IF. For high band operation, the 1st LO PLL (14) tunes the 1st LO (51) to a doubled integer multiple of a basic tuning step size, using the frequency doubler (59).

The 1st LO PLL (14) compares the 1st LO frequency or the doubled 1st LO frequency to the reference frequency and generates an error signal which controls the 1st LO (51). The 1st LO PLL (14) may include a switch to select whether to compare the 1st LO frequency or the doubled 1st LO frequency to the reference frequency. If the lower frequency is always selected, this switch may be eliminated. By selecting the LO frequency for comparison in the 1st LO PLL (14), depending on the band, the same channel stepping (e.g., 30KHz) can be maintained for both bands. In addition, current is saved by not operating the 1st LO PLL (14) at twice the low band frequency when low band operation is desired.

The receiver performs a second frequency down conversion in a receiver IF circuit (16a) which comprises, e.g., a mixer for mixing the first intermediate frequency down with a 2nd LO frequency from the 2nd LO (33). Although shown as separate components, the 2nd LO (33) can be contained in the receiver IF circuit (16a). The 2nd LO (33) is controlled to the desired frequency by the IF PLL circuit (17) which compares the 2nd LO frequency with a reference frequency from, e.g., a crystal oscillator (21) and produces an error signal.

The transmitter comprises a transmit frequency oscillator (45) for generating the transmit frequency. The transmit frequency is offset from the 1st LO frequency by the duplex spacing, combined with the first intermediate frequency. In the past, the transmitter frequency offset has been used to control the generation of the transmit frequency. A problem with using offset in this manner is that up-conversion products are generated which have to be filtered. This adds a filtering burden to the transmitter.

According to the second embodiment, this problem is avoided by mixing the 1st LO frequency down with the transmit frequency to produce a lock frequency and comparing the lock frequency and the reference frequency in the TX PLL (19). The comparison result is used to control the generation of the transmit frequency by the transmit frequency oscillator (45).

According to an exemplary embodiment, the transmit frequency signal generated by the transmit frequency oscillator (45) is multiplied by an integer X1, X2,... or XN in a buffer/multiplier (53) to produce an "on-channel" transmit frequency. This frequency is then mixed in a TX mixer (46) with a 1st LO frequency from 1st LO (51) to produce a lock frequency. The lock frequency is compared with a reference frequency from e.g., crystal oscillator (21) or any other suitable frequency source such as the second LO (33), and the result is used to control the TX LO (45).

A frequency doubler (54) doubles the low band transmit frequency to produce a high band transmit frequency when operation in the higher of the two

frequency bands is desired. The high band transmit frequency and the low band transmit frequency signals are amplified in amplifiers (55) and (56), respectively, then modulated in the I/Q modulator (18) with information from, e.g., the DSP (20).

The I/Q information is directly modulated onto the transmitter carrier via the I/Q modulator (18). The output of the doubler (54) is modulated when operation at the high band is desired, while the output of the multiplier (53) is modulated for low band operation. The modulated signal is amplified in variable gain amplifiers (57) and (58) which may be implemented as a single, wideband device or as individual narrowband devices, optimized for each band, as shown in FIG. 21. The output of the variable gain amplifiers (57) and (58) is amplified in a transmit power level using power amplifier (13), which may be implemented with a narrowband power amplifier as shown in FIG. 21 or with a broadband power amplifier. The mixer (46), multipliers (53) and (54), amplifiers (55) and (56), modulator (18), and variable gain amplifiers (57) and (58) may be implemented as a single device, as shown in FIG. 21.

The dual band radio architecture according to the second embodiment can be modified in several ways, depending on the particular standard in each band which is to be implemented. For example, the on-channel TX LO (45) may include a band switch if that is helpful in the tuning range between band use of the oscillator.

In addition, the output of the TX mixer (46) may be filtered in a filter (46a) before comparison in the TX PLL (19), as shown in FIG. 22. This reduces spur content.

The I/Q modulator (18) may be broadband, covering both transmit bands, as shown in FIGS. 21 and 22. Alternately, the I/Q modulator may be narrowband, optimized for each band, as shown in FIG. 23.

As shown in FIG. 24, the transmit frequency may be delivered directly to the TX mixer (46) from the TX LO (45). In this case, the multiplier (54) may be

replaced with a buffer (54b), and a divider (53c) may be added to the low band path.

As shown in FIG. 25, the transmit oscillator frequency may be at any integer multiplier/quotient of the desired transmit signal, including the integer 1. For this purpose, multiplexers/dividers (53a-b) and (54a) are included for the low band and the high band, respectively. A switch may be included in the high band path, to select multiplication/division in the multiplexer/divider (54a), depending on the multiplication/division in the multipliers/dividers (53a) and (53b). It will be appreciated that the transmit frequency may be delivered to the TX mixer (46) from any multiplier/divider.

Also, as shown in FIG. 25 and 26, variable gain amplifiers (59a) and (59b) may exist at the I/Q modulator input, in addition to or instead of the variable gain amplifiers (57) and (58) at the modulator output.

The dual band transceiver according to the second embodiment has many advantages. For example, the transmitter employs an on-channel transmit frequency to generate a lock frequency, as opposed to using an offset signal to produce the transmitter carrier. Consequently, fewer spurious signals are generated. An on-channel arrangement also reduces the filtering requirement to satisfy the transmitter masks of radio standards. This is especially helpful for radios that are not full duplex, such as those employing TDMA standards, which do not inherently demand significant transmitter band filtering. Surface acoustic wave (SAW) filters are customarily added to remove spurs generated in the conversion process that exceed the transmit mask.

Another advantage is that the lock frequency is the same type frequency that an offset oscillator would produce in a transmitter offset approach. Because this signal is a mix down product, it can be at a significantly lower power level with lower harmonic energy than what is generated by an oscillator circuit. With lower levels, there is less danger from signals leaking around filters and getting

out of the transmitter directly or through mixers. Thus, this embodiment has the benefit of reduced levels of spur signals.

The TX PLL (19) according to the second embodiment, performs a strong filtering function acting as a low pass filter with a cutoff frequency anywhere from 1KHz to 1MHz. The VHF frequency that is used as a reference frequency is filtered to a very small value before it is inserted into the transmitter up-conversion process. Therefore, very low spurious content is maintained. Filtering of a 50 to 250MHz signal is much easier at 1MHz than at 1 and 2GHz. Thus, this embodiment has the benefit of easier filtering of generated spur signals in the transmitter.

Another benefit is that current is saved in the transmitter in comparison to the offset approach, because the number of mixer/modulator stages between the IQ modulation and the transmit output frequency is reduced to one. For linear transmitters, every linear mixer adds current. In addition, current is saved by activating the doubler (54) only when operating in the high frequency band. Current is also saved by selecting the low band (900 MHz) input to the main receiver LO synthesizer to avoid running the synthesizer at twice the frequency when operating in the low band.

Another benefit is that a single channel stepper is shared for both the transmitter and the receiver channels in both bands, reducing space, current, and costs. Also, one TX LO and one 1st LO are shared for both bands, thus further reducing space and costs.

Yet another benefit is that full duplex operation is allowed for both bands. Generally, in a dual band transceiver, the duplex spacing is different between bands. For a shared channel stepper, this can be a problem if the channel stepper has to make up the difference in duplex spacing between bands. According to the second embodiment, the transmit loop resolves the duplex spacing difference, instead of the channel stepper, thereby enabling full duplex operation in both bands.

The dual band transceiver according to the second embodiment also enables the RX PLL (14) to step in full channel spacing for both the low and high bands. This avoids incrementing the TX PLL (14) in one-half channel spacing (15KHz for 30KHz channel spacing required in IS-136, IS-137) for the 1900MHz band in a 900/1900MHz dual band hand set.

In addition, the invention provides flexibility in the TX PLL (19). The transmit frequency provided to the TX mixer (46) from the transmitter can be at the lower band always or switched between bands.

Although the description of the embodiment above is directed to a dual band phone, it will be appreciated that it is also applicable to a single band phone by removing the components corresponding to the second band or by simply using only the components for one band.

The invention may be useful in contexts other than cellular radio. The invention may be adapted by a person skilled in the art using the above teachings while remaining within the spirit and scope of the invention as described by the following claims.

WHAT IS CLAIMED IS:

1. A radio transmitting and receiving apparatus for generating a signal for transmission on a transmit frequency and for receiving a signal on a receive frequency, comprising:

-a first downconvertor for mixing said received signal with a first local oscillator frequency signal and converting it to a first intermediate frequency signal;

-a second downconvertor for mixing said first intermediate frequency signal with a second local oscillator frequency signal and converting it to a second intermediate frequency;

-reference means for providing a reference frequency signal;

-first local oscillator frequency synthesizer means having a first input for said first local oscillator frequency signal and a second input for said reference frequency signal and in dependence thereon producing a control signal to control said first local oscillator to produce the desired first local oscillator frequency signal;

-second local oscillator frequency synthesizer means having a first input for said second local oscillator frequency signal and a second input for said reference frequency signal and producing in dependence thereon a control signal to control said second local oscillator to produce the desired second local oscillator frequency signal;

-transmit oscillator means for generating a transmit frequency signal;

-transmit downconvertor means for mixing the transmit frequency signal with the first local oscillator signal to produce a lock frequency signal;

-transmit synthesizer means having a first input for the lock frequency signal and a second input for the reference frequency signal and in dependence thereon producing a control signal for the transmit oscillator means to control the transmit frequency signal.

2. The apparatus of claim 1, further comprising a frequency doubler for doubling said first local oscillator frequency signal input to said first local oscillator frequency synthesizer means, wherein said first local oscillator frequency synthesizer means selects said first local oscillator frequency signal or the doubled first oscillator frequency for low band operation and high band operation, respectively.

3. The apparatus of claim 1, wherein the first down converter mixes said received signal with the first local oscillator frequency signal for low band operation and mixes said received signal with a doubled first oscillator frequency signal for high band operation.

4. The apparatus of claim 1, further comprising a frequency doubler for doubling the transmit frequency signal for high band operation.

5. The apparatus of claim 1, further comprising a frequency divider for dividing the transmit frequency signal for low band operation.

6. The apparatus of claim 1, further comprising frequency multipliers for multiplying the transmit frequency signal for low band operation and/or high band operation.

7. The apparatus of claim 1, further comprising frequency dividers for dividing the transmit frequency signal for low band operation and/or high band operation.

8. The apparatus of claim 1, further comprising a filter for filtering the lock frequency signal.

9. The apparatus of claim 1, further comprising a modulator for modulating the transmit frequency signal to produce the signal for transmission.

10. The apparatus of claim 1, further comprising a variable gain amplifier for amplifying the transmit frequency signal to produce the signal for transmission.

11. A method for generating a signal for transmission on a transmit frequency and for receiving a signal on a receive frequency, comprising the steps of:

-mixing said received signal with a first local oscillator frequency signal to produce a first mixed signal;

-converting said first mixed signal to a first intermediate frequency signal;

-mixing said first intermediate frequency signal with a second local oscillator frequency signal to produce a second mixed signal;

-downconverting said second mixed signal to a second intermediate frequency;

-comparing said first local oscillator frequency signal and a reference frequency signal and producing in dependence thereon a control signal to control the production of the desired first local oscillator frequency signal;

-comparing said second local oscillator frequency signal and said reference frequency signal and producing in dependence thereon a control signal to control production of the desired second local oscillator frequency signal;

-generating a transmit frequency signal;

-mixing the transmit frequency signal with the first local oscillator signal to produce a lock frequency signal;

-comparing the lock frequency signal and the reference frequency signal and in dependence thereon producing a control signal to control the generation of the transmit frequency signal.

12. The method of claim 11, further comprising the steps of:

-doubling said first local oscillator frequency signal; and

-selecting the first local oscillator frequency signal or the doubled first local oscillator frequency signal for comparison with the reference frequency signal for low band operation and high band operation, respectively.

13. The method of claim 11, wherein said received signal is mixed with the first local oscillator frequency signal for low band operation, and said received signal is mixed with a doubled first oscillator frequency signal for high band operation.

14. The method of claim 11, further comprising a step of doubling the transmit frequency signal for high band operation.

15. The method of claim of claim 11, further comprising a step of dividing the transmit frequency signal for low band operation.

16. The method of claim 11, further comprising a step of multiplying the transmit frequency signal for low band operation and/or high band operation.

17. The method of claim 11, further comprising a step of dividing the transmit frequency signal for low band operation and/or high band operation.

18. The method of claim 11, further comprising a step of filtering the lock frequency signal.

19. The method of claim 11, further comprising a step of modulating the transmit frequency signal to produce the signal for transmission.

20. The method of claim 11, further comprising a step of amplifying the transmit frequency signal for transmission.

FIGURE 1: PRIOR ART REFERENCE FREQUENCY DISTRIBUTION

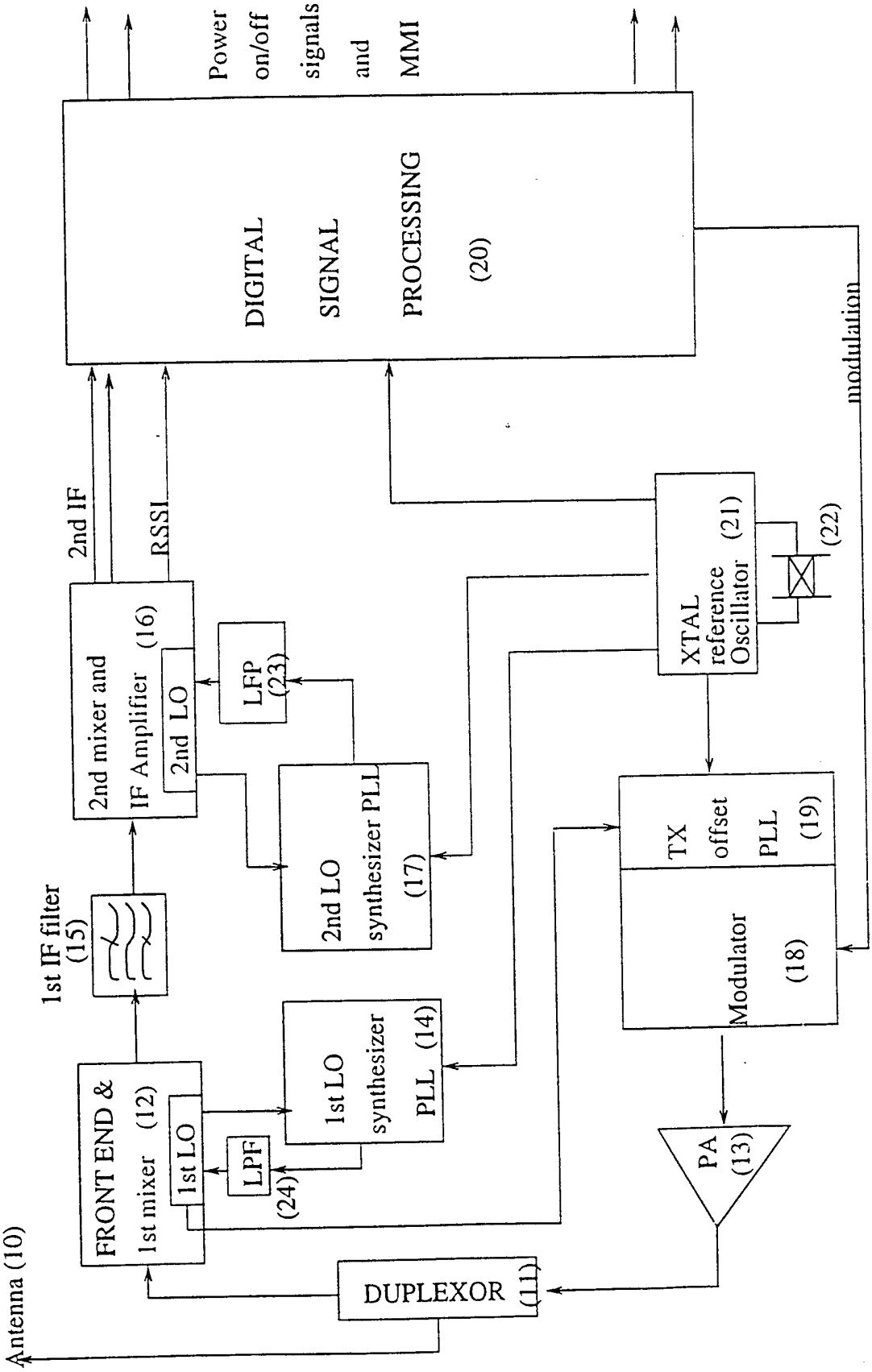


FIGURE 2: OTHER PRIOR ART REFERENCE DISTRIBUTION SCHEME

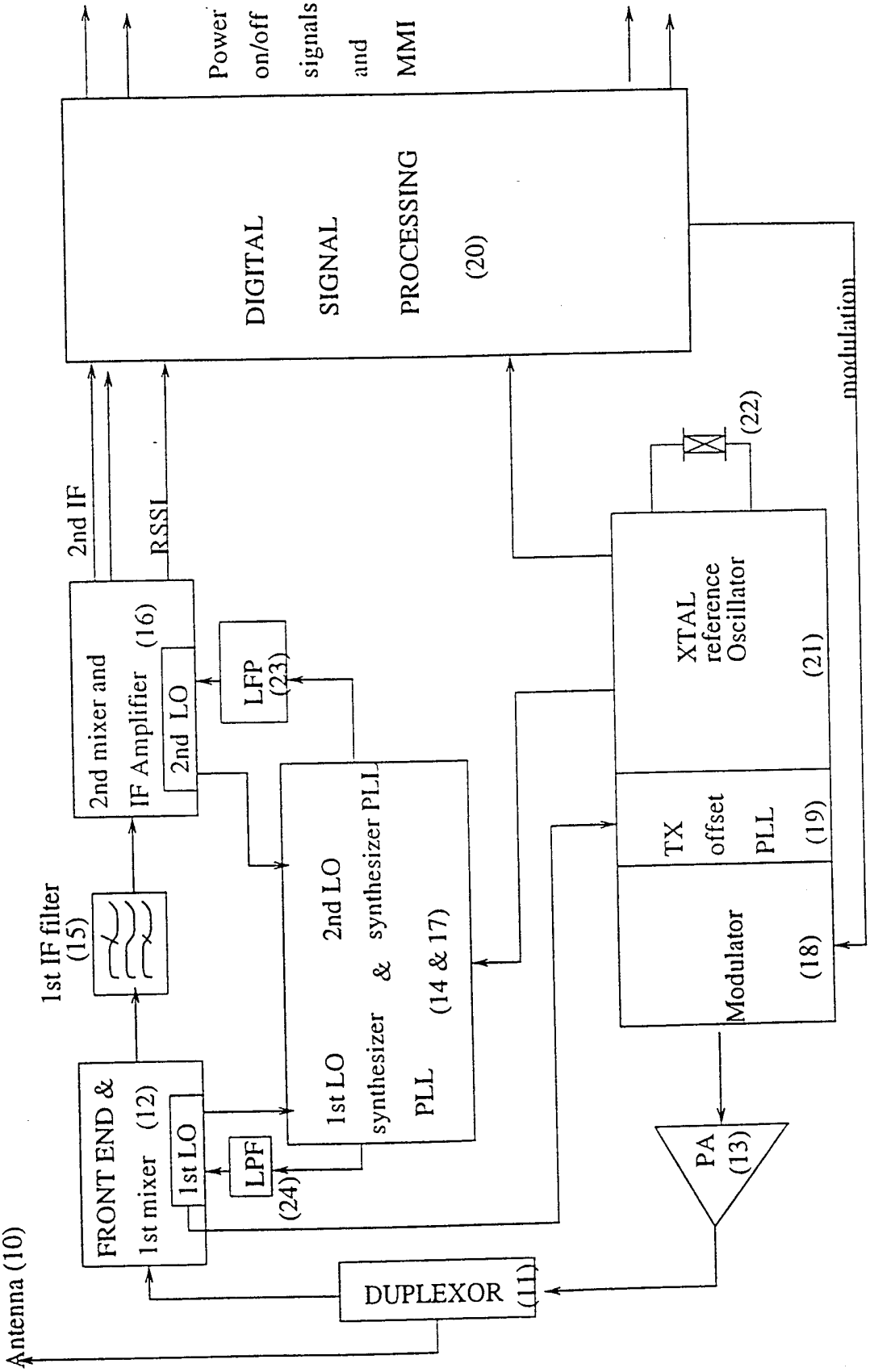


FIGURE 3: DOLMAN'S REFERENCE FREQUENCY DISTRIBUTION

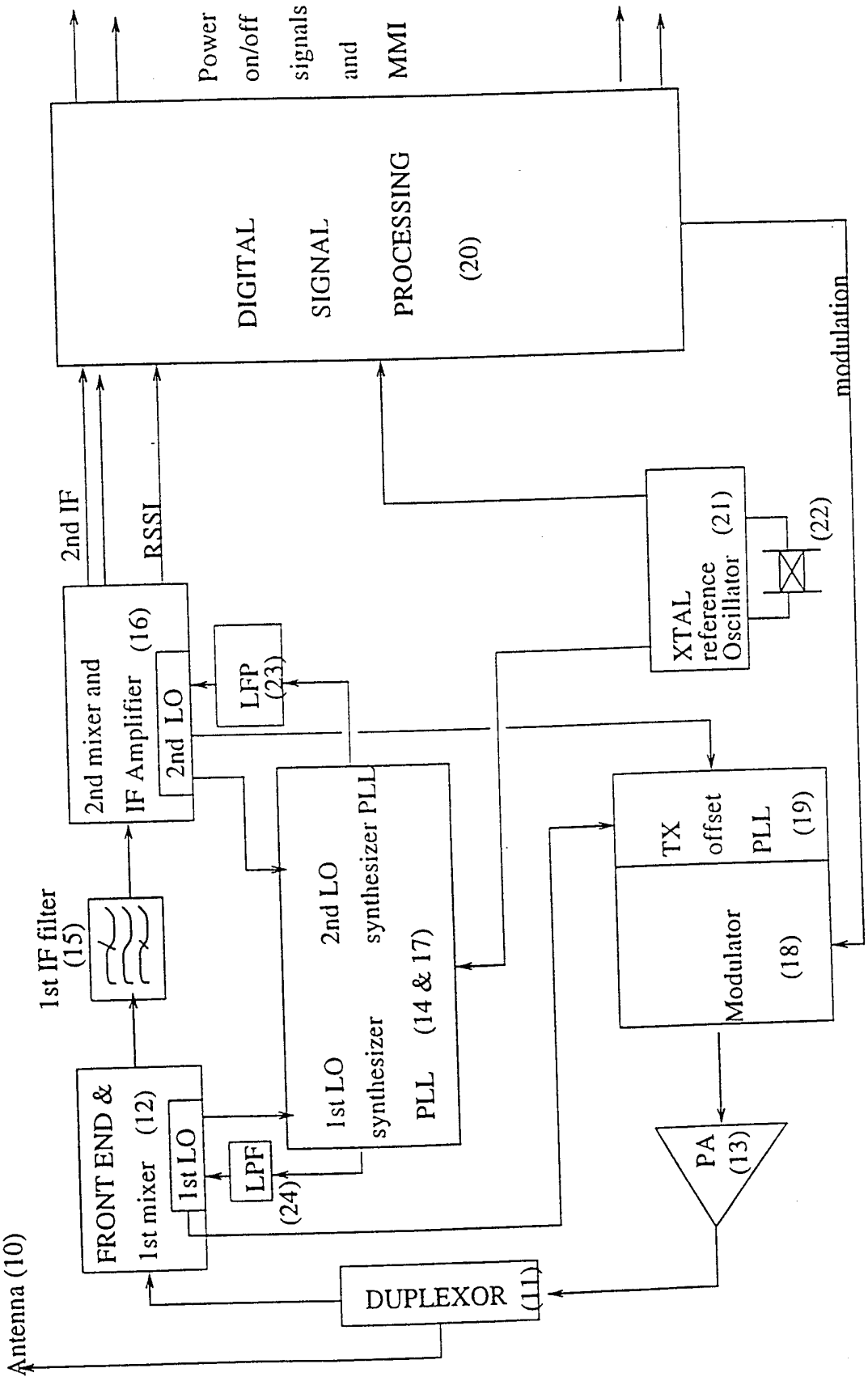


FIGURE4: INVENTIVE REFERENCE FREQUENCY DISTRIBUTION

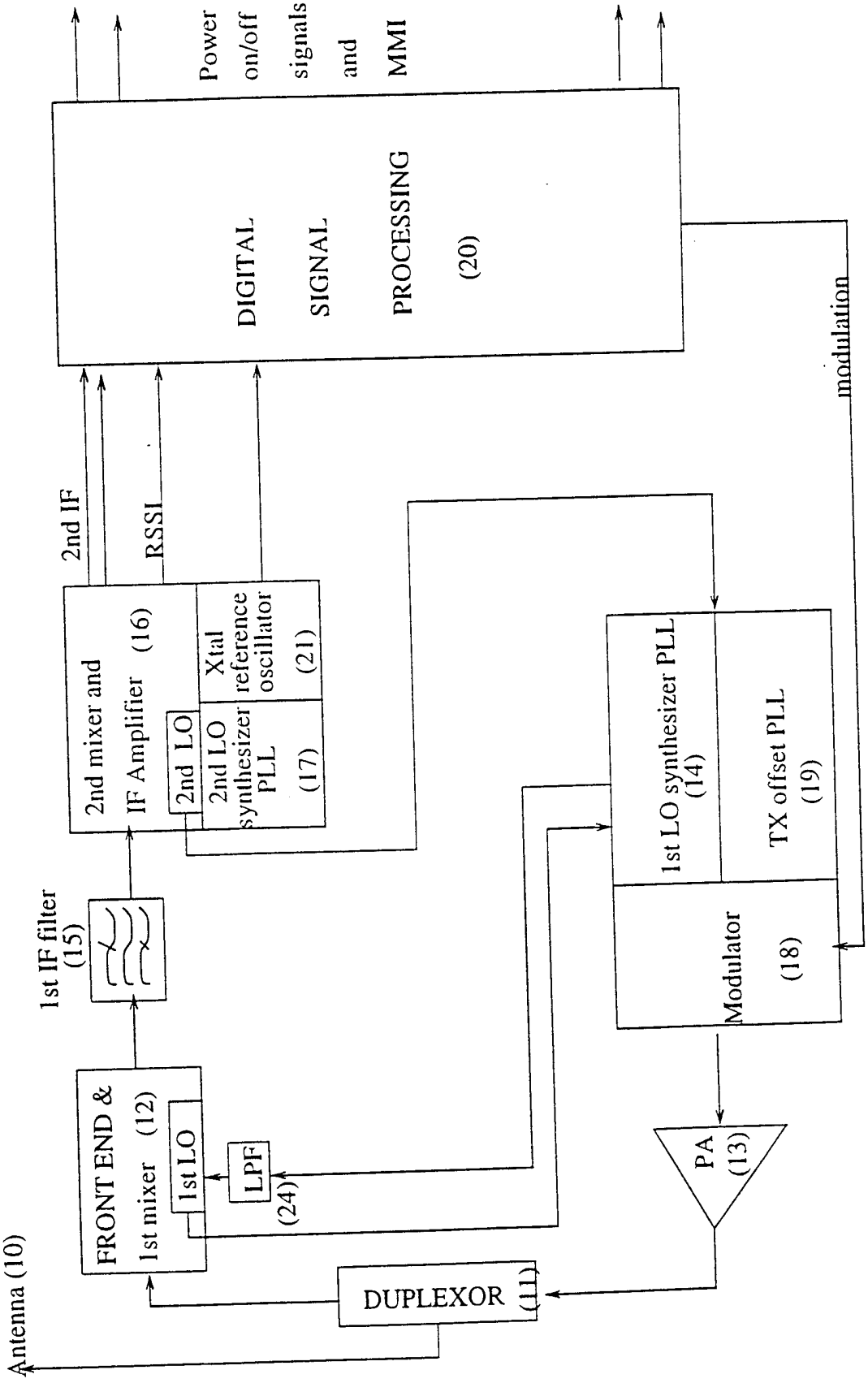


FIGURE 5: INVENTIVE FREQUENCY SYNTHESIS ARRANGEMENT

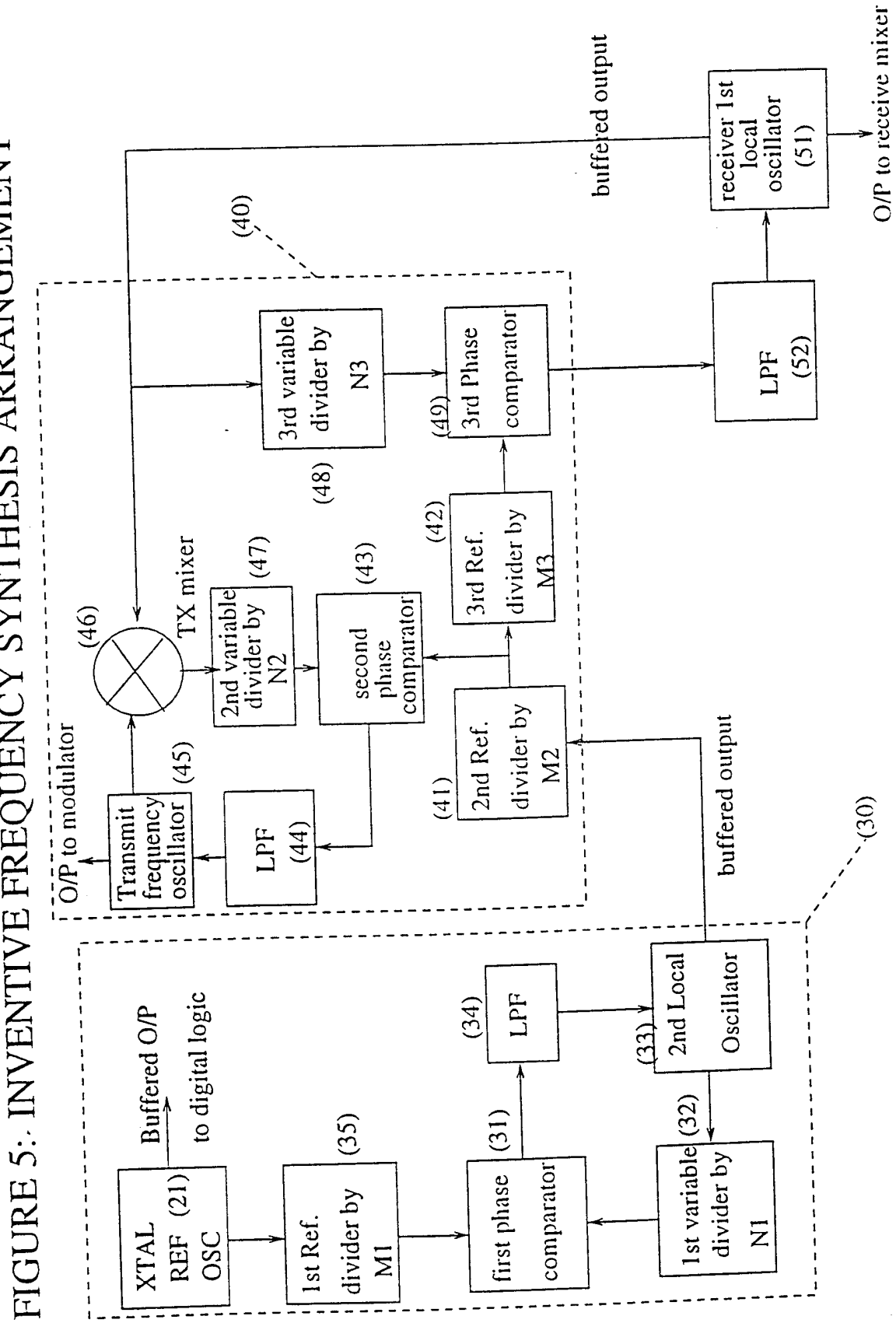


FIGURE 6: ANOTHER INVENTIVE SYNTHESIS ARRANGEMENT

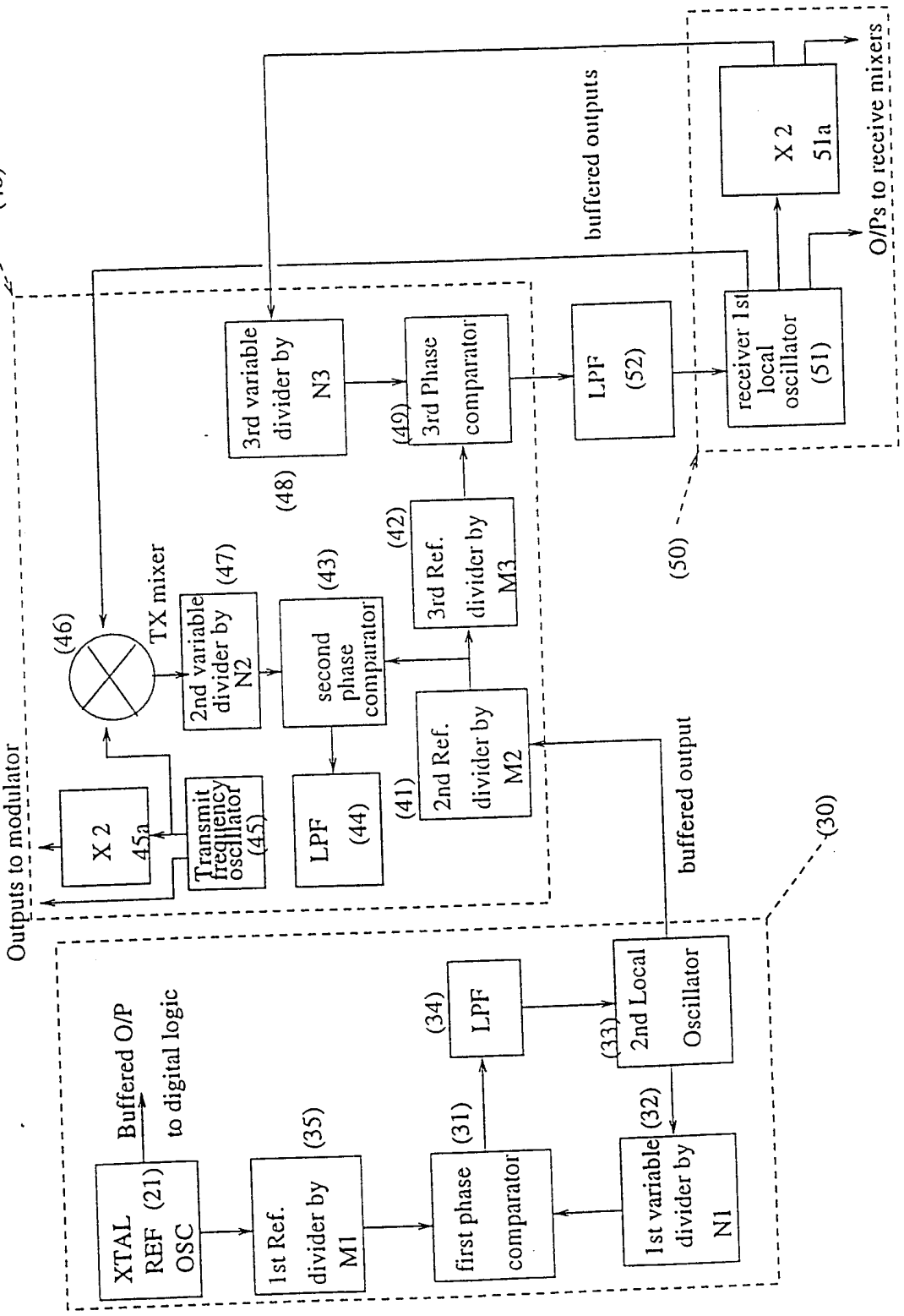


FIGURE 7: ALTERNATIVE WITHOUT FREQUENCY DOUBLERS

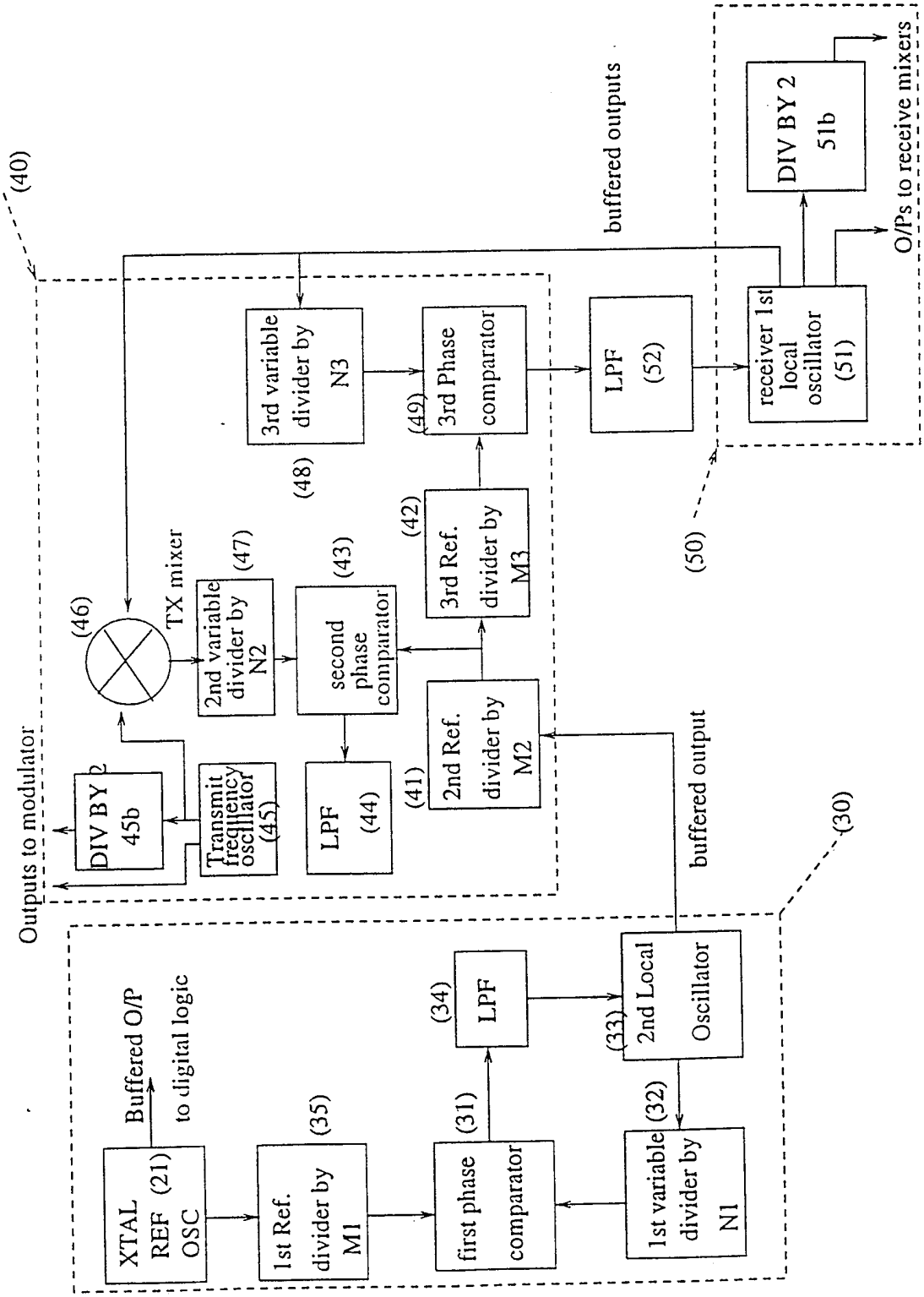


FIGURE 8: ALTERNATIVE WITH A DOUBLER AND A DIVIDE-BY 2

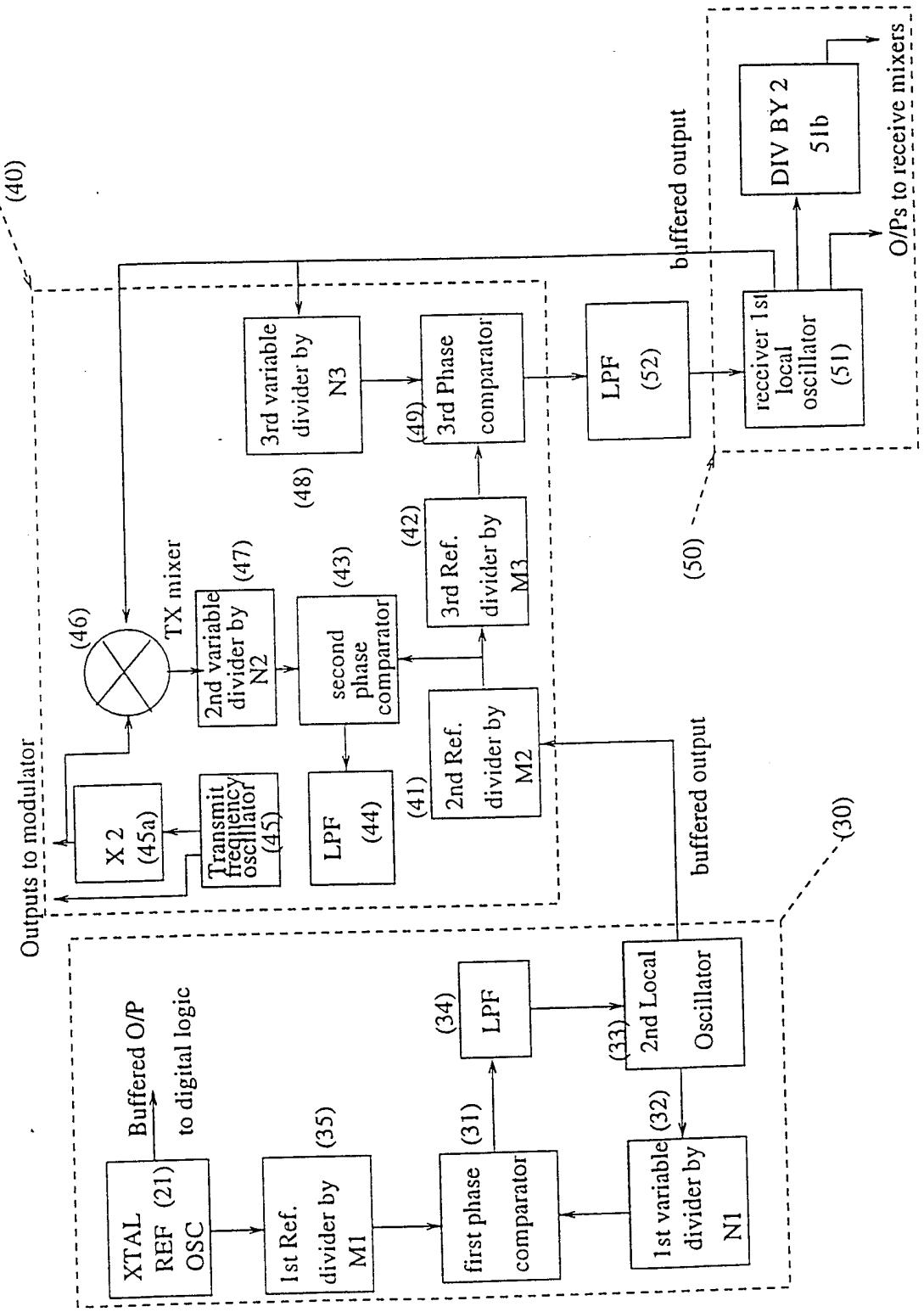


FIGURE 9: ALTERNATIVE WITH A DIVIDE BY 2 AND A DOUBLER

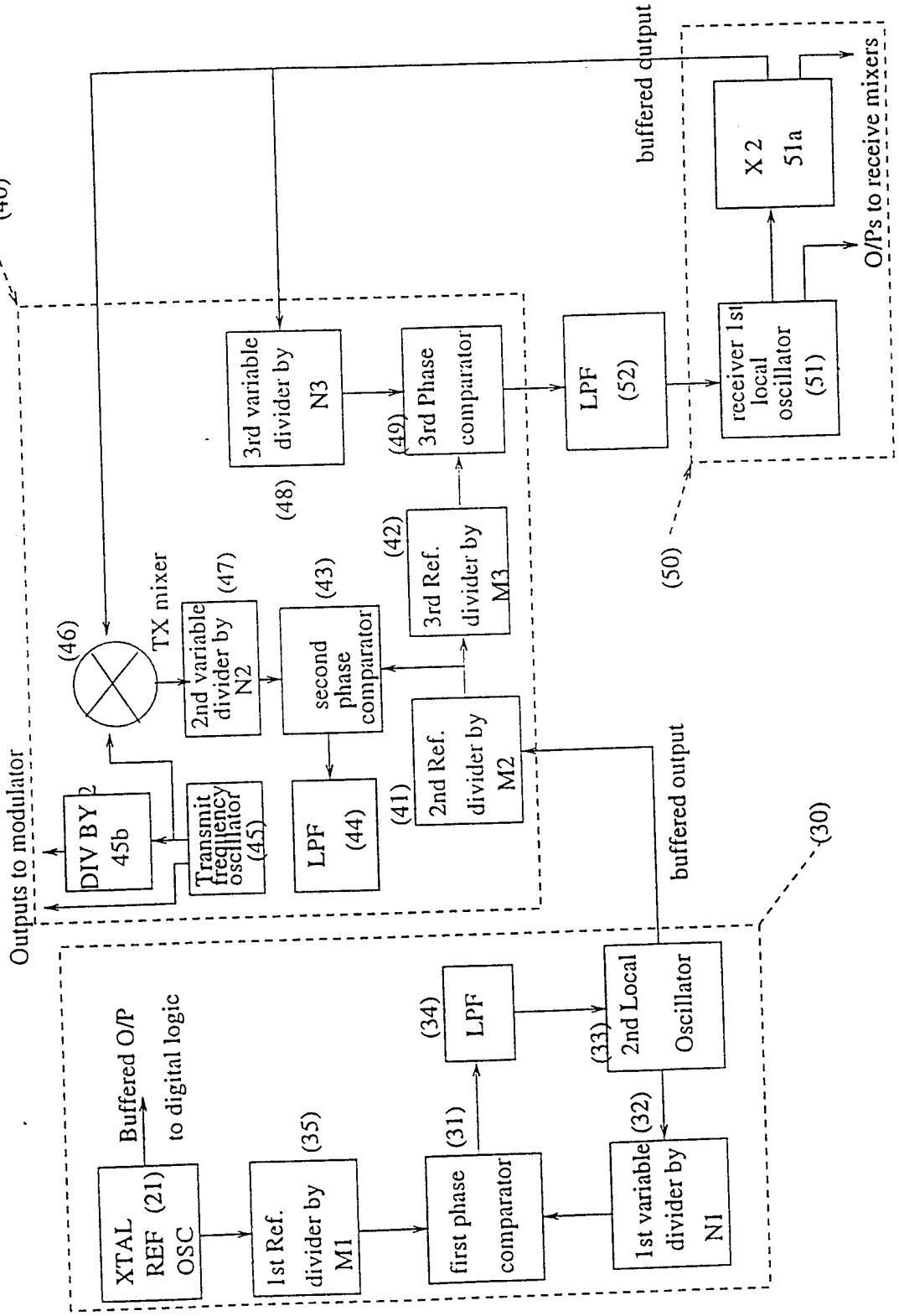


FIGURE 10: FIRST LO CONTROLLED AT LOWER FREQUENCY

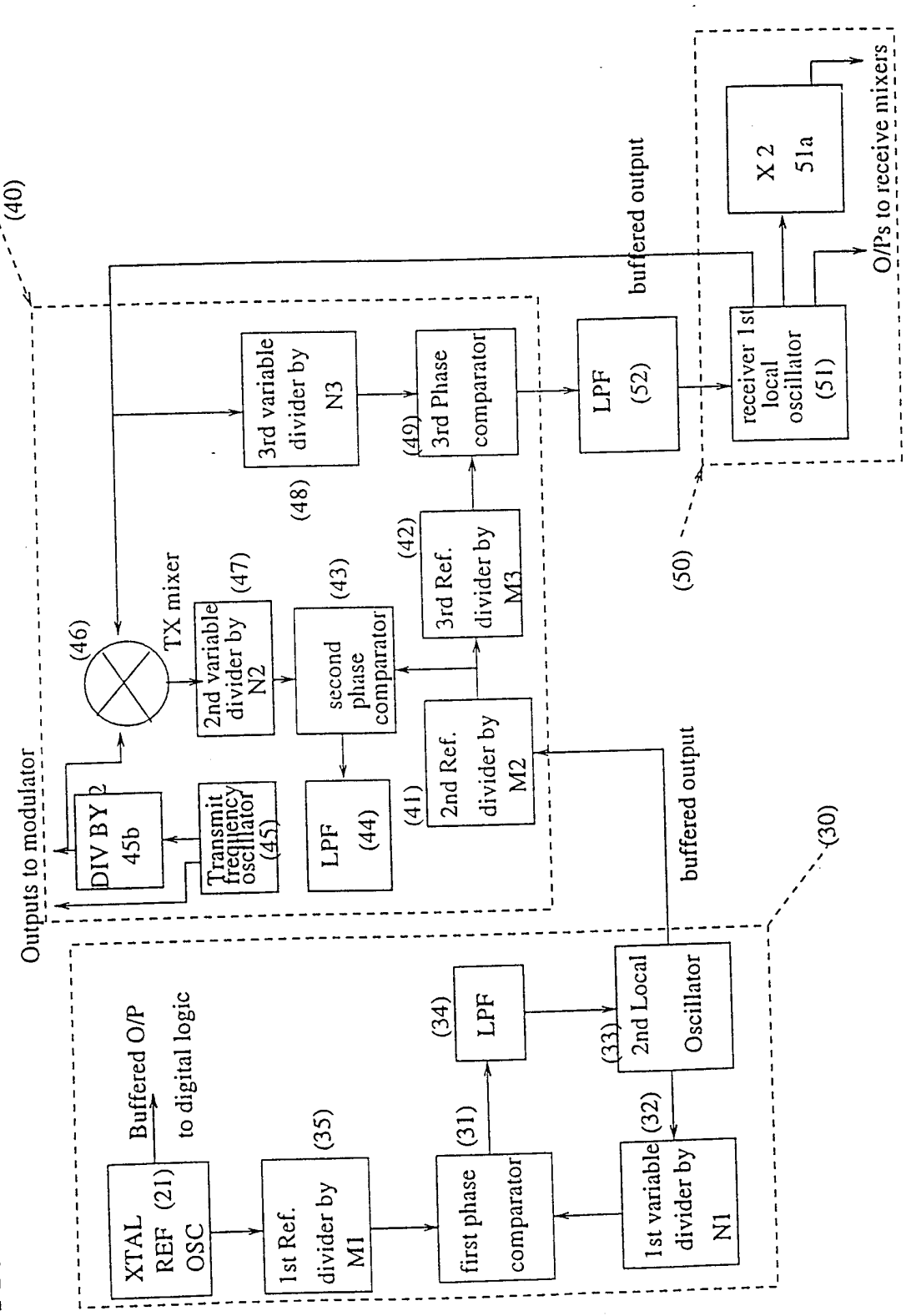


FIGURE 11: FIGURE 10 MODIFIED TO USE FREQUENCY HALVERS

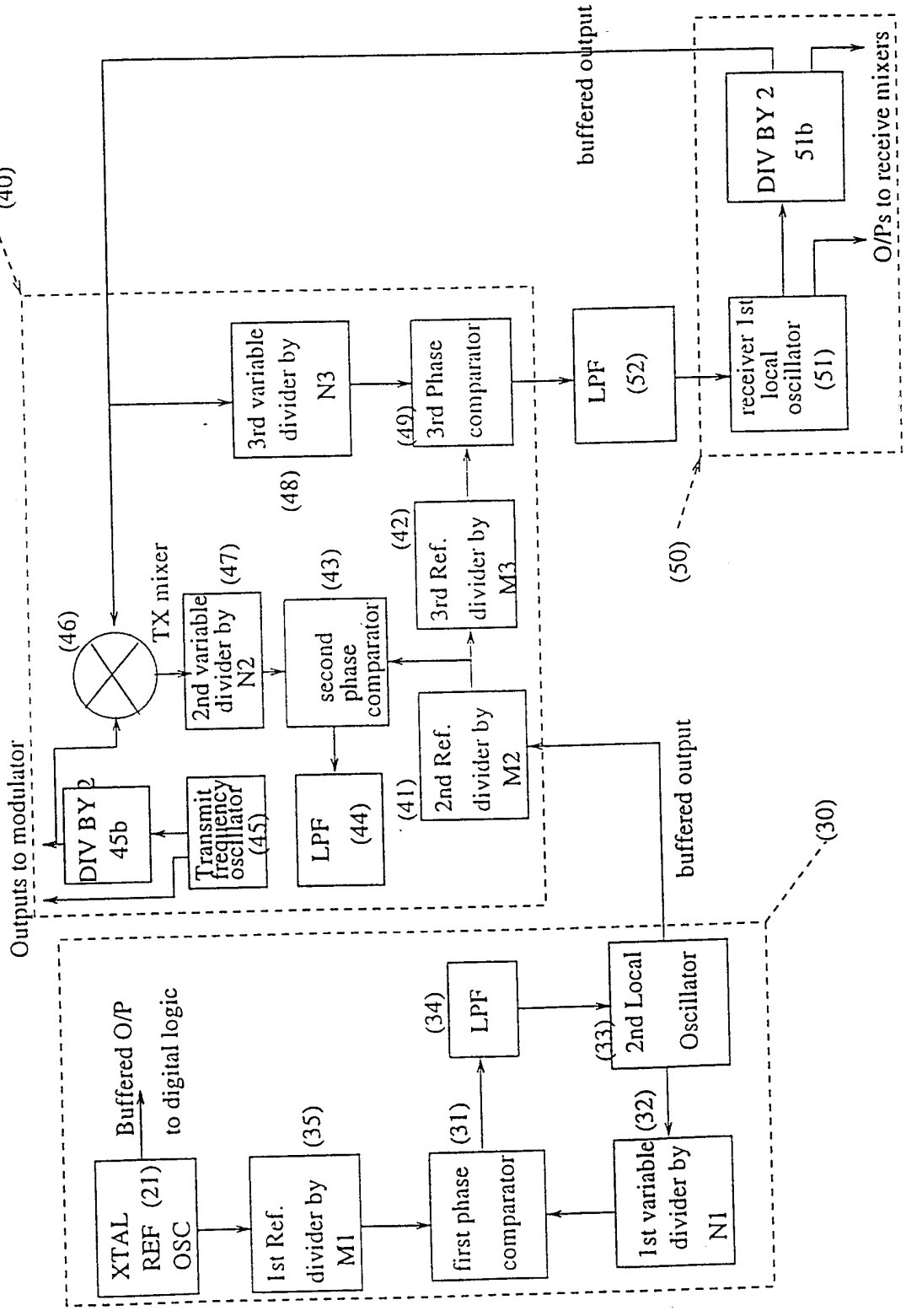


FIGURE 12: DUAL-MODE REFERENCE FREQUENCY DISTRIBUTION

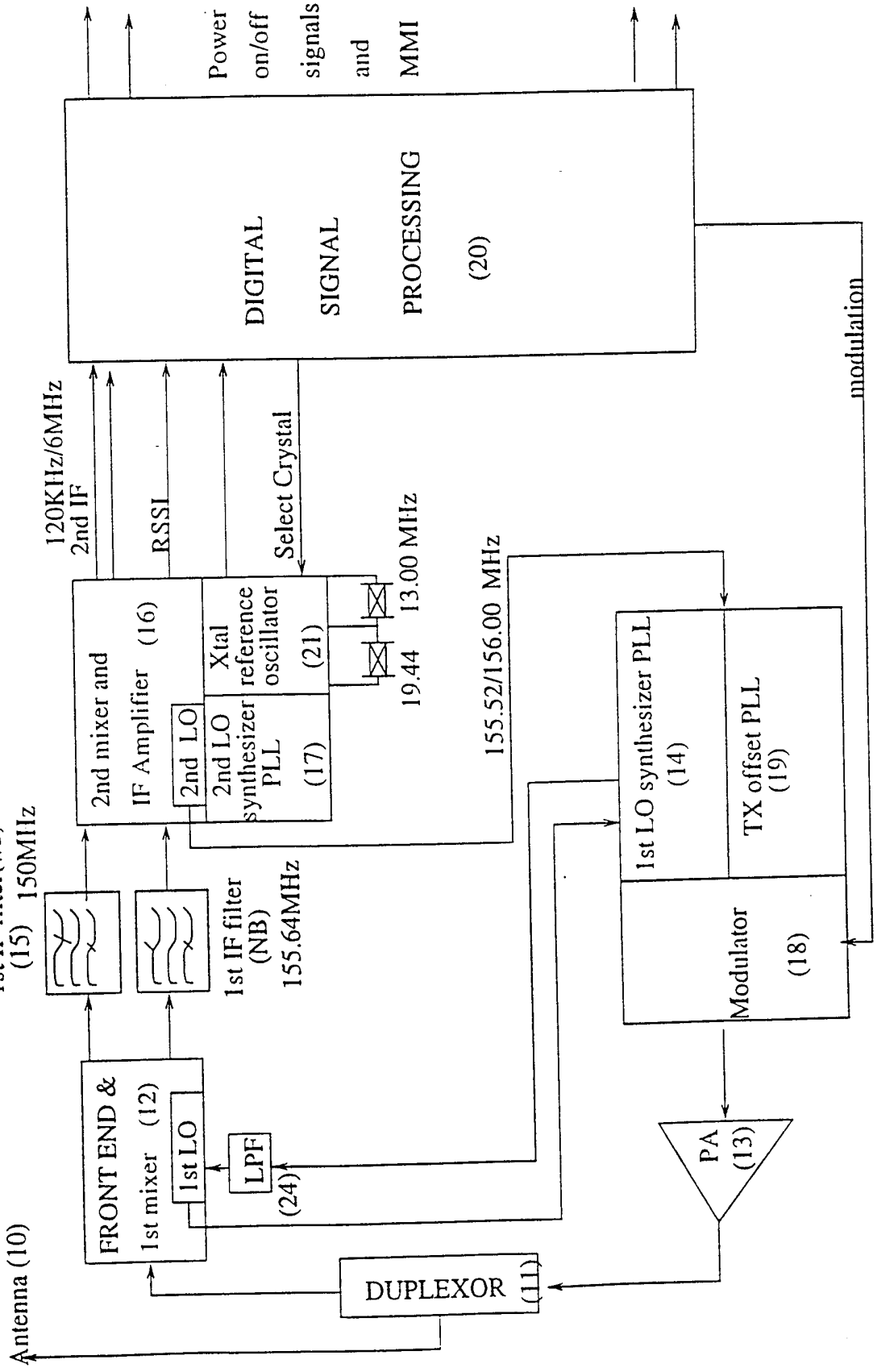


FIGURE 13: DIVIDER RATIOS FOR FIGURE 12

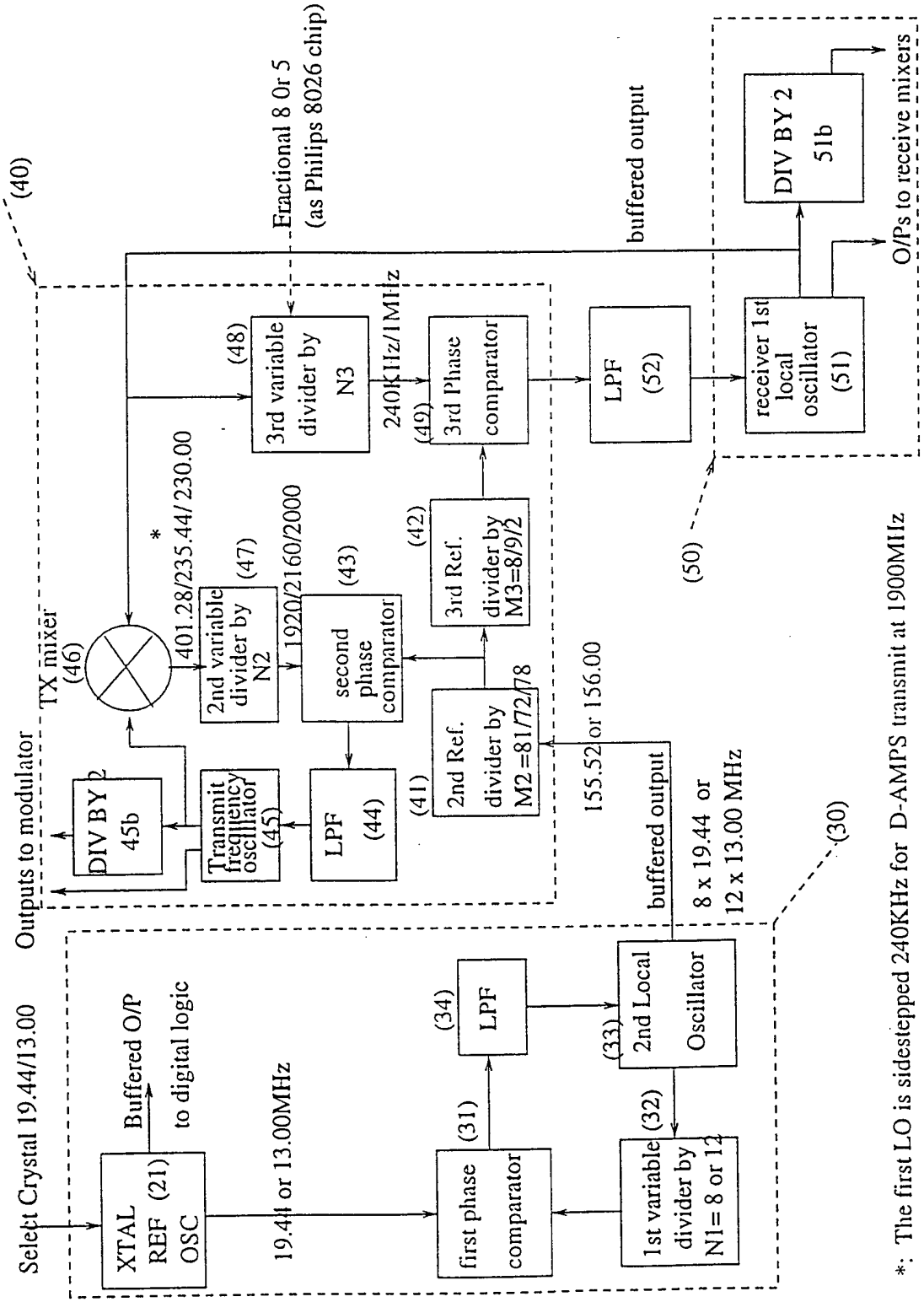


FIGURE 14: DUAL-MODE WITH I.F. HOMODYNE FOR PCS1900

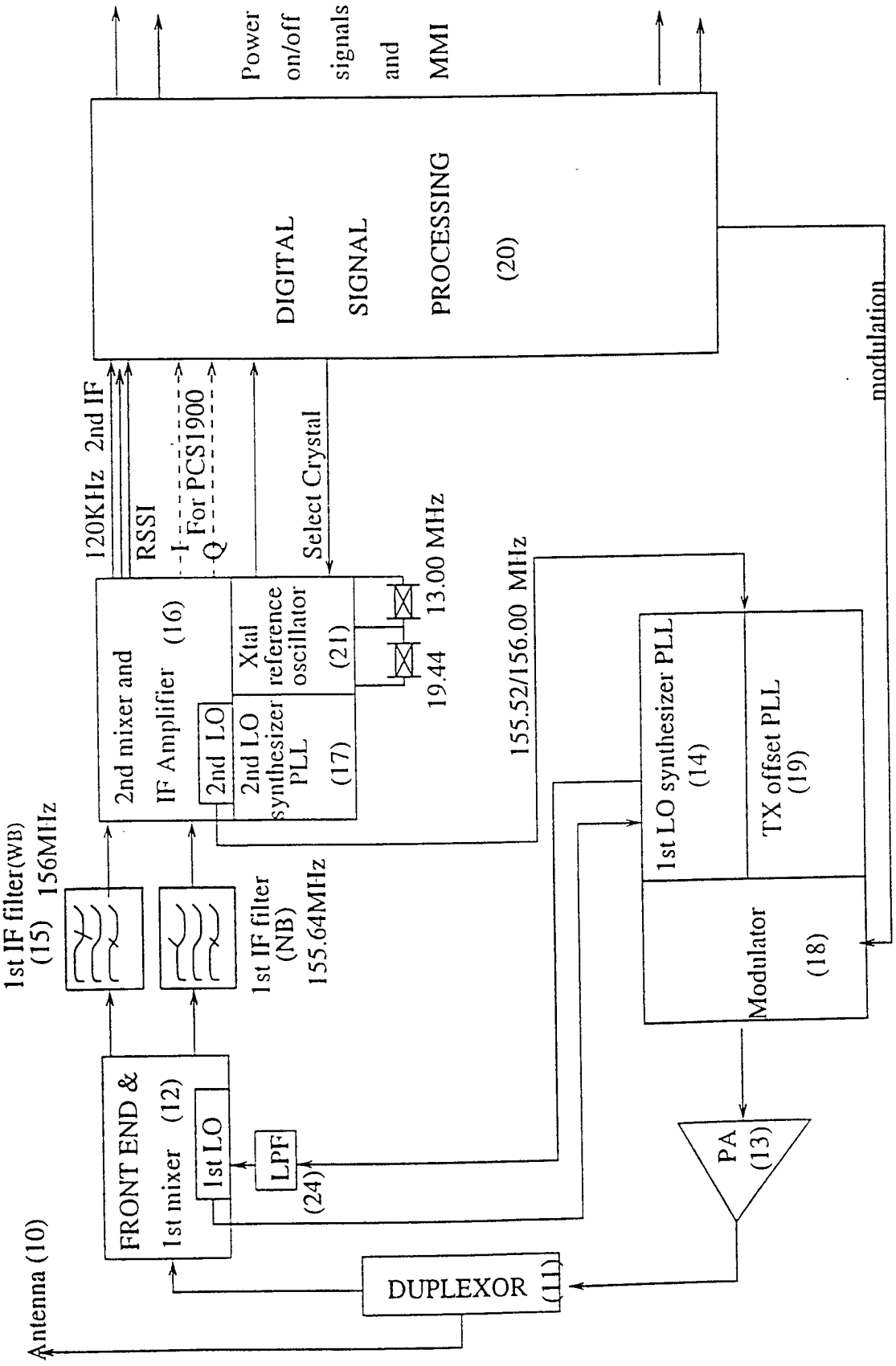


FIGURE 15: DUAL-MODE WITH SINGLE CRYSTAL

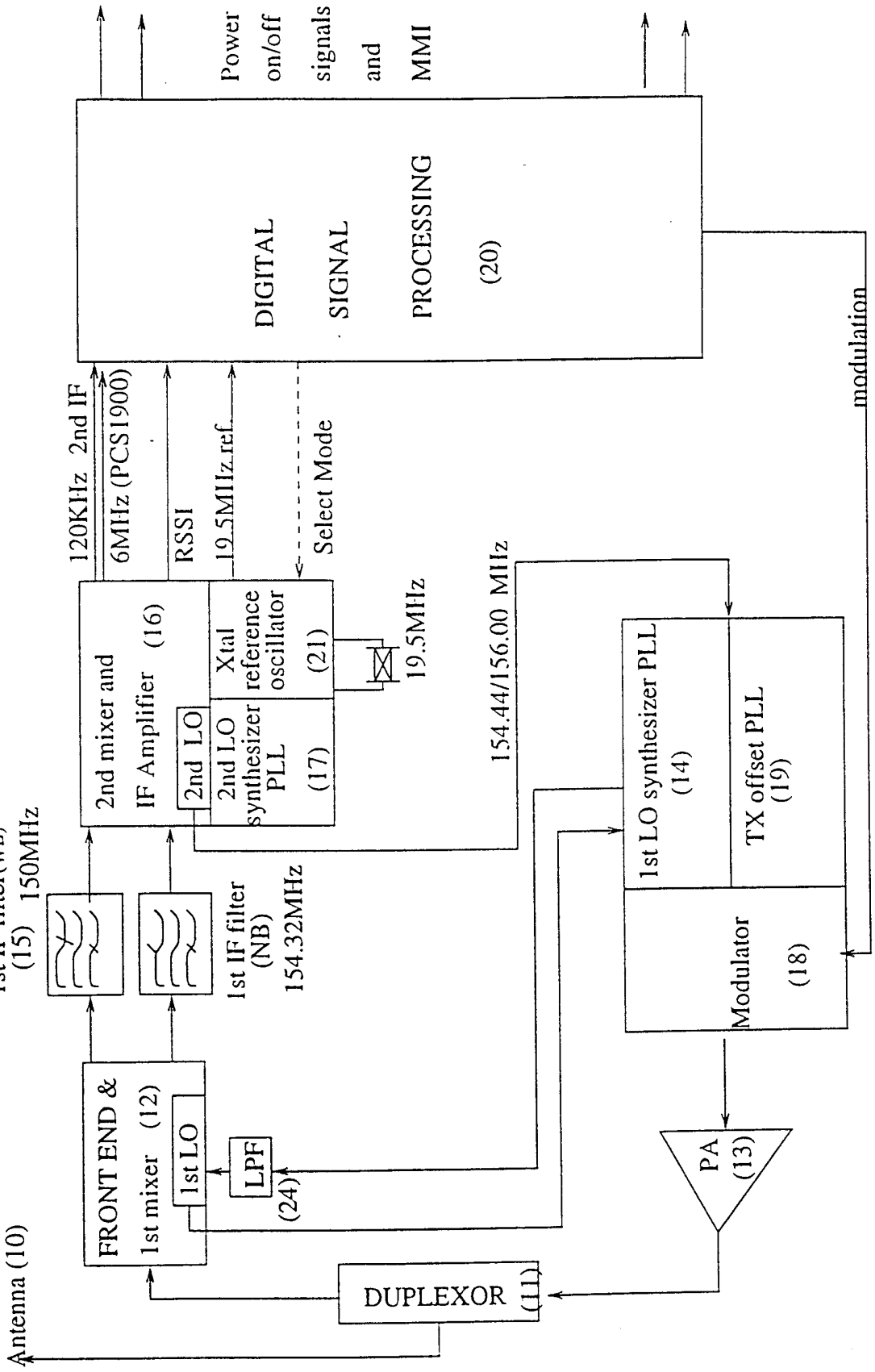


FIGURE 16: DIVIDER RATIOS FOR FIGURE 15

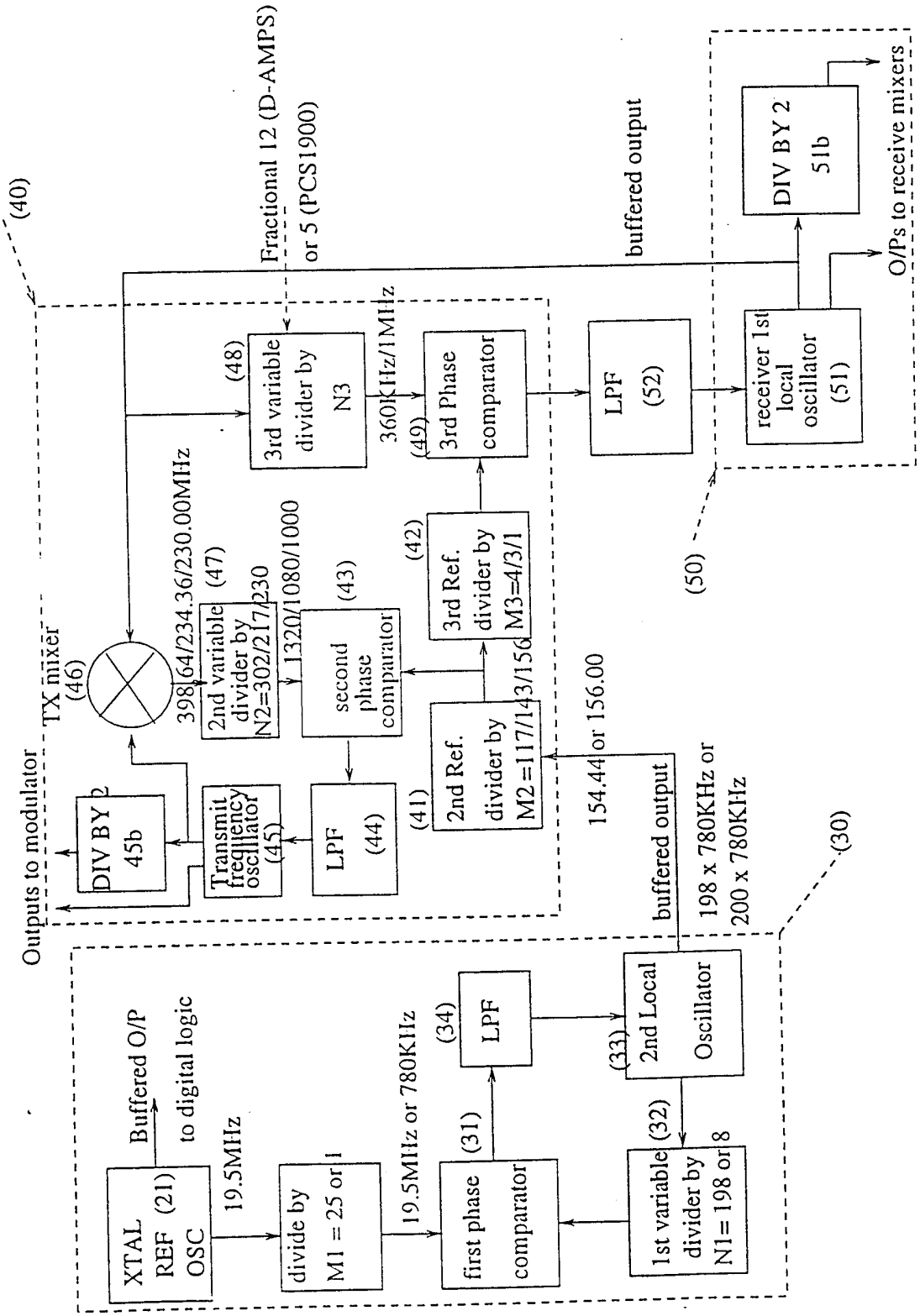


FIGURE 17: DUAL-MODE WITH TWO REFERENCE CRYSTALS

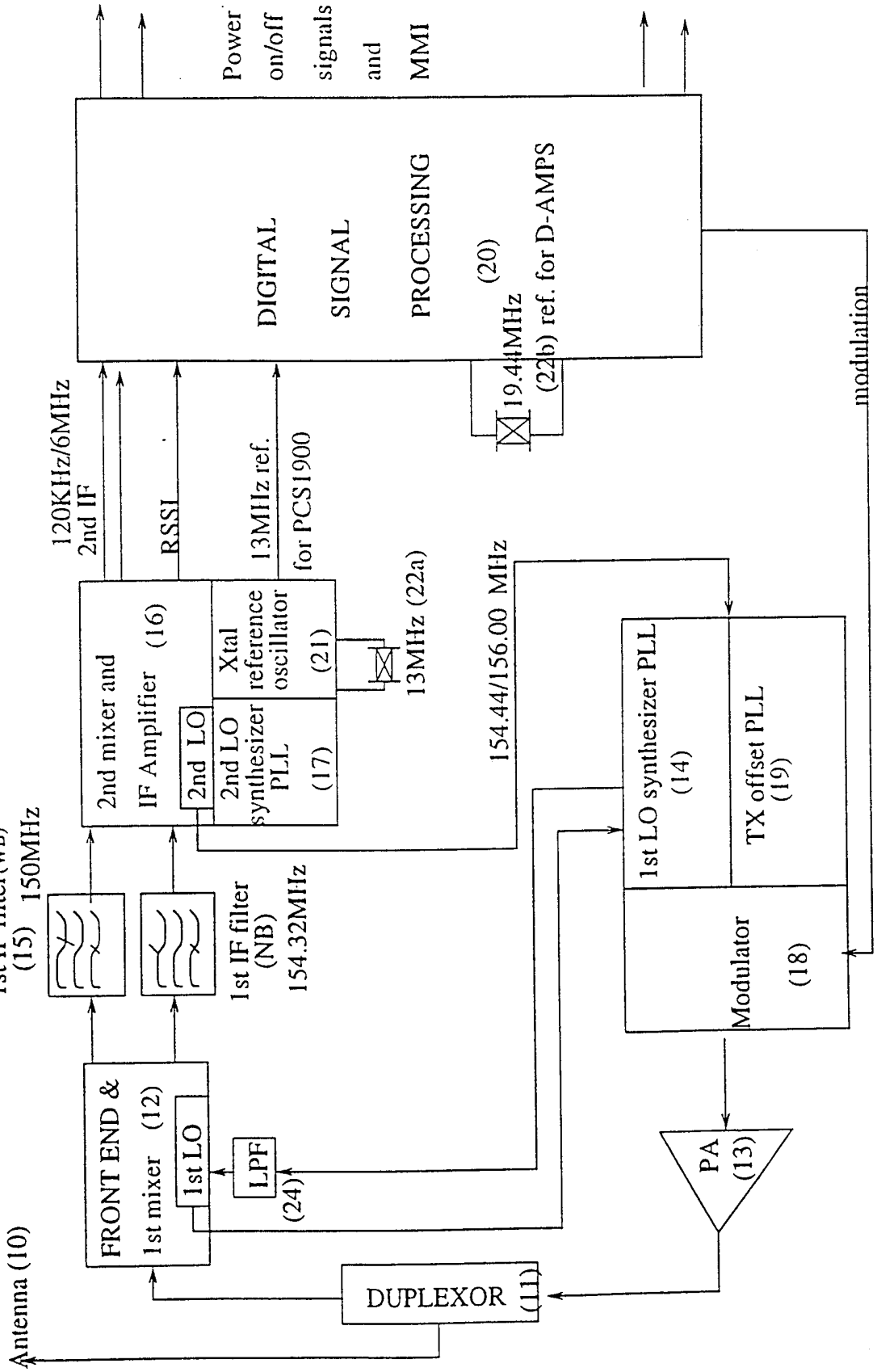


FIGURE 18: DIVIDER RATIOS FOR FIGURE 17

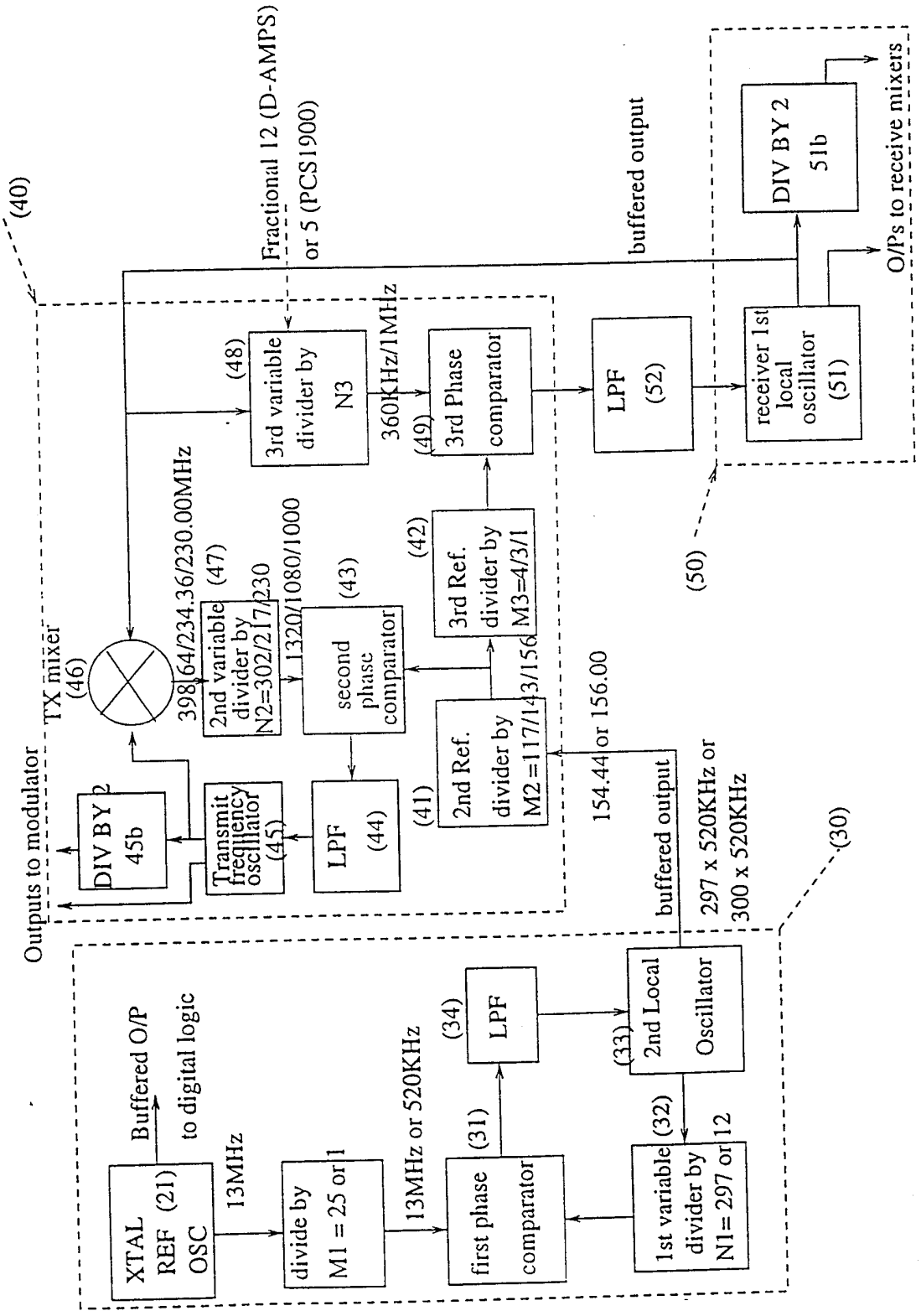


FIGURE 19: DIVIDER RATIOS TO ELIMINATE THE SECOND CRYSTAL

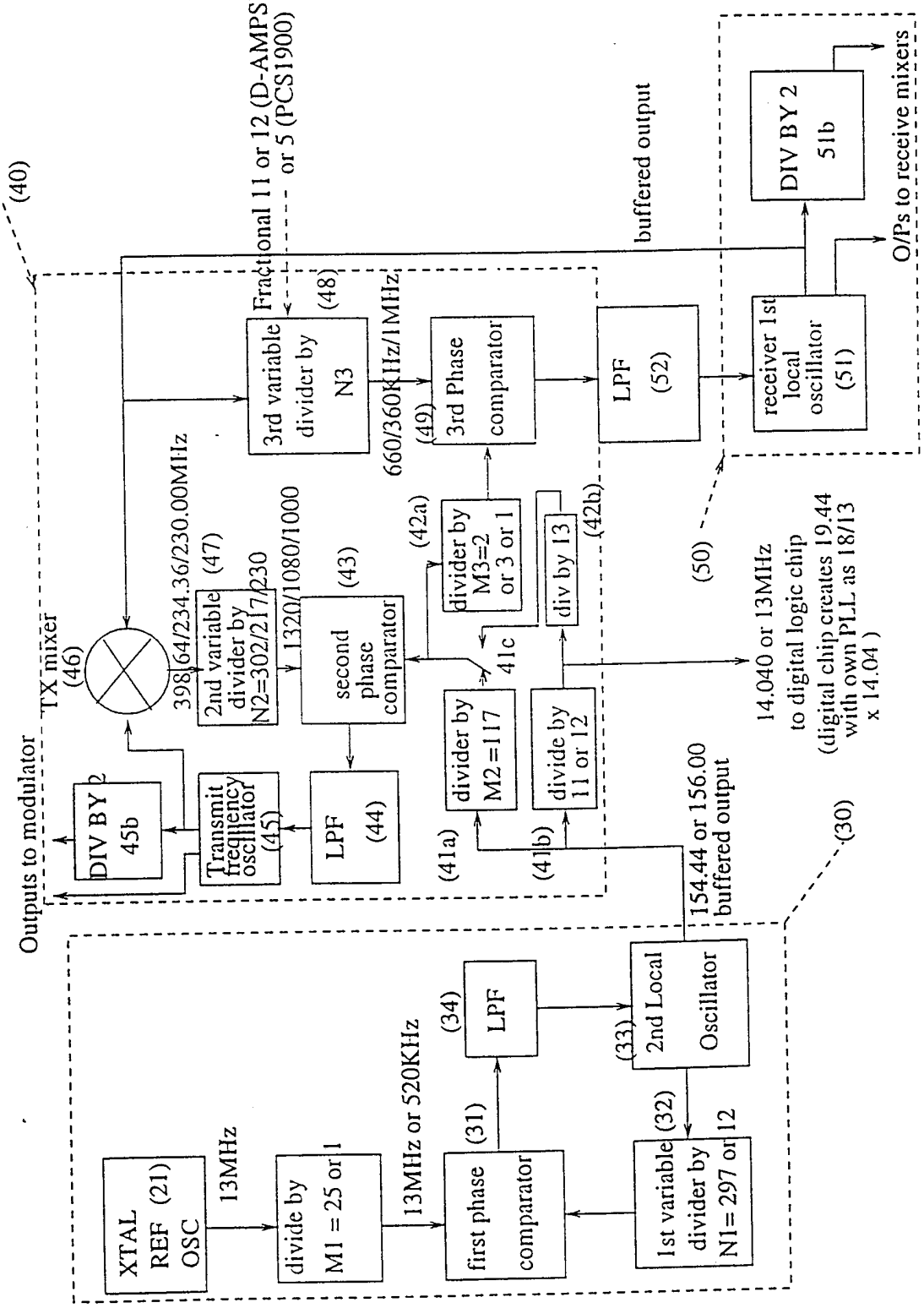


FIGURE 20: SKIP COUNTER TO GENERATE 194.4KS/S from 19.5MHz

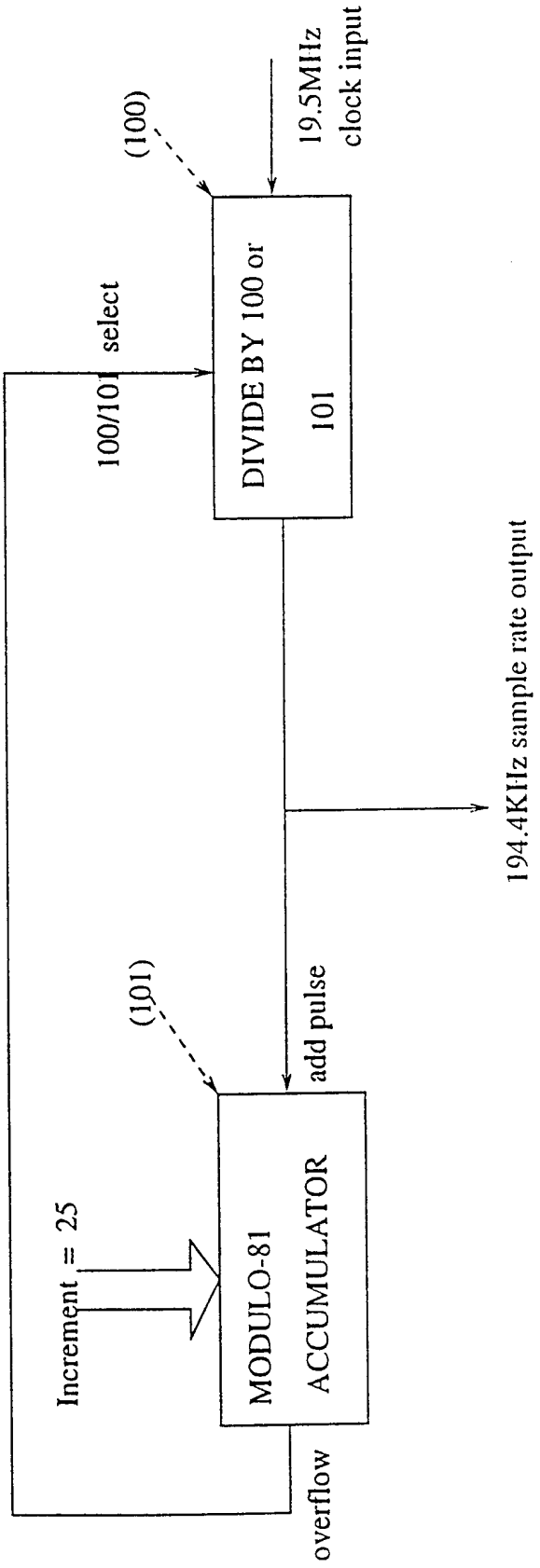
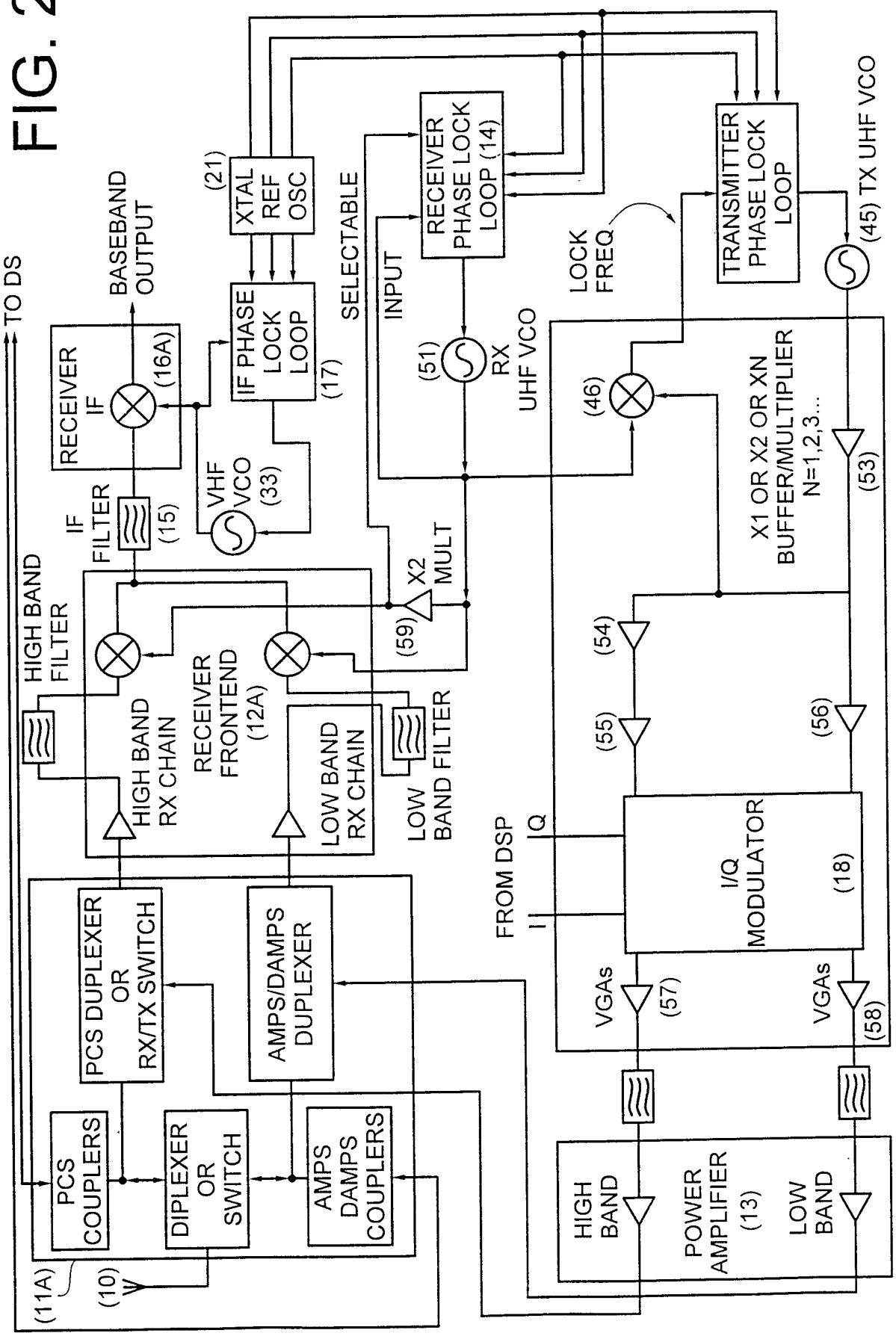


FIG. 21


TO DS
BASEBAND OUTPUT
(21) XTAL REF OSC
SELECTABLE INPUT
RECEIVER PHASE LOCK LOOP (14)
TRANSMITTER PHASE LOCK LOOP
(45) TX UHF VCO
LOCK FREQ
RECEIVER IF
(16A)
IF PHASE LOCK LOOP
(17)
(51) RX UHF VCO
(46)
X1 OR X2 OR XN BUFFER/MULTIPLIER N=1,2,3...
(53)
IF FILTER
(15)
VHF VCO
(33)
X2 MULT
(59)
(54)
(55)
(56)
HIGH BAND FILTER
RECEIVER FRONTEND
(12A)
HIGH BAND RX CHAIN
LOW BAND RX CHAIN
LOW BAND FILTER
FROM DSP
Q
I
I/Q MODULATOR
(18)
PCS DUPLEXER OR RX/TX SWITCH
AMPS/DAMPS DUPLEXER
VGAs
(57)
VGAs
(58)
PCS COUPLERS
DIPLEXER OR SWITCH
AMPS DAMPS COUPLERS
HIGH BAND
POWER AMPLIFIER
(13)
LOW BAND
(11A)
(10)

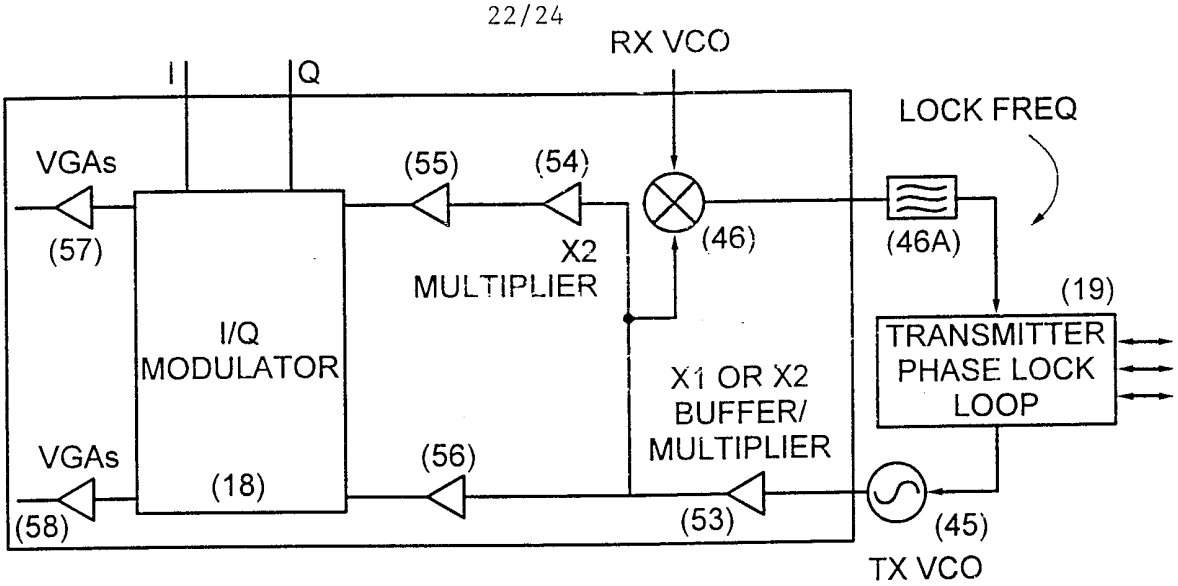

RX VCO
I
Q
LOCK FREQ
VGAs
(57)
(55)
(54)
X2
MULTIPLIER
(46)
(46A)
(19)
I/Q
MODULATOR
TRANSMITTER
PHASE LOCK
LOOP
X1 OR X2
BUFFER/
MULTIPLIER
VGAs
(58)
(18)
(56)
(53)
(45)
TX VCO

FIG. 22

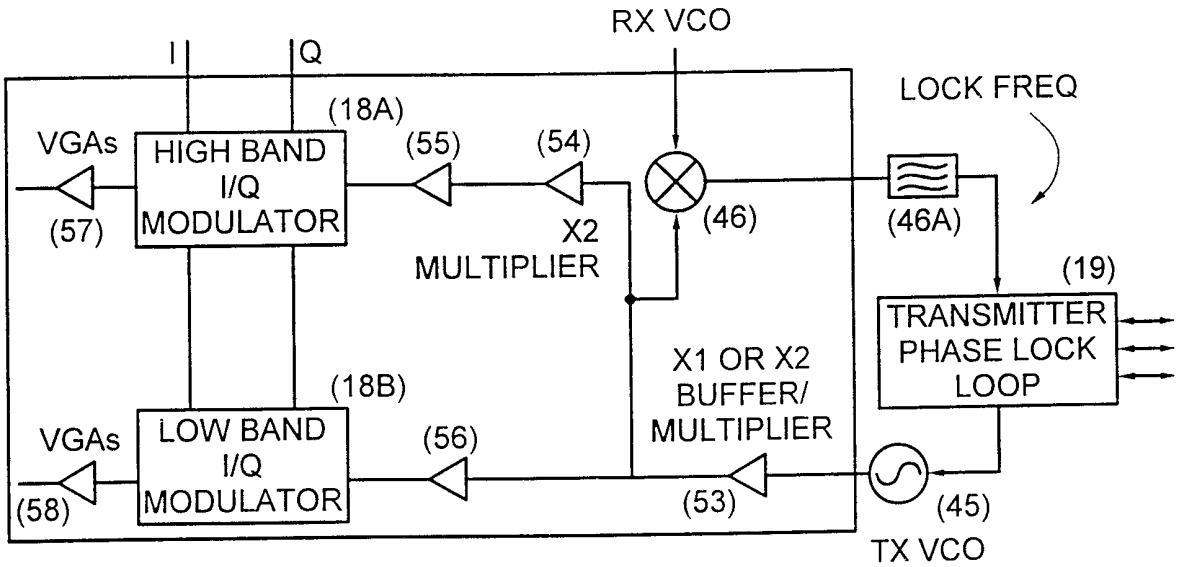

RX VCO
I
Q
LOCK FREQ
(18A)
VGAs
HIGH BAND
I/Q
MODULATOR
(55)
(54)
(57)
X2
MULTIPLIER
(46)
(46A)
(19)
TRANSMITTER
PHASE LOCK
LOOP
X1 OR X2
BUFFER/
MULTIPLIER
(18B)
VGAs
LOW BAND
I/Q
MODULATOR
(56)
(58)
(53)
(45)
TX VCO

FIG. 23

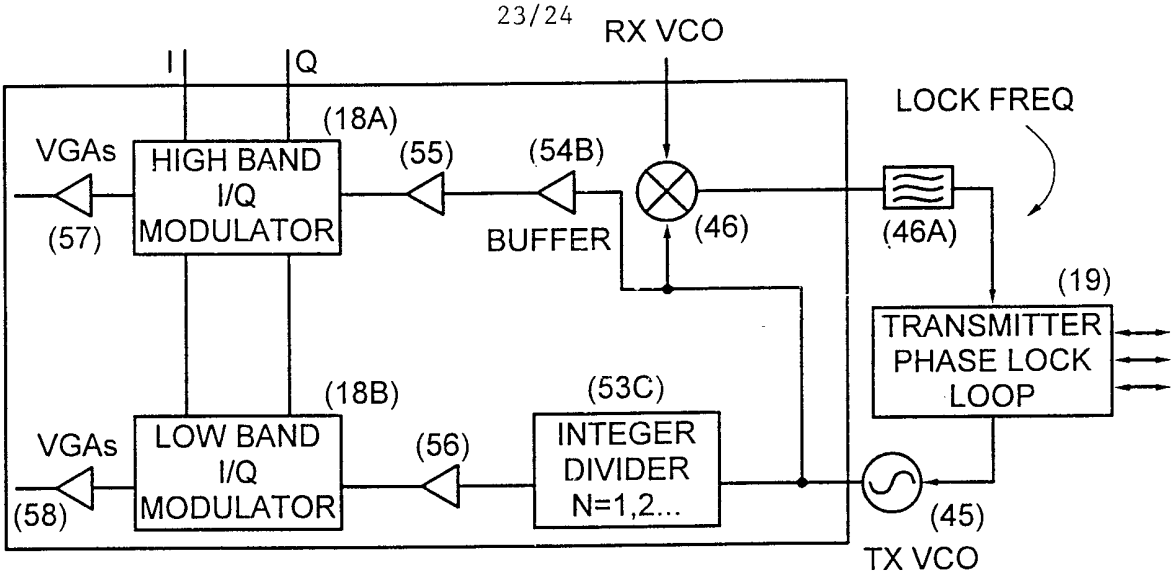

RX VCO
I
Q
LOCK FREQ
(18A)
VGAs
HIGH BAND I/Q MODULATOR
(55)
(54B)
(57)
BUFFER
(46)
(46A)
(19)
TRANSMITTER PHASE LOCK LOOP
(18B)
(53C)
VGAs
LOW BAND I/Q MODULATOR
(56)
INTEGER DIVIDER N=1,2...
(58)
(45)
TX VCO

FIG. 24

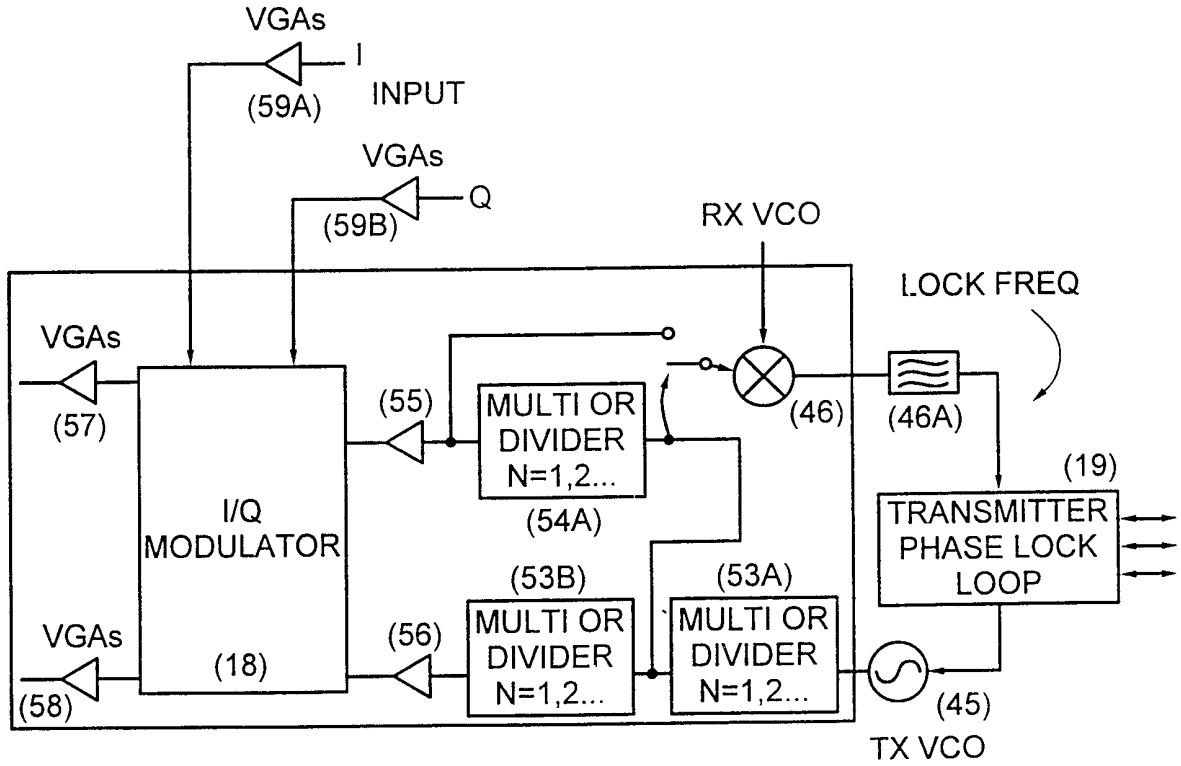

VGAs
I
(59A)
INPUT
VGAs
Q
(59B)
RX VCO
LOCK FREQ
VGAs
(57)
(55)
MULTI OR DIVIDER N=1,2...
(46)
(46A)
(54A)
(19)
TRANSMITTER PHASE LOCK LOOP
I/Q MODULATOR
(53B)
(53A)
VGAs
(56)
MULTI OR DIVIDER N=1,2...
MULTI OR DIVIDER N=1,2...
(18)
(58)
(45)
TX VCO

FIG. 25

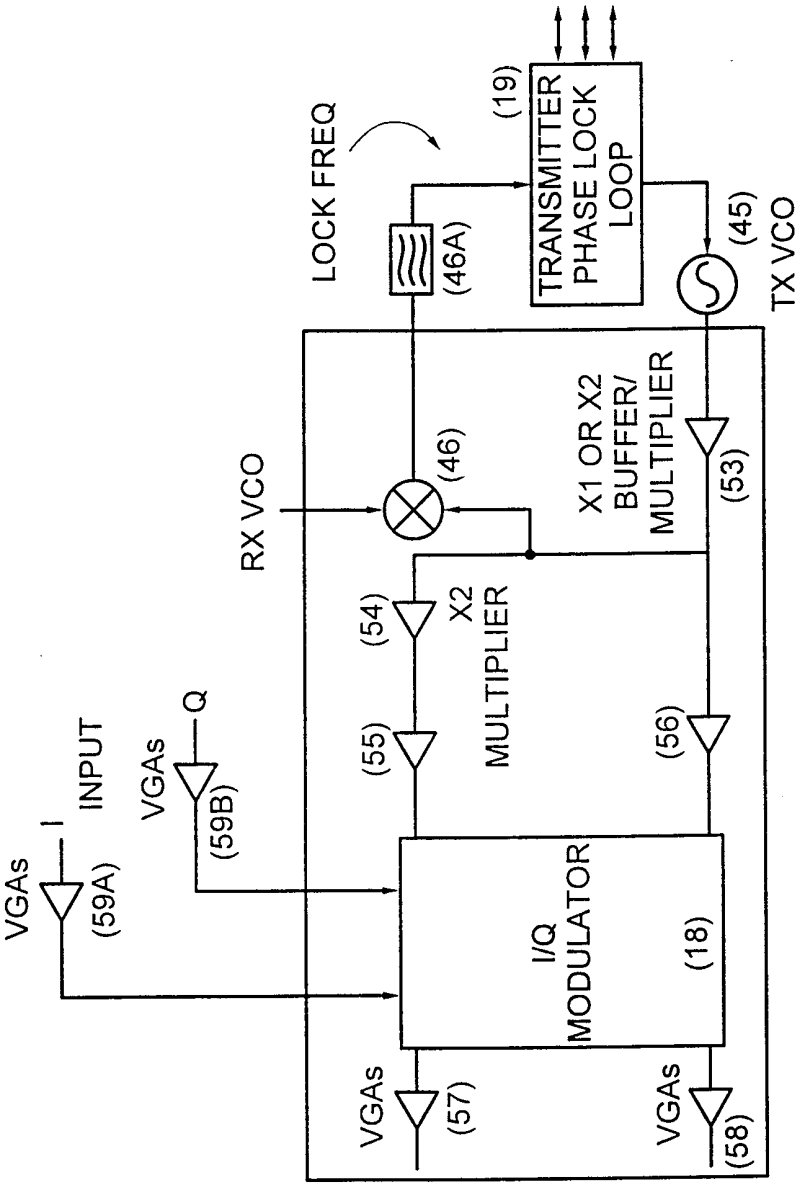

LOCK FREQ
(19)
TRANSMITTER PHASE LOCK LOOP
(46A)
(45)
TX VCO
RX VCO
(46)
X1 OR X2 BUFFER/ MULTIPLIER
(53)
(54)
X2 MULTIPLIER
(55)
(56)
VGAs
I
INPUT
(59A)
VGAs
Q
(59B)
I/Q MODULATOR
(18)
VGAs
(57)
VGAs
(58)

FIG. 26

INTERNATIONAL SEARCH REPORT

Interr ıal Application No
PCT/US 98/23216

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04B1/40 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04B H03D H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 535 432 A (DENT PAUL W) 9 July 1996 cited in the application see column 5, line 15 - column 7, line 46; figures 2,3	1,8,9, 11,18-20 2-7, 12-17
Y A	EP 0 798 880 A (NOKIA MOBILE PHONES LTD) 1 October 1997 see page 4, line 37 - page 7, line 24; figures 2,3A	2,4,6, 12,14,16 1,3,5, 7-11,13, 15,17-20
Y A	EP 0 800 283 A (NOKIA MOBILE PHONES LTD) 8 October 1997 see abstract; figure 3	3,5,7, 13,15,17 1,2,4,6, 8-12,14, 16,18-20

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 March 1999	26/03/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Andersen, J.G.

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interi nal Application No
PCT/US 98/23216

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5535432 A	09-07-1996	AU 691042 B	07-05-1998
		AU 3729795 A	29-03-1996
		EP 0781475 A	02-07-1997
		FI 971055 A	14-05-1997
		JP 10505981 T	09-06-1998
		WO 9608883 A	21-03-1996
		US 5610559 A	11-03-1997
EP 0798880 A	01-10-1997	FI 961428 A	30-09-1997
EP 0800283 A	08-10-1997	FI 100286 B	31-10-1997
		JP 10032520 A	03-02-1998