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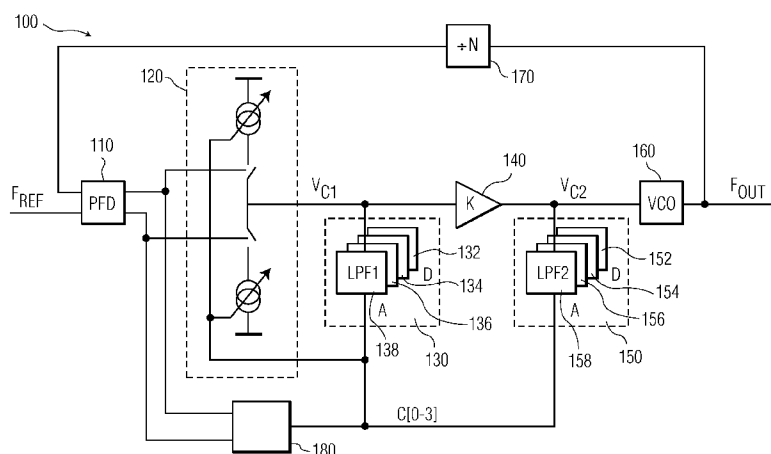
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Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: PHASE-LOCKED LOOP SYSTEMS USING ADAPTIVE LOW-PASS FILTERS IN SWITCHED BANDWIDTH FEEDBACK LOOPS



(57) Abstract: Methods and systems directed toward a PLL circuit (100) including a local lock detector (180) receiving an error signal and providing a lock signal, and a charge pump (120) for receiving the error signal and providing a charge signal. A loop filter provides a first loop filter bandwidth and a second loop filter bandwidth. The loop filter includes a first low-pass filter (130) configured to receive the charge and lock signals, alter a filter characteristic in response to the lock signal, and provide a first filter signal. The loop filter includes a second low-pass filter (150) configured to receive the first filter and lock signals, alter a filter characteristic in response to the lock signal, and provide a loop filter signal. The PLL circuit includes a VCO (160) for receiving the loop filter signal and providing an output signal, and a divider (170) for receiving the output signal and dividing it to provide the reference signal.



— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 097 227 A (HAYASHI TOMOHIRO [JP]) 1 August 2000 (2000-08-01) column 3, line 62 - column 5, line 39 column 6, line 43 - column 9, line 19 figures 4,7-10 ----- -/--	1-10



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BISHOP A J ET AL: "Adaptive phase locked loop for video signal sampling" PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. SAN DIEGO, MAY 10 - 13, 1992, PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. (ISCAS), NEW YORK, IEEE, US, vol. VOL. 4 CONF. 25, 3 May 1992 (1992-05-03), pages 1664-1667, XP010061490 ISBN: 0-7803-0593-0 page 1664, column 2, line 21 - page 1666, column 2, line 5 figures 1-9 -----	1,2,7,8

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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