



- (51) International Patent Classification:
G11C 11/00 (2006.01)
- (21) International Application Number:
PCT/US2014/068394
- (22) International Filing Date:
3 December 2014 (03.12.2014)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
61/911,393 3 December 2013 (03.12.2013) US
- (71) Applicant: **RAMBUS INC.** [US/US]; 1050 Enterprise Way, Suite 700, Sunnyvale, CA 94089 (US).
- (72) Inventors; and
(71) Applicants : **SEKAR, Deepak Chandra** [—/US]; 1050 Enterprise Way, Suite 700, Sunnyvale, CA 94089 (US). **HAUKNESS, Brent S.** [—/US]; 1050 Enterprise Way, Suite 700, Sunnyvale, CA 94089 (US). **BATEMAN, Bruce L.** [—/US]; 3808 Monte Sereno Terrace, Fremont, CA 94539 (US).
- (74) Agents: **COWGER, Graciela G.** et al.; 1140 SW 11th Avenue, Suite 400, Portland, OR 97205 (US).
- (81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: REDUCED CURRENT MEMORY DEVICE

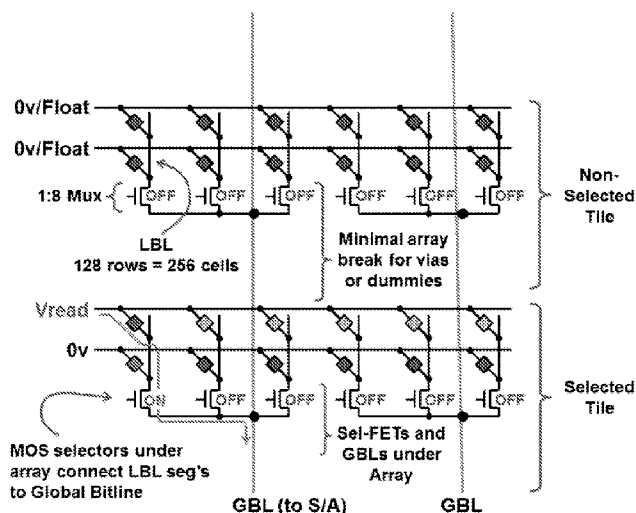


Fig. 1

(57) Abstract: A memory device includes a local bit line coupled to a plurality of memory cells and a global bit line through first and second selectable parallel paths having first and second impedances, respectively. The first path is active in at least one of a set operation or a forming operation and the second path is active in a reset operation. A select device to select a memory element includes a drain having a first doping level and a source having a second doping level lower than the first doping level, wherein the device is configured to provide a first on impedance or a second on impedance to the resistive memory element in response to a control signal.



Published:

— with international search report (Art. 21(3))

— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

REDUCED CURRENT MEMORY DEVICE

Technical Field

[0001] We disclose a reduced current memory device.

Background

[0002] Non-volatile memory devices that retain stored data in the absence of power are pervasively used in many electronic products. Unfortunately, many non-volatile memory devices have limitations that make them unsuitable for use as primary storage for these products including higher cost and lower performance when compared to volatile memory devices such as dynamic random access memory (DRAM). Examples of non-volatile memory devices include read-only memory (ROM), flash memory, ferroelectric random access memory (FRAM), resistive random access memory (RRAM), phase change memory, and the like.

[0003] RRAM, and filamentary RRAM in particular, have recently gained development momentum. A challenge to RRAM device commercialization is high write current requirements resulting from long bit lines having high capacitance. When the RRAM cell switches, capacitive surge currents from long bit lines discharge through the cell making the filament wider. Relatively high write currents are needed to break the wider filament. For example, if the capacitance of a bit line is 0.1pF and the RRAM switches in 1ns at 2V, the surge current is given by:

$$I = C \times dv/dt = 0.1 \times 2V/1ns = 200uA$$

[0004] This 200uA current during a SET operation often requires a similar 200uA current during a RESET operation, which, in turn, results in a power hungry RRAM device that reduces battery life. Many electronic products, however, require extended battery life. A need exists, therefore, for an improved reduced current memory device.

Brief Drawings Description

[0005] Figure 1 is a diagram of an embodiment of a memory device according to the present disclosure.

[0006] Figure 2 is a diagram of another embodiment of a memory device according to the present disclosure.

[0007] Figures 3A and 3B are diagrams of yet another embodiment of a memory device according to the present disclosure.

[0008] Figure 4A is a diagram of an embodiment of a select device according to the present disclosure.

[0009] Figures 4B and 4C are diagrams of an embodiment of a select device with a reversed and forward biased junction, respectively.

[0010] Figure 5 is a graph of a simulation of an embodiment of a select device according to the present disclosure.

[0011] Figure 6 is a diagram of an embodiment of a select device according to the present disclosure.

[0012] Figure 7 is a diagram of an embodiment of a memory device according to the present disclosure.

[0013] Figures 8A and 8B are diagrams of an embodiment of a method of achieving asymmetric source/drains according to the present disclosure.

Detailed Description

[0014] Figure 1 is a diagram of an embodiment of a memory device 100 according to the present disclosure. Referring to Figure 1, memory device 100 comprises an array of memory elements 102 (only some of which are labeled) arranged in vertical columns and horizontal rows in portions 103. Each memory element 102 comprises one transistor (1T) 104 and one resistive memory element (1R) 106, hence the 1T-1R moniker. A person of ordinary skill in the art will recognize that memory element 102 may comprise any type of two-terminal rewritable memory element capable of programming to a selective one of two or more memory states. In one embodiment, a memory element 102 comprises a discrete, non-volatile, re-writable resistive memory cell made from any number of materials (e.g., CMO) known to a person of ordinary skill in the art. In other embodiments, memory element 102 may comprise a filamentary resistive random access memory (RRAM) cell, an interfacial RRAM cell, a magnetoresistive RAM (MRAM) cell, a phase change element (e.g., chalcogenides including alloys of germanium, antimony, and tellurium), a memristor memory element, and a programmable metallization cell (e.g., conductive bridging RAM (CBRAM) cell). A person of ordinary skill in the art will recognize that other types of memory elements can be used, whether based on resistive states or on some other memory storing mechanism, whether re-writable or not, or whether volatile or not.

[0015] Each portion 103 is associated with one of (L+1) groups of word lines (WL) 110 and one of (M+1) global bit lines (GBLs) 112, where L and M are integers greater than or

equal to zero. Each portion 103 is also associated with one of (N+1) groups of local bit lines (LBL) 108 electrically coupled to a number of memory elements 102, where N is an integer greater than or equal to zero. Each memory element 102 is electrically coupled to both an LBL 108 and a WL 110. Each LBL 108 is electrically coupled to a pass gate transistor 113 having a gate controlled by column decoder 114, which is well-known to a person of ordinary skill in the art and not discussed in any further detail herein. LBLs 108, WLs 110, and GBLs 112 may comprise conductive material, e.g., metal, metal containing compositions, conductively-doped semiconductor materials, and the like.

[0016] The number of memory elements 102 per LBL 108 is set during design and determined by a number of factors, including but not limited to overall memory size, operating parameters, program or erase operation parameters, type of memory element 102, parasitic capacitance in both the memory element 102 and the LBL 108, resistance and capacitance of the LBL 108 associated with the GBL 112, and the like. Examples of operating parameters include but are not limited to read current, write current, program current, erase current, read speed, write speed, read disturb, write disturb, and the like.

[0017] GBL 112 is associated with one of the portions 103 and is electrically coupled to the LBLs of that portion through a first selectable parallel path 116 and a second selectable parallel path 118. First and second selectable parallel paths 116 and 118 may have first and second impedances, respectively, which may be selected using control signals 124A and 124B based on the specific operation type to be performed on memory element 102, e.g., SET, RESET, or FORM. Control signals 124A and 124B may be distinct or indistinct from one another and may be generated by a controller (not shown), design of which is well known to a person of ordinary skill in the art.

[0018] In an embodiment, first selectable parallel path 116 is selected or turned on to present a first impedance between GBL 112 and LBLs 108 during a first predetermined operation type to a given portion 103, e.g., SET or FORM, which results in dampening capacitive surge currents from capacitance associated with the GBL 112. A length of the LBLs 108 is kept relatively short to avoid transients from the capacitance associated with the LBLs 108. Conversely, second selectable parallel path 118 is selected or turned on to present a second impedance, which is lower relative to the first impedance of path 116, to drive large currents through memory elements 102 during a second predetermined operation type, e.g., RESET. By providing parallel selectable paths 116 and 118, memory device 100 may present different impedances between the GBL 112 and corresponding LBLs 108 that

advantageously conserve power by reducing the current needed in a predetermined operation type, e.g., SET.

[0019] In an embodiment, first selectable parallel path 116 comprises a first switching element 120, e.g., transistor T1, having a first impedance when selected in response to the first operation type, e.g., SET or FORM, to be performed on a memory element 102. Likewise, second selectable parallel path 118 comprises a second switching element 122, e.g., transistor T2, having a second impedance when selected in response to the second operation type, e.g., RESET, to be performed on a memory element 102. The first and second operations may be different from one another. First and second switching elements 120 and 122 may both be turned on during certain predetermined operation types, e.g., SET, RESET, or FORM.

[0020] In an embodiment, the first and second switching elements 120 and 122 are active or turned on in response to control signals 124A and 124B, which may be distinct or indistinct from one another and may be generated by a controller or other device (not shown) well known to a person of ordinary skill in the art.

[0021] In an embodiment, first and second switching elements 120 and 122 are of different types, e.g., second switching element 122 may be a low drive current transistor, which may be provided by, e.g., adjusting or tuning the source or drain during manufacture. Put differently, in such an embodiment, the first and second impedances are made to vary by changing the source or drain doping of each of the first and second switching elements 120 and 122, respectively, during their manufacture. The impedance presented by each of first and second switching elements 120 and 122 may change by orders of magnitude depending on the magnitude of the source and drain implant dose made to each of first and second switching elements 120 and 122. In an embodiment, first switching element 120 comprises a first source and drain doping level and second switching element 122 comprises a second source and drain doping level different or asymmetric from the first source and drain doping level. The first source and drain doping level may be lower than the second source and drain doping level by at least a factor of ten, e.g., $1\text{E}19/\text{cm}^3$ and $5\text{E}20/\text{cm}^3$.

[0022] In other embodiments, first and second switching elements 120 and 122 may present first and second impedances, respectively, e.g., by manufacturing first and second switching elements 120 and 122 to have different threshold voltages, different oxide thickness, and the like.

[0023] In an embodiment shown in Figure 2, memory device 200 comprises first selectable parallel path 216 and second selectable parallel path 218 having first and second impedances, respectively, and being controllable by control signals 224A and 224B. Control signals 224A and 224B may be distinct or indistinct from one another and may be generated by a controller or other device (not shown) well known to a person of ordinary skill in the art. GBL 212 may be associated with one of the portions 203 and may be electrically coupled to a corresponding group of LBLs of that portion through first selectable parallel path 216 and second selectable parallel path 218. Each memory element 202 is electrically coupled to both an LBL 208 and a WL 210. Each LBL 208 is electrically coupled to selectable paths 216 and 218 through a pass gate transistor 213 having a gate controlled by column decoder 214, which is well-known to a person of ordinary skill in the art and not discussed in any further detail herein.

[0024] First selectable parallel path 216 comprises a first switching element 220, e.g., transistor T1, having the first impedance when selected or turned on in response to a first predetermined operation type, e.g., RESET, to be performed on a memory element 202. Second switching element 222, e.g., transistor T2, is serially coupled to a resistor 221, the combination having the second impedance when selected or turned on in response to a second predetermined operation type, e.g., SET or FORM, to be performed on a memory element 202. The first and second operations may be different from one another. First and second switching elements 220 and 222 may both be turned on in an operation type, e.g., SET, RESET, or FORM, to be performed on memory element 202. Resistor 221 may comprise a dielectric resistor, metal-polysilicon-metal resistor, or any other resistor type appropriate for the task that is known to a person of ordinary skill in the art.

[0025] In an embodiment, transistors T1 and T2 are of a similar type, but since transistor T2 is serially coupled to resistor 221, second selectable parallel path 218 has a higher impedance than first selectable parallel path 216 comprising T1 only. The higher impedance second selectable parallel path 218 may be selected or turned on to allow for a low drive current during SET or FORM operations while the lower impedance first selectable parallel path 216 may be turned on or selected when higher currents are needed.

[0026] In an embodiment, first selectable parallel path 216 and second selectable parallel path 218 may comprise a multiple gate device (not shown) with independently-controllable gates, e.g., a FinFET, in which one gate is turned on to allow for a low drive current during

SET or FORM operations or in which more than one gate or a different gate is turned on to drive high current through the memory cells 202 during a RESET operation.

[0027] Referring to Figures 3A and 3B, memory device 300 comprises an array of memory elements 302 (only some of which are labeled). In an embodiment, memory device 300 may comprise a plurality of global bit lines (GBLs) 312 that extend along a horizontal direction and a plurality of word lines (WLs) 310 that extend in a horizontal direction but orthogonally to the GBLs 312. A plurality of even local bit lines (LBLs) 308A and a plurality of odd LBLs 308B extend in the horizontal direction at ends of a plurality of vertical bit lines (VBLs) 309. VBLs 309 extend vertically or upwardly from GBLs 312 through layers of WLs 310 and between adjacent columns of WLs 310. Even LBLs 308A, odd LBLs 308B, WLs 310, and VBLs 309 may comprise conductive material, e.g., at least one metal, metal containing composition, or conductively-doped semiconductor material.

[0028] Like memory elements 102 and 202, memory elements 302 may comprise two-terminal memory elements made from a material capable of being programmed to a selective one of two or more memory states. Memory elements 302 may be formed as memory “plugs” in a memory layer disposed between WLs 310 and VBLs 309 such that a memory element 302 is positioned at and between each intersection (e.g., a crosspoint) of a WL 310 with its associated VBL 309 on each layer of memory device 300. Memory elements 302 may be in any of a variety of configurations including the vertical crosspoint RRAM shown in Figures 3A and 3B and the like. Memory elements 302 may comprise a single homogenous composition, multiple discrete compositions, and the like.

[0029] Arranging memory device 300 in the crosspoint configuration shown in Figures 3A and 3B maximizes memory density and affords the ability to read data from or write data to memory elements 302 on a single bit basis, or simultaneously on a nibble, byte, word, page block, or other higher-bit basis.

[0030] GBLs 312 are coupled to LBLs 308A and 308B by pass gate transistors 313 through first selectable parallel path 316 or second selectable parallel path 318, which as their name implies, are each independently selectable through control signals 324A and 324B. Control signals 324A and 324B may be distinct or indistinct from one another. Pass gate transistors 313 may be controlled also by a controller or other device (not shown), which is well-known to a person of ordinary skill in the art and will not be discussed any further herein.

[0031] First and second selectable parallel paths 316 and 318 may comprise first and second impedances, respectively, which may be selected by control signals 324A or 324B based on the operation to be performed on memory elements 302, e.g., SET, RESET, or FORM. In an embodiment, control signals 324A and 324B may be generated by a controller or other device (not shown) well-known to a person of ordinary skill in the art.

[0032] In an embodiment, first selectable parallel path 316 is selected or turned on to present a first impedance between GBL 312 and LBLs 308A or 308B during, e.g., SET or FORM operations, which results in dampening capacitive surge currents from capacitance associated with the GBL 312. A length of the LBLs 308A and 308B and VBLs 309 is kept relatively short to avoid transients from the capacitance associated with the LBLs 308A and 308B. Conversely, second selectable parallel path 318 is selected or turned on to present a second impedance, which is lower relative to the first impedance of path 316, to drive large currents through memory elements 302 during e.g., a RESET operation. By providing parallel selectable paths 316 and 318, memory device 300 may present different impedances between the GBL 312 and corresponding LBLs 308A and 308B and VBLs 309 that advantageously conserve power by reducing the current needed in predetermined operation types, e.g., SET.

[0033] In an embodiment shown in Figure 3A, first selectable parallel path 316 comprises a first switching element 320, e.g., transistor T1, having a first impedance when selected in response to a first operation, e.g., SET or FORM, to be performed on memory element 302. Likewise, second selectable parallel path 318 comprises a second switching element 322, e.g., transistor T2, having a second impedance when selected in response to a second operation type, e.g., RESET, to be performed on the memory element 302. The first and second operation types may be different from one another.

[0034] First and second switching elements 320 and 322 may be of different types, e.g., second switching element 322 may be a low drive current transistor, which may be provided by adjusting or tuning the source drain doping. Put differently, the first and second impedances are made to vary by changing the doping of each of the first and second switching elements 320 and 322, respectively, during their manufacture. The impedance presented by each of first and second switching elements 320 and 322 may change by orders of magnitude depending on the magnitude of the source and drain implant dose made to each of first and second switching elements 320 and 322. In an embodiment, first switching element 320 comprises first source and drain doping level and second switching element 322 comprises

second source and drain doping level different or asymmetric from the first source and drain doping level. The first source and drain doping level may be lower than the second source and drain doping level by at least a factor of ten, e.g., $1\text{E}19/\text{cm}^3$ and $5\text{E}20/\text{cm}^3$.

[0035] In an embodiment shown in Figure 3B, first selectable parallel path 316 comprises a first switching element 320, e.g., transistor T1, having the first impedance when selected or turned on in response to a first operation, e.g., RESET, to be performed on memory element 302. Second switching element 322, e.g., transistor T2, is serially coupled to a resistor 321, the combination having the second impedance when selected or turned on in response to a second operation, e.g., SET or FORM, to be performed on memory element 302. The first and second operations may be different from one another. Resistor 321 may comprise a dielectric resistor, metal-polysilicon-metal resistor, or any other resistor type appropriate for the task that is known to a person of ordinary skill in the art.

[0036] In an embodiment, transistors T1 and T2 are of a similar type, but since transistor T2 is serially coupled to resistor 321, second selectable parallel path 318 has a higher impedance than first selectable parallel path 316 comprising T1 only. The higher impedance second selectable parallel path 318 may be selected or turned on to allow for a low drive current during SET or FORM operations while the lower impedance first selectable parallel path 316 may be turned on or selected when higher currents are needed.

[0037] In an embodiment, first selectable parallel path 316 and second selectable parallel path 318 may comprise a multi-gated device (not shown) with independently-controllable gates, e.g., a FinFET, in which one gate is turned on to allow for a low drive current during SET or FORM operations or in which one or more gates are turned on to drive high current through the memory elements 302 during a RESET operation.

[0038] In a similar manner that it is beneficial to couple GBLs to LBLs using selectable first and second parallel impedance paths in memory devices 100, 200, and 300 to control surge currents during predetermined operation types, it is beneficial to have a selecting element configured to select a memory element using selectable first and second parallel impedance paths.

[0039] Referring to Figure 4A, a memory device 400 comprises a memory element 402 coupled to a selecting or access element 404 through a contact 406. Selecting element 404 may limit current to the memory element 402 until a voltage differential across the memory element 402 and the selecting element 404 reaches a predetermined threshold. Selecting element 404 may be non-linear. More specifically, selecting element 404 may be highly

resistive until a voltage differential reaches a predetermined value, whereupon the electronic devices transform to a conducting state. Selecting element 404 is shown as an NMOS transistor in Figure 4A but may also be any kind of switching element, e.g., a PMOS transistor, a diode, switch, or the like, which is not shown. A person of ordinary skill in the art will recognize that memory element 402 may comprise any type of two-terminal memory element known to a person of ordinary skill in the art. An array of memory elements 402 may form a crosspoint array as is known to a person of ordinary skill in the art. Further, although only a single access device is shown in each memory device 400, there can be multiple selecting devices 404.

[0040] Selecting element 404 may comprise drain 408, source 410, gate 412, and body or substrate 414. Drain 408 may have a different higher (or asymmetric) doping level than source 410 such that selecting element 404 is capable of providing a low impedance path for a first operation, e.g., RESET, and high impedance for a second operation type, e.g., SET or FORM. For example, drain 408 may have a higher doping level of $5E20/cm^3$ while source 410 may have a doping level of $3E19/cm^3$. A control signal applied to gate 412 may determine the operation that is applied to memory element 402, e.g., RESET, SET, or FORM. The control signal 412 may be generated by a controller that is known to a person of ordinary skill in the art and not described herein in any further detail.

[0041] Source 410 may be a doped semiconductor material, e.g., an N-type semiconductor material. Contact 406 may be a metal or a composite material including a metal. A junction between source 410 and contact 406 may therefore form a diode 416, which provides impedance that changes depending on the voltage applied across it. In an embodiment, diode 416 is a Schottky-type diode that will allow high currents with a low turn on voltage for positive polarity voltages and low currents with high impedance for negative polarity voltages.

[0042] In an embodiment in which diode 416 is 100nmX100nm, drain 408 may have a doping level of $5E20/cm^3$ while source 410 may have a doping level of $3E19/cm^3$, the simulated current/voltage graph is shown in Figure 5. Diode 416 has a high OFF impedance, e.g., in the hundred kilo ohms and a low ON impedance, e.g., in the hundred ohms.

[0043] Diode 416 may be a single crystal silicon, polysilicon, or amorphous silicon Schottky diode in series with memory element 402. At least some embodiments of diode 416 may require additional layers not shown in the figures but well-known to a person of ordinary skill in the art.

[0044] In an embodiment shown in Figure 4B, SET voltages V_{set} are applied to the memory array that includes memory element 402. Diode 416 is reverse biased with the application of (negative polarity) SET voltage V_{set} across the memory element 402, which provides a high impedance in the OFF state that may act as a current limiter to dampen capacitive surge currents from wires and junctions during a first operation type, e.g., SET or FORM.

[0045] In an embodiment shown in Figure 4C, RESET voltage V_{reset} is applied to the memory array that includes memory element 402. Diode 416 is forward biased with the application of (positive polarity) RESET voltage V_{reset} across memory element 402, which provides a low impedance in the ON state that may allow a low drive current during a second operation type, e.g., RESET.

[0046] Referring to Figure 6, memory device 600 comprises a diode 616 in series with a memory element 602, which in turn is coupled to a selecting element 604 through a contact 606. Selecting element 604 may limit current to the memory element 602 until a voltage differential across the memory element 602 and the selecting element 604 reaches a predetermined threshold. Selecting element 604 may be non-linear. More specifically, selecting element 604 may be highly resistive until a voltage differential reaches a predetermined value, whereupon the electronic devices transform to a conducting state. Selecting element 604 may be a diode, transistor, switch, or the like. A person of ordinary skill in the art will recognize that memory element 602 may comprise any type of two-terminal memory element known to a person of ordinary skill in the art. An array of memory elements 602 may form a crosspoint array as is known to a person of ordinary skill in the art. Further, although only a single access device is shown in each memory device 600, there can be multiple selecting devices 604.

[0047] Selecting element 604 comprises drain 608, source 610, gate 612, and body or substrate 614. A control signal applied to gate 612 may be generated by a controller that is known to a person of ordinary skill in the art and not described herein in any further detail. Source 610 and drain 608 may be a doped semiconductor material, e.g., an N-type semiconductor material.

[0048] Diode 616 may be a Metal-Insulator-Metal (MIM) diode or other non-linear element that exhibits high impedance for SET and low impedance for RESET operations.

[0049] Figure 7 is a diagram of an embodiment of a memory device 700 according to the present disclosure. Referring to Figure 7, a memory device 700 comprises a 1T-many R

architecture implementing the asymmetric source drain concept disclosed with reference to Figure 4A. Memory device 700 comprises an array of memory elements 702 formed between WLs 710 and VBLs 709. Like memory elements 102, 202, 302, and 402, memory elements 702 may comprise any type of two-terminal memory element known to a person of ordinary skill in the art including resistive memory and the like. An array of memory elements 702 may form a crosspoint array in any of a variety of configurations including the vertical RRAM shown in Figure 7. A person of ordinary skill in the art will recognize that other configurations of memory elements 702 are possible.

[0050] In an embodiment, memory elements 702 may comprise WLs 710 that extend orthogonally to the BLs 720. VBLs 709 extend vertically or upwardly from selecting element 704 through layers of WLs 710 and between adjacent columns of WLs 710. BLs 720, WLs 710, and VBLs 709 may comprise conductive material, e.g., at least one metal, metal containing composition, or conductively-doped semiconductor material.

[0051] Like memory elements 102, 202, 302, and 402, memory elements 702 may comprise two-terminal memory elements made from a material capable of storing two or more memory states. Memory elements 702 may be formed in a memory layer disposed between WLs 710 and VBLs 709 such that a memory element 702 is positioned at and between each intersection (e.g., a crosspoint) of a WL 710 with its associated VBL 709 on each layer of memory device 700. Memory elements 702 may be in any of a variety of configurations including the vertical crosspoint RRAM shown in Figure 7. Memory elements 702 may comprise a single homogenous composition, multiple discrete compositions, and the like.

[0052] BL 720 is coupled to VBLs 709 by selecting elements 704A and 704B through contact 706. Selecting element 704A comprises drain 708 coupled to source 711A, gate 712A, and body 714. Likewise selecting element 704B comprises drain 708 coupled to source 711B, gate 712B, and body 714. Selecting element 704A may be serially coupled to selecting element 704B. Drain 708 may have a different (or asymmetric) doping level than sources 711A and 711B such that selecting elements 704A and 704B are capable of providing a low impedance path for a first operation type, e.g., RESET, and high impedance for a second operation, e.g., SET or FORM. For example, drain 708 may have a higher doping level of $5 \times 10^{20}/\text{cm}^3$ while sources 711A and 711B may have a doping level of $3 \times 10^{19}/\text{cm}^3$.

[0053] A junction between sources 711A and 711B and contacts 707A and 707B, respectively, may form diodes 716A and 716B, which provides impedance that changes

depending on the voltage applied across it. In an embodiment, diodes 716A and 716B will be Schottky-type diodes that will allow high currents with a low turn on voltage for positive polarity voltages and low currents with high impedance for negative polarity voltages.

[0054] Diodes 716A and 716B may be a single crystal silicon, polysilicon, or amorphous silicon Schottky diode. At least some embodiments of diodes 716A and 716B may require additional layers not shown in the figures but well-known to a person of ordinary skill in the art.

[0055] Figures 8A and 8B are diagrams of an embodiment of a method of achieving asymmetric source/drains according to the present disclosure. Referring to Figures 8A and 8B, an active region (not shown) is formed on a P-type body 814. Gate 812 is formed over the active region by first forming a gate oxide layer over the active region followed by a deposit of a conducting layer that is patterned and etched. Gate 812 may comprise polysilicon. Ion implantation 824 is then applied to implant N-type impurities into body 814 to form N-type source 808 and drain 810. A large angle ion implantation 826 may create N-type heavily doped source 808. A barrier layer (not shown) formed over drain 810 may prevent unintended doping of drain 810 during the large angle ion implantation 826. A person of ordinary skill in the art will recognize that many different ion types may be used, e.g., boron, arsenic, and the like, as well as implanting energies and dosage that vary with the specific design requirements. For example, a first doping level N⁺ is implanted in source 808 and drain 810. To achieve asymmetry, a second doping level N⁺⁺ is implanted only in drain 810 to result in drain 810 having a higher doping level of 5E20/cm³ while source 808 may have a doping level of 3E19/cm³.

[0056] The process shown and described above may be similarly applied to an N-type substrate to fabricate a P-type asymmetric lightly-doped drain transistor device.

[0057] A person of ordinary skill in the art will recognize that they may make many changes to the details of the above-described memory device without departing from the underlying principles. Only the following claims, however, define the scope of the memory device.

Claims

1. A memory device, comprising:
a local bit line electrically coupled to a plurality of resistive memory cells; and
a global bit line electrically coupled to the local bit line through first and second selectable parallel paths having first and second impedances, respectively;
wherein the first path is active in at least one of a set operation and a forming operation; and
wherein the second path is active in a reset operation.
2. The memory device of claim 1,
wherein the first impedance is higher than the second impedance.
3. The memory device of claim 1,
wherein the first impedance is lower than the second impedance.
4. The memory device of claim 1,
wherein the first path comprises a first switching element serially coupled to a first resistor;
and
wherein the second path comprises a second switching element.
5. The memory device of claim 4,
wherein the first resistor comprises a dielectric resistor or a metal-polysilicon-metal resistor.
6. The memory device of claim 1,
wherein the first path comprises a first type of switching element; and
wherein the second path comprises a second type of switching element different from the first type of switching element.

7. The memory device of claim 6,
wherein the first type of switching element comprises a first source and drain doping level;
and
wherein the second type of switching element comprises a second source and drain doping level different from the first source and drain doping level.
8. The memory device of claim 7,
wherein the first source and drain doping level is lower than the second source and drain doping level by at least a factor of ten.
9. The memory device of claim 7,
wherein the first type of switching element has a first threshold voltage; and
wherein the second type of switching element has a second threshold voltage different from the first threshold voltage.
10. The memory device of claim 7,
wherein the first type of switching element has a first oxide thickness; and
wherein the second type of switching element has a second oxide thickness different from the first oxide thickness.
11. The memory device of claim 7,
wherein the first switching element and the second switching element are active in at least one of the set operation, the reset operation, or the forming operation.
12. The memory device of claim 1,
wherein the global bit line electrically couples to the local bit line through a multiple gate switching element.
13. The memory device of claim 12,
wherein the multiple gate switching element comprises a finFET device.

14. A memory device, comprising:
a local bit line electrically coupled to a plurality of resistive memory cells; and
a global bit line electrically coupled to the local bit line through first and second selectable parallel paths having first and second impedances, respectively;
wherein the first path is active in at least one of a reset operation and a forming operation;
and
wherein the second path is active in a set operation.

15. A memory device, comprising:
a global bit line;
a local bit line coupled to a plurality of resistive memory cells; and
a coupling circuit configured to couple the global bit line to the local bit line through first and second selectable parallel impedance paths, such that a first coupling impedance is selectable for at least one of a set operation, a reset operation, and a forming operation, and a second coupling impedance is selectable for at least one other of the set operation, the reset operation, and the forming operation.

16. The memory device of claim 15,
wherein the first impedance path comprises a first impedance; and
wherein the second impedance path comprises a second impedance lower than the first impedance.

17. The memory device of claim 16,
wherein the coupling circuit is configured to couple the global bit line to the local bit line through the first impedance path based on a set operation.

18. The memory device of claim 16,
wherein the coupling circuit is configured to couple the global bit line to the local bit line through the second impedance path based on a reset operation.

19. The memory device of claim 15,
wherein the first impedance path comprises a first switching element serially coupled to a first resistor; and
wherein the second impedance path comprises a second switching element.
20. The memory device of claim 19,
wherein the first resistor comprises a dielectric resistor or a metal-polysilicon-metal resistor.
21. The memory device of claim 15,
wherein the first impedance path comprises a first type of switching element; and
wherein the second impedance path comprises a second type of switching element different from the first type of switching element.
22. The memory device of claim 21,
wherein the first type of switching element comprises a first source and drain doping level;
and
wherein the second type of switching element comprises a second source and drain doping level.
23. The memory device of claim 22,
wherein the first source and drain doping level is lower than the second source and drain doping level by at least a factor of ten.
24. The memory device of claim 15,
wherein the coupling circuit comprises a multiple gate switching element.
25. The memory device of claim 24,
wherein the multiple gate switching element comprises a finFET device.

26. A non-volatile memory device, comprising:
a resistive memory element; and
a selecting element having a first impedance path electrically coupled to the resistive memory element in response to a first control signal and having a second impedance path parallel to the first impedance path coupled to the resistive memory element in response to a second control signal.
27. The non-volatile memory device of claim 26,
wherein the first impedance path comprises a first impedance; and
wherein the second impedance path comprises a second impedance higher than the first impedance.
28. The non-volatile memory device of claim 26,
wherein the first control signal is configured to indicate a reset operation; and
wherein the second control signal is configured to indicate at least one of a set operation and a form operation.
29. The non-volatile memory device of claim 26,
wherein the selecting element comprises a source having a first doping level and a drain having a second doping level lower than the first doping level.
30. The non-volatile memory device of claim 29,
wherein the source of the selecting element is electrically coupled in series with the resistive memory element to form a junction.
31. The non-volatile memory device of claim 30,
wherein the junction comprises a Schottky junction.
32. The non-volatile memory device of claim 30,
wherein the Schottky junction comprises a first impedance in response to a reverse bias and comprises a second impedance in response to a forward bias.

33. The non-volatile memory device of claim 29,
wherein the first doping level is lower than the second doping level by at least a factor of ten.

34. The non-volatile memory device of claim 26,
wherein the selecting element comprises a single crystal silicon Schottky diode, a polysilicon Schottky diode, or an amorphous silicon Schottky diode.

35. A device to select a resistive memory element, comprising:
a drain having a first doping level; and
a source having a second doping level lower than the first doping level;
wherein the device is configured to provide a first on impedance or a second on impedance to the resistive memory element in response to a control signal.

36. The device of claim 35,
wherein the source is coupled to the resistive memory element.

37. The device of claim 36,
wherein the first impedance is lower than the second impedance; and
wherein the device is configured to provide the first impedance in a reset operation.

38. The device of claim 37,
wherein the device is configured to provide the second impedance in at least one of a set operation and a form operation.

39. The device of claim 35,
wherein the source is configured to form a junction with the resistive memory element.

40. The device of claim 39,
wherein the junction comprises a Schottky junction.

41. The device of claim 40,
wherein the Schottky junction is configured to provide the first impedance in response to a reverse bias and is configured to provide the second impedance in response to a forward bias.

42. The device of claim 35,
wherein the first doping level is lower than the second doping level by at least a factor of ten.

1/13

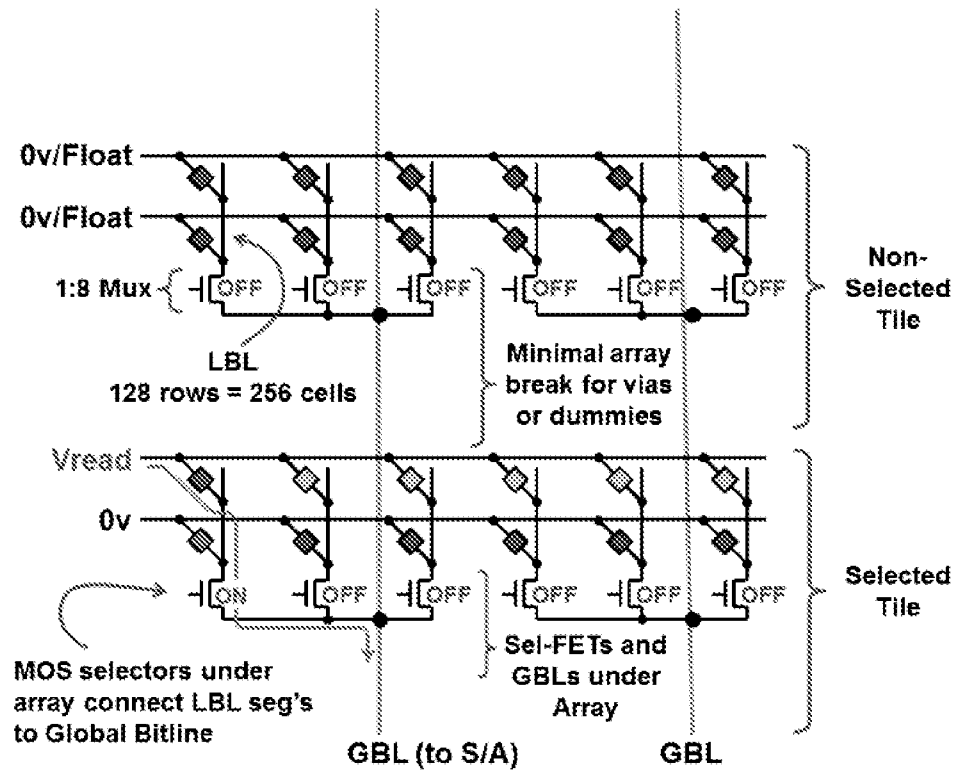


Fig. 1

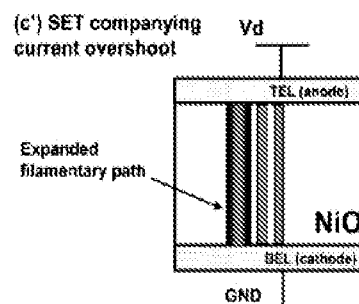


Fig. 2

2/13

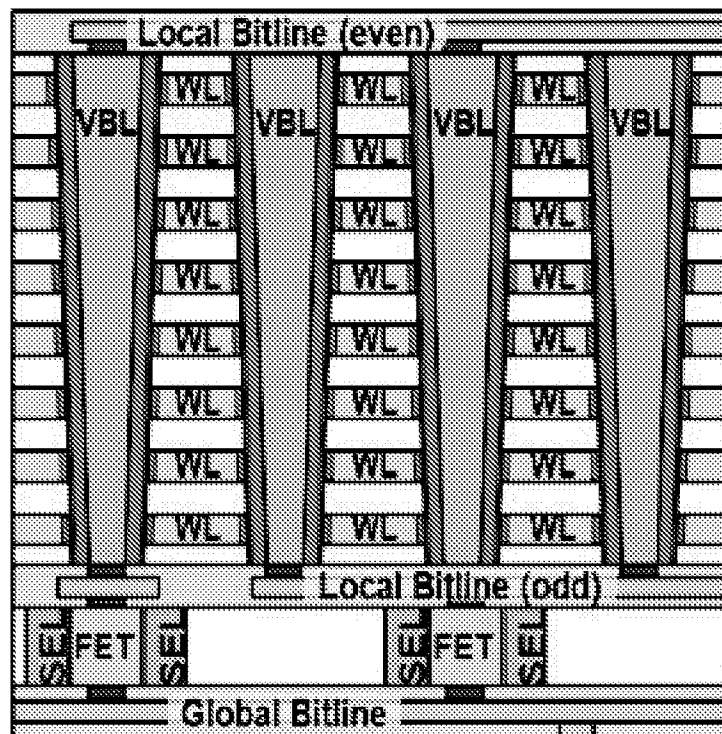


Fig. 3

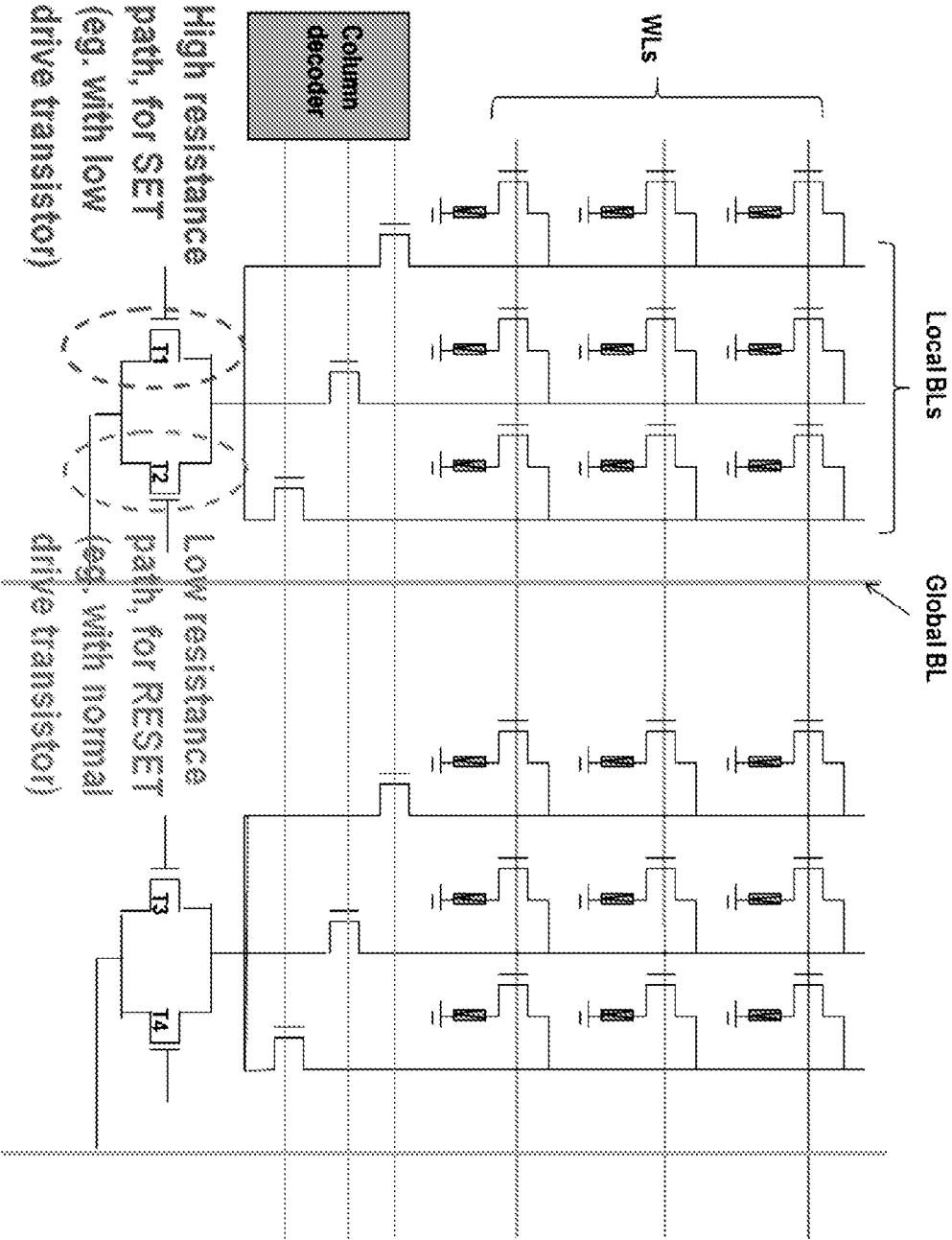


Fig. 4

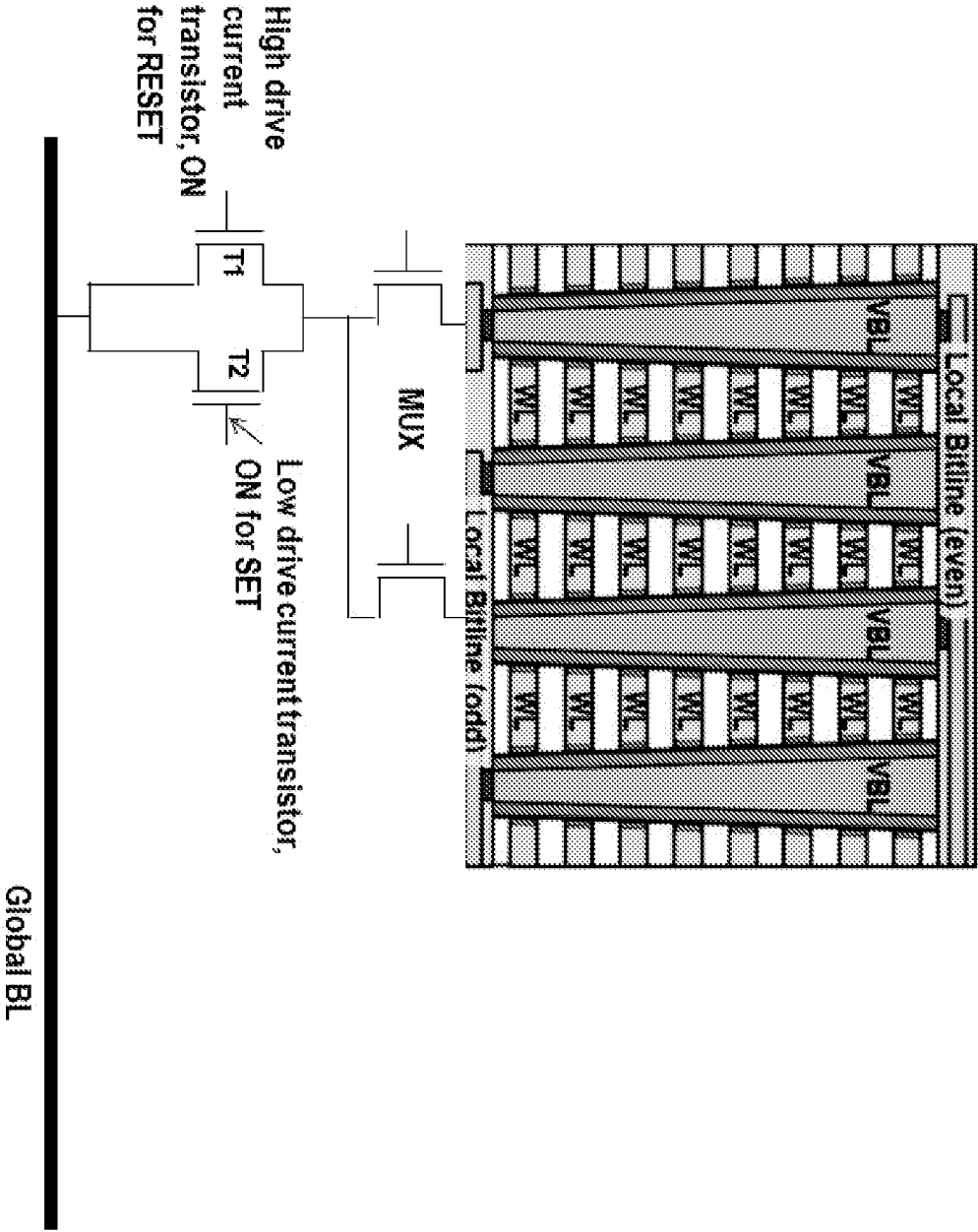


Fig. 5

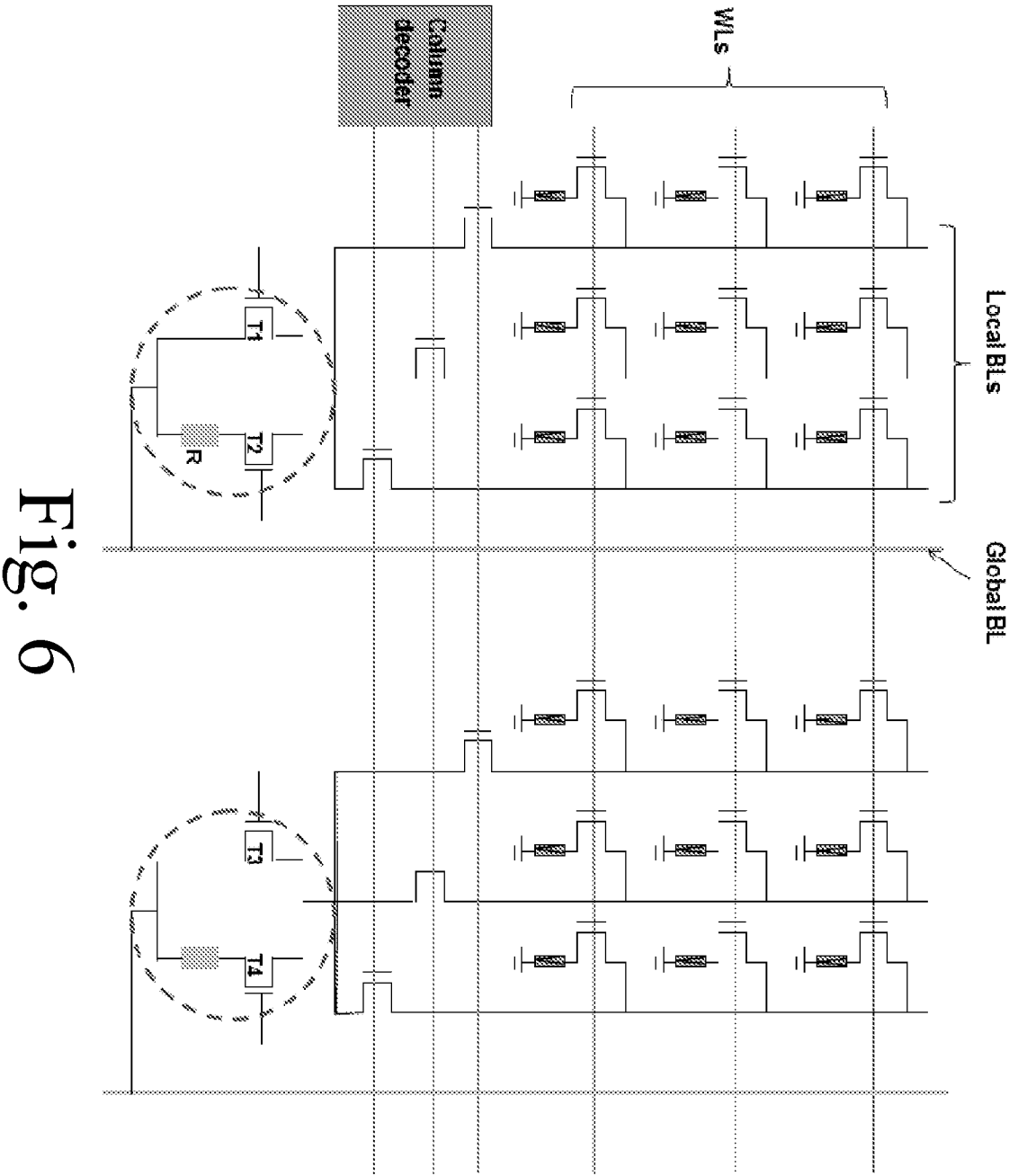


Fig. 6

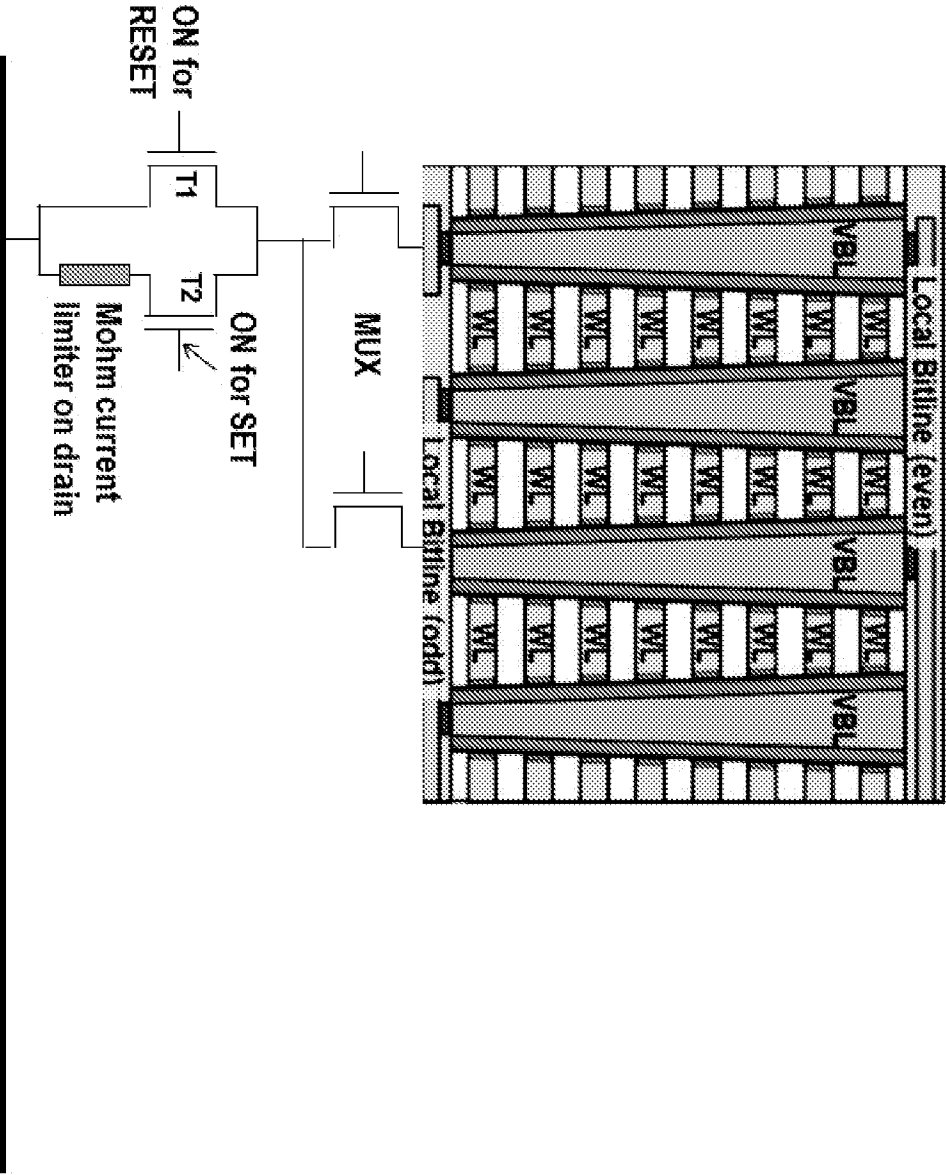


Fig. 7

Global BL

7/13

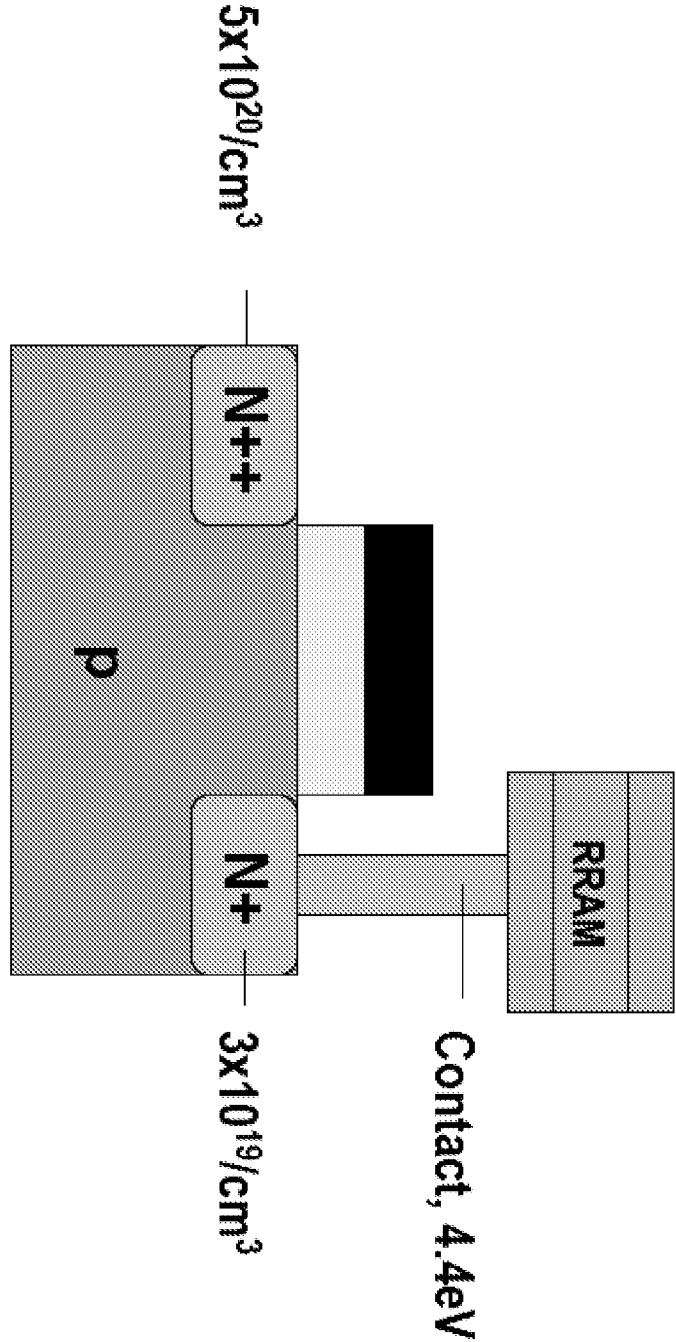


Fig. 8

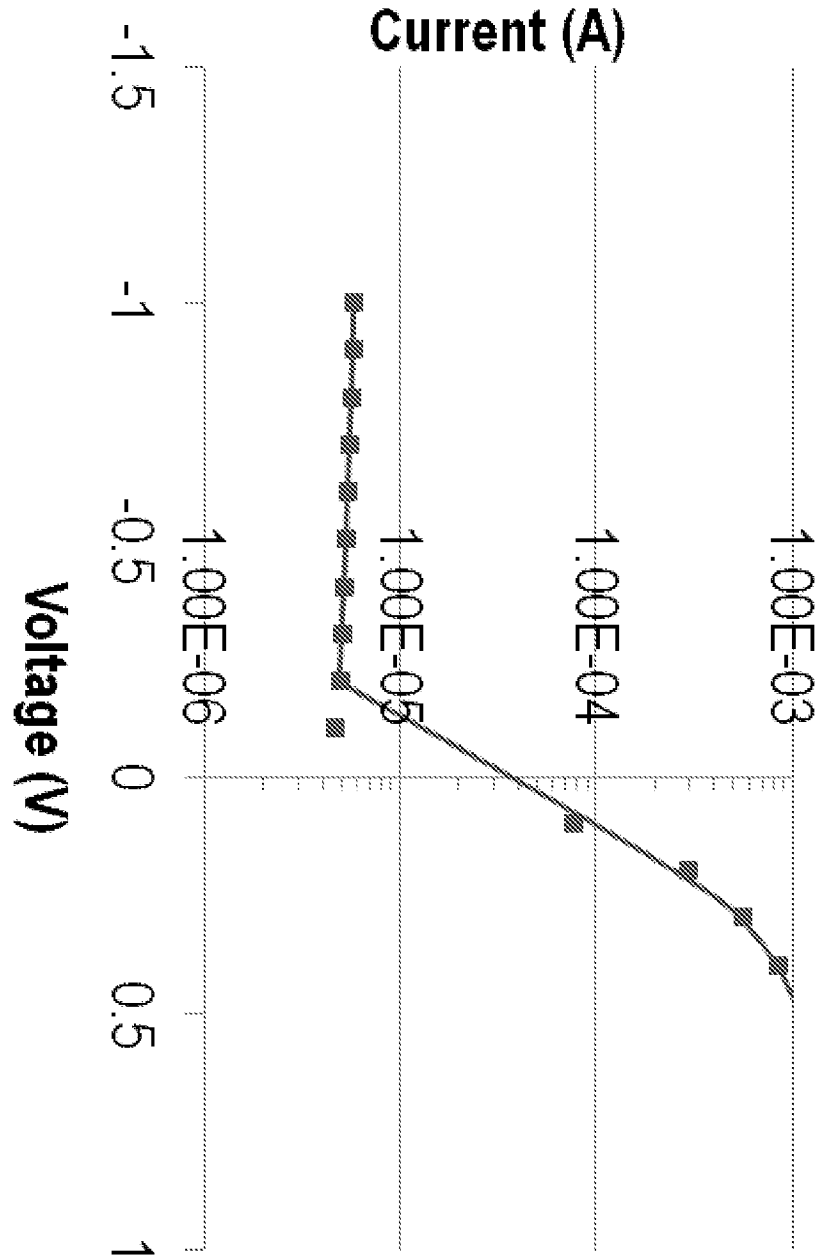


Fig. 9

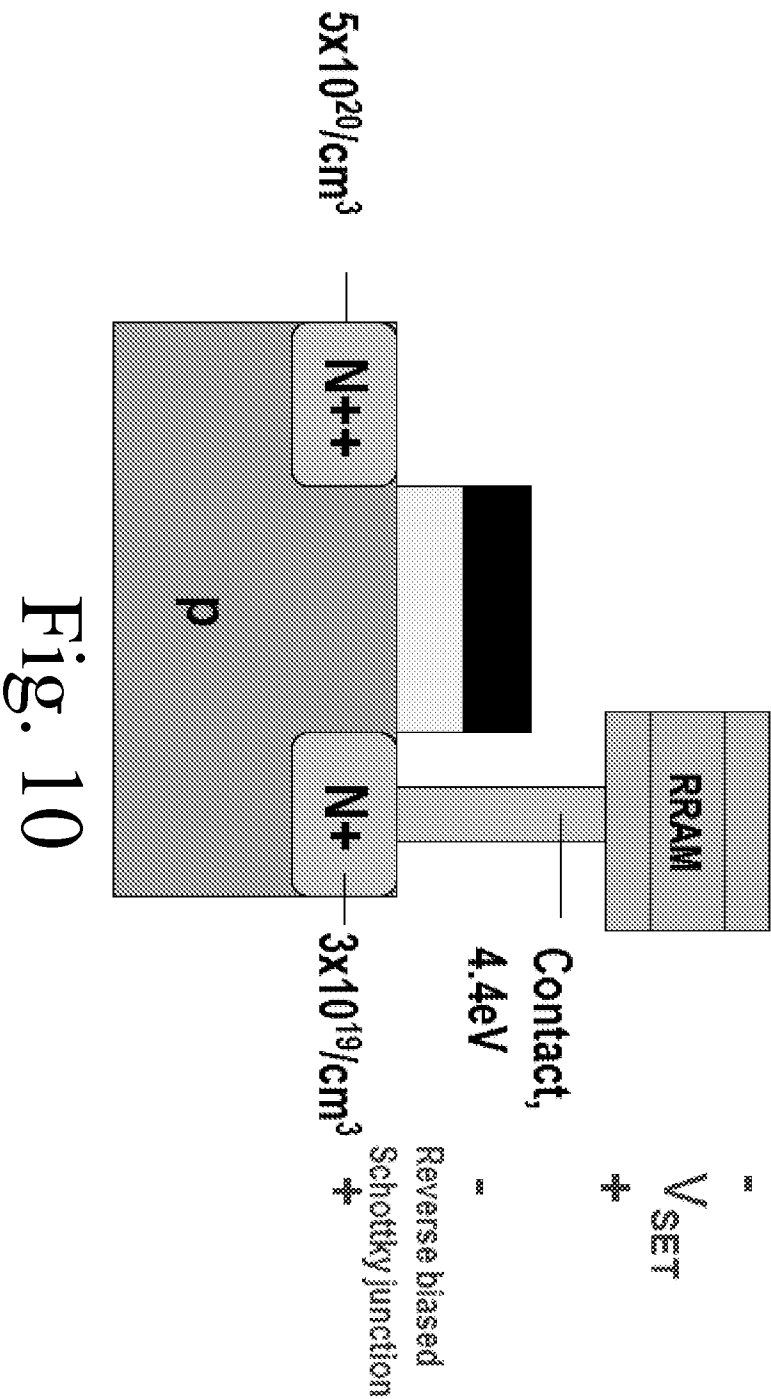


Fig. 10

10/13

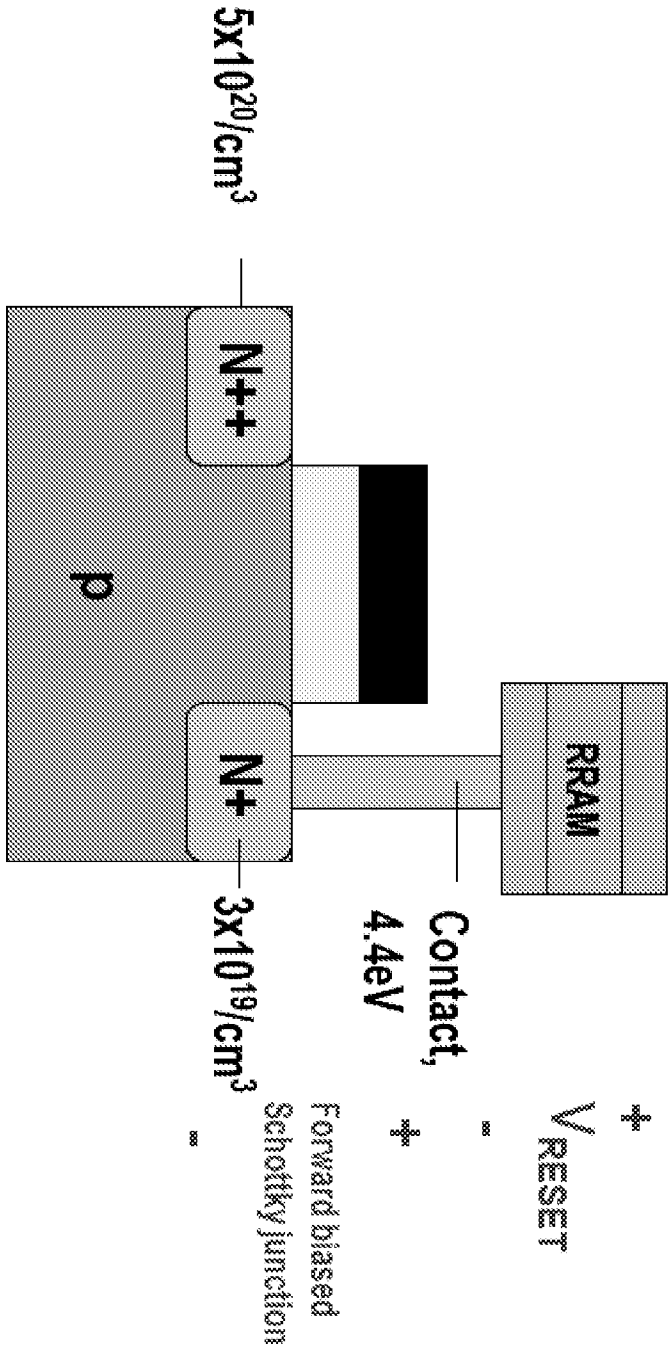
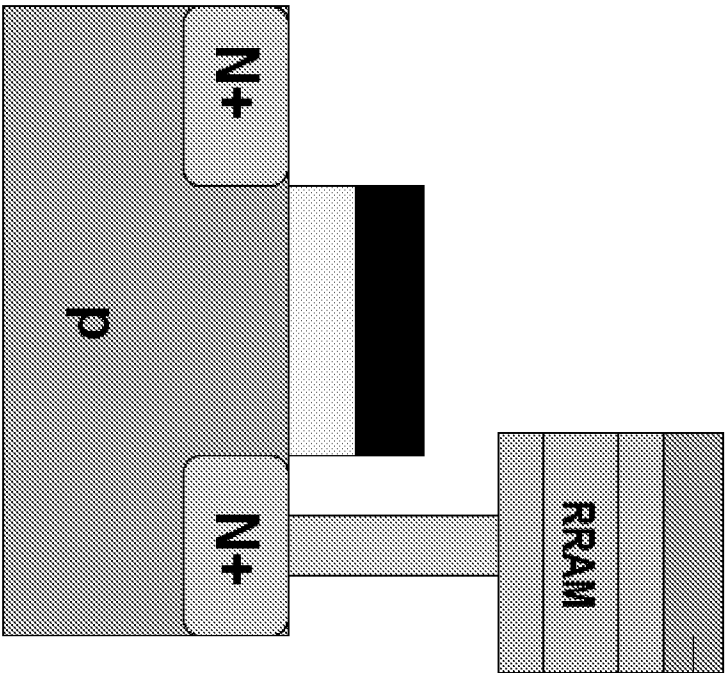


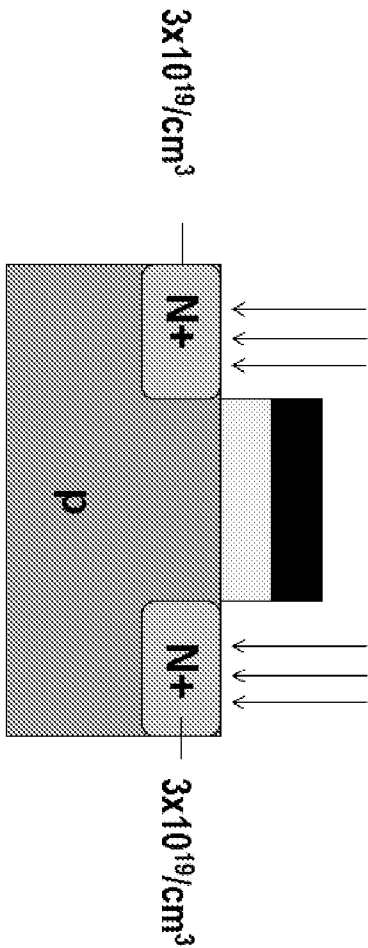
Fig. 11



Schottky diode, MIM diode or some other non-linear element that has a high impedance for SET polarity but low impedance for RESET polarity

Fig. 12

Step 1: N+ implant



Step 2: Tilted N++ implant to get asymmetric source-drains

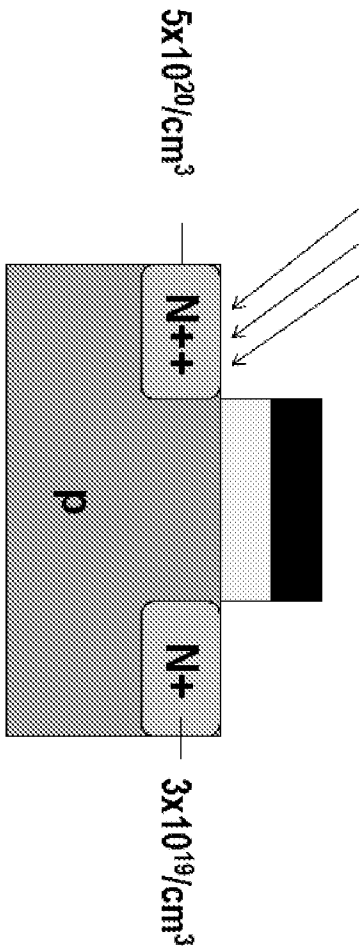


Fig. 13

13/13

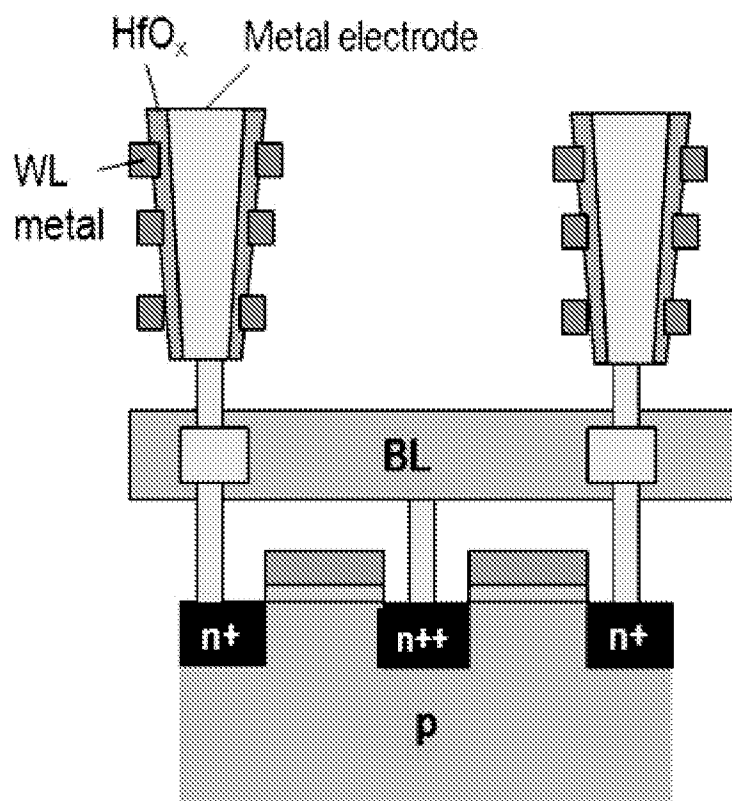


Fig. 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 14/68394

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G11C 11/00 (2015.01)

CPC - G11C 5/025; G11C 11/02; G11C 11/16; H01L 21/8239

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G11C 11/00 (2015.01)

CPC: G11C 5/025; G11C 11/02; G11C 11/16; H01L 21/8239

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

IPC: G11C 11/00 (2015.01)

CPC: G11C 5/025; G11C 11/02; G11C 11/16; H01L 21/8239; USPC: 365/50,55,148,100

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Patbase, Google Patents, Google Scholar

Search terms used - Resistive, memory, ram, rram, rram, bit line, bitline, global, control, set, reset, forming, impedance, resistor, dope, doping, dopant, amount, level, transistor, nmos, pmos, mosfet, drain, switch, select, different, individual, distinct, second, two, three, third, plural, mul

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013/0170283 A1 (LAN et al.) 04 July 2013 (04.07.2013), para [0036], [0144]-[0145], [0152]-[0153], [0163], [0187]-[0190]; Fig 12, 18	1-25
Y	US 2003/0039166 A1 (SHAU) 27 February 2003 (27.02.2003), para [0065]	1-25
Y	US 2013/0208528 A1 (KWAK et al.) 15 August 2013 (15.08.2013), para [0008], [0067]-[0068]	4, 5, 19, 20
Y	US 2013/0070506 A1 (KAJIGAYA) 21 March 2013 (21.03.2013), para [0074]	13, 25
Y	US 2013/0221314 A1 (PRAMANIK et al.) 29 August 2013 (29.08.2013), para [0047], [0072], [0073]	5, 20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 March 2015 (30.03.2015)

Date of mailing of the international search report

14 APR 2015

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-3201

Authorized officer:

Lee W. Young



PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 14/68394

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I: Claims 1-25 drawn to a memory device having a local bit line electrically coupled to a plurality of resistive memory cells.

Group II: Claims 26-34, drawn to a non-volatile memory device having a resistive memory element and a selecting element.

Group III: Claims 35-42, drawn to a device to select a resistive memory element a source and a drain with first and second doping levels.

--please see continuation on extra page--

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-25

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 14/68394

Continuation of Box No. III -- Observations where unity of invention is lacking

The inventions listed as Groups I through III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features

Group I includes the special technical feature of a local bit line electrically coupled to a plurality of resistive memory cells; and a global bit line electrically coupled to the local bit line, not included in the other groups.

Group II includes the special technical feature of a selecting element having a first impedance in response to a first control signal and having a second impedance in response to a second control signal, not included in the other groups.

Group III includes the special technical feature of a drain having a first doping level; and a source having a second doping level lower than the first doping levels, not included in the other groups.

Common Technical Features:

The only technical features shared by Groups I-III that would otherwise unify the groups, are a memory device comprising a resistive memory and first and second selectable parallel impedance paths. However, these shared technical features do not represent a contribution over prior art, because the shared technical features are disclosed by US 8,248,838 B2 (Tonomura) 21 August 2012 (21.08.2012).

Tonomura discloses a memory device comprising a resistive memory (col 3, ln 3-11) and first and second selectable parallel impedance paths (col 3, ln 38-46; col 6, ln 33-43 ; claim 14, 15; Fig 1, DR1 to DRn, through RTRD1 to RTRDn)).

The only additional technical feature shared by Groups II-III that would otherwise unify the groups, is a first impedance or a second impedance to the resistive memory element in response to a control signal. However, this shared technical feature does not represent a contribution over prior art, because the shared technical feature is disclosed by Tonomura.

Tonomura discloses a first impedance or a second impedance to the resistive memory element in response to a control signal (col 4, ln 18-30; col 6, ln 33-43)..

As the technical features were known in the art at the time of the invention, these cannot be considered special technical features that would otherwise unify the groups.

Therefore, Groups I-III lack unity under PCT Rule 13.