United States Patent [19]

Nomiya et al.

[11] **3,813,623**

[45] **May 28, 1974**

[54] **SERIAL BCD ADDER**

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[73] Assignee: **Hitachi Ltd.,** Tokyo, Japan

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[21] Appl. No.: **317,303**

[30] **Foreign Application Priority Data**

Dec. 24, 1971 Japan 46-104579

[52] **U.S. Cl.** **235/176,** 235/170

[51] **Int. Cl.** **G06f 7/50**

[58] **Field of Search** 235/176, 170, 169, 174, 235/165

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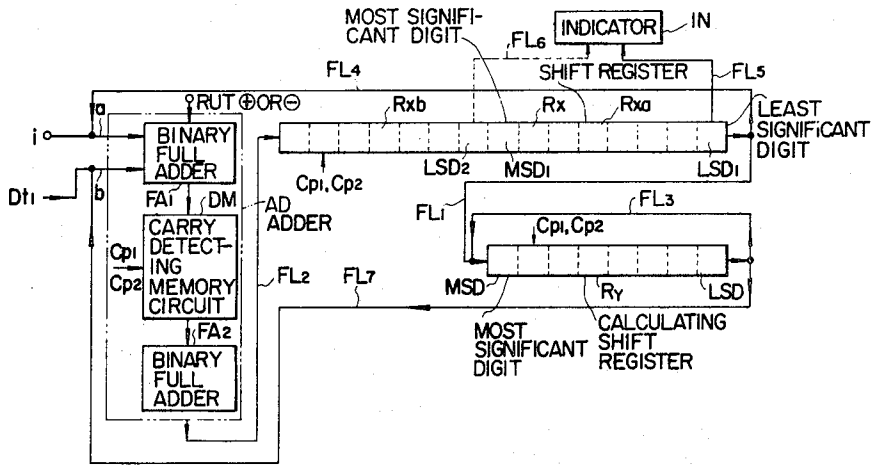
Primary Examiner—Malcolm A. Morrison
Assistant Examiner—David H. Malzahn
Attorney, Agent, or Firm—Craig and Antonelli

[57] **ABSTRACT**

A digital processing system wherein a binary-coded decimal full adder forms along with a display shift register a loop-like circuit for circulating information signals. The system provides a series synchronism system which reduces the number of circuit elements.

9 Claims, 18 Drawing Figures



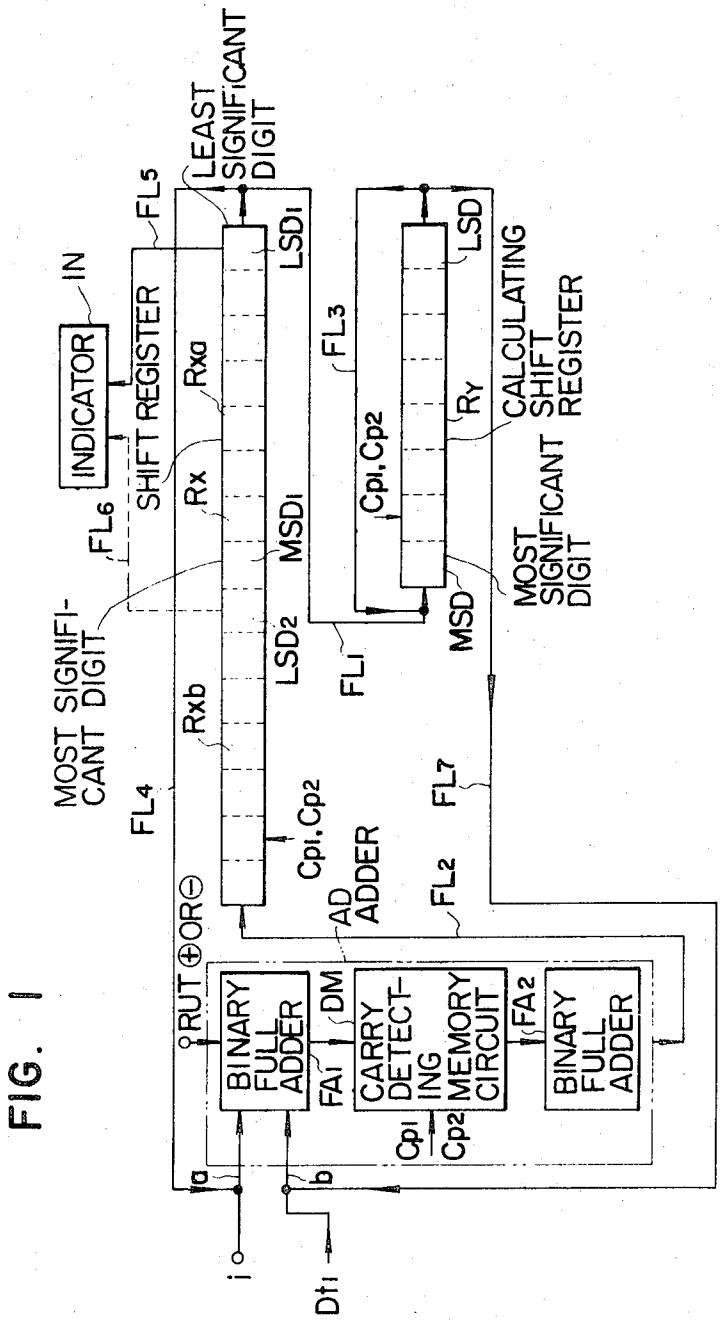

IN
INDICATOR
SHIFT REGISTER
FL5
LEAST SIGNIFICANT DIGIT
LSD1
FL3
Rxa
Rx
MSD1
Cp1, Cp2
LSD
CALCULATING SHIFT REGISTER
Ry
MOST SIGNIFICANT DIGIT
MSD
FL6
MOST SIGNIFICANT DIGIT
LSD2
FL1
Rxb
FL4
FL7
Cp1, Cp2
AD ADDER
FL2
RUT ⊕OR⊖
BINARY FULL ADDER
DM
FA1
CARRY DETECTING MEMORY CIRCUIT
FA2
BINARY FULL ADDER
Cp1
Cp2
a
b
i
Dt1

FIG. 1

FIG. 2a

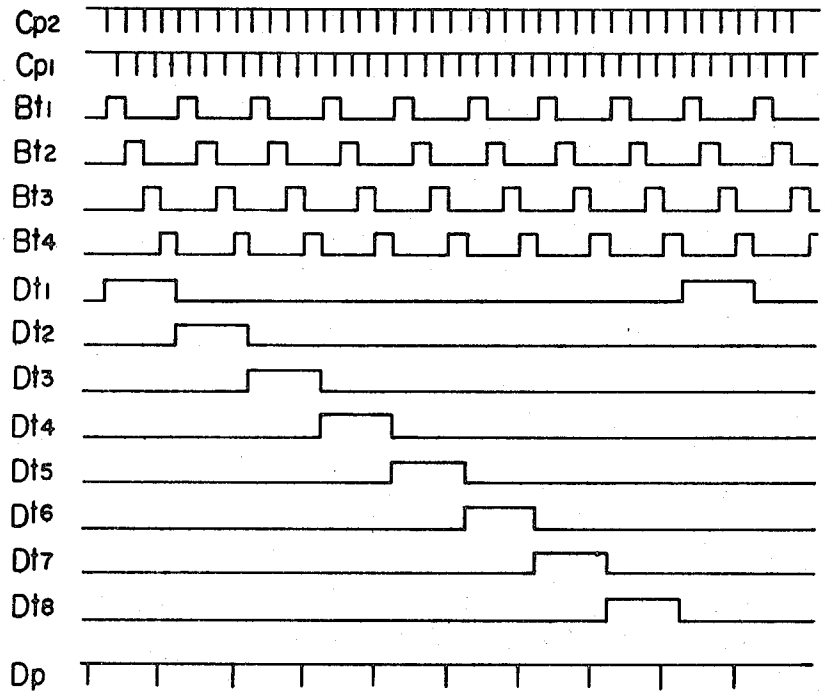

Cp2
Cp1
Bt1
Bt2
Bt3
Bt4
Dt1
Dt2
Dt3
Dt4
Dt5
Dt6
Dt7
Dt8
Dp

FIG. 2b

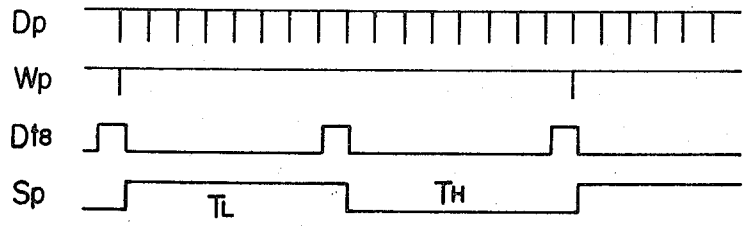

Dp
Wp
Dt8
Sp
TL
TH

FIG. 3

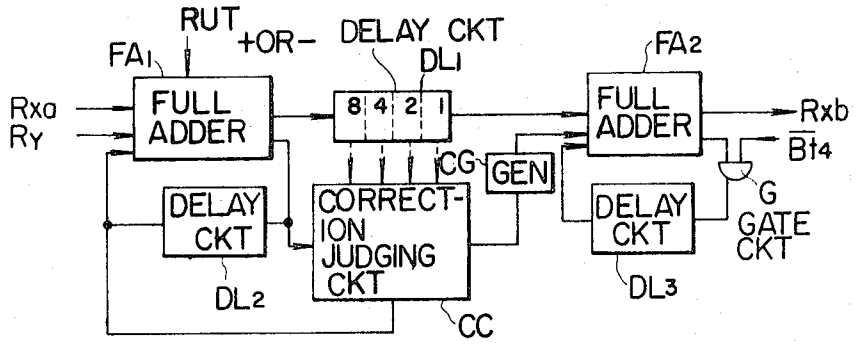

RUT
+OR-
DELAY CKT
DL1
FA1
FA2
Rxa
Ry
FULL ADDER
8 4 2 1
FULL ADDER
Rxb
Bt4
CG
GEN
G
GATE CKT
DELAY CKT
CORRECT-ION JUDGING CKT
DELAY CKT
DL2
DL3
CC

FIG. 4

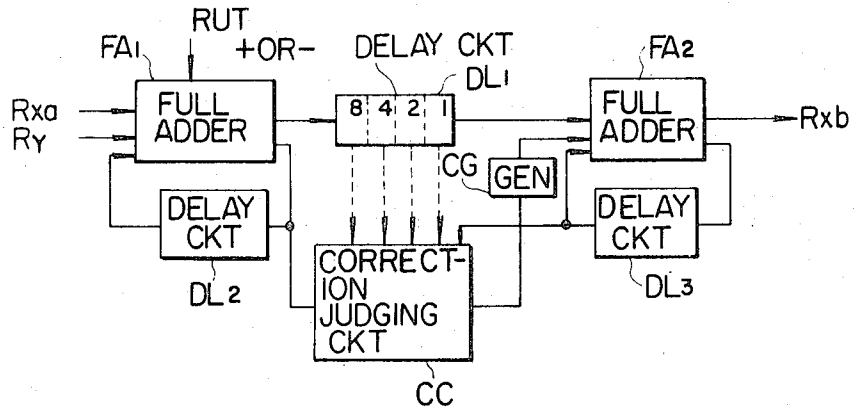

RUT
+OR-
DELAY CKT
DL1
FA1
FA2
Rxa
Ry
FULL ADDER
8 4 2 1
FULL ADDER
Rxb
CG
GEN
DELAY CKT
CORRECT-ION JUDGING CKT
DELAY CKT
DL2
DL3
CC

FIG. 5a

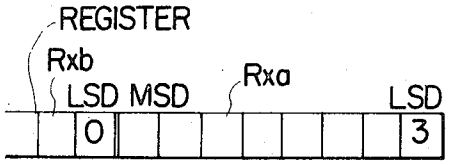


FIG. 5b

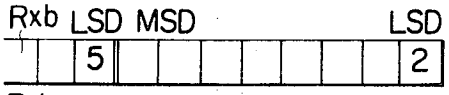


FIG. 5c

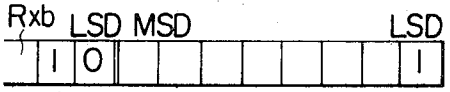


FIG. 5d

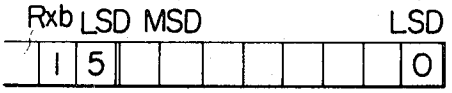


FIG. 5e

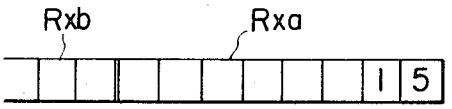


FIG. 6a

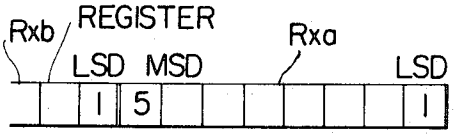


FIG. 6b

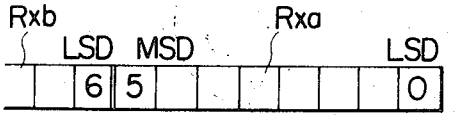
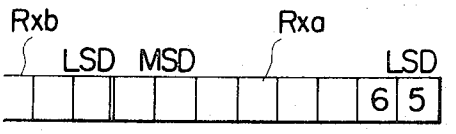


FIG. 6c



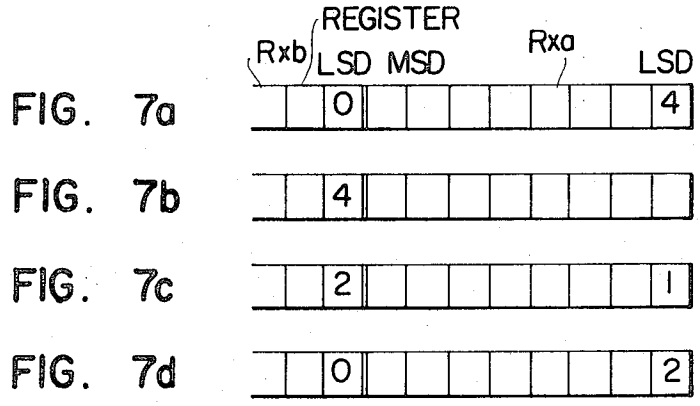


FIG. 7a

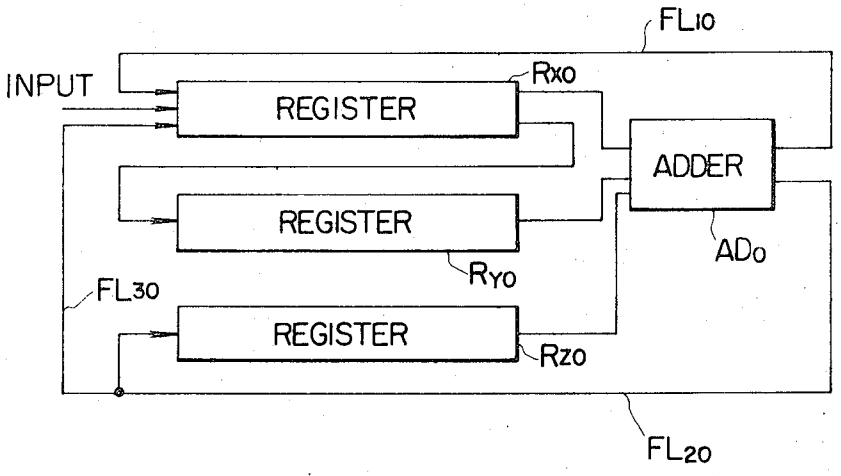
FIG. 7b

FIG. 7c

FIG. 7d

FIG. 8

PRIOR ART



SERIAL BCD ADDER

The present invention relates to a digital processing system which employs shift registers connected in series.

A principal object of the present invention is to provide a processing system wherein the number of circuit elements is reduced, and more particularly, a digital processing system which is suitable for a small-sized calculator such as a desk-top calculator.

Another object of the present invention is to provide a digital processing system which can easily display processed information signals.

Still another object of the present invention is to provide a digital processing system which can easily execute arithmetics such as multiplication and division.

Yet another object of the present invention is to provide a digital processing system which can shorten the length of the register means.

A further object of the present invention is to provide a digital processing system which is free from overflow of a processed result.

According to the present invention, there is provided a digital processing system characterized by a first display shift register of a certain capacity prescribed for numerical information for display in a display unit (for example, a capacity for storing numerical information of eight digits), a calculating shift register having the same capacity as said first display shift register, a binary digit full adder connected to the output side of said first display shift register and having a memory circuit (delay circuit) with a capacity of two to four bits, and a second display shift register disposed between said binary digit full adder and said first display shift register and having a capacity which is equal to one obtained by subtracting the capacity of said memory circuit of said binary digit full adder from the capacity of said first display shift register; said first display shift register, said second display shift register and said full adder forming a circulative closed circuit for information signals; the total capacity bit time of said first display shift register, said second display shift register and said delay circuit in said full adder is time-shared by a sector pulse corresponding to the capacity bit time of said calculating shift register; thus the information signals of the two series-connected display shift registers are subjected to calculating processing.

These and further objects, features and advantages of the present invention will become more obvious from the following description when taken in connection with the accompanying drawings which show, for purposes of illustration only, several embodiments in accordance with the present invention, and wherein

FIG. 1 is a block diagram showing an embodiment of a digital processing system according to the present invention;

FIGS. 2*a* and 2*b* are wave-form diagrams of controlling and synchronizing pulses which are used in the digital processing system of the present invention;

FIGS. 3 and 4 are block diagrams each showing a delay type full adder which is employed in the present invention;

FIGS. 5*a* – 5*e*, 6*a* – 6*c* and 7*a* – 7*d* are explanatory diagrams for illustrating changes of information signals of display shift registers in the digital processing system of the present invention; and

FIG. 8 is a block diagram showing an example of a prior-art digital processing system.

Referring to FIG. 1, R_{Xa} designates the first display shift register which has a fixed capacity. In the illustrated embodiment, the capacity of the shift register R_{Xa} is eight digits (32 bits) from the least significant digit LSD_1 to the most significant digit MSD_1. R_{Xb} indicates the second display shift register which is directly coupled to the register R_{Xa} at a stage preceding thereto. The capacity of the register R_{Xb} is set so that the total capacity (32 bits) of the capacity (for example, four bits) of a binary digit full adder AD referred to below and the capacity (for example, 28 bits) of the register R_{Xb} itself may be equal to the capacity (32 bits) of the first display shift register R_{Xa}. R_Y represents a calculating shift register, which has the same capacity (32 bits) as the first display shift register R_{Xa}. Shown at AD is the binary digit full adder, to which are supplied the output of the display register R_{Xa} for the posterior stage and the output of the calculating register R_Y or a different control input Dt_1. The output of the binary-coded decimal full adder AD is supplied through a line FL_2 to the input side of the display register R_{Xb} for the anterior stage. The binary-coded decimal full adder AD is composed of a binary full adder FA_1, a memory circuit DM for carry detection (for BCD correction) and a binary full adder FA_2. The carry detecting memory circuit DM has, for example, N_1 digits (at least two bits). The number of digits of the memory capacity of the display register R_{Xb} for the anterior stage is subtracted to the amount of the length of the N_1 digits. Letting N_2, N_3 and N_4 be the numbers of digits of the anterior stage display register R_{Xb}, posterior-stage display register R_{Xa} and calculating register R_Y, respectively, they are thus set so as to hold the relation of $N_2 + N_1 = N_3 = N_4$. Accordingly, among the three registers, the length of the anterior-stage display register R_{Xb} is shorter by the N_1 digits than that of the other register R_{Xa} or R_Y, while the sum between the length of the carry detecting memory circuit DM and that of the anterior-stage display register R_{Xb} becomes equal to the length of the other register R_{Xa} or R_Y. The above-noted relation may also be defined in the manner the memory capacity of the circuit DM is $4N_1$ bits, the memory capacities of the first display shift register R_{Xa} and the calculating shift register R_Y are both $4N_2$ bits and the memory capacity of the second display shift register is $4(N_2-N_1)$ bits, where N_1 and N_2 are integers of at least one and $N_2 > N_1$. An indicator unit IN for indicating the information contents of the display register R_X (the first and second display registers R_{Xa} and R_{Xb}) is also provided. Information subjected to calculating processing are read out from the output side of the first display shift register R_{Xa} to the indicator unit by a line FL_5, and are brought into visible display or recording display by the indicator unit. A decoder circuit and a drive circuit which are connected between the display shift register R_{Xa} and the indicator unit IN, are omitted for the sake of convenience of explanation. In the case where the display system of the indicating unit is a dynamic one, it is desireable in order to make the display efficiency high (in order to raise the duty ratio) that the information signal to-be-indicated is also read out from the output side of the second display shift register R_{Xb} by a line FL_6. In this case, it is possible to increase the application repetition period of the information signal to the indicating unit, thereby lengthening the lighting (light

emitting) time of the indicator unit. It is required, however, that either the information stored at the last digit LSD of the shift register R_{Xa} or the last digit LSD of the shift register R_{Xb} is always in the blank ("0") state so as to prevent the information from both registers being mixed and displayed. In other words, the foregoing construction is very effective in a processing system in which the information stored in the circulating path including the registers R_{Xa} and R_{Xb} and the memory circuit DM amounts to eight digits being a half of the total capacity, and in which the remaining eight digits are brought into the blank state after completion of the calculation. The transfer of information from the display shift register R_X to the calculating shift register R_Y is accomplished by a line FL_1. Although a controlling gate portion necessary for the calculating processing is incorporated into each of the lines which is controlled on-and-off by a synchronizing pulse for control, the controlling gate section is omitted from the drawing.

The information signal stored in the calculating register R_Y, the display register R_X, and the memory circuit DM of the full adder AD is shifted by clock pulses Cp_1 and Cp_2 as shown in FIG. 2*a*. The total capacity bit time (64-bit time) of the loop-like closed circuit passing through the display register R_X and the full adder AD is prescribed at double of the capacity bit time (32-bit time) of the calculating register R_Y. The information of the first display register R_{Xa} and the second display register R_{Xb} are distinguished by timing pulses (pulses for distinguishing higher digits and lower digits) Sp shown in FIG. 2*b*, and are subjected to the calculating processing. The timing pulse Sp has a pulse width equal to the period of the digit pulse Dt_1 shown in FIG. 2*a*, and is synchronized with the digit pulse DT_1. At this time, the information of the first display shift register R_{Xa} is processed for a period of time T_L in which the timing pulse Sp is of a high level, while the information of the second display shift register R_{Xb} is processed for a period of time T_H in which it is of a low level. For example, in case of subjecting the information of R_{Xa} and that of R_Y to addition processing, the information of R_{Xa} and R_Y are applied to the adder Ad in the period of time T_L of the timing pulse Sp.

With reference to FIGS. 2*a* and 2*b*, description will now be made of various pulse signals used in the embodiment and in a desk calculator etc., to which the embodiment is applied. In the figures, the upper level of a pulse signal indicates a reference potential or the ground potential (logic "1"), while the lower level represents a negative potential (logic "0"). The clock pulses Cp_1 and Cp_2 are generated by, e.g., astable multivibrators, and tick away the time by themselves in the calculator. They are used for the drive or shift of, e.g., memory elements (delay type flip-flop circuits) connected in cascade within the shift registers R_{Xa}, R_{Xb} and R_Y and the memory circuit DM for correcting a binary-coded decimal number. The respective output signals of the memory elements are transmitted to those at the succeeding stages by the timing of the clock pulses Cp_1. Bit signals $Bt_1 - Bt_4$ are used in case of, e.g., converting binary parallel signals derived from the encoder into binary series signals. In the embodiment, the judging signal of the bit signal Bt_4 is utilized in the binary-coded decimal full adder as stated below. Digit signals $Dt_1 - Dt_8$ are used as, e.g., digit changing signals in the dynamic display system. In the embodiment, they are used in order to add 1 to or subtract the same from the second operand in multiplication and division as is stored in the shift register for display. The sector pulses Sp have the state changed to T_L or T_H every eight digits, and can be composed from the digit signal Dt_1 or Dt_8 by utilizing a flip-flop circuit and a logical gate circuit. Digit pulses Dp distinguish the digits of a binary-coded decimal number. Word pulses Wp are used for distinguishing words or instructions. The characteristic equations of the respective pulses Dp and Wp are represented by $D_p\ 165 = \overline{Bt_4 \cdot Cp_2}$ and $W_p = \overline{Dt_8 \cdot Cp_2 \cdot S_p}$, which can be composed of the foregoing pulses. The bit signals $Bt_1 - Bt_4$ and the digit signals $Dt_1 - Dt_8$ can be respectively generated from the clock pulses Cp_2 and the bit signal Bt_1 by making use of, e.g., counters. Herein, the pulse width of the bit signals $Bt_1 - Bt_4$ corresponds to the period of the clock pulses Cp_1 or Cp_2, and to the time of 1 bit of the series binary signal. The pulse width of the digit signals $Dt_1 - Dt_8$ and the period of the digit pulses Dp correspond to the period of the bit signals $Bt_1 - Bt_4$, namely, the time of one digit (four bits) of the series binary-coded decimal number. The period of the word pulses Wp corresponds to double of the period of the digit signals $Dt_1 - Dt_8$.

The delay type full adder AD is constructed as shown, by way of example, in FIG. 3. Referring to the figure, DL_1 represents a delay circuit having a memory capacity of four bits (one digit), DL_2 and DL_3 delay circuits for effecting delay of one-bit time, CC a correction judging circuit, G a gate circuit which has its gate opened by a predetermined timing signal $\overline{Bt_4}$, and CG a generator for generating in response to an output of the correction judging circuit CC an output which serves to add 6 in decimal number (0110 in binary number) to the binary full adder FA_2. The delay circuits $DL_1 - DL_3$, correction judging cirucit CC, generator CG and gate circuit G constitute the carry detecting memory circuit DM.

With such a construction, in the case where the result of addition in the binary full adder FA_1 is "0 – 9," the output of the binary full adder FA_1 is supplied through the delay circuit DL_1 to the binary full adder FA_2 in consequence of the addition of the outputs of the posterior-stage register X and the register Y as have been supplied to the binary full adder FA_1. The output of the binary full adder Fa_2 is transmitted to the anterior-stage register X or R_{xb}. In the case where a carry arises in consequence of the addition in the binary full adder FA_1, a binary carry signal is supplied through the delay circuit DL_2 to the input side of the binary full adder FA_1, to add "1" to a higher binary digit. At this time, it is a matter of course that, even with the binary carry, no overflow occurs beyond four binary digits. The correction judging circuit CC and the gate circuit G do not operate.

In the case where the result of the addition in the binary full adder FA_1 is 10–15, the binary carry signal is supplied through the delay circuit DL_2 to the input side of the binary full adder FA_1 for the binary carry in the binary full adder FA_1. In addition, the correction judging circuit CC is operated by an instruction of the delay circuit DL_1. The correction judging circuit CC supplies an output to the generator CG, and simultaneously supplies a decimal carry signal to the binary full adder FA_1 to conduct decimal carry. The output of the delay circuit DL_1 and that of the generator CG are added by the binary full adder FA_2. The binary carry is conducted in such way that the output of the binary full

adder FA_2 is supplied through the gate circuit G, adapted to be opened by the predetermined timing signal $\overline{Bt_4}$, to the input side of the binary full adder FA_2 with delay of one-bit time by the delay circuit DL_3. In this manner, 0–5 in the binary-coded decimal notation is transmitted from the binary digit full adder AD, that is, the binary full adder FA_2.

Further, in the case where the result of the addition in the binary full adder FA_1 is 16–19, the output of the binary full adder FA_1 is supplied through the delay circuit DL_2 to the input side of the binary full adder FA_1, thereby to conduct the binary carry and the decimal carry. The instructing output of the delay circuit DL_1 is not supplied to the correction judging circit CC. Instead, the instructing output of the binary full adder FA_1 operates the correction judging circuit CC. The output of the correction judging circuit CC operates the generator CG. The output of the generator CG is supplied to the input side of the binary full adder FA_2. On the other hand, the output of the binary full adder FA_1 is supplied through the delay circuit DL_1 to the input side of the binary full adder FA_2. The binary carry signal is supplied through the gate circuit G and delay circuit DL_3 from the output side of the binary full adder FA_2. Since the decimal carry has been already conducted in the binary full adder FA_1, no decimal carry is executed in the binary full adder FA_2. In this manner, an output of 6–9 is transmitted as the output of the binary digit full adder AD, that is, the output of the binary full adder FA_2.

FIG. 4 shows another embodiment of the binary-coded decimal full adder in FIG. 1. In FIG. 4, the same parts or parts having the same functions as in FIG. 3 are assigned with the same symbols. The delay circuits DL_1 – DL_3, the correction judging circuit CC and the generator CG constitute the carry detecting memory circuit. A point of difference from the embodiment in FIG. 3 resides in that, without using the gate circuit G, the output of the binary full adder FA_2 is supplied through the delay circuit DL_3 to the correction judging circuit CC and the input side of the binary full adder FA_2.

With such a construction, in the case where the result of addition in the binary full adder FA_1 is 0–9 or 16–19, the foregoing applies,

In the case where the result of the addition in the binary full adder FA_1 is 10–15, the output of the binary full adder FA_1 is supplied through the delay circuit DL_2 to the input side of the binary full adder FA_1, thereby to conduct binary carry. The output of the binary full adder FA_1 is supplied through the delay circuit DL_1 to the binary full adder FA_2. On the other hand, the instructing output of the delay circuit DL_1 is supplied to the correction judging circuit CC. The output of the binary full adder FA_2 is supplied through the delay circuit DL_3 to the input side of the binary full adder FA_2 as a binary carry signal and to the correction judging circuit CC as a decimal carry signal. The output of the correction judging circuit CC operates the generator CG. The output 0110 of the generator CG is supplied to the input side of the binary full adder FA_2. In this way, 0–5 is transmitted as the output of the binary-coded decimal full adder AD, namely, that of the binary full adder FA_2.

Although, in the embodiment, the carry detecting memory circuit DM has the memory capacity of four bits, it is a matter of course that the invention is not restricted thereto, but that three bits, for example, may also be employed. In this case, a delay circuit for 1-bit delay is incorporated into an output supply line of, for example, from the correction judging circuit CC to the binary full adder FA_1 in FIG. 4.

A case where multiplication is carried out with the processing system of the present invention, will now be explained with reference to FIG. 5. FIG. 5 illustrates changes with time in information stored in the display register R_X in a calculating process in the case of executing the multiplication of $5 \times 3 = 15$.

First, the contents of all the shift registers are cleared to 0 beforehand. Next, when the multiplicand 5 is set by means of a number setting key 5 (not shown) of the calculator, it is inputted from an input terminal *i* (FIG. 1) into and stored in the circulative memory circuit which the shift register R_X, the correcting memory circuit DM and the feedback line FL_4 constitute. Subsequently, a function key x is depressed, and the multiplier 3 is set by a number setting key 3. Then, the multiplicand 5 is transferred from the register R_X through the line FL_1 to the register R_Y, and is circulated and held by the feedback path FL_3. On the other hand, the multiplier 3 is stored, as in the foregoing setting of the multiplicand 5, in the circulative memory circuit constituted of the shift register R_X, the correcting memory circuit DM and the feedback path FL_4. The circulative memory circuit stores therein the first or second operand corresponding to eight digits. The remaining eight digits are held in the blank 0 state.

Next, a calculation starting key (⊟key) is depressed, to initiate the calculation. Then, the multiplicand 5 set in the calculating register R_Y is added to the information of the second display register R_{Xb} through the adder AD three times. The addition is carried out in the period of time in which the timing pulse Sp shown in FIG. 2*b* is at T_H. FIG. 5*b* illustrates the state in which, after the first addition, an added result 5 is set in the display register R_{Xb}. When the first addition is thus executed, 1 is subtracted from the multiplier 3 in R_{Xa}, and the information of R_{Xa} at LSD becomes 3−1=2. The subtraction for R_{Xa} is carried out by the information Dt_1 (refer to FIG. 1) for subtracting 1 as is generated in the period of time T_L of the timing pulse shown in FIG. 2*b*, and through the adder AD. Thereafter, the multiplicand 5 in R_Y is successively added to the information in R_{Xb} in the same way, until the information at LSD of R_{Xa} becomes 0. The situations are illustrated in FIGS. 5*c* and 5*d*. When the information of R_{Xa} becomes 0, the calculation is stopped. The calculated result 15 is shifted rightwards from R_{Xb} to R_{Xa}, and is set as in FIG. 5*e*. Thus, the multiplication is performed. In the case where the multiplier has many digits (at most eight digits), 1 is successively subtracted from the least significant digit to the most significant digit. In this case, the subtraction at each digit of the multiplier is carried out at LSD of R_{Xa}. By way of example, consider the case of the multiplication of $5 \times 13 = 65$. In a state in which the additions for 3 at the first digit of the multiplier 13 have been completed (refer to FIG. 5*d*), the whole information in R_X is shifted rightwards, and is set as in FIG. 6*a*. Thereafter, the addition for 1 at the second digit of the multiplier is conducted as shown in FIG. 6*b*. In this manner, the calculation is performed while the information of the multiplicand at the respective digits in R_{Xa} are successively shifted rightwards to the least significant digit LSD of R_{Xa}. Upon completion of the calculation, the answer is set with the standard

at LSD of R_{Xa} as illustrated in FIG. 6c. With such measure, if the calculated result exceeds the most significant digit MSD of R_{Xa}, part of the information of the calculated result can be also set in R_{Xb}, and hence, overflow is prevented. In the state before initiation of the calculation, it has been assumed that the second operand is stored in the circulative memory circuit of the register R_X, while the first operand is stored in the register R_Y. The calculation, however, may also be carried out with the positions of the first and second operands exchanged.

In case of performing division, processing is as below. By way of example, consider the case where the division of $4 \div 2 = 2$ is executed. As in the foregoing case of the multiplication, in a state in which number setting keys and a function key have been depressed, the first operand 4 is stored in the register R_Y, while the second operand 2 is stored in the circulative memory circuit including the register R_X. Next, the calculation starting key (=Key) is depressed. Then, a shift instruction is first issued, so that the second operand **2** is shifted from the register R_X through the line FL_1 to the register R_Y and is stored therein, while the first operand **4** is shifted from the register R_Y through the line FL_7 to the circulative memory circuit composed of the register R_X, adder AD and feedback line FL_4 and is stored therein (FIG. 7*a*). When a calculation starting instruction is subsequently issued to initiate the calculation, the dividend 4 is transferred to the least significant digit LSD of R_{Xb} as illustrated in FIG. 7*b*. The divisor 2 is successively subtracted from the information of LSD of R_{Xb}. FIG. 7*c* shows a state in which the subtraction has been conducted once, and in which an information (calculated result) 1 indicating the one subtraction is set (added) at LSD of R_{Xa}. In this manner, the subtractions are executed between R_{Xb} and R_Y until the information of R_{Xb} becomes 0. In consequence, the answer 2 of the division can be obtained at LSD of R_{Xa} as shown in FIG. 7*d*. In this case, the addition of 1 to the information of R_{Xa} is effected from the input Dt_1 shown in FIG. **1**. In the foregoing embodiments, the eight-digit register R_Y is prepared for eight-digit numerical information. However, such modification is possible that, in order to prevent overflow of an integral part or to discriminate the sign of a number, one more digit is added to make the memory capacity of the register R_Y **9** digits, that the memory capacity of the circulative memory circuit including the register R_X is accordingly made 18 digits, and that a digit signal Dt_9 is added to those $Dt_1 - Dt_8$.

As described above, according to the present invention, the delay type full adder for binary-coded decimal signals is adopted. It forms the loop-like closed circuit jointly with the display shift register having a capacity integral times as large as that of the calculating shift register, and conducts additions in the series synchronism system. Therefore, the system of the invention makes it unnecessary to employ a number of controlling gates between shift registers, as compared with a prior-art system shown in FIG. **8** in which the shift registers of equal capacities are arrayed in parallel. Further, the use of the delay type binary-coded decimal adder makes it possible to constitute of a single line the line of the loop-like closed circuit which is formed by the display register R_X, the delay type adder AD, a line *a* and the line FL_2. A line *b* for the connection between the calculating register R_Y and the adder AD can also be constituted of a single line.

Consequently, in accordance with the present invention, the number of controlling gate circuits to be connected anteriorly and posteriorly to each shift register can be made small. The correction memory circuit DM for correcting a pure binary number to a binary-coded decimal number, and the circulating register for display can be combined into one unit. Therefore, the circuit arrangement can be made simple. In case of bringing the construction according to the present invention into the form of an integrated semi-conductor circuit, the above feature is very advantageous in the degree of integration and the arrangement of the respective elements. In addition, in conformity with the present invention, the display register forms, along with the delay type adder, the loop-like closed circuit. Therefore, a predetermined position of the display register can be easily selected and controlled by the sector pulse. Processed information signals from the adder AD (information signals for display) can be successively set from the least significant digit of the lower digit portion one of the series-connected display shift registers. Therefore, the memory capacity for the display information signal can be made equal to the total capacity of the loop-like closed circuit. For example, in the case of the embodiment, a calculated result of at most **16** digits can be stored. In this case, when the number of digits of the indicating unit is eight, it is also allowed to control the lines FL_5 and FL_6 in FIG. **1** by making use of the foregoing sector pulses Sp, so as to display the higher eight digits or the lower eight digits. Overflow due to multiplication processing etc. can be prevented in this way.

Moreover, in conformity with the present invention, a calculated result to be displayed is circularly held by the loop-like closed circuit which includes the display register and the delay type adder. Therefore, it is not necessary to provide any special feedback path for the display register, and the dynamic display system can be easily adopted for the indicator unit (IN). More specifically, information is transmitted from the LSD part of the higher-digit display register R_{Xb} or that of the lower-digit display register R_{Xa} to the indicator in FIG. **1** every digit by means of a gate controlled by every four-bit time. Thus, dynamic display signals can be easily taken out.

In this manner, with the digital processing system according to the present invention, calculating processing such as multiplication and division can be easily executed in the simple construction and using the binary-coded decimal numbers. In accordance with the invention, the circulative register can have the length shortened in its joint use for the memory circuit for the binary-coded decimal number correction. In addition, overflow can be aliminated with the resultant various advantages.

Obviously, many modifications and variations of the present invention are possible in the light of the above teachings. It should therefore be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

We claim:

1. A digital processing system comprising a binary-coded decimal full adder having two binary full adders and a correction detecting memory circuit arranged therebetween and serving to subject two information

inputs to addition and subtraction, the correction detection memory circuit having a memory capacity, a first shift register having a fixed memory capacity and having an output connected to an input of said binary-coded decimal full adder, a second shift register having a memory capacity and having an output connected to another input of said binary-coded decimal full adder, means for connecting an output of said binary-coded decimal full adder with an input of said second shift register so as to form a loop-like circuit of said second shift register and said binary-coded decimal full adder, the total memory capacity of said second shift register and said detecting memory circuit being n times as large as said memory capacity of said first shift register where *n* is an integer of at least 2, and means for actuating the binary-coded decimal full adder to define a plurality of predetermined positions of said second shift register, information signals at said predetermined positions of said second shift register and in said first shift register being subjected to calculating and processing by said binary-coded decimal full adder, and a calculated and processed information signal being circularly held in said loop-like circuit.

2. A digital processing system according to claim **1**, wherein said correction detection memory circuit means includes first, second and third delay circuit means, correction judging circuit means, generator means, said first full adder having an output connected to said first delay circuit means and another output connected to said second delay circuit means and to said correction judging circuit means, said second delay circuit means having an output connected to a third input of said first full adder which receives an output from said first shift register and an output from said calculating shift register means, said first delay circuit means having an output connected to a first input of said second full adder and an output connected to said correction judging circuit means, said correction judging circuit means having an output connected to the third input of said first full adder and an output connected to said generator means, said generator means having an output connected to a second input of said second full adder, said second full adder having an output connected to said second shift register and an output connected to an input of a gate circuit means, said gate circuit means adapted to receive a predetermined timing signal at another input thereof and having an output connected to said third delay circuit means, said third delay circuit means having an output connected to a third input of said second full adder.

3. A digital processing system comprising binary-coded decimal full adder means for subjecting two information inputs to at least one of addition and subtraction, said full adder means including circuit memory means having a fixed memory capacity, display shift register means providing an output to one input of said full adder means and including first and second series connected shift registers each having a memory capacity, and calculating shift register means having a predetermined memory capacity, said calculating shift register means receiving the output of said display shift register means at an input thereof and providing an output to another input of said full adder means, the output of the full adder means being applied to an input of the second shift register and the output of the first shift register being applied to the one input of said full adder means so as to form a loop-like circuit for circulation of information signals through the full adder means and the display shift register, the total memory capacity of said circuit memory means of said full adder means and said display shift register means being n times as large as the memory capacity of said calculating shift register means, where n is any integer greater than 1.

4. A digital processing system according to claim **3**, wherein the memory capacity of the first display shift register is equal to the memory capacity of the calculating shift register means, and the memory capacity of the second display shift register is equal to the memory capacity of the first display shift register minus the memory capacity of the circuit memory means of said full adder means.

5. A digital processing system according to claim **3**, wherein said binary-coded decimal full adder means includes first and second binary full adders and correction detection memory circuit means connected therebetween, said correction detection memory circuit means including said circuit memory means.

6. A digital processing system according to claim **5**, further comprising display means for displaying the contents of said display shift register means.

7. A digital processing system comprising binary-coded decimal full adder means for subjecting two information inputs to at least one of addition and subtraction, said binary-coded decimal full adder means including first and second binary full adders and correction detection memory circuit means connected therebetween; display shift register means providing an output to one input of said full adder means, said display shift register means including first and second series connected shift registers; and calculating shift register means having a predetermined memory capacity, said calculating shift register means receiving the output of said display shift register means at an input thereof and providing an output to another input of said full adder means; the output of the full adder means being applied to an input of the second shift register and the output of the first shift register being applied to the one input of said full adder means so as to form a loop-like circuit for circulation of information signals through the full adder means and the display shift register; said correction detection memory circuit means including first, second and third delay circuit means, correction judging circuit means, and generator means, said first full adder having an output connected to said first delay circuit means and another output connected to said second delay circuit means and to said correction judging circuit means, said second delay circuit means having an output connected to a third input of said first full adder, said first full adder also receiving an output from said first shift register and an output from said calculating shift register, said first delay circuit means having an output connected to said second full adder and an output connected to said correction judging circuit means, said second full adder having an output connected to said second display register and another output connected to said third delay circuit means, said third delay circuit means having an output connected to an input of said second full adder and to an input of said correction judging circuit means, said correction judging circuit means having an output connected to said generator means, and said generator means having an output connected to another input of said second full adder.

8. A digital processing system comprising binary-coded decimal full adder means for subjecting two information inputs to at least one of addition and subtraction, said full adder means having circuit memory means having a memory capacity, display shift register means including a first and a second shift register connected in series and having memory capacities, respectively, calculating shift register means having a memory capacity, first means for supplying an output of said first shift register to an input of said full adder means, second means for supplying an output of said full adder means to an input of said second shift register, third means for supplying an output of said calculating shift register to another input of said full adder means, and fourth means for supplying an output of said first shift register to an input of said calculating shift register and bypassing said full adder means.

9. A system according to claim 8, wherein the memory capacity of said circuit memory means of said full adder means is 4 N_1 bits, the memory capacities of said first shift register and said calculating shift register are both $4N_2$ bits and the memory capacity of said second shift register is $4(N_2-N_1)$ bits, where N_1 and N_2 are integers of at least one, and $N_2 > N_1$.

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