(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 December 2016 (01.12.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/189751 A1

(51) International Patent Classification:
H03K 19/177 (2006.01)

(21) International Application Number:
PCT/JP2015/066125

(22) International Filing Date:
28 May 2015 (28.05.2015)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

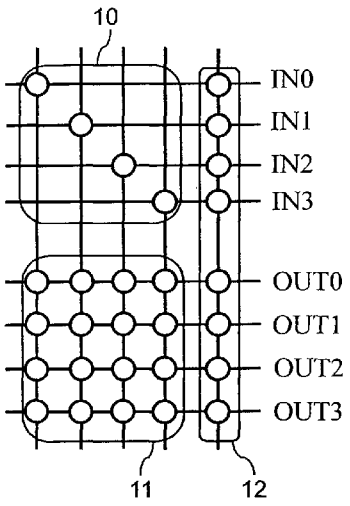
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: RECONFIGURABLE CIRCUIT

FIG.3



(57) **Abstract**: A reconfigurable circuit comprises: a first level crossbar switch (10) that has first non-volatile resistive switches; a second level crossbar switch (11) that has second non-volatile resistive switches; and a first wire and third non-volatile resistive switches that are used for redundancy, wherein input wires of the second level crossbar switch (11) are connected to output wires of the first level crossbar switch (10) one-to-one, and input wires of the first level crossbar switch (10) and output wires of the second level crossbar switch (11) are connected to the first wire through the third non-volatile resistive switches. The reconfigurable circuit relieves both fixed ON and OFF defects of non-volatile resistive switches automatically.

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DESCRIPTION

TITLE OF THE INVENTION

RECONFIGURABLE CIRCUIT

Technical Field

[0001]

This invention is about a reconfigurable circuit using non-volatile resistive switches.

Background Art

[0002]

Semiconductor integrated circuit (IC) is constructed by transistors built on a semiconductor substrate and upper layer wires used to connect transistors. The patterns of the transistors and wires are determined in the IC design stage. The interconnections between the transistors cannot be changed after fabrication.

[0003]

In reconfigurable circuits such as FPGAs (Field-Programmable Gate Arrays), configuration data including operation and interconnection information is stored in memories, so that different logic operations and interconnections can be realized by configuring the memories after fabrication according to requirements of end users. In most of commercial FPGAs, SRAM (Static Random Access Memory) is used to store the configuration data.

[0004]

Typically, each SRAM is composed of 6 transistors and each modern FPGA chip has more than 10M SRAMs, which causes extremely large area overhead and cost. Data routing is realized by a large number of CMOS switches (each composed of one SRAM and one nMOS transistor), which causes low logic density, large power consumption and large delay.

[0005]

To overcome the problems of SRAM-based FPGAs, non-volatile resistive switches (NVRSs) integrated between wires up on transistor layer have been proposed for small area overhead. Non-volatility also contributes to zero standby power consumption.

[0006]

As an example, in the reconfigurable circuits shown in the non-patent document 1 and patent document 1, a non-volatile resistive atom switch (NVRAS) composed of a solid-electrolyte sandwiched between an active electrode (Cu) and an inert electrode (Ru) has high OFF/ON resistance ratio (>10^5), therefore the NVRAS can replace the CMOS switch for small area overhead and high logic density. Moreover, lower capacitance of the NVRAS than nMOS transistor leads to low power consumption and high speed. The ON/OFF state of the NVRAS is hold even when not powered, therefore when power is turned on configuration data can be loaded immediately.

Problem to be solved by the invention

[0007]

Reconfigurable circuits may contain redundant circuitry that can be used to repair a reconfigurable circuit that contains defective transistors and wires in manufacturing, thereby improving production yield. For example, in patent document 2 and patent document 3, if defects are detected prior to shipment, redundant circuitry will replace the defective circuit before shipping to customers. Customers can configure the repaired device to perform desired logic functions correctly. However, the redundant circuitry is wasted if there is no defect, which causes area, delay and power consumption overhead.

[0008]

Moreover, for the NVRS-based FPGA, rewrite cycle count of the NVRSs is limited (typically 1000 for the NVRAS in patent document 1). Defects of NVRSs may occur when customers configure the device after shipment, because a few of the NVRSs may have less rewrite cycle count than guaranteed rewrite cycle count. The defective NVRSs may be fixed ON or OFF when reconfiguration is performed, so that customers cannot configure the device to implement desired logic functions correctly. As a result, the broken device should be recalled and a substitute device should be delivered, which causes large cost.

[0009]

It is desired to relieve defective NVRSs automatically after shipment to make sure customers can perform desired logic function correctly even if defects of NVRSs occur. One of relief methods usually used in memory chip is replacement of defective row/column NVRSs by redundant row/column NVRSs as shown in patent document 4.

In NVRS-based reconfigurable circuit, crossbar switch using NVRSs realizes data routing. The relief method may be used to relieve defective NVRSs. As an example shown in FIG. 1A, one-level crossbar switch 301 is used to realize 4 inputs and 4 outputs data routing, and redundant switches 302 are used to relieve a defective NVRS S_{22}. The box in FIG. 1A shows simbols that indicate the ON and OFF states in which a normal NVRS is set and a defective NVRS is fixed. The data routing from IN2 to OUT2 cannot be realized because of the fixed OFF S_{22}. As shown in FIG. 1B, the redundant NVRSs S_{R2} and S_{2R} can be turned ON to relieve the data routing from IN2 to OUT2. The fixed OFF S_{22} is successfully relieved by redundant switches 302. However, as shown in FIG.2A, if a fixed ON NVRS S_{12} defect occurs, both the IN1 and IN2 are shorted, even if the redundant NVRSs S_{R2} and S_{2R} are turned ON shown in FIG.2B, the fixed ON defect cannot be relieved. The fixed ON S_{12} is unsuccessfully relieved by redundant switches 302.

[0010]

The purpose of this patent is to provide a reconfigurable circuit to relieve both fixed ON and OFF defects of NVRSs automatically to make sure customer can perform desired logic function even if defects occur.

[0011]

Non-patent document 1: N. Banno et al., "Reliable Solid-Electrolyte Crossbar Switch for Programmable Logic Device", Symposium on VLSI Technology, pp. 115-116, (2010).

Patent document 1: US8816312

Patent document 2: US4899067

Patent document 3: US8860460

Patent document 4: US8837242

Summary of the Invention

[0012]

The present invention provides a reconfigurable circuit comprises: a first level crossbar switch that has first non-volatile resistive switches; a second level crossbar switch that has second non-volatile resistive switches; and a first wire and third non-volatile resistive switches that are used for redundancy, wherein input wires of the second level crossbar switch are connected to output wires of the first level crossbar

switch one-to-one, and input wires of the first level crossbar switch and output wires of the second level crossbar switch are connected to the first wire through the plurality of third non-volatile resistive switches.

[0013]

According to the reconfigurable circuit by the present invention, both fixed ON and OFF defects of NVRSs can be automatically relieved to make sure customer can perform desired logic function even if defects occur.

Brief Description of the Drawings

[0014]

The invention will now be described with reference to the accompanying drawings.

FIG.1A illustrates that a fixed OFF NVRS defect occurs in a conventional one-level crossbar switch with redundant switches.

FIG.1B illustrates that the fixed OFF NVRS defect can be relieved by the redundant switches.

FIG.2A illustrates that a fixed ON NVRS defect occurs in a conventional one-level crossbar switch with redundant switches.

FIG. 2B illustrates that the fixed OFF NVRS defect cannot be relieved by the redundant switches.

FIG.3 illustrates a two-level crossbar switch with a redundant column in a NVRS-based reconfigurable circuit according to embodiment 1.

FIG.4A illustrates that a fixed OFF NVRS defect occurs in a two-level crossbar switch with a redundant column according to embodiment 1.

FIG.4B illustrates that the fixed OFF NVRS defect can be relieved by the redundant column according to embodiment 1.

FIG.5A illustrates that a fixed ON NVRS defect occurs in a two-level crossbar switch with a redundant column according to embodiment 1.

FIG.5B illustrates that the fixed ON NVRS defect can be relieved by the redundant column according to embodiment 1.

FIG.6 illustrates structure of the NVRS-based reconfigurable circuit according to embodiment 1.

FIG.7 illustrates a write circuit of the NVRS in a two-level crossbar switch with a

redundant column according to embodiment 1.

FIG.8 illustrates a read circuit of the NVRS in a two-level crossbar switch with a redundant column according to embodiment 1.

FIG.9 illustrates an address comparator in the NVRS-based reconfigurable circuit according to embodiment 1.

FIG.10 illustrates a pre-decoder in the NVRS-based reconfigurable circuit according to embodiment 1.

FIG.11 illustrates a controller in the NVRS-based reconfigurable circuit according to embodiment 1.

FIG.12 illustrates configuration flow chart of the NVRS-based reconfigurable circuit when a fixed OFF NVRS defect occurs according to embodiment 1.

FIG.13 illustrates configuration flow chart of the NVRS-based reconfigurable circuit when a fixed ON NVRS defect occurs according to embodiment 1.

FIG.14 illustrates a two-level crossbar switch with multiple redundant columns in a NVRS-based reconfigurable circuit according to embodiment 2.

FIG.15 illustrates structure of the NVRS-based reconfigurable circuit according to embodiment 2.

FIG.16 illustrates a pre-decoder in the NVRS-based reconfigurable circuit according to embodiment 2.

FIG.17 illustrates a write circuit of the NVRS in a two-level crossbar switch with multiple redundant columns according to embodiment 2.

FIG.18 illustrates a read circuit of the NVRS in a two-level crossbar switch with multiple redundant columns according to embodiment 2.

FIG.19A illustrates that multiple fixed OFF NVRS defects occur in a two-level crossbar switch with multiple redundant columns according to embodiment 2.

FIG.19B illustrates that the fixed OFF NVRS defects can be relieved by the redundant columns according to embodiment 2.

FIG.20A illustrates that fixed ON NVRS defects occur in a two-level crossbar switch with multiple redundant columns according to embodiment 2.

FIG.20B illustrates that the fixed ON NVRS defects can be relieved by the redundant column according to embodiment 2.

FIG.21A illustrates a two-level crossbar switch in a NVRS-based reconfigurable

circuit according to embodiment 3.

FIG.21B illustrates a two-level crossbar switch in a NVRS-based reconfigurable circuit according to embodiment 3.

FIG.21C illustrates a two-level crossbar switch in a NVRS-based reconfigurable circuit according to embodiment 3.

FIG 21D illustrates a two-level crossbar switch in a NVRS-based reconfigurable circuit according to embodiment 3.

FIG.22 illustrates a write circuit of the NVRS in a two-level crossbar switch with multiple redundant columns according to embodiment 3.

FIG.23 illustrates a read circuit of the NVRS in a two-level crossbar switch with multiple redundant columns according to embodiment 3.

FIG.24A illustrates a non-volatile switch cell using 1 NVRS.

FIG.24B illustrates a non-volatile switch cell using 1 transistor 2 NVRSs.

Detailed description of embodiments

[0015]

Embodiment 1

A first exemplary embodiment of the present invention will be described. FIG.3 illustrates a two-level crossbar switch with a redundant column in a NVRS-based reconfigurable circuit. A 4x4 crossbar switch is used as an example. First and second wires are disposed in a first direction, while third wires and a fourth wire are disposed in a second direction intersecting the first direction. Inputs IN0, IN1, IN2 and IN3 are coupled to the first wires one-to-one, and outputs OUT0, OUT1, OUT2 and OUT3 are coupled to the second wires one-to-one. The NVRS-based reconfigurable circuit comprises first level crossbar switch 10, second level crossbar switch 11 and redundant column 12. In first level crossbar switch 10, first NVRSs through which the first wires are connected to the third wires. In second level crossbar switch 11, second NVRSs through which the second wires are connected to the third wires. In redundant column 12, third NVRSs through which the fourth wire are connected to the first and second wires. The third NVRSs in the redundant column should be kept OFF, if there is no defective NVRS in the two-level crossbar switch. FIG.3 only shows one kind of two-level crossbar switches. The present invention is available for the other kinds of two-level crossbar switches. For example, both the first NVRSs and second NVRSs

may be sparsely arranged.

[0016]

FIGs.4A and 4B illustrate relief of a fixed OFF NVRS defect in the reconfigurable circuit according to embodiment 1. The box in FIG. 4A shows simbols that indicate the ON and OFF states in which a normal NVRS is set and a defective NVRS is fixed. As shown in FIG.4A, to perform routing paths IN1-to-OUT1 and IN2-to-OUT2, NVRSs S_{11}, S_{22}, S_{51} and S_{62} should be turned on. However, the routing path IN2-to-OUT2 cannot be successfully performed, because the NVRS S_{62} fails to be turned ON (fixed OFF defect). To relieve the fixed OFF S_{62}, redundant column 12 replaces the defective column VL2. The NVRSs R_{S2} and R_{S6} in redundant column 12 are turned ON as shown in FIG.4B. As a result, the routing path IN2-to-OUT2 is relieved.

[0017]

FIGs.5A and 5B illustrate relief of a fixed ON NVRS defect in the reconfigurable circuit according to embodiment 1. As shown in FIG.5A, to perform routing paths IN1-to-OUT1 and IN2-to-OUT2, NVRSs S_{11}, S_{22}, S_{51} and S_{62} should be turned on. However, the NVRS S_{52} fails to be turned OFF (fixed ON defect), which results in collision of IN1 and IN2. As a result, both the routing paths IN1-to-OUT1 and IN2-to-OUT2 cannot be successfully performed. To relieve the fixed ON S_{52}, redundant column 12 replaces the defective column VL2. The NVRSs R_{S2} and R_{S6} in redundant column 12 are turned ON, and S_{22} and S_{62} in defective column VL2 are turned OFF shown in FIG.5B. As a result, both the routing paths IN1-to-OUT1 and IN2-to-OUT2 are relieved.

[0018]

FIG.6 illustrates structure of the reconfigurable circuit according to embodiment 1. The reconfigurable circuit comprises controller 21, programmable logic cell array (PLCA) 22, row and column write drivers 23, 24, row and column address decoders 33, 34, sense amplifier (SA) 25, non-volatile memory 26, address comparator (CMP) 27, pre-decoder 28, a special-purpose input/output (SPIO) and a general-purpose input/output (GPIO). In PLCA 22, many logic blocks are connected with each other using the two-level crossbar switches shown in FIG.3. Any logic function can be performed according to configuration data from outside through the SPIO. Controller 21 receives configuration data and row/column addresses from outside, controls write and

read operation of NVRSs, detect the defective column address by comparing actual configuration result of NVRSs with the configuration data. Row and column address decoders 33, 34 receiving addresses from controller 21 select a NVRS to be written or read. Row and column write drivers 23, 24 generate set/reset voltage to turn ON/OFF the selected NVRS. SA 25 reads the state of the selected NVRS. Non-volatile memory 26 stores defective column address detected by controller 21. If a defect of a NVRS occurs, controller 21 will enable CMP 27 to compare a column address with the defective column address stored in non-volatile memory 26. If same, a redundant column enable signal HIT will be activated to "HIGH". Pre-decoder 28 will prevent the column address from entering column address decoder 34, and enable redundant column 12. As a result, the NVRSs in redundant column 12 will be configured instead of the NVRSs in the defective column. The redundant column enable signal HIT corresponds to a redundancy enable signal. A line, through which the HIT is transmitted, is referred to as a redundancy enable signal line.

[0019]

FIG.7 illustrates a write circuit for the NVRSs in NVRS-based reconfigurable circuit according to embodiment 1. The first and second wires are connected to first transistors one-to-one. Row address decoder 33 controls the first transistors to select one of the first and second wires to be connected to a row write driver PV_X. The third wires are connected to second transistors one-to-one. Column address decoder 34 controls the second transistors to select one of the third wires to be connected to a column write driver PV_Y. The fourth wire is connected to the column write driver PV_Y through a third transistor controlled by redundant column 12 enable signal HIT. Let me explain how to write S51 as an example. We set row address X=5 and column address Y=1, PV_X and PV_Y are connected to a NVRS S_{51}. In case S_{51} is a NVRAS, PV_X is connected to an active electrode (Cu) and PV_Y is connected to an inert electrode (Ru). If we want to configure S_{51} as "ON" state, PV_X should supply a high voltage and PV_Y should supply a low voltage. In another word, a positive voltage is applied to S_{51}. On the other hand, if we want to configure S_{51} as "OFF" state, PV_X should supply a low voltage and PV_Y should supply a high voltage. In another word, a negative voltage is applied to S_{51}.

[0020]

FIG.8 illustrates a read circuit for the NVRSs in NVRS-based reconfigurable

circuit according to embodiment 1. The principle is to apply a relative small positive voltage to a target NVRS, and use SA 25 to detect the current flows through the target NVRS to read its state. It is different from FIG.7 that the the first and second wires are connected to ground line GND through the first transistors, and the third wires and the fourth wire are connected to SA 25 through the second transistors and the third transistor, respectively. Let me explain how to read state of S51 as an example. We set row address X=5 and column address Y=1, S_{51} is connected to SA 25 and GND. SA 25 clamps a fixed voltage (typically lower than 1V) applied to S_{51}, and detects current flow through S_{51}. If large current flows, the state of S_{51} is ON, otherwise, if there is almost no current flow, the state is OFF.

[0021]

FIG.9 illustrates the CMP in NVRS-based reconfigurable circuit according to embodiment 1. CMP 27 includes 4 XNOR gates that compare respective bits of a defective column address YDAdd with respective bits of the column address YAdd, and a 5-input AND gate that receives the enable bit EN and 4 output signals from these 4 XNOR gates. HIT is activated to "HIGH" on condition that all the bits of the defective column address YDAdd match the bits of the column address YAdd and that the enable bit EN is "HIGH".

[0022]

FIG.10 illustrates the pre-decoder in NVRS-based reconfigurable circuit according to embodiment 1. Pre-decoder 28 consists of 4 AND gates and a NOT gate. When HIT is activated to "HIGH", the output pre-decoded column address bits $YAddpr_0$~$YAddpr_3$ become "LOW". Otherwise, when HIT is "LOW", the output pre-decoded column address bits $YAddpr_0$~$YAddpr_3$ are equal to the column address bits $YAdd_0$~$YAdd_3$.

[0023]

FIG.11 illustrates the controller in NVRS-based reconfigurable circuit according to embodiment 1. Controller 21 comprises external I/F circuit 41, functional unit (FU) 42, memory 43, address buffer 44, data buffer 45 and internal bus 46. External I/F circuit 41 controls input/output data transfer of the SPIO. FU 42 is used to control write/read operation of NVRSs, and detect defective NVRSs according to the program stored in memory 43. Address buffer 44 stores addresses from outside. Data buffer 45 stores configuration data from outside and configuration result read from PLCA 22.

[0024]

FIG.12 illustrates configuration flow chart of the NVRS-based reconfigurable circuit when a fixed OFF NVRS defect occurs according to embodiment 1. We assume initial status is that a NVRS-based reconfigurable circuit has been programmed to perform a logic circuit A, and no NVRS defect has occurred. Purpose is to reprogram the NVRS-based reconfigurable circuit to perform another logic circuit B. First step 101 is to reset (turn OFF) all the NVRSs except the NVRSs in a redundant column which are initially set to be "OFF" state prior to shipment. Second step 102 is to configure the NVRS-based reconfigurable circuit according to the configuration data of the circuit B. Third step is get actual configuration result by reading out state of NVRSs using the read circuit shown in FIG.7 (steps 103 and 104). Fourth step 105 is to compare the actual configuration result with the configuration data. If they are matched at step 106, the circuit B is successfully performed in the NVRS-based reconfigurable circuit. Otherwise, if a fixed OFF NVRS defect occurs, the corresponding defective column is replaced by the redundant column (step 107). As shown in FIG.4, the NVRS S_{22} is not necessary to be turned OFF for the replacement. Therefore the process directly loops back to second step 102 to configure the redundant column. As a result, the defective column is automatically replaced by the redundant column.

[0025]

FIG.13 illustrates configuration flow chart of the NVRS-based reconfigurable circuit when a fixed ON NVRS defect occurs according to embodiment 1. It is different from the FIG.12 that if a fixed ON NVRS defect occurs, the process loops back to first step 101 (reset all the NVRSs). As shown in FIG.5, to replace of the defective column VL2 by the redundant column VLR, it is necessary to turn OFF the S_{22} and S_{62}. If not, collision of the IN1 and IN2 still occurs even if replacement is done.

[0026]

Embodiment 2

Next, a second embodiment according to the present invention will be presented. The present embodiment discloses a two-level crossbar switch with multiple redundant columns in a NVRS-based reconfigurable circuit according to embodiment 2. More than one defect column can be relieved.

[0027]

FIG.14 illustrates a two-level crossbar switch with multiple redundant columns in a NVRS-based reconfigurable circuit. A 4x4 crossbar switch is used as an example. First and second wires are disposed in a first direction, while third and fourth wires are disposed in a second direction intersecting the first direction. Inputs IN0, IN1, IN2 and IN3 are coupled to the first wires one-to-one, and outputs OUT0, OUT1, OUT2 and OUT3 are coupled to the second wires one-to-one. The NVRS-based reconfigurable circuit comprises first level crossbar switch 10, second level crossbar switch 11 and redundant columns 13. In first level crossbar switch 10, first NVRSs through which the first wires are connected to the third wires. In second level crossbar switch 11, second NVRSs through which the second wires are connected to the third wires. In redundant columns 13, third NVRSs through which the fourth wires are connected to the first and second wires. The third NVRSs in redundant columns 13 should be kept OFF, if there is no defective NVRS in the two-level crossbar switch. FIG.14 only shows one kind of two-level crossbar switches. The present invention is available for the other kinds of two-level crossbar switches. For example, both the first NVRSs and second NVRSs may be sparsely arranged.

[0028]

FIG.15 illustrates structure of the reconfigurable circuit according to embodiment 2. Different parts of the reconfigurable circuit according to embodiment 2 from the reconfigurable circuit according to embodiment 1 are shown as follows. We use 4 redundant columns 13 as an example to explain the differences. 4 non-volatile memories 26 are used to store addresses of maximum 4 defective columns. 4 CMPs 27 are used to match the maximum 4 defective columns' addresses and a column address from controller 21, and generate HIT_0~HIT_3 to control corresponding to 4 redundant columns 13 in PLCA 22.

[0029]

The pre-decoder shown in FIG.16 is different from that shown in FIG.10 of the reconfigurable circuit according to embodiment 1. Pre-decoder 38 according to embodiment 2 consists of 4 AND gates and a NOR gate. When at least one of the HIT_0~HIT_3 is activated to "HIGH", the output pre-decoded column address bits $YAddpr_0$~$YAddpr_3$ become "LOW". Otherwise, when all of HIT_0~HIT_3 are "LOW", the output pre-decoded column address bits $YAddpr_0$~$YAddpr_3$ are equal to input

column address bits $YAdd_0$~$YAdd_3$.

[0030]

FIG.17 and FIG.18 illustrate write and read circuits for the NVRSs in NVRS-based reconfigurable circuit according to embodiment 2, respectively. It is different from the write and read circuits according to embodiment 1 that HIT_0~HIT_4 are used to control third transistors of redundant columns 13. For example, if the column VL1 is defective and its address Y=1 is stored in a non-volatile memory M0 shown in FIG.15, when controller 21 sends an column address Y=1, HIT_0 is active to "HIGH", and the redundant column VLR0 is written or read instead of the defective column VL1.

[0031]

FIGs.19A and 19B illustrate relief of multiple fixed OFF NVRS defects in the reconfigurable circuit according to embodiment 2. As shown in FIG.19A, to perform routing paths IN0-to-OUT0, IN1-to-OUT1 and IN2-to-OUT2, NVRSs S_{00}, S_{11}, S_{22}, S_{40}, S_{51} and S_{62} should be turned on. However, the routing paths IN0-to-OUT0 and IN2-to-OUT2 cannot be successfully performed, because the NVRSs S_{40} and S_{62} fail to be turned ON (fixed OFF defect). To relieve the fixed OFF S_{40} and S_{62}, the redundant columns VLR0 and VLR1 replace the defective columns VL0 and VL2, respectively. The NVRSs R_{00}, R_{40}, R_{21} and R_{61} in the redundant columns VLR0 and VLR1 are turned ON as shown in FIG.19B. As a result, the routing paths IN0-to-OUT0 and IN2-to-OUT2 are relieved.

[0032]

FIGs.20A and 20B illustrate relief of multiple fixed ON NVRS defects in the reconfigurable circuit according to embodiment 2. As shown in FIG.20A, to perform routing paths IN0-to-OUT0, IN1-to-OUT1 and IN2-to-OUT2, NVRSs S_{00}, S_{11}, S_{22}, S_{40}, S_{51} and S_{62} are turned on. However, the NVRSs S_{41} and S_{52} fail to be turned OFF (fixed ON defect), which results in collision of IN0, IN1 and IN2. As a result, all the routing paths IN0-to-OUT0, IN1-to-OUT1 and IN2-to-OUT2 cannot be successfully performed. To relieve the fixed ON S_{41} and S_{52}, the redundant columns VLR0 and VLR1 replace the defective column VL1 and VL2, respectively. The NVRSs R_{10}, R_{50}, $R_{21}$and R_{61} in the redundant columns VLR0 and VLR1 are turned ON, and S_{11}, S_{51}, S_{22} and S_{62} in defective columns VL1 and VL2 are turned OFF shown in FIG.20B. As a result, all the

routing paths IN0-to-OUT0, IN1-to-OUT1 and IN2-to-OUT2 are relieved.

[0033]

Embodiment 3

Next, a third embodiment according to the present invention will be presented. The present embodiment discloses low-power high-write-reliability NVRS-based reconfigurable circuit.

[0034]

The present embodiment focuses on a particular kind of two-level crossbar switch, where NVRSs are arranged on the diagonal line of the first or second level crossbar switch. FIGs.21A to 21D show some examples. As shown in FIGs.21A and 21B, diagonally arranged NVRSs in each of first level crossbar switches 10, 14 are used to control inputs IN0~IN3 connected to second level crossbar switch 11, and second level crossbar switch 11 can be reconfigured to perform different routing paths. As shown in FIGs.21C and 21D, first level crossbar switch 15 can be reconfigured to perform different routing paths, and diagonally arranged NVRSs in each of second level crossbar switches 16, 17 are used to control outputs OUT0~OUT3. The diagonally arranged NVRSs are used to enable the two-level crossbar switch, and are initially turned ON prior to shipment. Diagonally arranged NVRS in a first (second) level crossbar switch are turned OFF only when fixed "ON" NVRS defects occur in a second (first) level crossbar switch, which leads to high reliability of the diagonally arranged NVRSs.

[0035]

FIG.22 and FIG.23 illustrates write and read circuits of the NVRS in a two-level crossbar switch with multiple redundant columns according to embodiment 3, respectively. The two-level crossbar switch shown in FIG.21A is used as an example to show the difference between the write and read circuits according to embodiment 2 and those according to embodiment 3. First and second level row address decoders 33-1, 33-2 are used for the first and second level crossbar switches 10, 11, respectively. A first switch is coupled between power supply VDD and first row address decoder 33-1. A second switch is coupled between ground line GND and first row address decoder 33-1. When the first and second switches are turned OFF, first row address decoder 33-1 loses power entirely. On the other hand, when the first and second switches are turned ON, first row address decoder 33-1 receives power. If the two- level crossbar

switch shown in FIG.21C or 21D is used, the first and second switches will be provided in second row address decoder 33-2 instead of first row address decorder 33-1. Power gating technology is introduced in the first level row address decoder. Sleep signal is not active to "HIGH" until fixed ON NVRS defects occur in the second level crossbar switch, which leads low power consumption.

[0036]

In the present invention, a circular symbol used to indicate a NVRS in embodiments 1 to 3 may include all kinds of switch cells composed of NVRSs. For example, not only the switch cell composed of one NVRS R1 shown in FIG.24A but also the switch cell composed of two NVRSs R1, R2 and one transistor shown in FIG.24B are included in the present invention. ON/OFF resistance ratio of each of the NVRSs in enbodiments 1 to 3 is over 10^4. Each of the NVRSs in enbodiments 1 to 3 comprises a metal oxide resistance change device or a solid electrolyte resistance change device. A semiconductor device may comprise the reconfigurable circuit in embodiments 1 to 3.

[0037]

The reconfigurable circuit in the present invention may be used in mobile phone, IoT (Internet of Things) devices, and so on.

[0038]

It is apparent that the present invention is not limited to the above embodiments, but may be modified and changed without departing from the scope and spirit of the invention.

[0039]

(Further exemplary embodiment 1) A reconfigurable circuit comprising:

a first level crossbar switch that has first non-volatile resistive switches;

a second level crossbar switch that has second non-volatile resistive switches; and

a first wire and third non-volatile resistive switches that are used for redundancy, wherein

input wires of said second level crossbar switch are connected to output wires of said first level crossbar switch one-to-one, and

input wires of said first level crossbar switch and output wires of said second level crossbar switch are connected to said first wire through said plurality of third

non-volatile resistive switches.

[0040]

(Further exemplary embodiment 2) The reconfigurable circuit according to Further exemplary embodiment 1, wherein

said third non-volatile resistive switches are fully arranged on said first wire.

[0041]

(Further exemplary embodiment 3) The reconfigurable circuit according to Further exemplary embodiment 1, wherein

more than two said first wires are provided; and

said first wires are connected to said input wires of said first level crossbar switch and said output wires of said second level crossbar switch through said third non-volatile resistive switches.

[0042]

(Further exemplary embodiment 4) The reconfigurable circuit according to Further exemplary embodiment 3, wherein

said third non-volatile resistive switches are fully arranged on said first wires.

[0043]

(Further exemplary embodiment 5) The reconfigurable circuit according to Further exemplary embodiment 1, wherein

said first non-volatile resistive switches are diagonally arranged in said first level crossbar switch, and said second non-volatile resistive switches are fully or sparsely arranged in said second level crossbar switch.

[0044]

(Further exemplary embodiment 6) The reconfigurable circuit according to Further exemplary embodiment 5, wherein

said input wires of said first level crossbar switch are connected to source terminals of first transistors one-to-one, wherein

gate terminals of said first transistors are connected to a first row address decoder, and drain terminals of said first transistors are connected to a row write driver;

said output wires of said second level crossbar switch are connected to source terminals of second transistors one-to-one, wherein

gate terminals of said second transistors are connected to a second row address

decoder, and drain terminals of said second transistors are connected to said row write driver.

[0045]

(Further exemplary embodiment 7) The reconfigurable circuit according to Further exemplary embodiment 6, wherein

a first switch is coupled between power supply and said first row address decoder, and a second switch is coupled between ground line and said first row address decoder, wherein

when said first and second switches are turned OFF, said first row address decoder loses power entirely, and when said first and second switches are turned ON, said first row address decoder receives power.

[0046]

(Further exemplary embodiment 8) The reconfigurable circuit according to Further exemplary embodiment 1, wherein

said first non-volatile resistive switches are fully or sparsely arranged in said first level crossbar switch, and said second non-volatile resistive switches are diagonally arranged in said second level crossbar switch.

[0047]

(Further exemplary embodiment 9) The reconfigurable circuit according to Further exemplary embodiment 8, wherein

said input wires of said first level crossbar switch are connected to source terminals of first transistors one-to-one, wherein

gate terminals of said first transistors are connected to a first row address decoder, and drain terminals of said first transistors are connected to a row write driver;

said output wires of said second level crossbar switch are connected to source terminals of second transistors one-to-one, wherein

gate terminals of said second transistors are connected to a second row address decoder, and drain terminals of said second transistors are connected to said row write driver.

[0048]

(Further exemplary embodiment 10) The reconfigurable circuit according to Further exemplary embodiment 9, wherein

a first switch is coupled between power supply and said second row address decoder, and a second switch is coupled between ground line and said second row address decoder, wherein

when said first and second switches are turned OFF, said second row address decoder loses power entirely, and when said first and second switches are turned ON, said second row address decoder receives power.

[0049]

(Further exemplary embodiment 11) The reconfigurable circuit according to any one of Further exemplary embodiments 1 to 10, wherein

ON/OFF resistance ratio of each of said first, second and third non-volatile resistive switches is over 10^4.

[0050]

(Further exemplary embodiment 12) The reconfigurable circuit according to any one of Further exemplary embodiments 1 to 10, wherein

each of said first, second and third non-volatile resistive switches comprises a metal oxide resistance change device or a solid electrolyte resistance change device.

[0051]

(Further exemplary embodiment 13) A semiconductor device comprising:

the reconfigurable circuit according to any one of Further exemplary embodiments 1 to 12.

[0052]

(Further exemplary embodiment 14) A method for utilizing the reconfigurable circuit according to Further exemplary embodiment 9; the method comprising:

said first and second switches are turned ON when a fixed ON defect occurs in one switch from among said second non-volatile resistive switches.

[0053]

(Further exemplary embodiment 15) A method for utilizing the reconfigurable circuit according to Further exemplary embodiment 10; the method comprising:

said first and second switches are turned ON when a fixed ON defect occurs in one switch from among said first non-volatile resistive switches.

Claims

What is claimed is:

1. A reconfigurable circuit comprising:

a first level crossbar switch that has first non-volatile resistive switches;

a second level crossbar switch that has second non-volatile resistive switches; and

a first wire and third non-volatile resistive switches that are used for redundancy, wherein

input wires of said second level crossbar switch are connected to output wires of said first level crossbar switch one-to-one, and

input wires of said first level crossbar switch and output wires of said second level crossbar switch are connected to said first wire through said third non-volatile resistive switches.

2. The reconfigurable circuit according to claim 1, wherein

said input wires of said first level crossbar switch and said output wires of said second level crossbar switch are connected to source terminals of first transistors one-to-one, wherein

gate terminals of said first transistors are connected to a row address decoder, and drain terminals of said first transistors are connected to a row write driver;

said output wires of said first level crossbar switch are connected to source terminals of second transistors one-to-one, wherein

gate terminals of said second transistors are connected to a column address decoder, and drain terminals of said second transistors are connected to a column write driver;

said first wire is connected to a source terminal of a third transistor, wherein

a gate terminal of said third transistor is connected to a redundancy enable signal line, and a drain terminal of said third transistor is connected to said column write driver.

3. The reconfigurable circuit according to claim 1, wherein

more than two of said first wires are provided; and

said first wires are connected to said input wires of said first level crossbar switch

and said output wires of said second level crossbar switch through said third non-volatile resistive switches.

4. The reconfigurable circuit according to claim 3, wherein

said input wires of said first level crossbar switch and said output wires of said second level crossbar switch are connected to source terminals of first transistors one-to-one, wherein

gate terminals of said first transistors are connected to a row address decoder, and drain terminals of said first transistors are connected to a row write driver;

said output wires of said first level crossbar switch are connected to source terminals of second transistors one-to-one, wherein

gate terminals of said second transistors are connected to a column address decoder, and drain terminals of said second transistors are connected to a column write driver;

said first wires are connected to source terminals of third transistors, wherein

gate terminals of said third transistors are connected to redundancy enable signal lines one-to-one, and drain terminals of said third transistors are connected to said column write driver.

5. The reconfigurable circuit according to claim 1, wherein

said first non-volatile resistive switches are diagonally arranged in said first level crossbar switch, and said second non-volatile resistive switches are fully or sparsely arranged in said second level crossbar switch.

6. The reconfigurable circuit according to claim 5, wherein

said input wires of said first level crossbar switch are connected to source terminals of first transistors one-to-one, wherein

gate terminals of said first transistors are connected to a first row address decoder, and drain terminals of said first transistors are connected to a row write driver;

said output wires of said second level crossbar switch are connected to source terminals of second transistors one-to-one, wherein

gate terminals of said second transistors are connected to a second row address

decoder, and drain terminals of said second transistors are connected to said row write driver.

7. The reconfigurable circuit according to claim 1, wherein

said first non-volatile resistive switches are fully or sparsely arranged in said first level crossbar switch, and said second non-volatile resistive switches are diagonally arranged in said second level crossbar switch.

8. The reconfigurable circuit according to claim 7, wherein

said input wires of said first level crossbar switch are connected to source terminals of first transistors one-to-one, wherein

gate terminals of said first transistors are connected to a first row address decoder, and drain terminals of said first transistors are connected to a row write driver;

said output wires of said second level crossbar switch are connected to source terminals of second transistors one-to-one, wherein

gate terminals of said second transistors are connected to a second row address decoder, and drain terminals of said second transistors are connected to said row write driver.

9. A method for utilizing the reconfigurable circuit according to claim 5; the method comprising:

said first non-volatile resistive switches are initially set to be ON, wherein

when a fixed ON defect occurs in one switch from among said second non-volatile resistive switches, said first non-volatile resistive switch, which is arranged on the same wire of defective second non-volatile resistive switch corresponding to said fixed ON defect, is turned OFF.

10. A method for utilizing the reconfigurable circuit according to claim 7; the method comprising:

said second non-volatile resistive switches are initially set to be ON, wherein

when a fixed ON defect occurs in one switch from among said first non-volatile resistive switches, said second non-volatile resistive switch, which is arranged on the

same wire of defective first non-volatile resistive switch corresponding to said fixed ON defect, is turned OFF.

FIG.1A

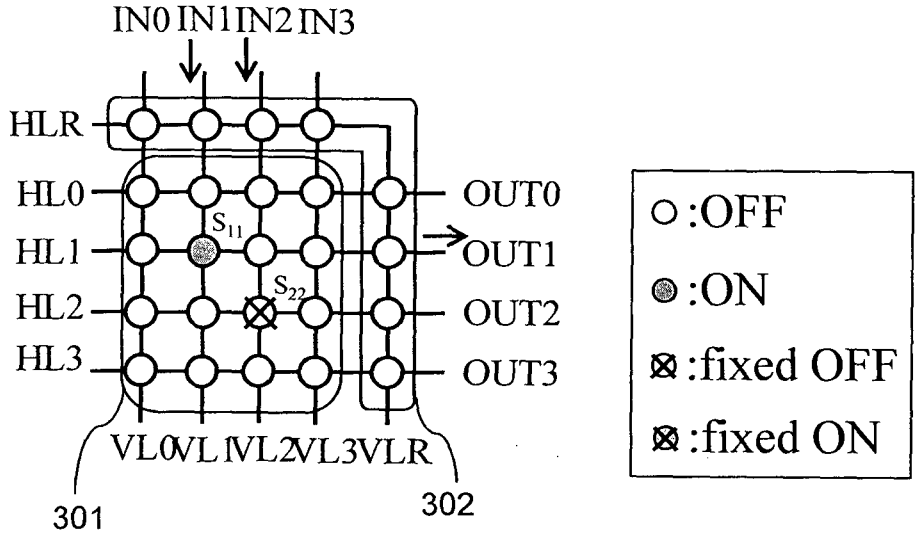

IN0 IN1 IN2 IN3
HLR
HL0
HL1
HL2
HL3
S_{11}
S_{22}
OUT0
OUT1
OUT2
OUT3
VL0 VL1 VL2 VL3 VLR
301
302
○:OFF
◉:ON
⊠:fixed OFF
⊠:fixed ON

FIG.1B

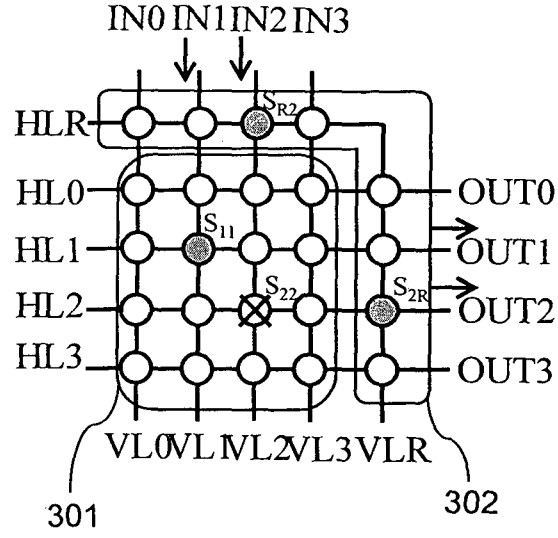

IN0 IN1 IN2 IN3
S_{R2}
HLR
HL0
HL1
HL2
HL3
S_{11}
S_{22}
S_{2R}
OUT0
OUT1
OUT2
OUT3
VL0 VL1 VL2 VL3 VLR
301
302

FIG.2A

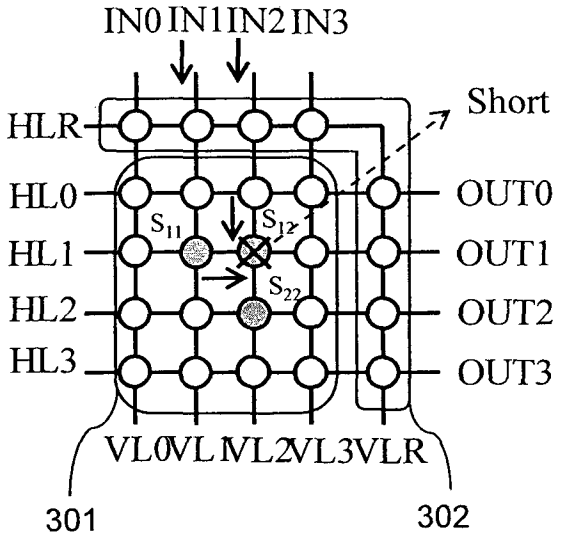

IN0 IN1 IN2 IN3
HLR
HL0
HL1
HL2
HL3
Short
OUT0
OUT1
OUT2
OUT3
S11
S12
S22
VL0 VL1 VL2 VL3 VLR
301
302

FIG.2B

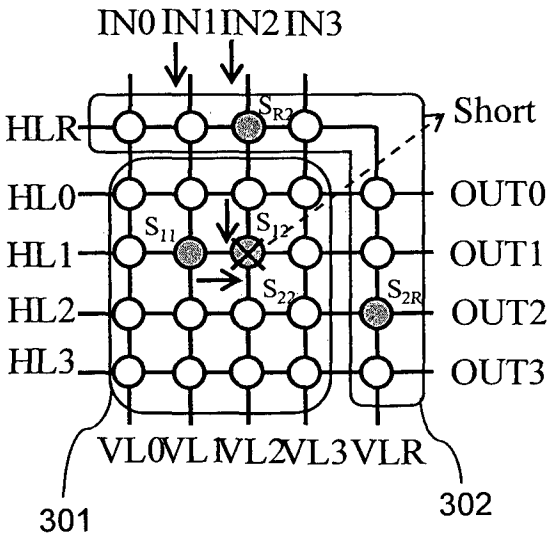

IN0 IN1 IN2 IN3
HLR
HL0
HL1
HL2
HL3
SR2
Short
OUT0
OUT1
OUT2
OUT3
S11
S12
S22
S2R
VL0 VL1 VL2 VL3 VLR
301
302

FIG.3

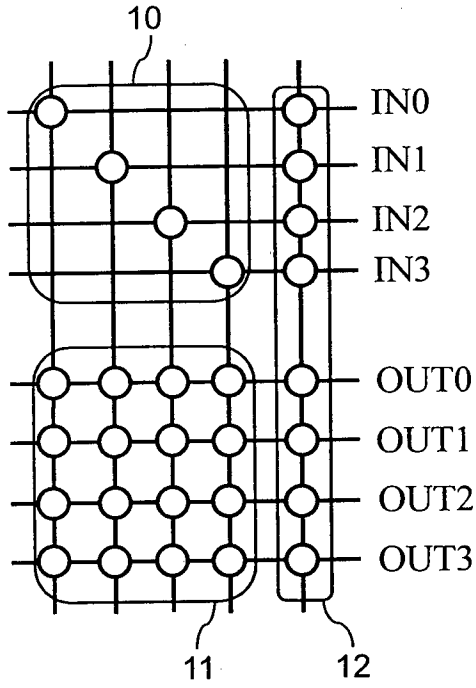


FIG.4A

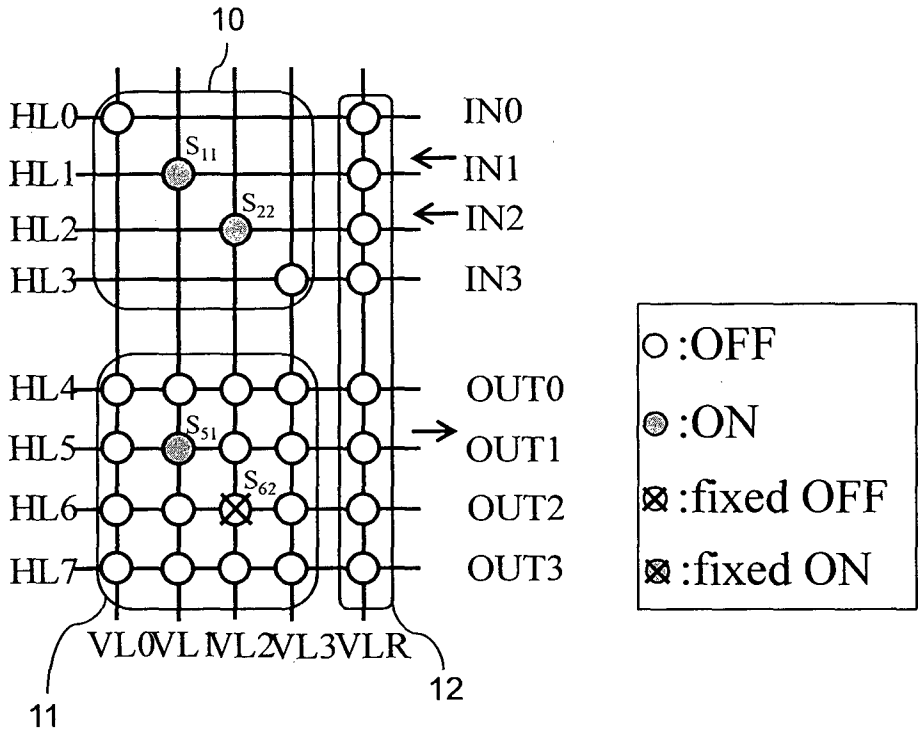

10
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
S11
S22
S51
S62
VL0
VL1
VL2
VL3
VLR
11
12
:OFF
:ON
:fixed OFF
:fixed ON

FIG.4B

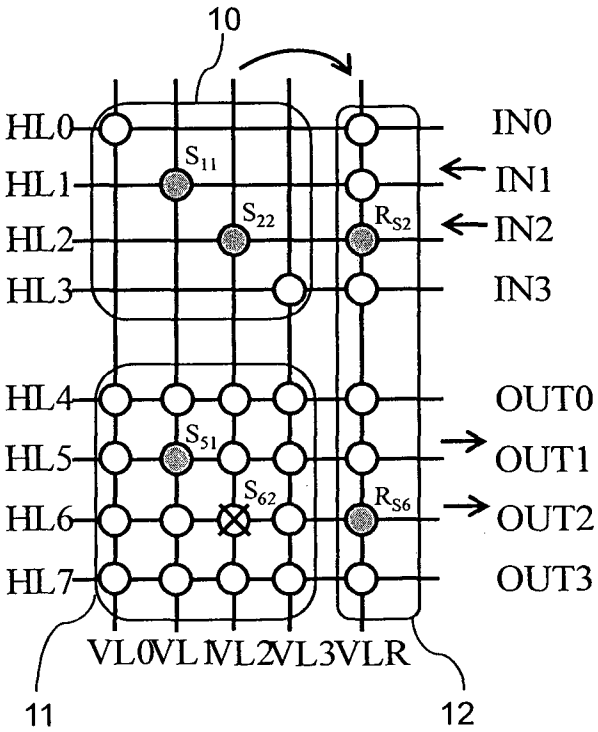

10
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
S11
S22
S51
S62
RS2
RS6
VL0
VL1
VL2
VL3
VLR
11
12

FIG.5A

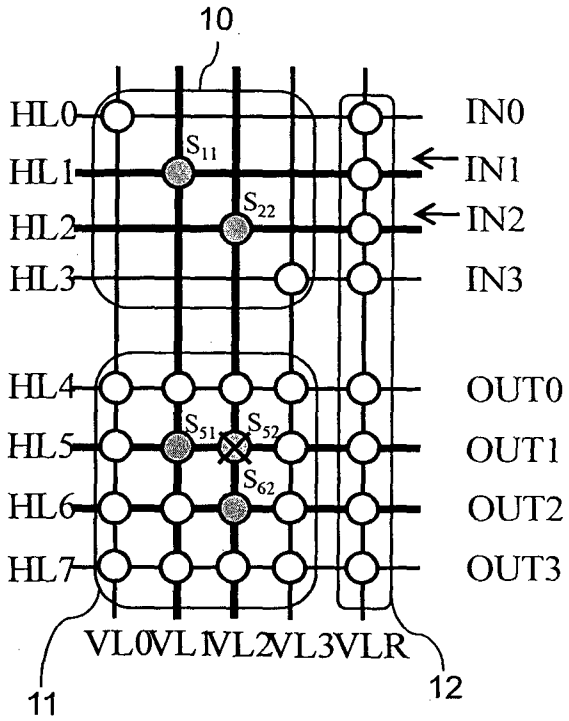
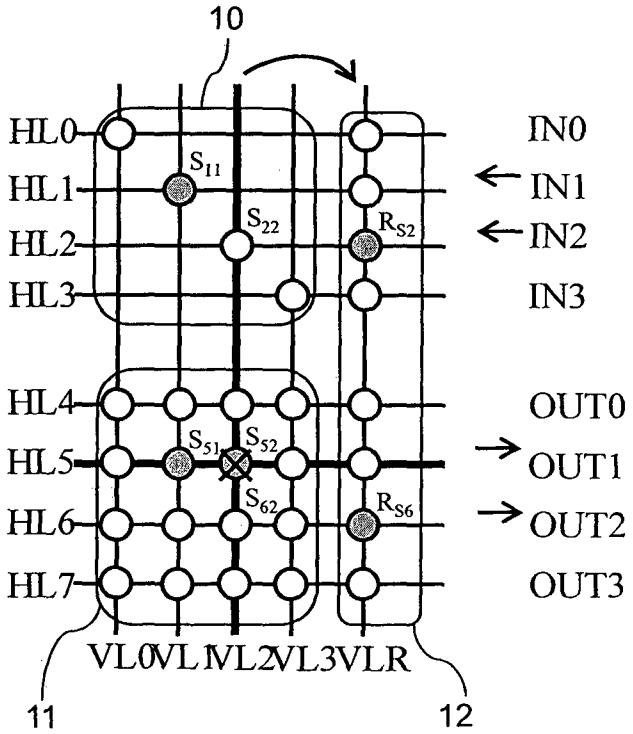

10
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
S_{11}
S_{22}
S_{51}
S_{52}
S_{62}
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
VL0VL1VL2VL3VLR
11
12

FIG.5B


10
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
S_{11}
S_{22}
R_{S2}
S_{51}
S_{52}
S_{62}
R_{S6}
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
VL0VL1VL2VL3VLR
11
12

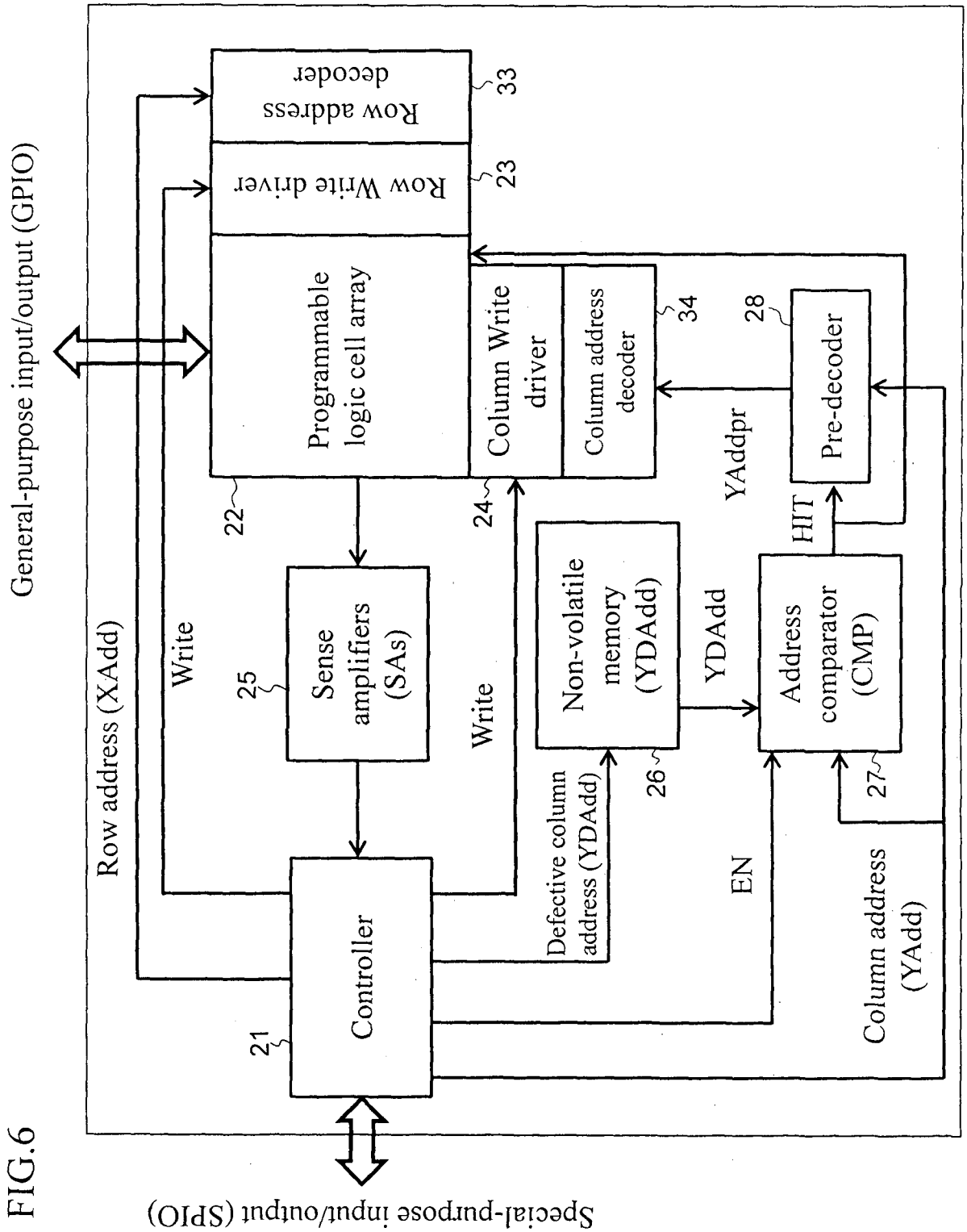

General-purpose input/output (GPIO)
Row address (XAdd)
Write
Row address decoder
33
Row Write driver
23
Programmable logic cell array
22
Column Write driver
24
Column address decoder
34
28
Pre-decoder
YAddpr
HIT
Sense amplifiers (SAs)
25
Write
Non-volatile memory (YDAdd)
26
YDAdd
Address comparator (CMP)
27
Defective column address (YDAdd)
EN
Column address (YAdd)
Controller
21
Special-purpose input/output (SPIO)

FIG.6

FIG.7

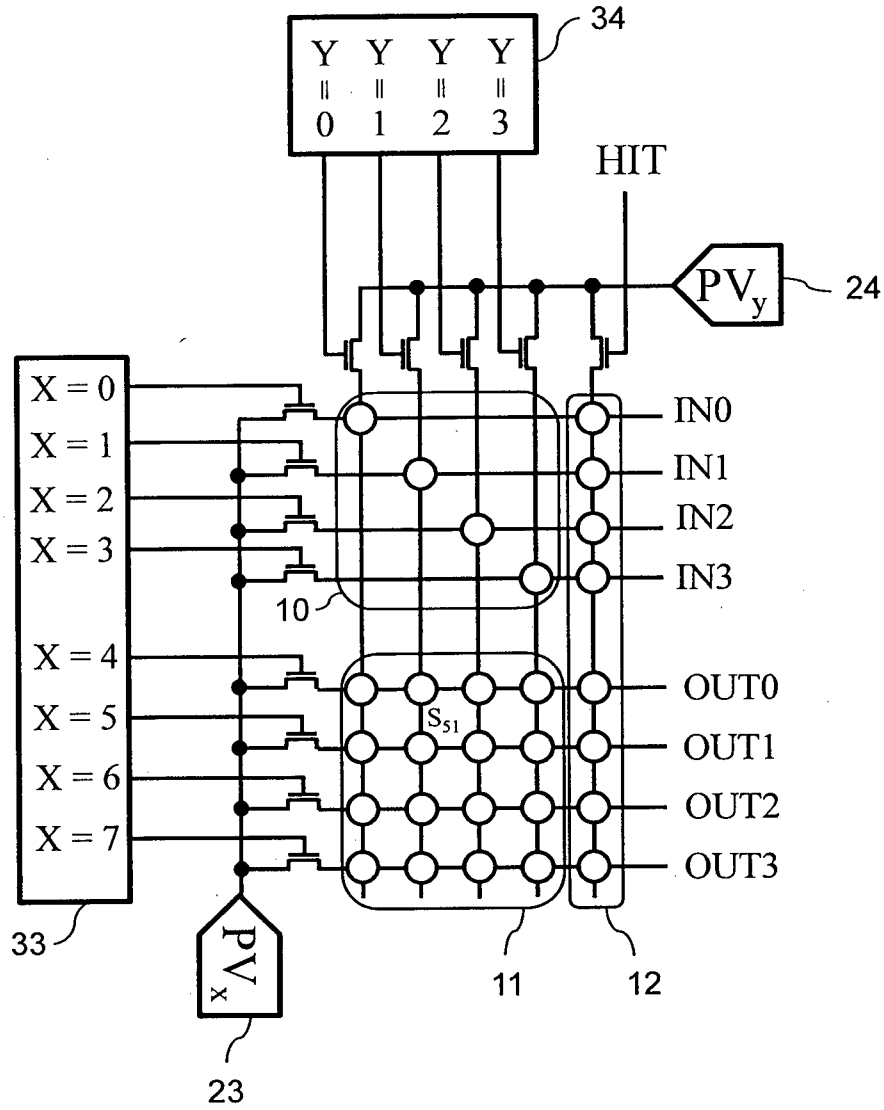

Y Y Y Y
0 1 2 3
34
HIT
PV$_y$
24
X = 0
X = 1
X = 2
X = 3
X = 4
X = 5
X = 6
X = 7
IN0
IN1
IN2
IN3
10
OUT0
OUT1
OUT2
OUT3
S$_{51}$
33
PV$_x$
23
11
12

FIG.8

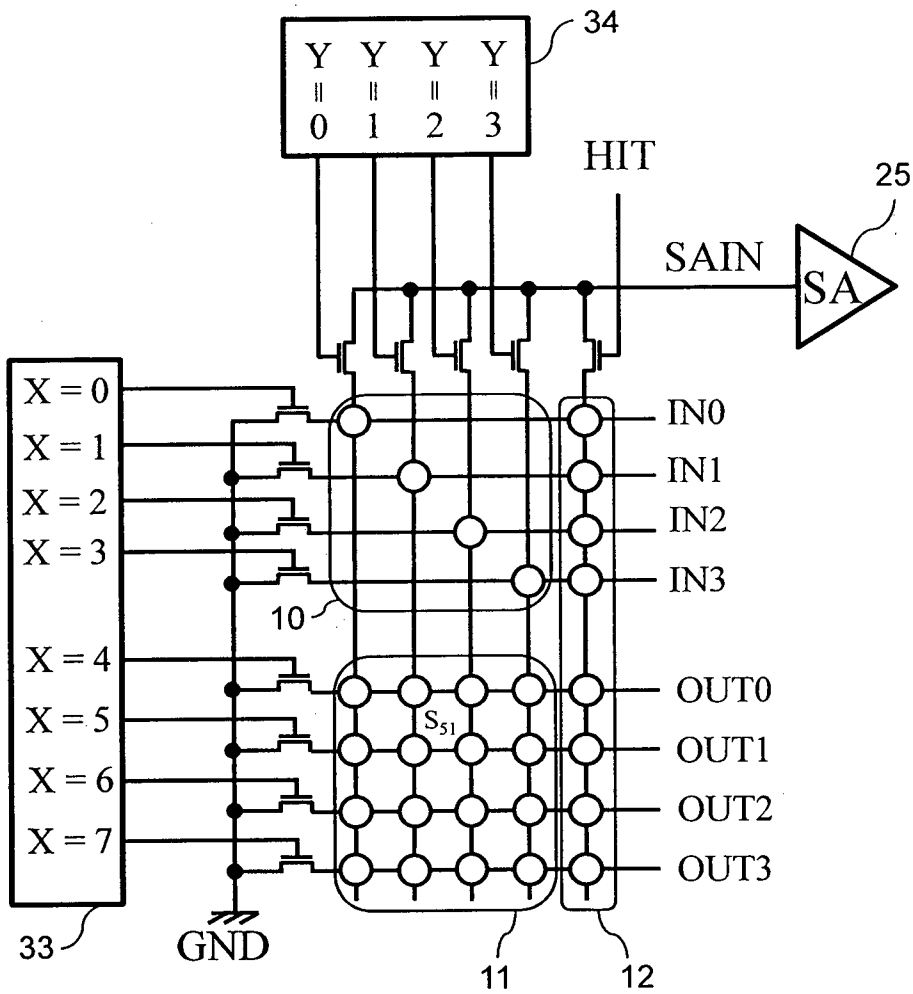

Y Y Y Y
0 1 2 3
34
HIT
25
SAIN
SA
X = 0
X = 1
X = 2
X = 3
X = 4
X = 5
X = 6
X = 7
IN0
IN1
IN2
IN3
10
OUT0
OUT1
OUT2
OUT3
S_{51}
33
GND
11
12

FIG.9

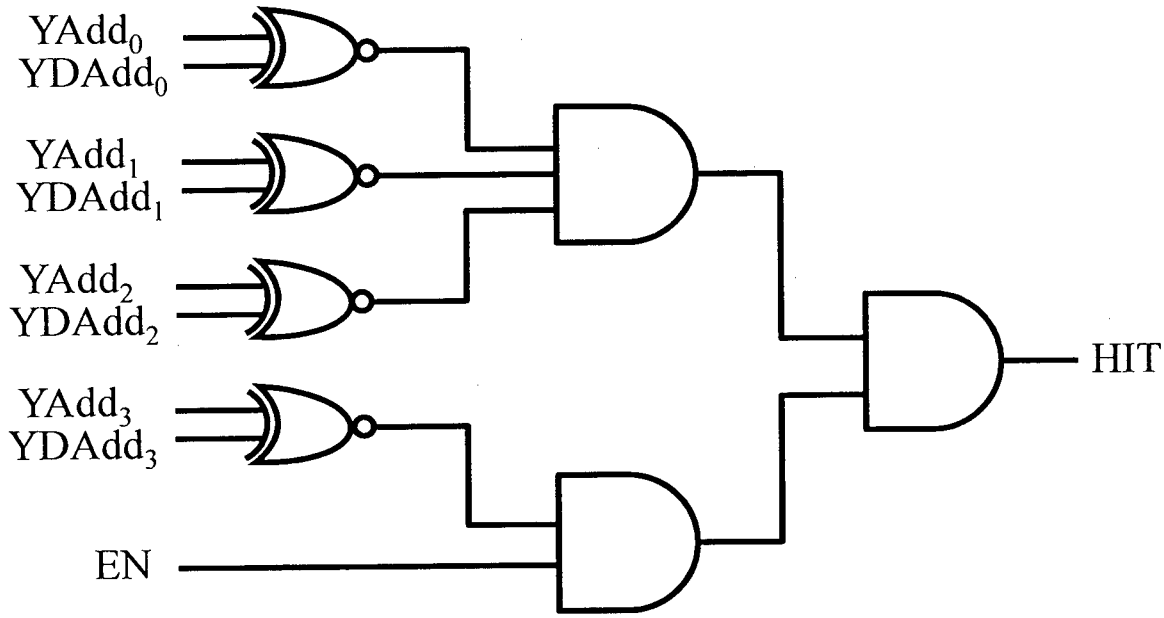
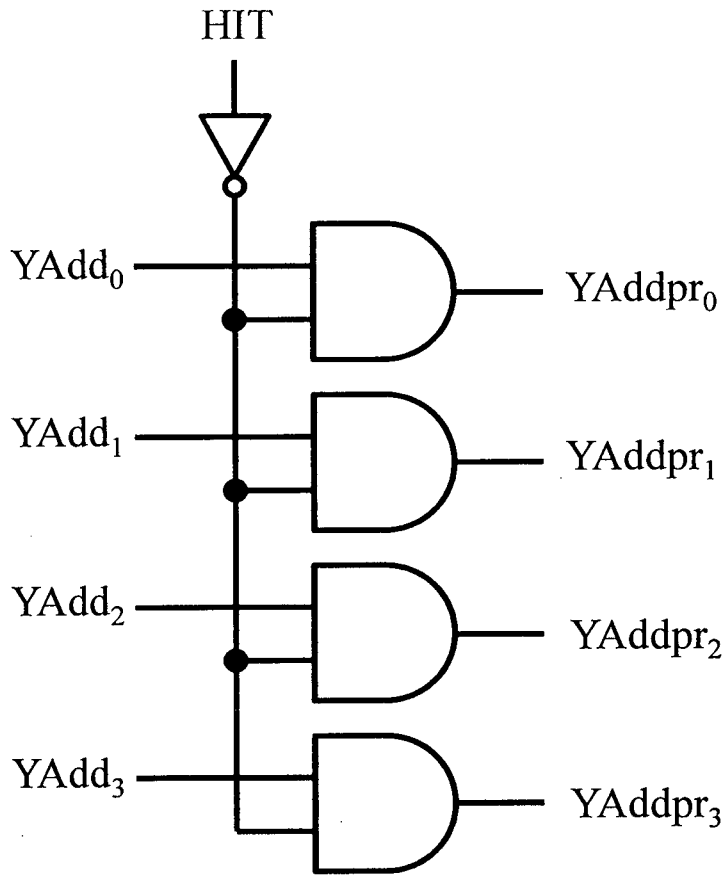


FIG.10


HIT
YAdd0
YAdd1
YAdd2
YAdd3
YAddpr0
YAddpr1
YAddpr2
YAddpr3

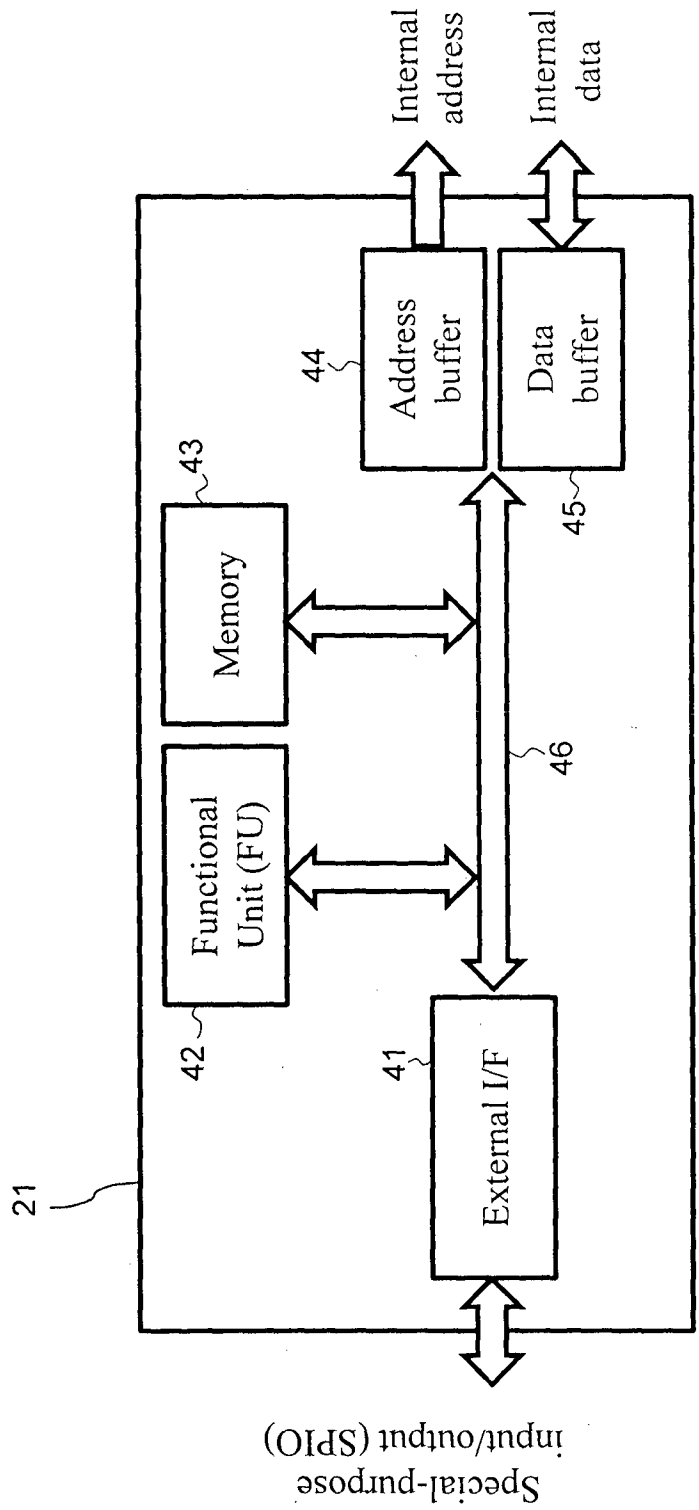

Internal address
Internal data
Address buffer
Data buffer
44
43
45
Memory
Functional Unit (FU)
46
42
41
External I/F
21
Special-purpose input/output (SPIO)

FIG.11

FIG.12

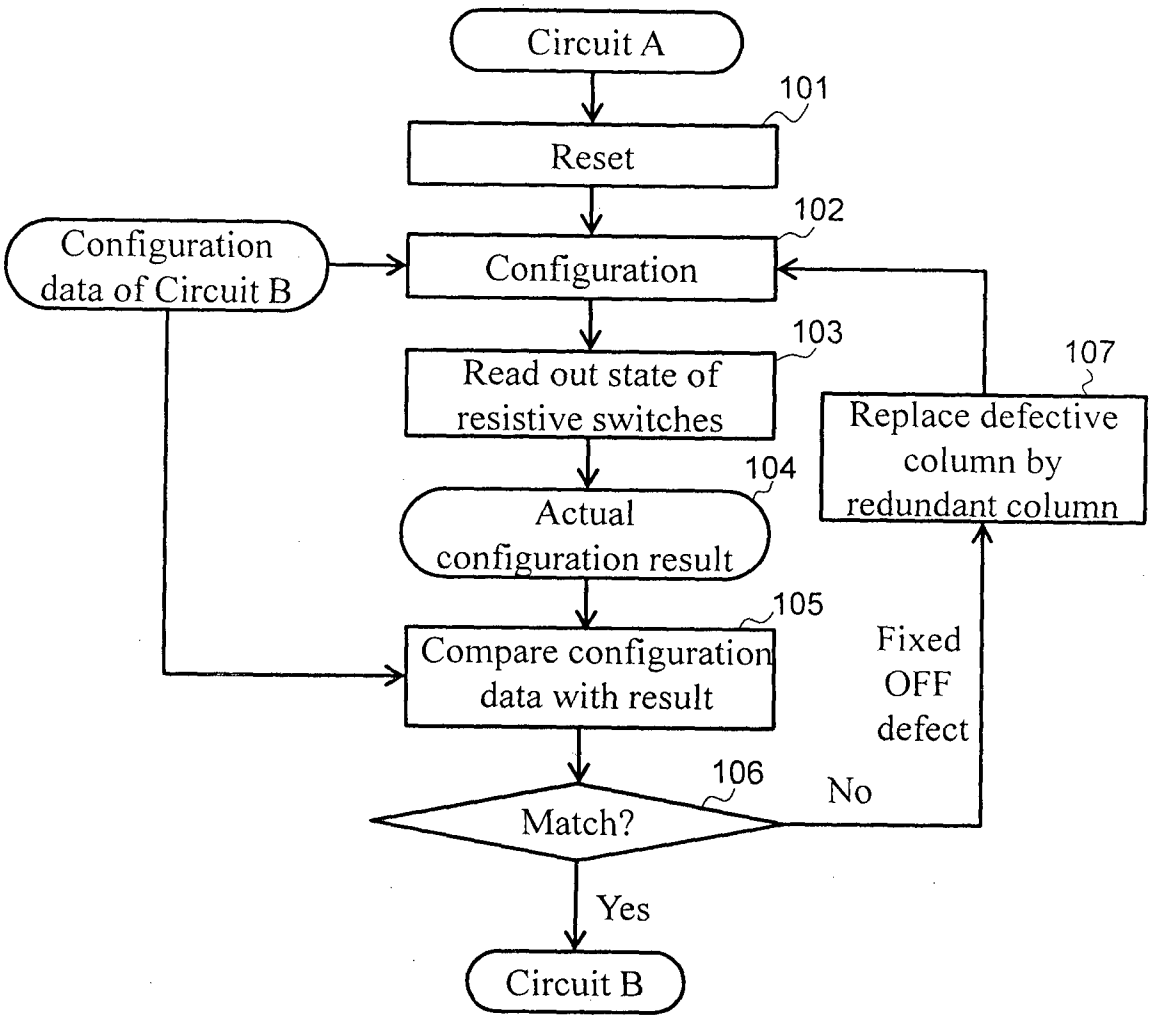

Circuit A
101
Reset
102
Configuration data of Circuit B
Configuration
103
Read out state of resistive switches
107
Replace defective column by redundant column
104
Actual configuration result
105
Compare configuration data with result
Fixed OFF defect
106
Match?
No
Yes
Circuit B

FIG.13

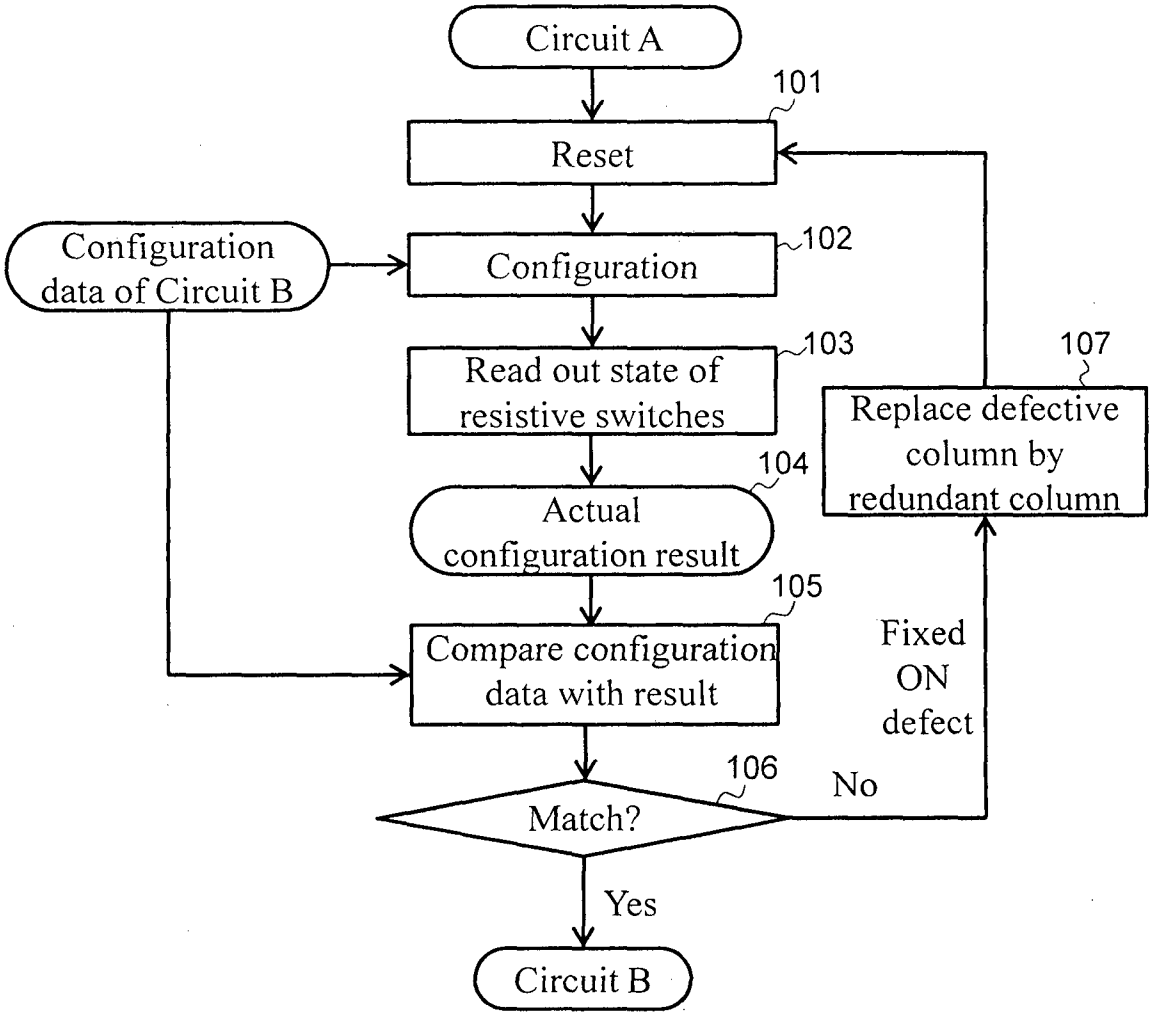
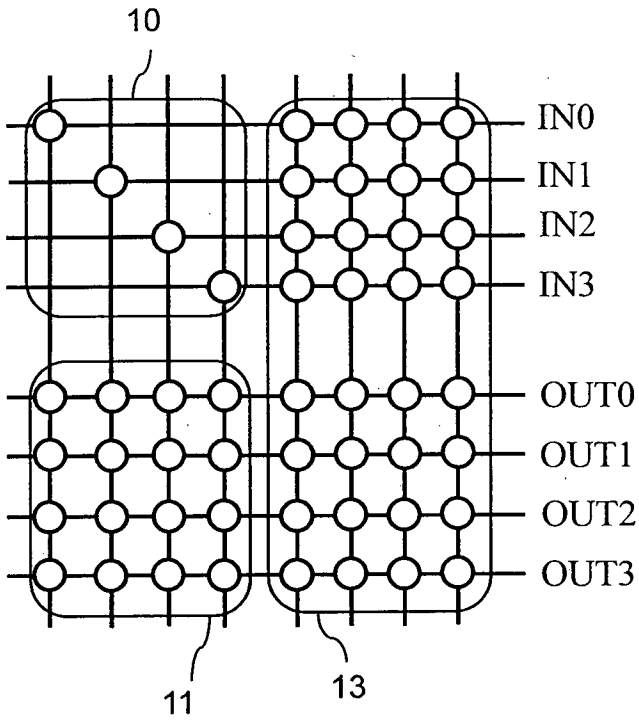

Circuit A
101
Reset
Configuration data of Circuit B
102
Configuration
103
Read out state of resistive switches
107
Replace defective column by redundant column
104
Actual configuration result
105
Compare configuration data with result
Fixed ON defect
106
No
Match?
Yes
Circuit B

FIG.14



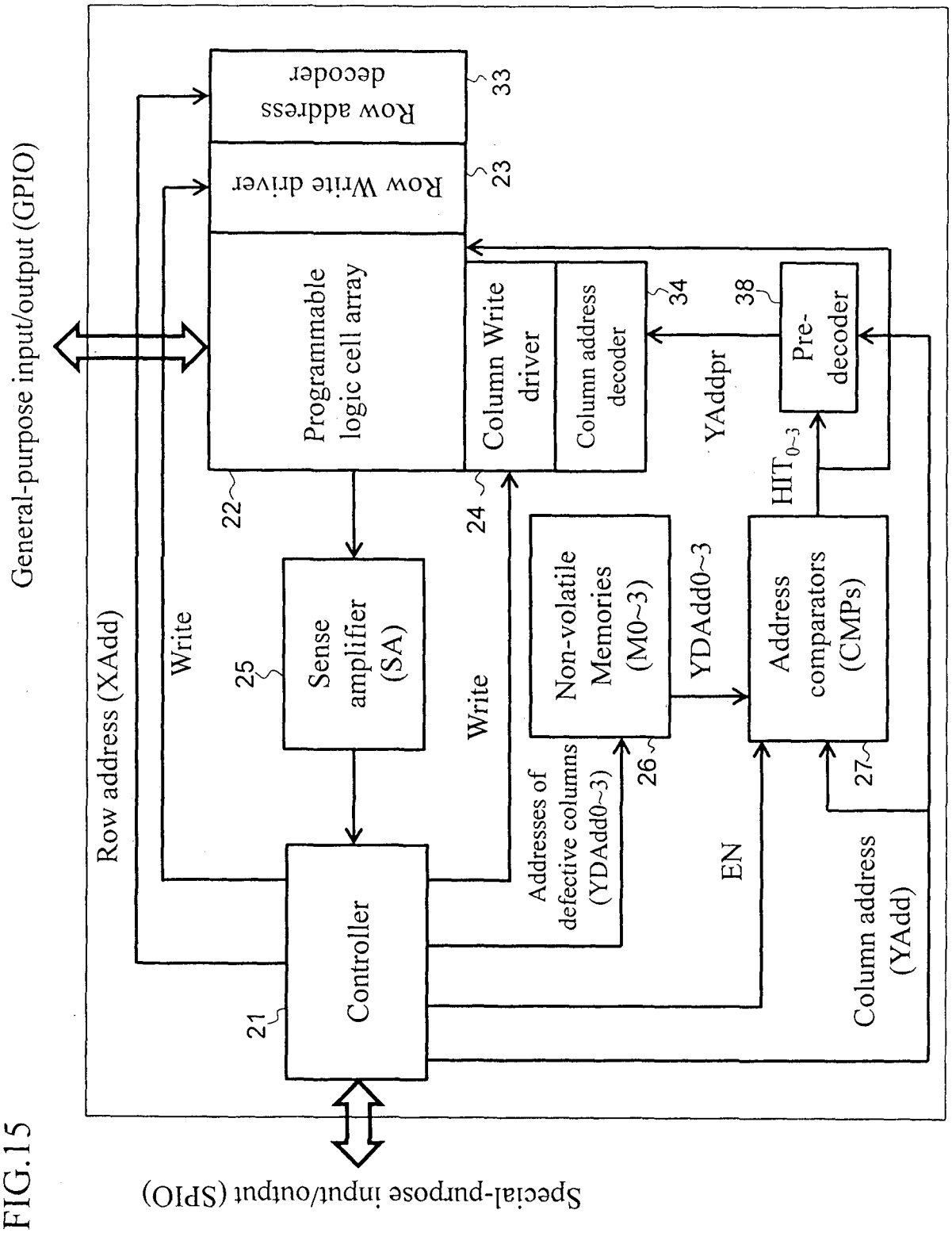

General-purpose input/output (GPIO)
Row address (XAdd)
Write
Row address decoder
33
Row Write driver
23
Programmable logic cell array
22
Column Write driver
24
Column address decoder
34
YAddpr
38
Pre-decoder
$HIT_{0\sim3}$
Sense amplifier (SA)
25
Write
Non-volatile Memories (M0~3)
YDAdd0~3
Address comparators (CMPs)
Addresses of defective columns (YDAdd0~3)
26
EN
27
Column address (YAdd)
Controller
21
Special-purpose input/output (SPIO)

FIG.15

FIG.16

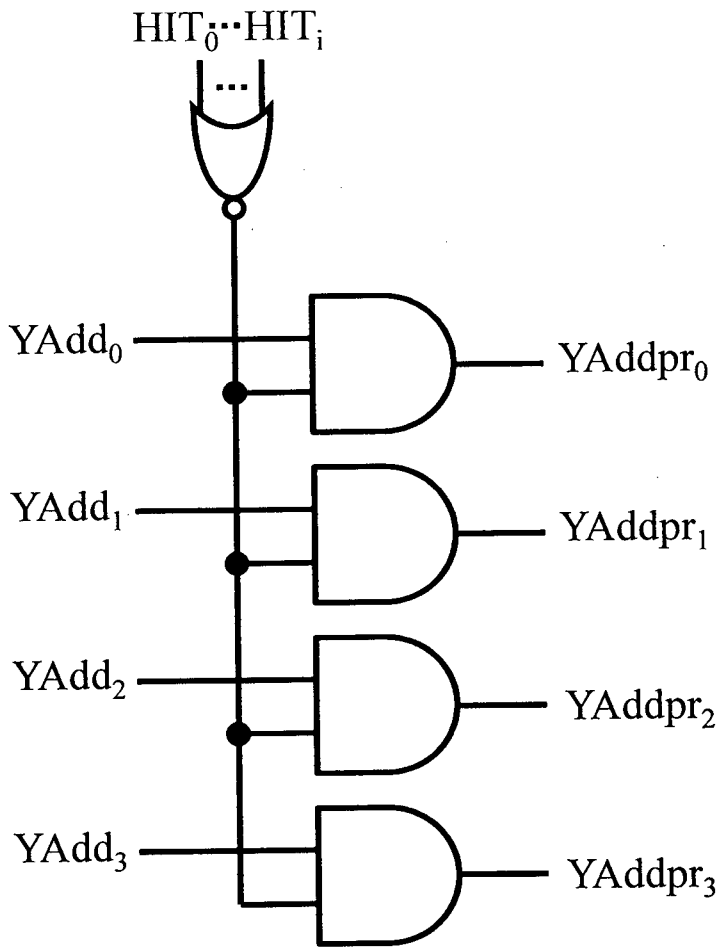

HIT0···HITi
YAdd0
YAddpr0
YAdd1
YAddpr1
YAdd2
YAddpr2
YAdd3
YAddpr3

FIG.17

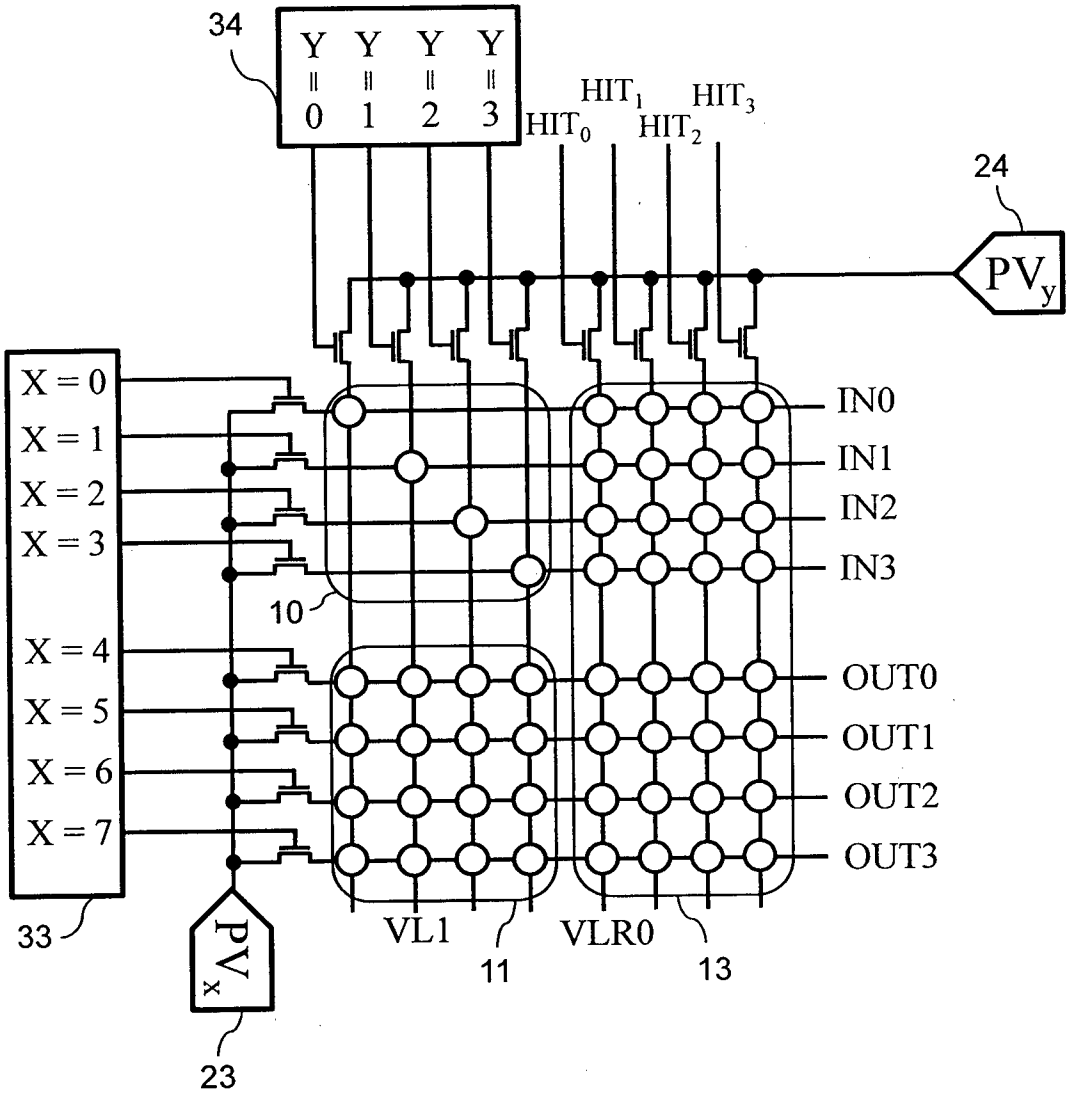
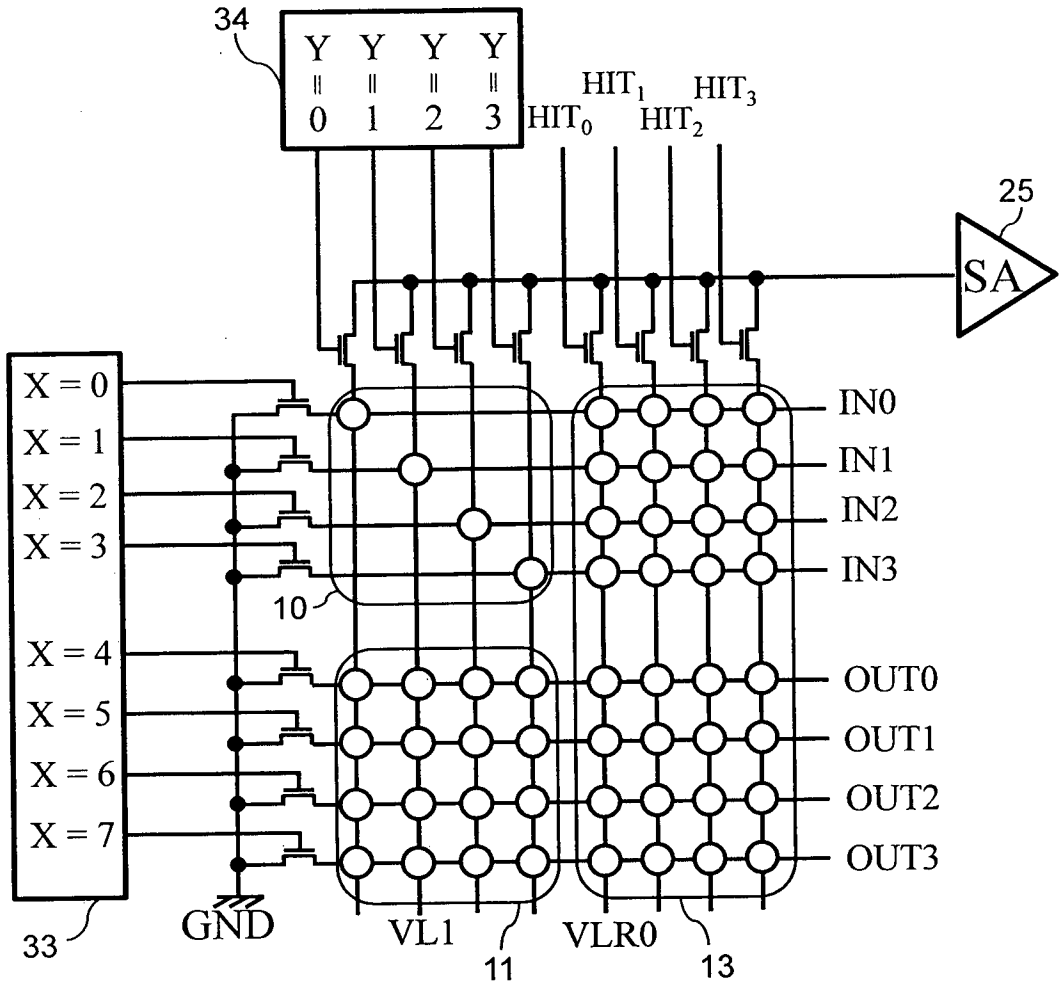

34
Y 0
Y 1
Y 2
Y 3
HIT0
HIT1
HIT2
HIT3
24
PVy
X = 0
X = 1
X = 2
X = 3
X = 4
X = 5
X = 6
X = 7
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
10
33
PVx
23
VL1
11
VLR0
13

FIG.18


34
Y Y Y Y
0 1 2 3
HIT0 HIT1 HIT2 HIT3
25
SA
X = 0
X = 1
X = 2
X = 3
X = 4
X = 5
X = 6
X = 7
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IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
10
33
GND
VL1
11
VLR0
13

FIG.19A

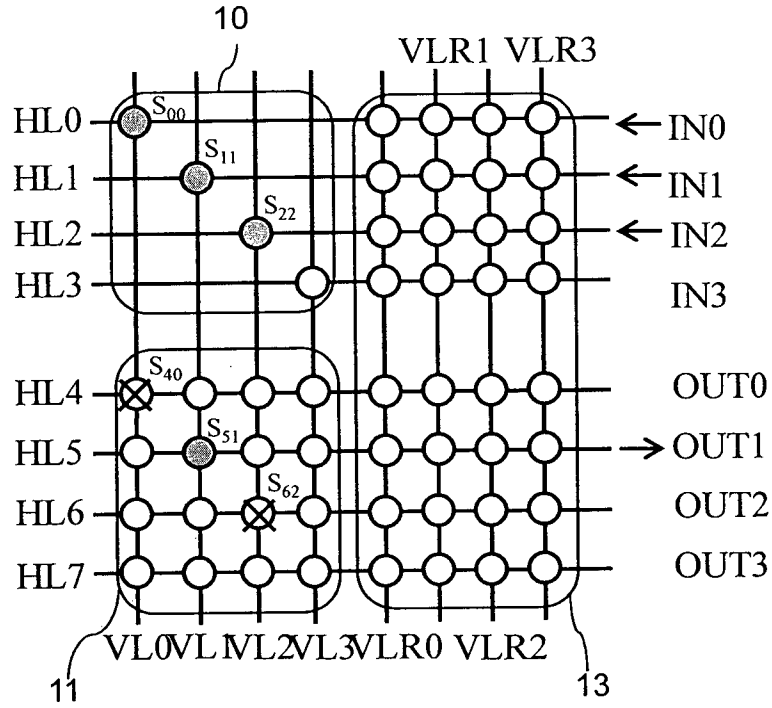


FIG.19B

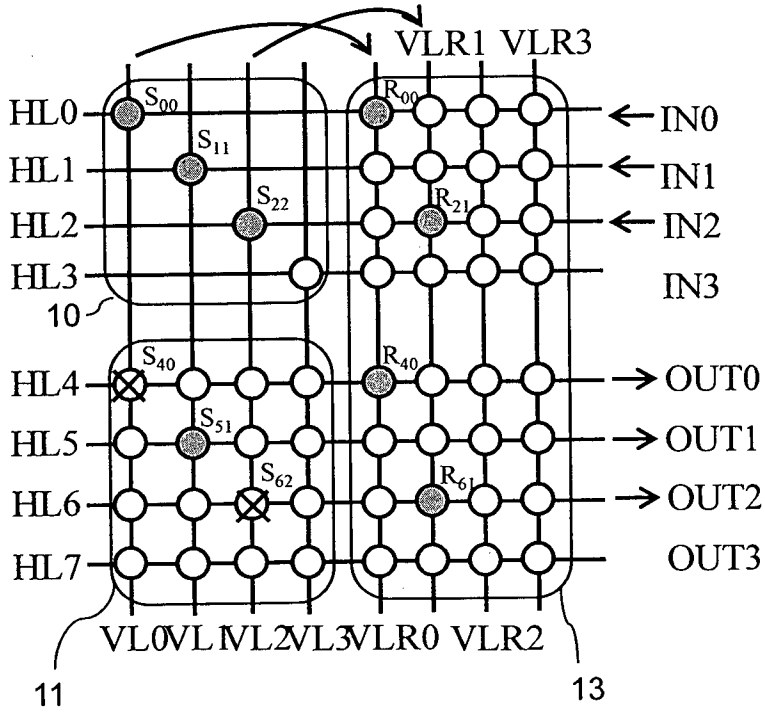


FIG.20A

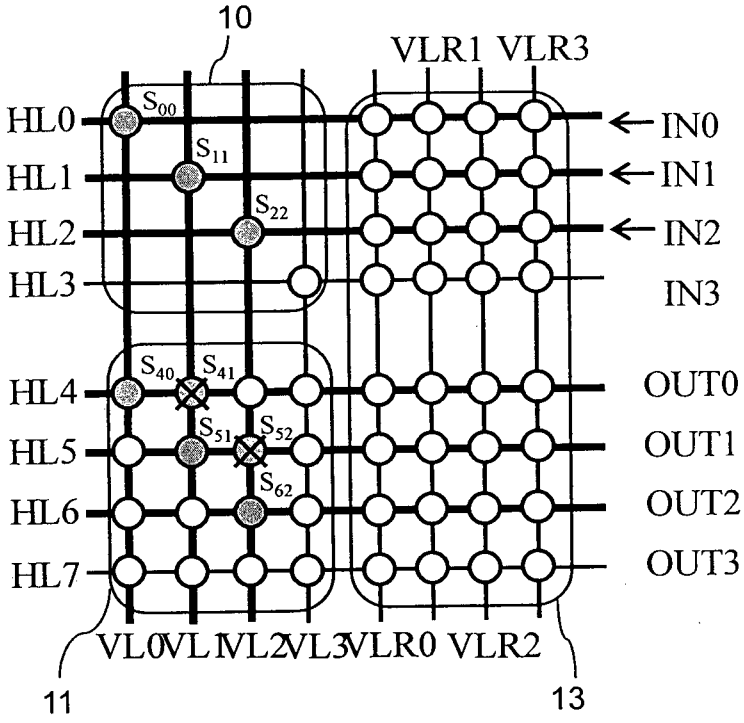


FIG.20B

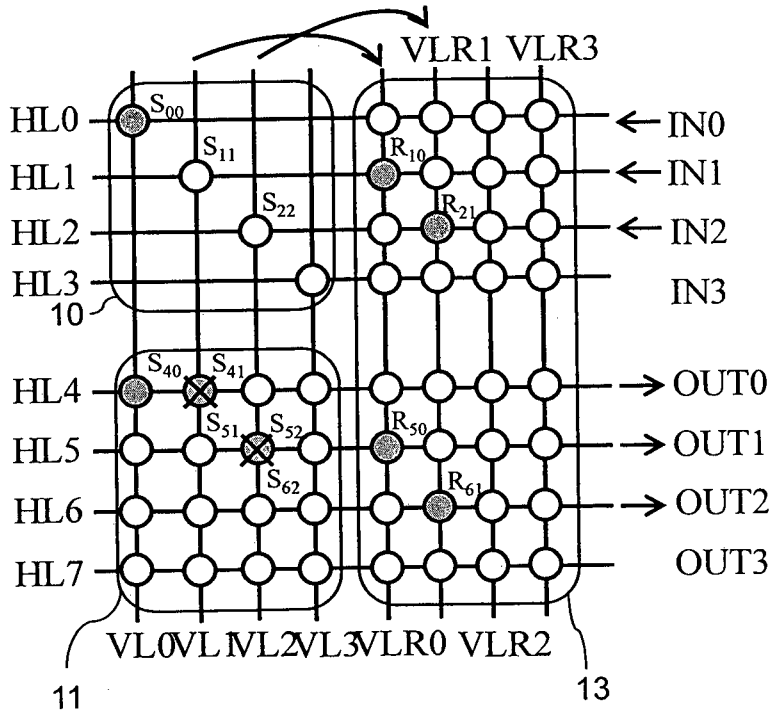


FIG.21A

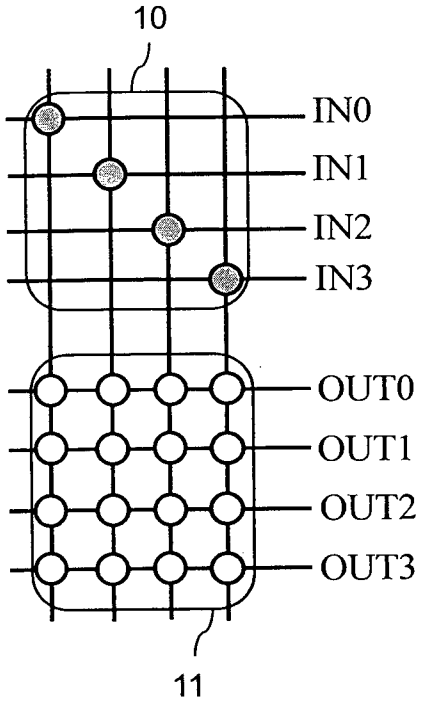


FIG.21B

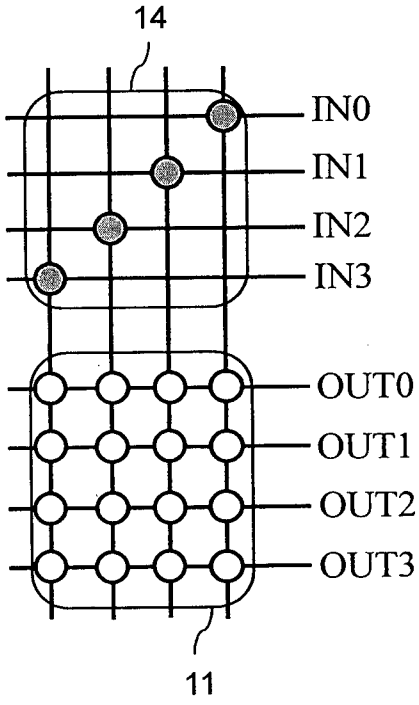


FIG.21C

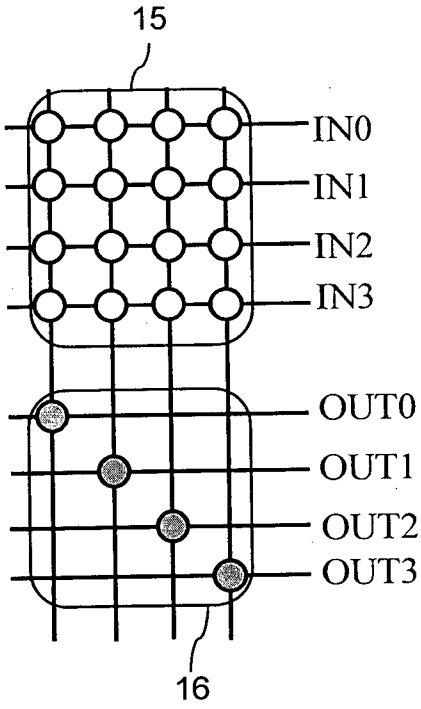
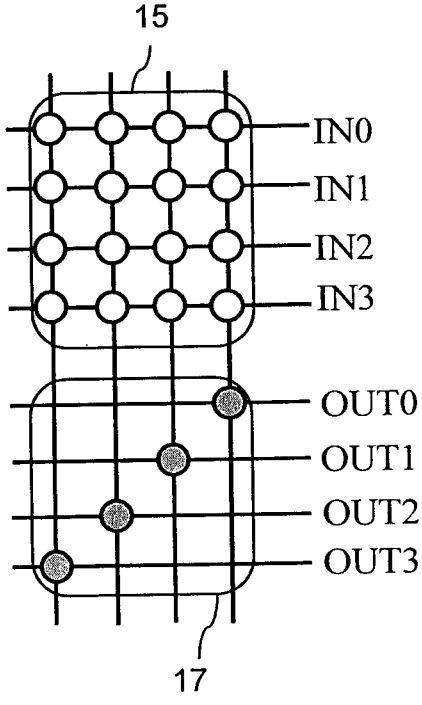
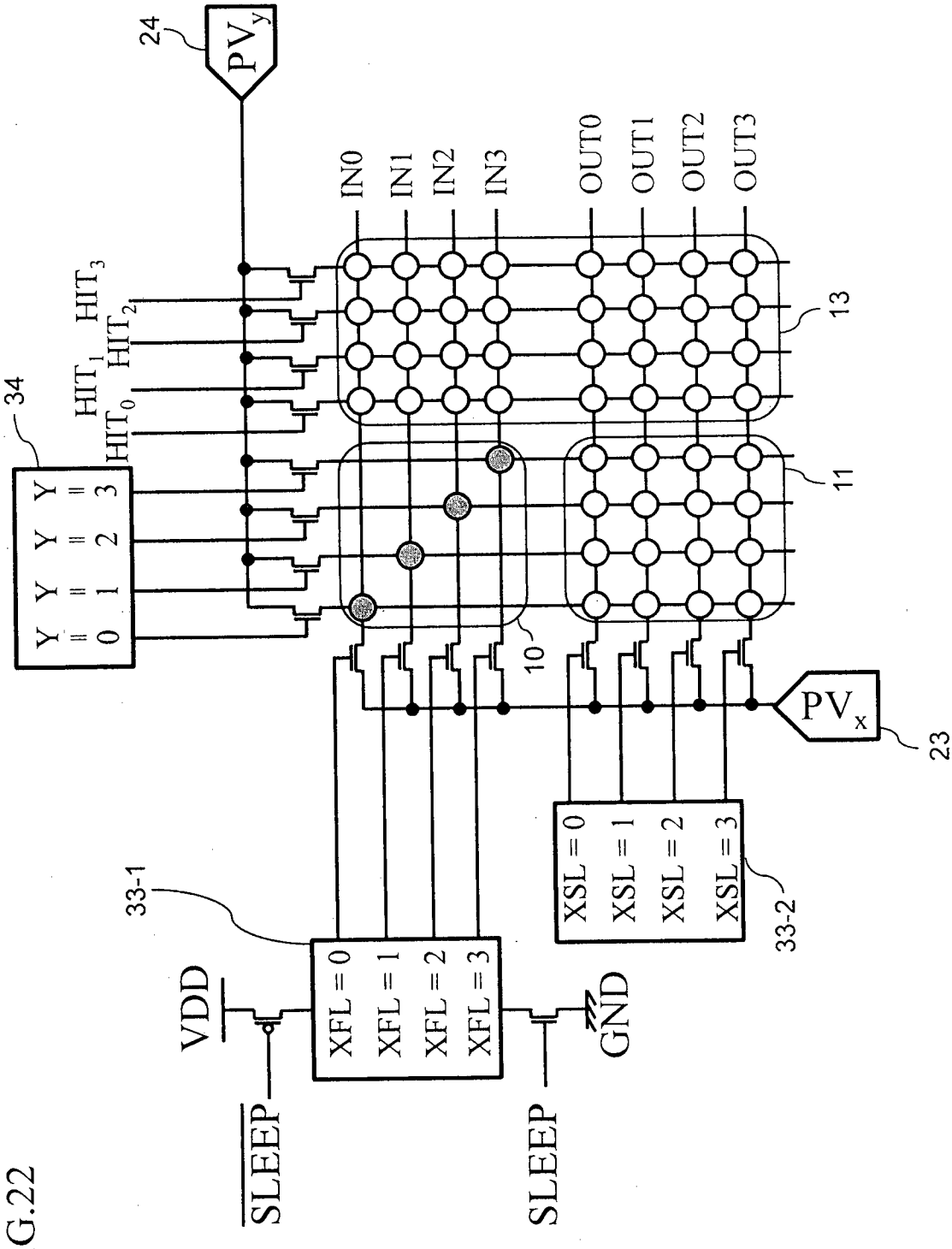


FIG.21D

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IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
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HIT2
HIT1
HIT0
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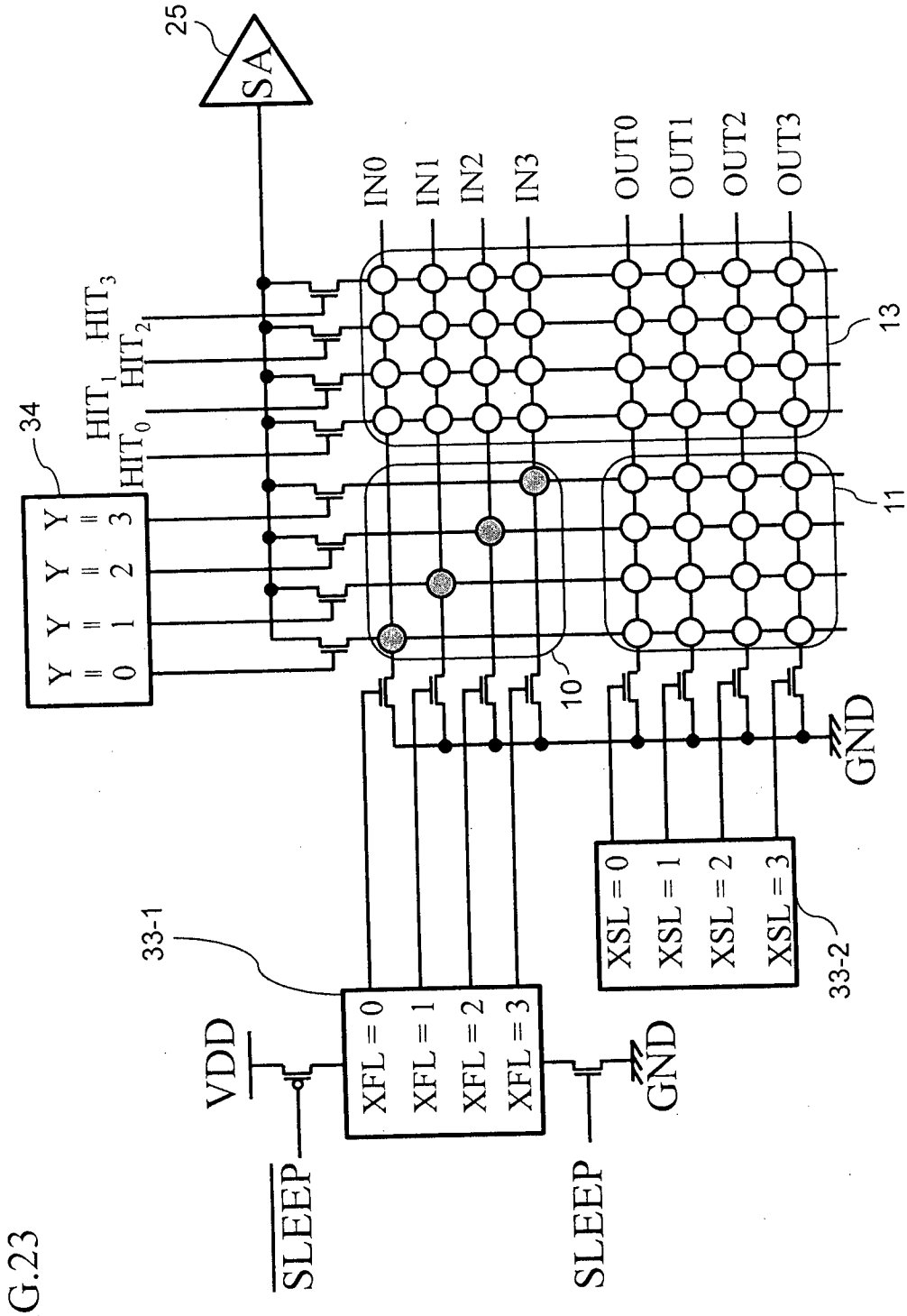
Y Y Y Y
= = = =
0 1 2 3
13
11
10
PVx
23
XSL = 0
XSL = 1
XSL = 2
XSL = 3
33-2
33-1
VDD
XFL = 0
XFL = 1
XFL = 2
XFL = 3
GND
SLEEP
SLEEP

FIG.22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IN2
IN3
OUT0
OUT1
OUT2
OUT3
HIT3
HIT2
HIT1
HIT0
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Y = 1
Y = 2
Y = 3
13
11
10
GND
33-1
XFL = 0
XFL = 1
XFL = 2
XFL = 3
VDD
SLEEP
GND
SLEEP
XSL = 0
XSL = 1
XSL = 2
XSL = 3
33-2

FIG.23

FIG.24A

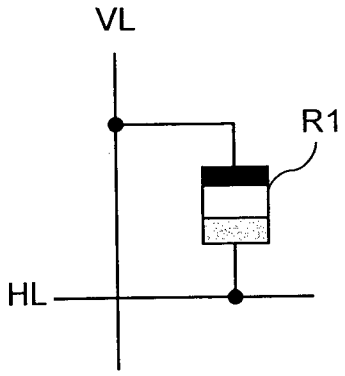
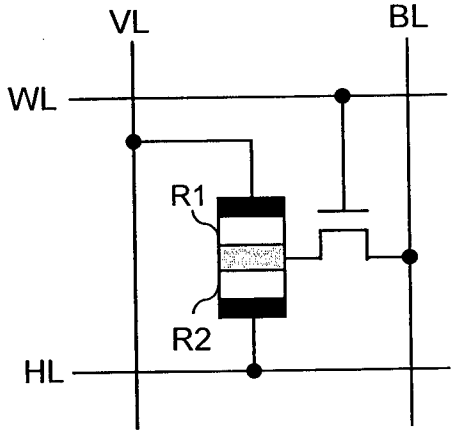


FIG.24B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2015/066125

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H03K19/177(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H03K19/177

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2015
Registered utility model specifications of Japan 1996-2015
Published registered utility model applications of Japan 1994-2015

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

IEEE Xplore

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Tada, M., et al., Polymer Solid-Electrolyte Switch Embedded on CMOS for Nonvolatile Crossbar Switch, IEEE Transactions on Electron Devices, 2011.12, Vol.58, No.12, pages 4398-4406	1-10
A	Jing Huang; Tahoori, M.B.; Lombardi, Fabrizio, On the defect tolerance of nano-scale two-dimensional crossbars, Proceedings of the 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI systems (DFT2004), 2004, pages 96-104	1-10

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search	Date of mailing of the international search report
06.08.2015	18.08.2015

Name and mailing address of the ISA/JP	Authorized officer
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