



- (51) **International Patent Classification:**
H01L 27/108 (2006.01)
- (21) **International Application Number:**
PCT/US2013/074713
- (22) **International Filing Date:**
12 December 2013 (12.12.2013)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
13/715,181 14 December 2012 (14.12.2012) US
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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) **Title:** THREE DIMENSIONAL CAPACITOR

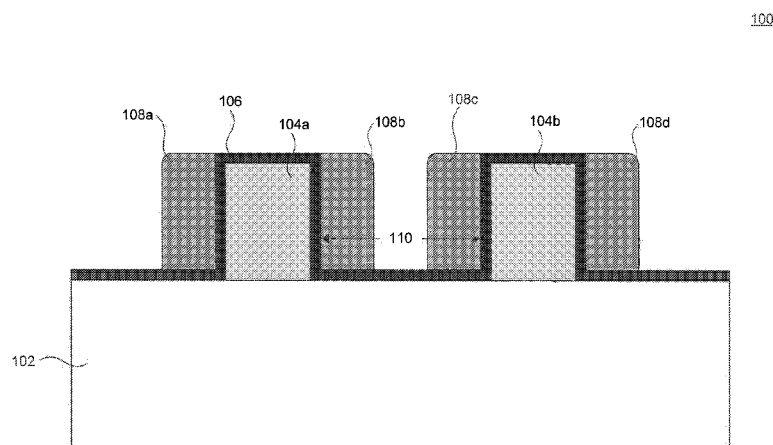


FIG. 1A

(57) **Abstract:** Integrated capacitor structures and methods for fabricating same are provided. In an embodiment, the integrated capacitor structures exploit the capacitance that can be formed in a plane that is perpendicular to that of the substrate, resulting in three-dimensional capacitor structures. This allows for integrated capacitor structures with higher capacitance to be formed over relatively small substrate areas. Embodiments are suitable for use by charge pumps and can be fabricated to have more or less capacitance as desired by the application.

THREE DIMENSIONAL CAPACITOR

BACKGROUND

Field of the Invention

[0001] The present disclosure relates generally to integrated capacitors.

Background Art

[0002] Capacitors are commonly needed in integrated circuits. Although capacitors serve various functions depending on the circuit design and purpose, it is desirable to minimize the substrate area required to form the capacitors. For instance, one common use of capacitors is to enable charge pumps, which are used to produce necessary voltages for other circuits. One way to produce higher voltages using a charge pump includes employing a larger number of capacitors in the charge pump. However, when the capacitors are integrated with the circuits that they support, this solution can require a significant area of the substrate. Another way to produce higher voltages using a charge pump includes decreasing the thickness of the dielectric that separates the charge pump capacitors' plates. This, however, reduces the maximum voltage that can be stored in the resulting capacitors, and may be precluded in some cases by the minimum required breakdown voltage of the capacitors and/or other devices integrated with the capacitors.

BRIEF SUMMARY

[0003] Integrated capacitor structures and methods for fabricating same are provided. In an embodiment, the integrated capacitor structures exploit the capacitance that can be formed in a plane that is perpendicular to that of the substrate, resulting in three-dimensional capacitor structures. This allows for integrated capacitor structures with higher capacitance to be formed over relatively small substrate areas. Embodiments are suitable for use by charge pumps and can be fabricated to have more or less capacitance as desired by the application.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

- [0004] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate the present disclosure and, together with the description, further serve to explain the principles of the disclosure and to enable a person skilled in the pertinent art to make and use the disclosure.
- [0005] FIG. 1A illustrates an example capacitor structure according to an embodiment.
- [0006] FIG. 1B illustrates example capacitances that can result from the example capacitor structure of FIG. 1A.
- [0007] FIG. 2A illustrates another example capacitor structure according to an embodiment.
- [0008] FIG. 2B illustrates example capacitances that can result from the example capacitor structure of FIG. 2A.
- [0009] FIG. 3A illustrates another example capacitor structure according to an embodiment.
- [0010] FIG. 3B illustrates example capacitances that can result from the example capacitor structure of FIG. 3A.
- [0011] FIG. 4 illustrates another example capacitor structure according to an embodiment.
- [0012] FIGs. 5A-5E are cross sectional views illustrating various example steps in a method of fabricating a capacitor structure according to an embodiment.
- [0013] The present disclosure will be described with reference to the accompanying drawings. Generally, the drawing in which an element first appears is typically indicated by the leftmost digit(s) in the corresponding reference number.

DETAILED DESCRIPTION OF EMBODIMENTS

- [0014] Capacitors are commonly needed in integrated circuits. For instance, one common use of capacitors is to enable charge pumps, which are used to produce necessary voltages for integrated circuits. For example, charge pumps are integrated into most non-volatile memory integrated circuits in order to produce the necessary (commonly high) voltages for programming, reading, and erasing the memory cells of the memory. Typically, the charge pump receives a single external power supply voltage (e.g., 1.8 or 3.3 Volts) and produces various higher or lower voltages as needed by the

memory. For example, the charge pump can double the external power supply voltage by charging two capacitors up to the external power supply voltage, disconnecting the two capacitors from the external power supply, and then connecting the two capacitors in series.

[0015] One way to produce higher currents using a charge pump includes employing a larger number of capacitors or capacitors with larger areas. Typically, however, charge pump capacitors are integrated with the same integrated circuits that they support. For example, charge pump capacitors are commonly plate capacitors, formed between a conductor layer (e.g., a polycrystalline silicon layer used for forming gate devices of the integrated circuits) and a conducting substrate, separated by a dielectric (e.g., a gate oxide layer of the gate devices). As such, this solution can require a significant area of the substrate.

[0016] Another way to produce higher currents using a charge pump includes increasing the capacitance of the charge pump capacitors. With increasing the capacitor surface area being undesirable, the capacitance can be increased by decreasing the thickness of the dielectric separating the charge pump capacitors' plates. This, however, reduces the maximum voltage that can be stored in the resulting capacitors, and may be precluded in some cases by the minimum required breakdown voltage of the capacitors and/or other devices integrated with the capacitors. For example, if the charge pump capacitors use as dielectric the gate oxide layer of integrated gate devices, then the decrease of the dielectric thickness can be limited by voltage requirements of the integrated gate devices.

[0017] Accordingly, there is a need for integrated capacitor structures that can provide high capacitance while requiring small substrate area. Embodiments as further described below provide such integrated capacitor structures by exploiting the capacitance that can be formed in a plane that is perpendicular to that of the substrate. As such, embodiments enable what is referred to herein as a three-dimensional capacitor structure. Embodiments are suitable for use by charge pumps and can be fabricated to have more or less capacitance as desired by the application. A fabrication method for fabricating integrated capacitor structures according to embodiments is also provided.

[0018] This specification discloses one or more embodiments that incorporate the features of this invention. The disclosed embodiment(s) merely exemplify the present invention. The scope of the present invention is not limited to the disclosed embodiment(s). The present invention is defined by the claims appended hereto.

[0019] The embodiment(s) described, and references in the specification to "one embodiment," "an embodiment," "an example embodiment," etc., indicate that the embodiment(s) described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is understood that it is within the knowledge of one skilled in the art to effect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0020] FIG. 1A illustrates an example capacitor structure 100 according to an embodiment. Example capacitor structure 100 is provided for the purpose of illustration and is not limiting of embodiments. As shown in FIG. 1A, example capacitor structure 100 includes a substrate 102, a first conductor layer disposed over substrate 102 and patterned to form first and second conductors 104a and 104b, a dielectric 106 disposed over first and second conductors 104a and 104b, and a second conductor layer 108 disposed over dielectric layer 106.

[0021] First and second conductors 104a and 104b are separated by a separation region 110, and each has a top surface, a first sidewall, and a second sidewall. In an embodiment, first and second conductors 104a and 104b comprise doped polycrystalline silicon (poly), but can be of any conducting material as would be apparent to a person of skill in the art based on the teachings herein.

[0022] Dielectric 106 is disposed over first and second conductors 104a and 104b to cover the first sidewall, the second sidewall and optionally the top surface of each of first conductors 104a and 104b. In an embodiment, dielectric 106 also covers the exposed regions of substrate 102, including separation region 110.

[0023] In an embodiment, dielectric 106 includes one or more dielectric layers. For example, dielectric 106 may include a silicon nitride layer sandwiched between two silicon dioxide layers to create a three-layer stack collectively and commonly referred to as "ONO." In an embodiment, the silicon nitride layer is used as a charge trapping layer. Other charge trapping dielectric may also be used including a silicon-rich nitride film, or any film that includes, but is not limited to, silicon, oxygen, and nitrogen in various stoichiometries.

[0024] The second conductor layer includes a portion 108a disposed along the first sidewall of first conductor 104a, a portion 108b disposed along the second sidewall of first conductor 104a, a portion 108c disposed along the first sidewall of second conductor 104b, and a portion 108d disposed along the second sidewall of second conductor 104b. In an embodiment, the second conductor layer comprises poly, but can be of any conducting material as would be apparent to a person of skill in the art based on the teachings herein.

[0025] FIG. 1B illustrates example capacitances that can result from example capacitor structure 100 of FIG. 1A. Specifically, with respect to the structure formed around first conductor 104a, a first capacitance C_1 can be formed between the first sidewall of first conductor 104a and portion 108a of the second conductor layer, and a second capacitance C_2 can be formed between the second sidewall of first conductor 104a and portion 108b of the second conductor layer. Capacitances C_1 and C_2 are formed in a plane that is perpendicular to the plane provided by the top surface of substrate 102.

[0026] The first and second capacitances C_1 and C_2 are electrically coupled by a common end provided by first conductor 104a. In an embodiment, the first and second capacitances C_1 and C_2 are also electrically coupled by their respective other ends (provided by portion 108a and portion 108b respectively), resulting in the first and second capacitances C_1 and C_2 being coupled in parallel. This parallel coupling increases the overall capacitance that can be produced by the structure formed around first conductor 104a. Similar capacitances can be produced using the structure formed around second conductor 104b.

[0027] FIG. 2A illustrates another example capacitor structure 200 according to an embodiment. Example capacitor structure 200 is provided for the purpose of illustration and is not limiting of embodiments. In this example, separation region 110 between first and second conductors 104a and 104b is completely bridged by the second conductor layer. This occurs when a ratio between a height (thickness) of the second conductor layer, when disposed over dielectric 106, and a length of separation region 110 is configured such that portions 108b and 108c form a contiguous portion 108e across separation region 110. In an embodiment, the ratio is configured such that portion 108e includes a pinch off region where portions 108b and 108c meet, as shown in FIG. 2A.

[0028] FIG. 2B illustrates example capacitances that can result from example capacitor structure 200 of FIG. 2A. Like example structure 100 described above, with respect to

the structure formed around first conductor 104a, a first capacitance C_1 can be formed between the first sidewall of first conductor 104a and portion 108a of the second conductor layer, and a second capacitance C_2 can be formed between the second sidewall of first conductor 104a and portion 108e of the second conductor layer. Similar capacitances can be produced using the structure formed around second conductor 104b.

[0029] In addition, a third capacitance C_3 can be formed between portion 108e and substrate 102. As a result, in an embodiment, higher capacitance can be realized using example capacitor structure 200 than using example capacitor structure 100. However, with third capacitance C_3 being a function of the length of separation region 110, the realized capacitance may be sensitive to process variations in the length of separation region 110.

[0030] FIG. 3A illustrates another example capacitor structure 300 according to an embodiment. Example capacitor structure 300 is provided for the purpose of illustration and is not limiting of embodiments. In this example, the second conductor layer is disposed over dielectric 106 and is not etched back, resulting in a single contiguous layer. Specifically, the second conductor layer includes (among other portions) portions 108a, 108b, 108c, 108d, a portion 108f disposed over the top surface of first conductor 104a, a portion 108h disposed over the top surface of second conductor 104b, and a portion 108g disposed between portions 108b and 108c (portion 108g is disposed laterally to first conductor 104a and adjacent to portion 108b).

[0031] FIG. 3B illustrates example capacitances that can result from example capacitor structure 300 of FIG. 3A. Like example structure 100 described above, with respect to the structure formed around first conductor 104a, a first capacitance C_1 can be formed between the first sidewall of first conductor 104a and portion 108a of the second conductor layer, and a second capacitance C_2 can be formed between the second sidewall of first conductor 104a and portion 108b of the second conductor layer. Further, a fourth capacitance C_4 can be formed between portion 108f of the second conductor layer, which is disposed over the top surface of first conductor 104a, and the top surface of first conductor 104a. Similar capacitances can be produced using the structure formed around second conductor 104b.

[0032] The first, second, and fourth capacitances C_1 , C_2 , and C_4 are electrically coupled by a common end provided by first conductor 104a. In an embodiment, the first, second, and fourth capacitances C_1 , C_2 , and C_4 are also electrically coupled by their respective

other ends (provided by portions 108a, 108b, and 108f respectively of the second conductor layer), resulting in the first, second, and fourth capacitances C_1 , C_2 , and C_4 being coupled in parallel. This parallel coupling increases the overall capacitance that can be produced by the structure formed around first conductor 104a.

[0033] In addition, like example capacitor structure 200, a third capacitance C_3 can be formed between the portion of the second conductor layer that sits between first and second conductors 104a and 104b and substrate 102. This portion of the second conductor includes portion 108g and respective regions of portions 108b and 108c that sit above substrate 102.

[0034] In an embodiment, higher capacitance can be realized using example capacitor structure 300 than using example capacitor structures 100 and 200. However, the overall realized capacitance may vary with third capacitance C_3 being a function of the length of separation region 110 (and may thus be sensitive to process variations in the length of separation region 110) and fourth capacitance C_4 being a function of the width of the first and second conductors 104a and 104b (and thus may be sensitive to lithography critical dimension (CD) variations that may cause the width of the disposed conductors to vary from one capacitor structure to another).

[0035] In the embodiments described above in FIGs. 1A, 2A, and 3A, the first conductor layer is disposed directly over substrate 102 and then patterned to form first and second conductors 104a and 104b. Dielectric 106 is then disposed over first and second conductors 104a and 104b to cover the top surface, the first sidewall, and the second sidewall of each of first conductors 104a and 104b and the exposed regions of substrate 102, including separation region 110. In other embodiments, as illustrated in FIG. 4, for example, an isolation layer 402 is disposed over substrate 102 before disposing the first conductor layer. The first conductor layer is then disposed over isolation layer 402 and patterned to form first and second conductors 104a and 104b over isolation layer 402. Isolation layer 402 can be a dielectric (e.g., oxide) or an insulating substrate, for example, and serves to increase the voltage potential that can be applied to the resulting capacitor structure without causing it damage.

[0036] FIGs. 5A-5E are cross sectional views illustrating various example steps in a method of fabricating a capacitor structure according to an embodiment. These example steps are provided for the purpose of illustration and are not limiting of embodiments.

The method illustrated in FIGs. 5A-5E can be used to fabricate the example capacitor structures described in FIGs. 1A, 2A, 3A, and 4 above.

[0037] Description of the fabrication method begins with reference to FIG. 5A, which shows a first conductor layer 504 disposed over a substrate 502. Substrate 502 can be a silicon substrate, and first conductor layer 504 can be a polycrystalline silicon (poly), for example. First conductor layer 504 can be disposed over substrate 502 by a standard deposition process. In another embodiment, an isolation layer (e.g., dielectric or insulating substrate) (not shown in FIG. 5A) is disposed over substrate 502, and first conductor layer 504 is disposed over the isolation layer. This increases the voltage potential that can be applied to the resulting capacitor structure without causing it damage.

[0038] Then, as shown in FIG. 5B, first conductor layer 504 is patterned to form first and second conductors 510, spaced by a separation region 512. Each of the first and second conductors 510 has a top surface 514, a first sidewall 516, and a second sidewall 518. In an embodiment, patterning first conductor layer 504 to form first and second conductors 510 includes creating a photo resist mask (e.g., using standard lithography steps) over substrate 502 and etching (e.g., dry etching) first conductor layer 504 according to the created photo resist mask. The photo resist mask is then stripped and a wet clean is performed.

[0039] Subsequently, as illustrated in FIG. 5C, a dielectric 506 is disposed over first and second conductors 510 and the exposed regions of substrate 502. In an embodiment, the dielectric includes one or more dielectric layers. For example, the dielectric may include a silicon nitride layer sandwiched between two silicon dioxide layers to create a three-layer stack collectively and commonly referred to as "ONO." In an embodiment, the silicon nitride layer is used as a charge trapping layer. Other charge trapping dielectric may also be used including a silicon-rich nitride film, or any film that includes, but is not limited to, silicon, oxygen, and nitrogen in various stoichiometries.

[0040] In an embodiment, dielectric 506 includes a bottom oxide layer, a nitride layer, and a top oxide layer. To form the dielectric, bottom oxide layer is formed (e.g., grown or deposited) over the first and second conductors 510 and the exposed regions of substrate 502. Then, the nitride layer is formed (e.g., deposited) over the bottom oxide layer, and the top oxide layer is formed (e.g., grown or deposited) over the nitride layer.

[0041] Then, as illustrated in FIG. 5D, a second conductor layer 508 is disposed over dielectric 506. Second conductor layer 508 can be a poly layer, for example. Second conductor layer 508 can be disposed over dielectric layer 506 by a standard deposition process, for example. In an embodiment, a height 520 of second conductor layer 508 is greater than a half length of separation region 512 between first and second conductors 510. As such, the portion of second conductor layer 508 that is disposed over separation region 512 bridges separation region 512 between first and second conductors 510 as shown in FIG. 2A, for example.

[0042] In an embodiment, the fabrication method terminates with the step illustrated in FIG. 5D, resulting in a capacitor structure similar to example capacitor structure 300 described above in FIGs. 3A and 3B. As described above, such capacitor structure has the added capacitance that results between second conductor layer 508 and top surface 514 of first or second conductors 510. For the same reason, however, the overall capacitance of the structure may vary due to lithography critical dimension (CD) variations that may cause the width of the disposed first and second conductor 510 to vary from one capacitor structure to another.

[0043] In another embodiment, the fabrication method then proceeds as illustrated in FIG. 5E, where second conductor layer 508 is etched (e.g., anisotropically dry etched). In an embodiment, second conductor layer 508 is etched over top surfaces 514 of first and second conductors 510 until dielectric 506 is exposed. The etching also exposes dielectric 506 in a portion 522 of separation region 512 and results in the formation of first and second spacers 524 and 526 (of second conductor layer 508) along first sidewalls 516 of first and second conductors 510 respectively. The resulting capacitor structure is similar to example capacitor structure 100 described above in FIGs. 1A and 1B. As described above, this structure is less sensitive to lithography CD variations, which makes it suitable for applications requiring substantially constant capacitance, such as charge pumps, for example.

[0044] Embodiments have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0045] The foregoing description of the specific embodiments will so fully reveal the general nature of the disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0046] The breadth and scope of embodiments of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A capacitor structure, comprising:
 - a substrate;
 - a first conductor disposed over the substrate, the first conductor having a top surface, a first sidewall, and a second sidewall;
 - a dielectric layer disposed over the first conductor, the dielectric layer covering the first sidewall and the second sidewall of the first conductor; and
 - a second conductor disposed over the dielectric layer, the second conductor having a first portion disposed along the first sidewall of the first conductor and a second portion disposed along the second sidewall of the first conductor.
2. The capacitor structure of claim 1, wherein a first capacitance is formed between the first sidewall of the first conductor and the first portion of the second conductor, and a second capacitance is formed between the second sidewall of the first conductor and the second portion of the second conductor.
3. The capacitor structure of claim 1, wherein the dielectric layer further covers the top surface of the first conductor, and wherein the second conductor comprises a third portion disposed over the top surface of the first conductor.
4. The capacitor structure of claim 3, wherein a capacitance is formed between the top surface of the first conductor and the third portion of the second conductor.

5. The capacitor structure of claim 3, wherein the second conductor further comprises a fourth portion disposed laterally to the first conductor and adjacent to the first portion.

6. The capacitor structure of claim 5, wherein a capacitance is formed between the substrate and the fourth portion of the second conductor.

7. The capacitor structure of claim 1, wherein the dielectric layer comprises an oxide-nitride-oxide (ONO) layer.

8. The capacitor structure of claim 1, wherein the first conductor is disposed directly over the substrate.

9. The capacitor structure of claim 1, further comprising:
an isolation layer disposed over the substrate, wherein the first conductor is disposed over the isolation layer.

10. The capacitor structure of claim 1, wherein at least one of the first conductor and the second conductor comprises a polycrystalline silicon.

11. A capacitor structure, comprising:
a substrate;
a first conductor layer disposed over the substrate, the first conductor layer patterned to form first and second conductors spaced by a separation region, the first and second conductors each having a top surface, a first sidewall, and a second sidewall;

a dielectric layer disposed over the first and second sidewalls of each of the first and second conductors; and

a second conductor layer disposed over the dielectric layer, the second conductor layer having a first portion disposed along the first sidewall of the first conductor, a second portion disposed along the first sidewall of the second conductor, and a third portion disposed in the separation region between the second sidewall of the first conductor and the second sidewall of the second conductor.

12. The capacitor structure of claim 11, wherein a height of the second conductor layer is greater than a half length of the separation region.

13. The capacitor structure of claim 11, wherein the third portion of the second conductor layer bridges the separation region between the first and second conductors.

14. The capacitor structure of claim 11, wherein the third portion of the second conductor layer includes a pinch off region.

15. The capacitor structure of claim 11, wherein the dielectric layer is further disposed over the top surfaces of the first and second conductors, and wherein the second conductor layer further comprises a fourth portion disposed over the top surfaces of the first and second conductors.

16. A method of fabricating a capacitor structure, comprising:
disposing a first conductor layer over a substrate;

patterning the first conductor layer to form first and second conductors spaced by a separation region, the first and second conductors each having a top surface, a first sidewall, and a second sidewall;

disposing a dielectric layer over the first and second conductors and the substrate; and
disposing a second conductor layer over the dielectric layer.

17. The method of claim 16, further comprising:

etching the second conductor layer along the top surfaces of the first and second conductors.

18. The method of claim 17, further comprising:

etching the second conductor layer in a portion of the separation region to form a first spacer of the second conductor layer along the first sidewall of the first conductor and a second spacer of the second conductor layer along the first sidewall of the second conductor.

19. The method of claim 16, further comprising:

disposing an isolation layer over the substrate, wherein the first conductor layer is disposed over the isolation layer.

20. The method of claim 16, wherein disposing the dielectric layer comprises:

disposing a first oxide layer over the first conductor layer;
disposing a nitride layer over the first oxide layer; and
disposing a second oxide layer over the nitride layer.

100

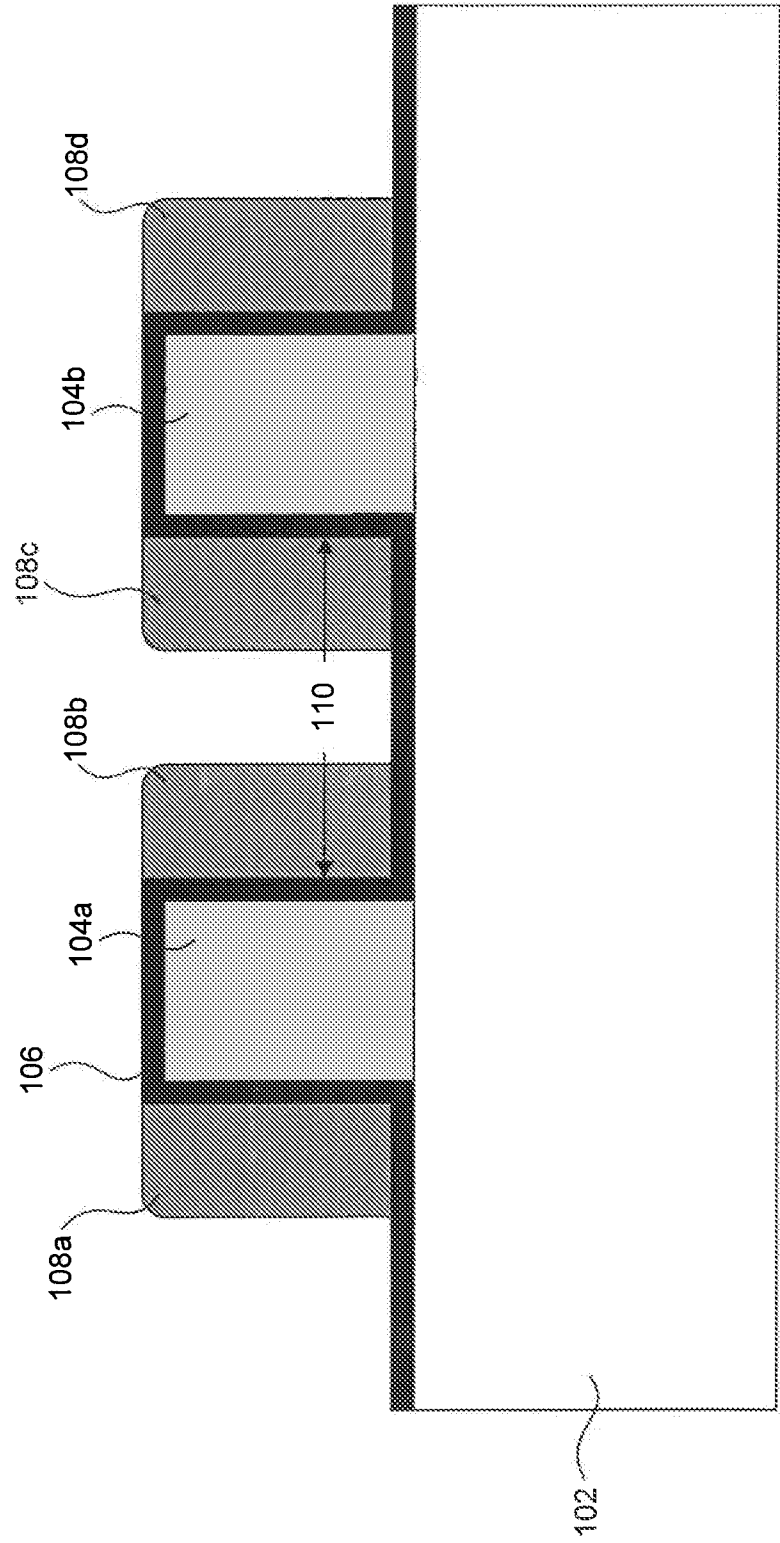
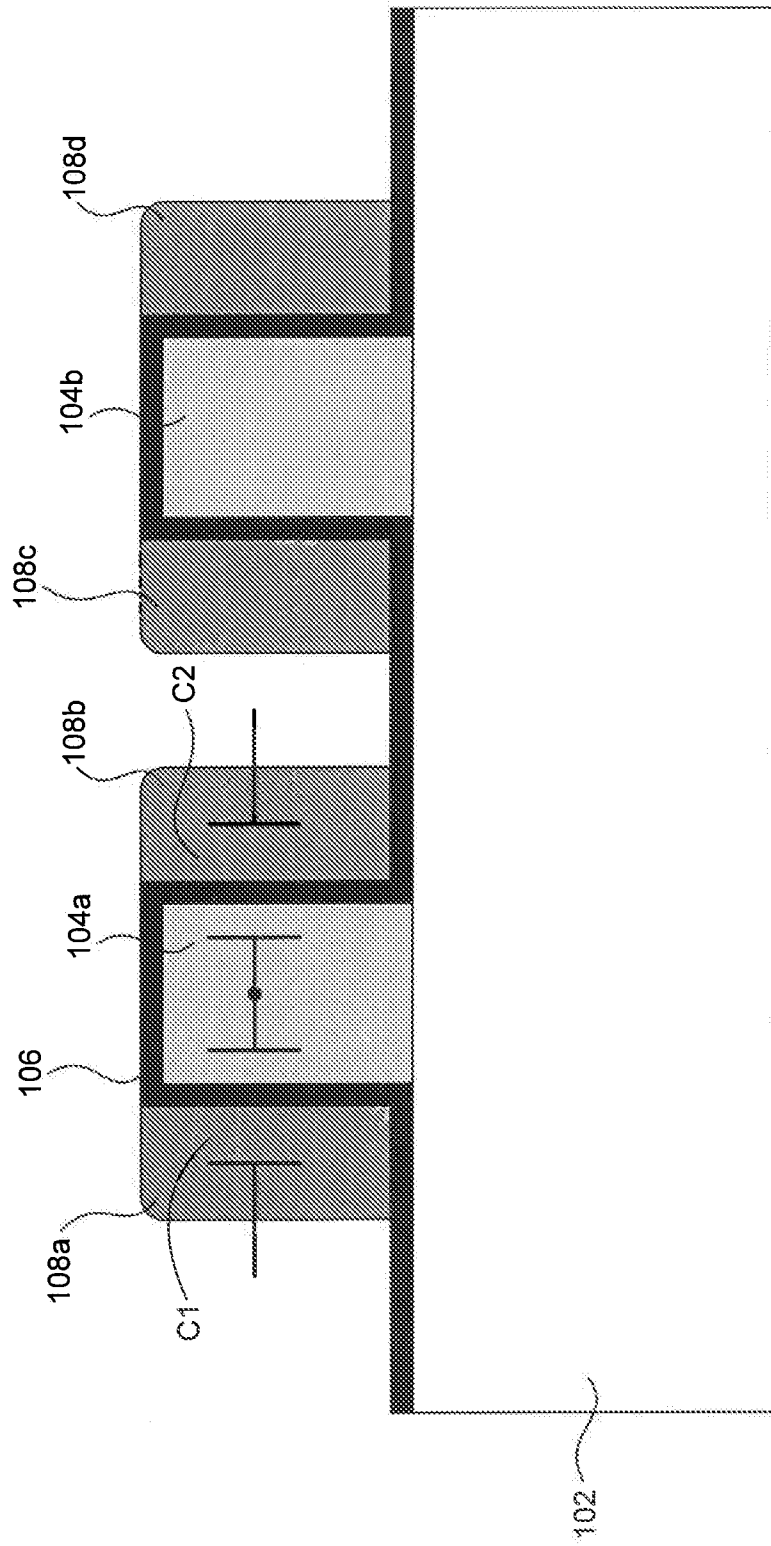


FIG. 1A

100

200

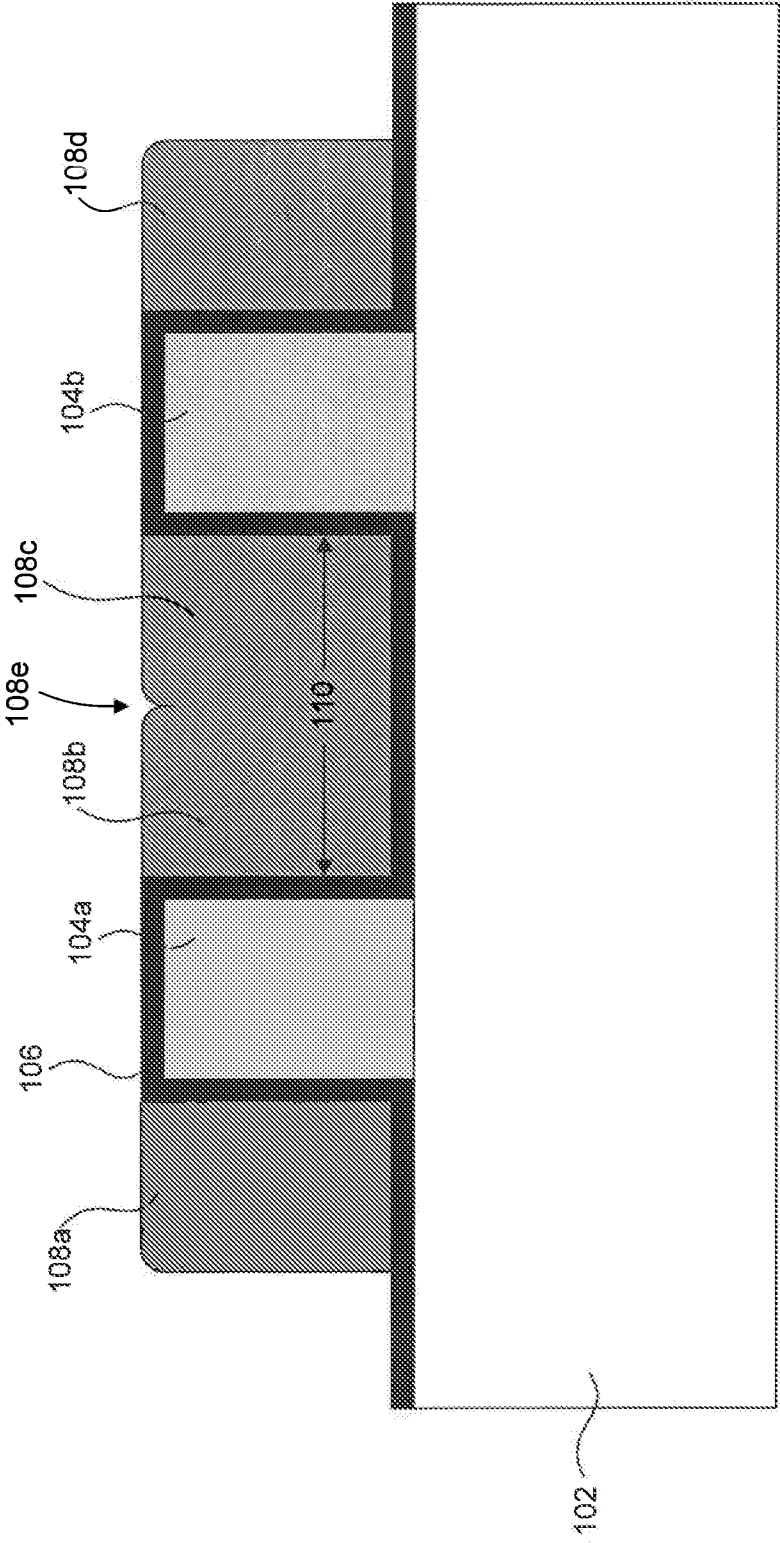
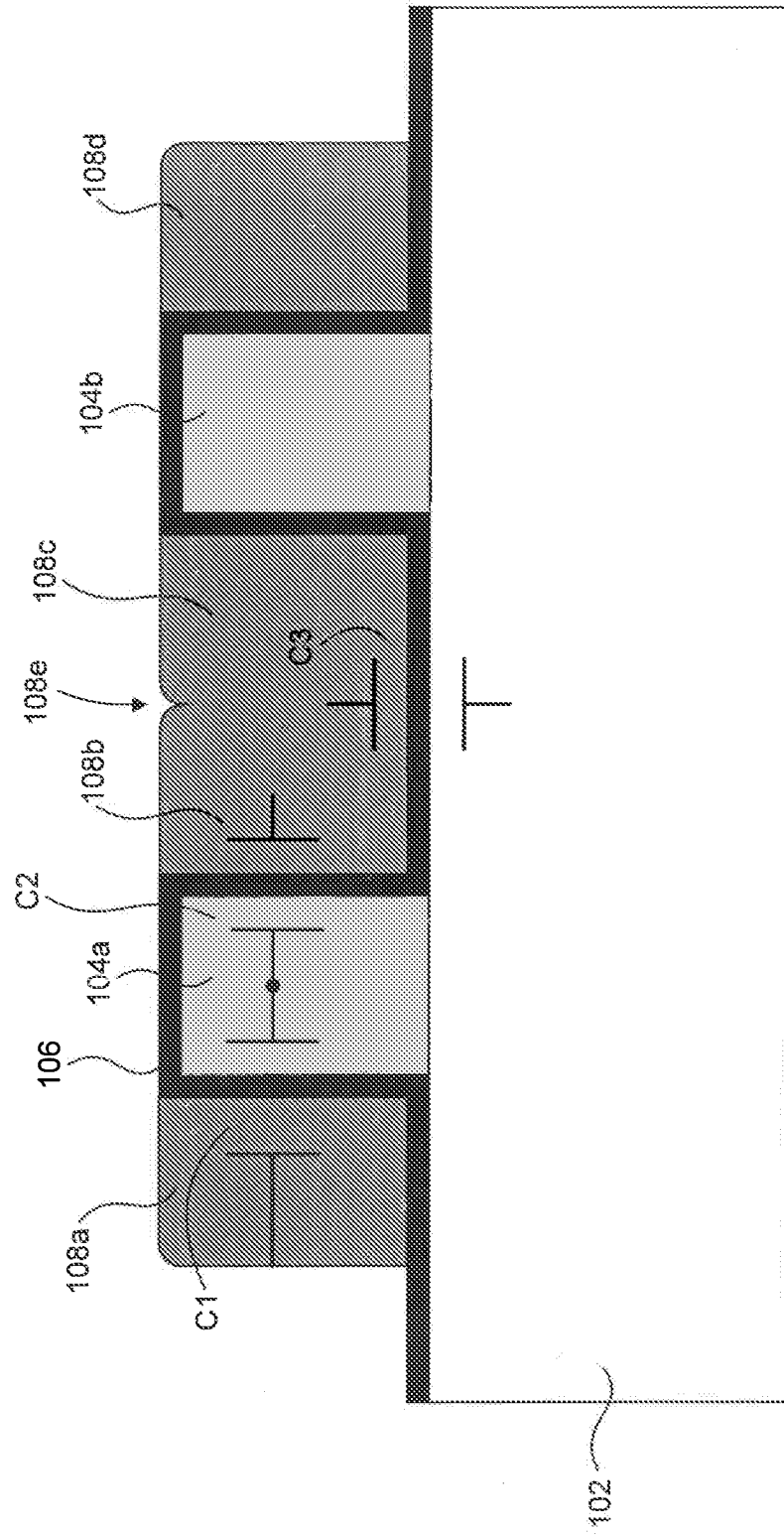


FIG. 2A



2025

300

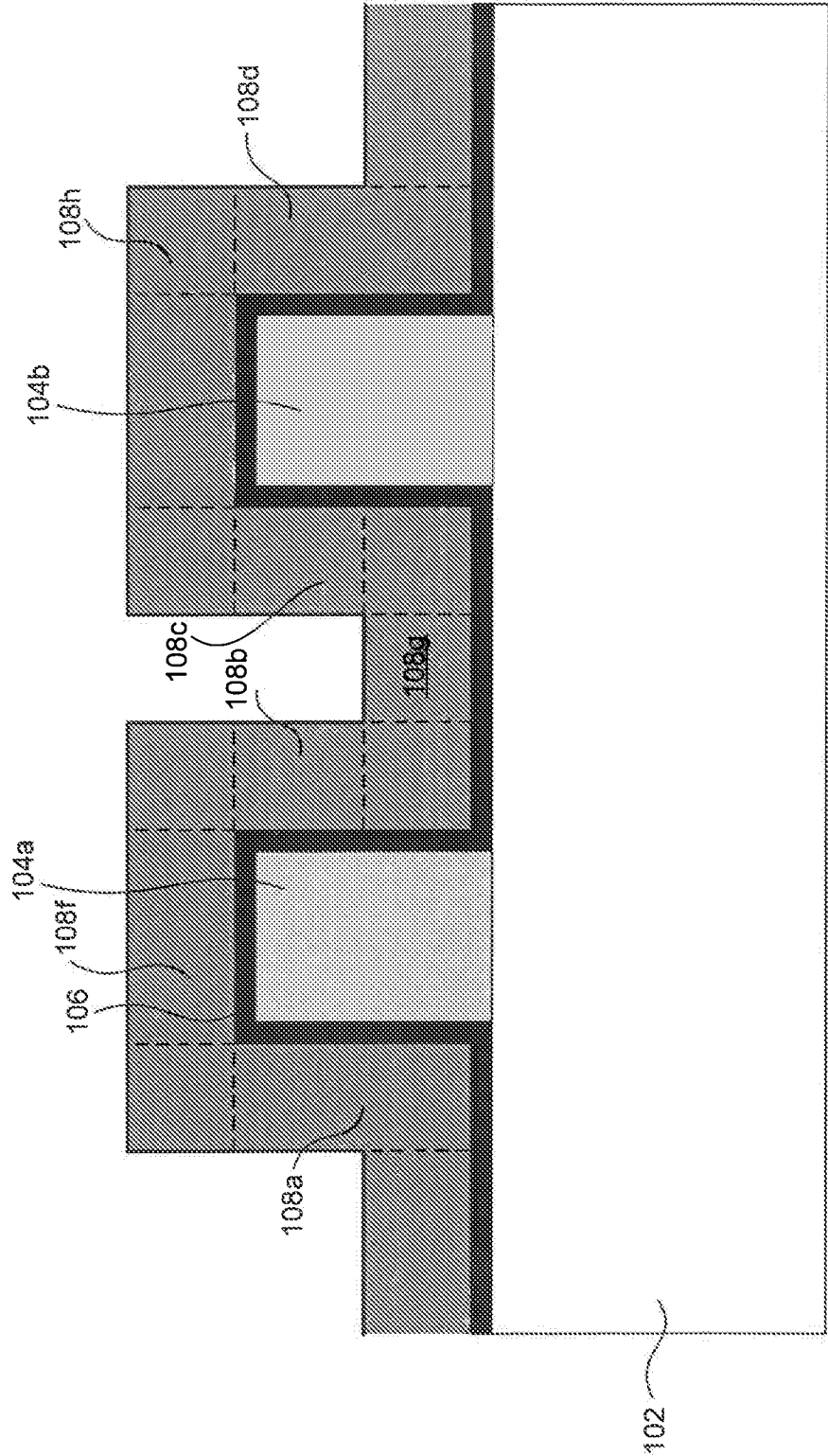


FIG. 3A

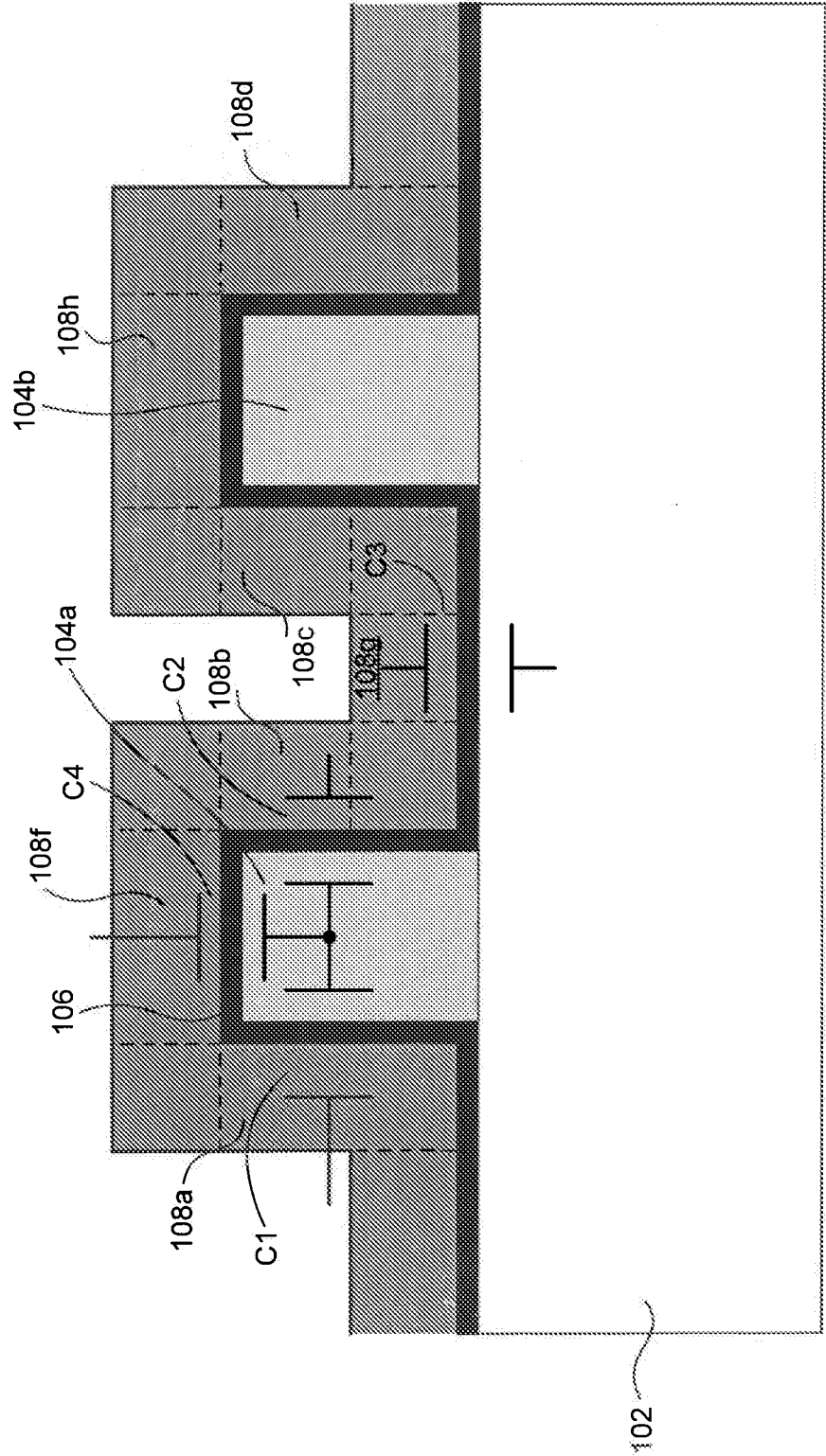


FIG. 3B

400

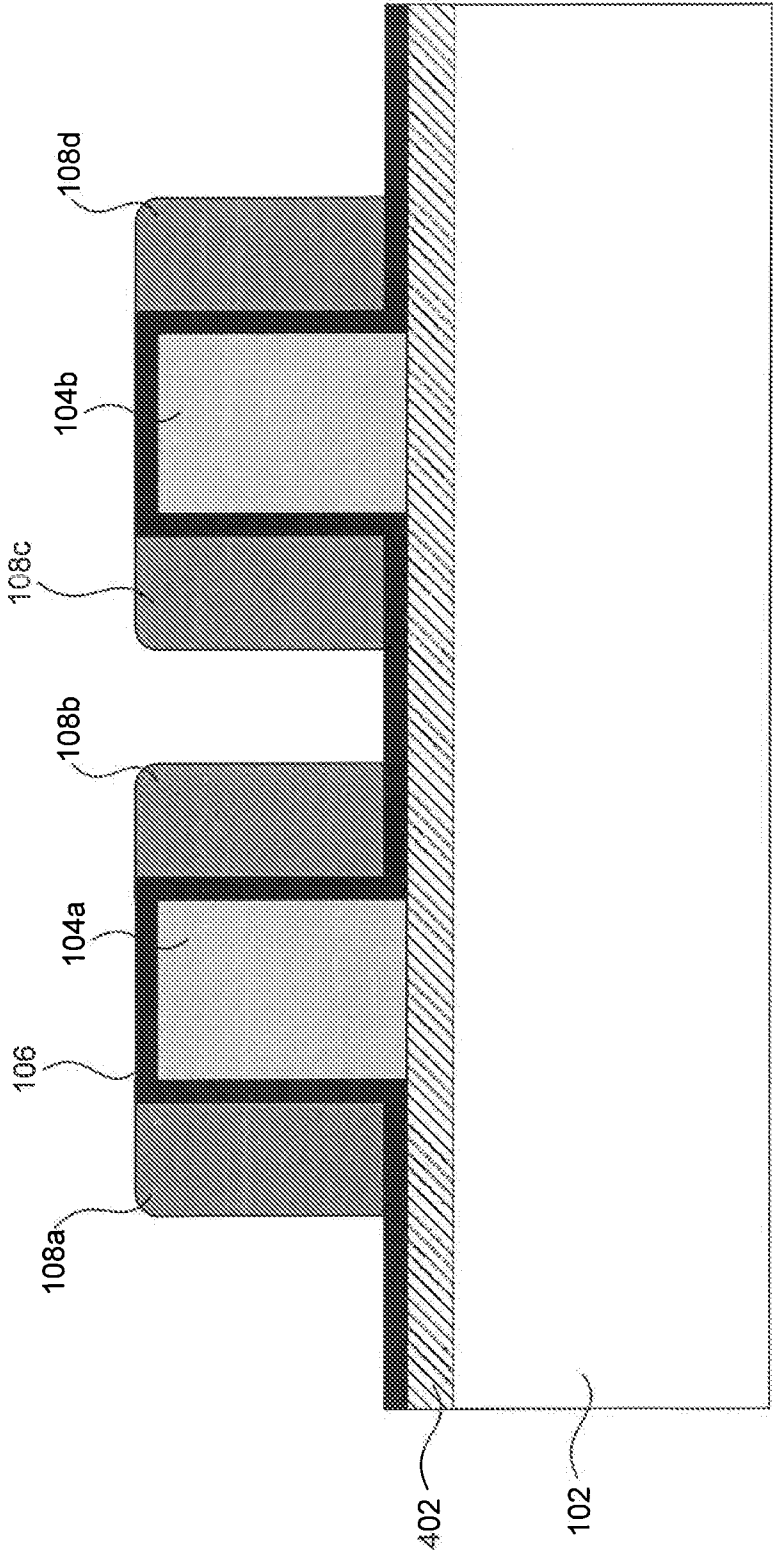


FIG. 4

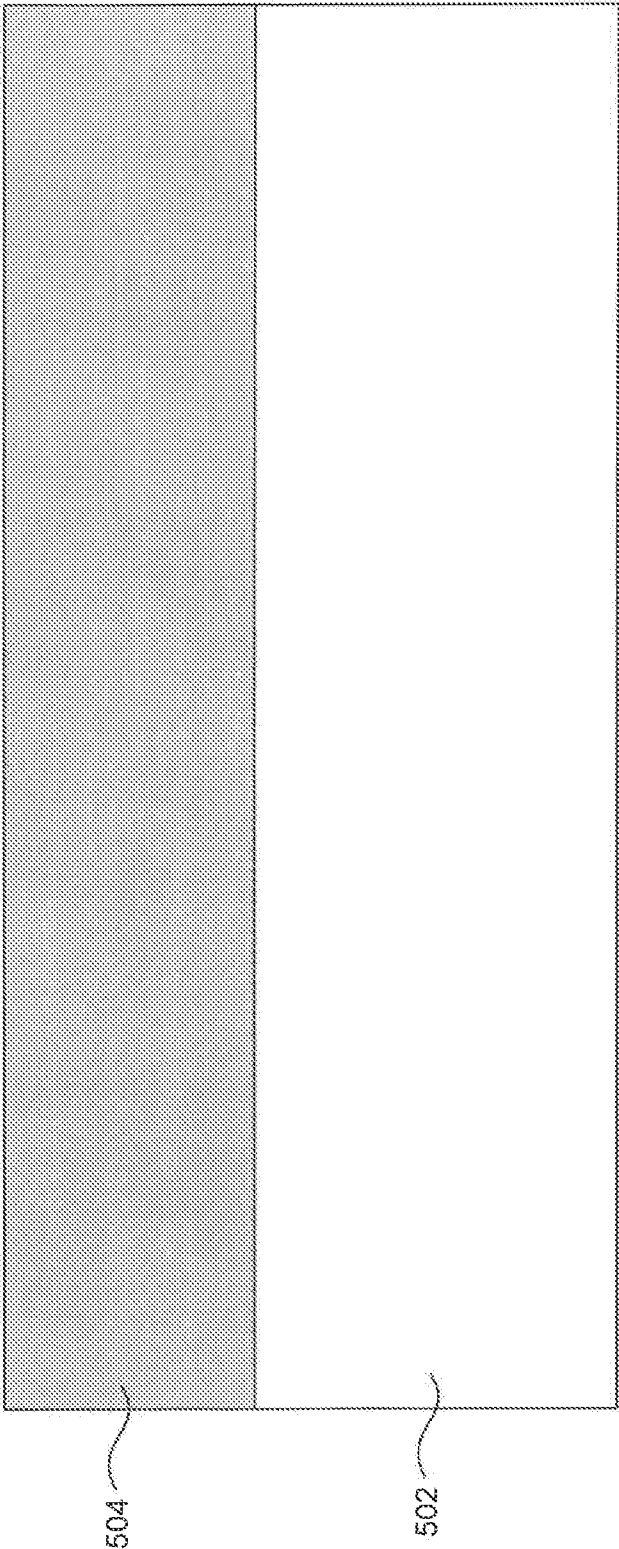


FIG. 5A

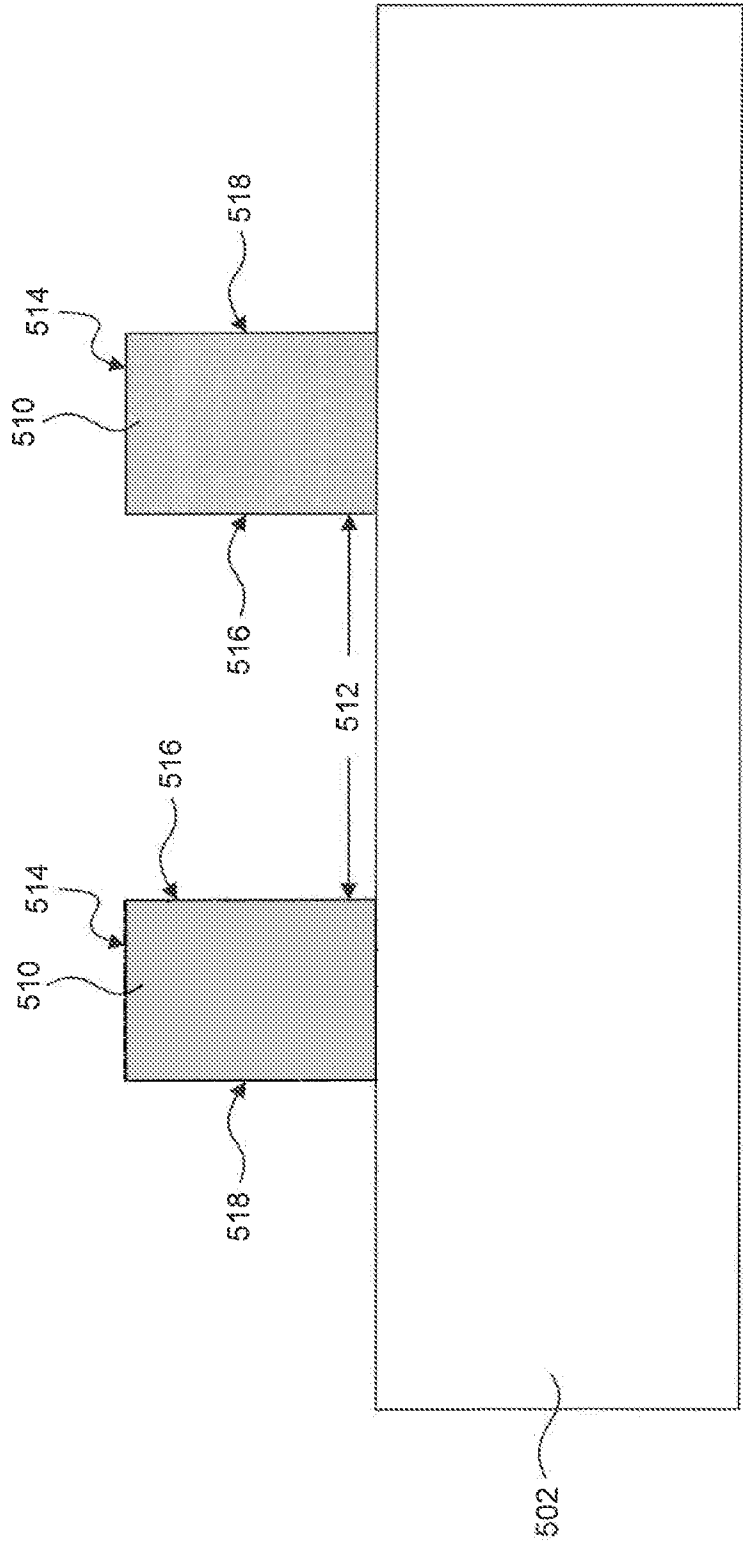


FIG. 5B

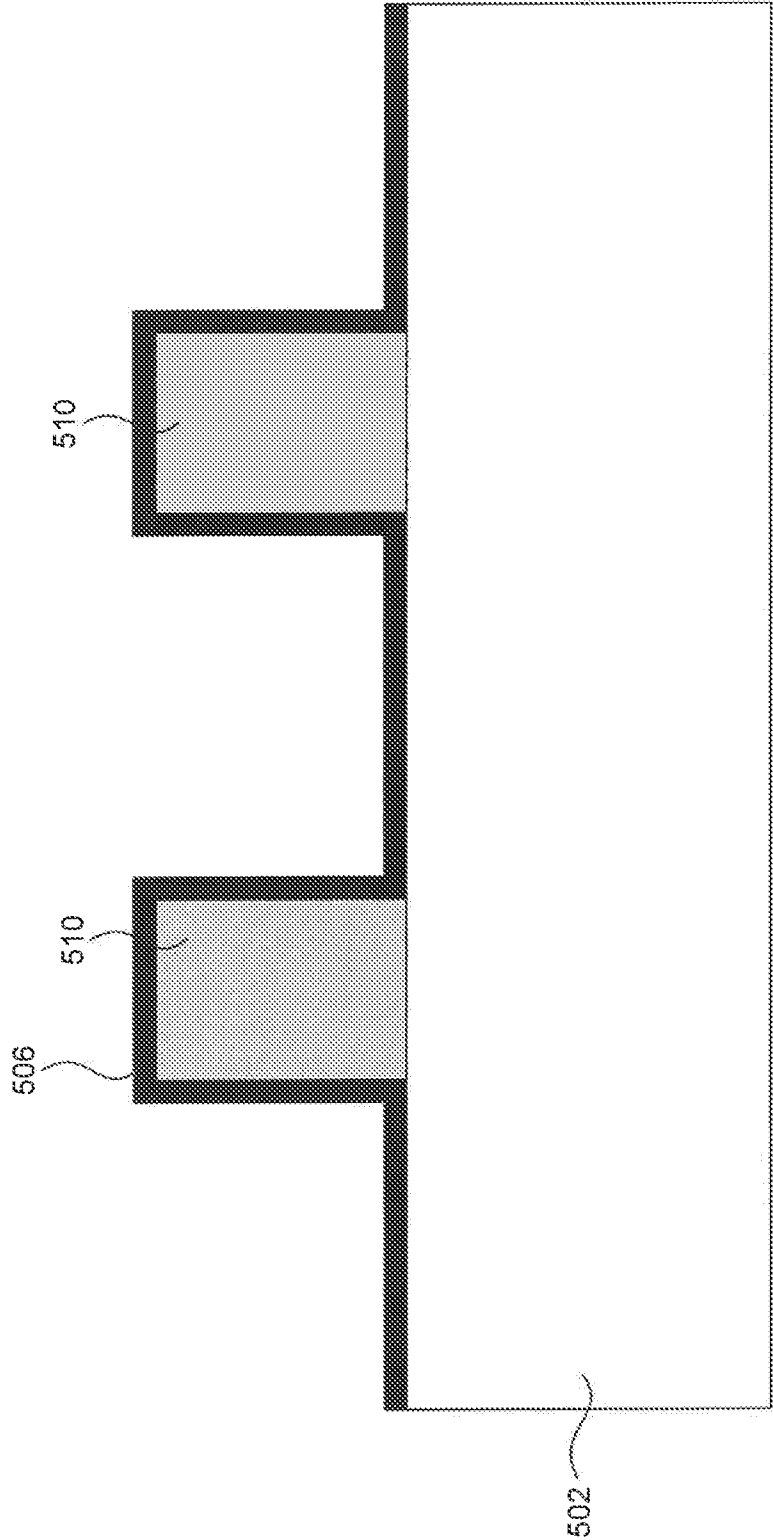


FIG. 5C

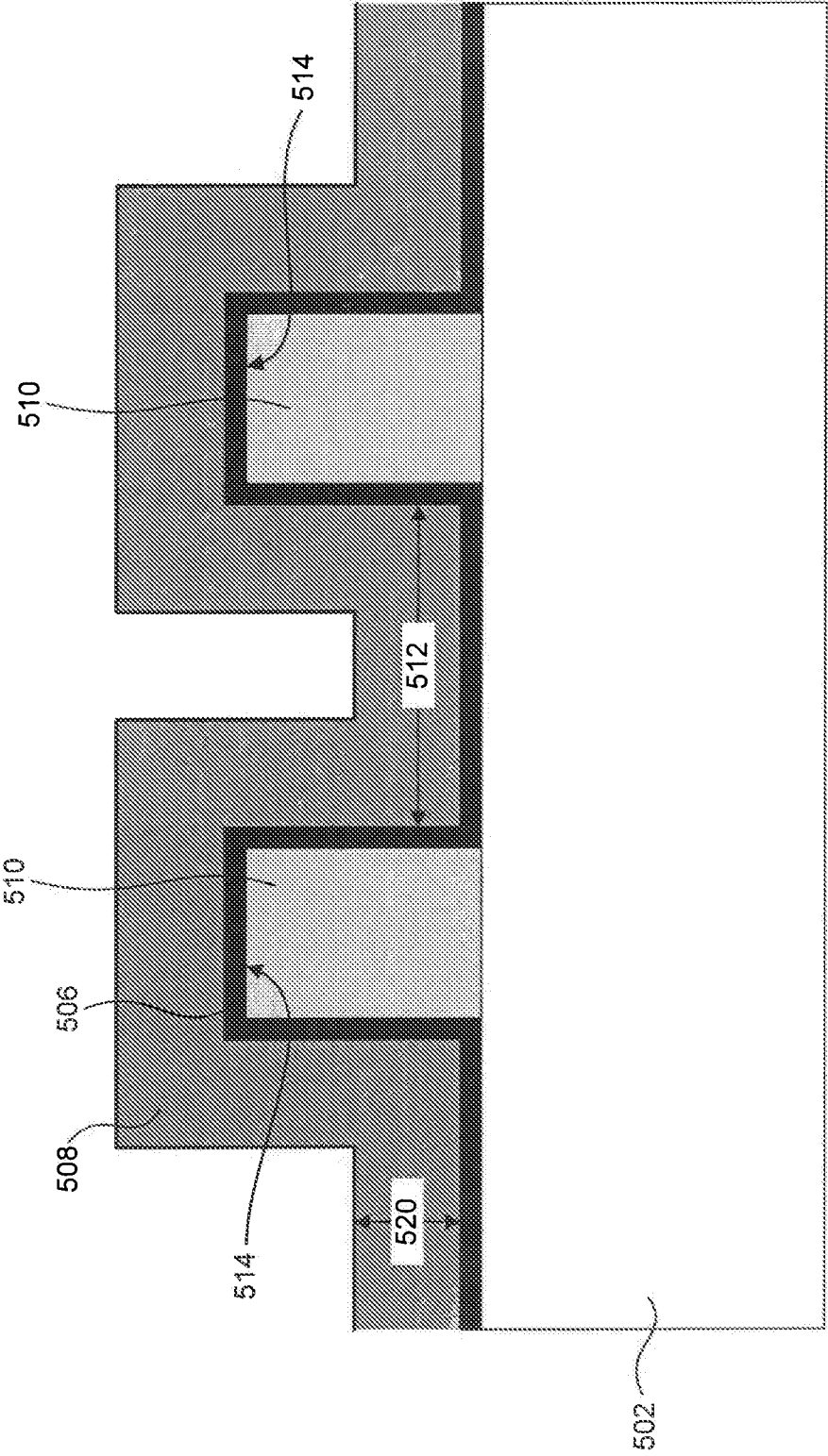


FIG. 5D

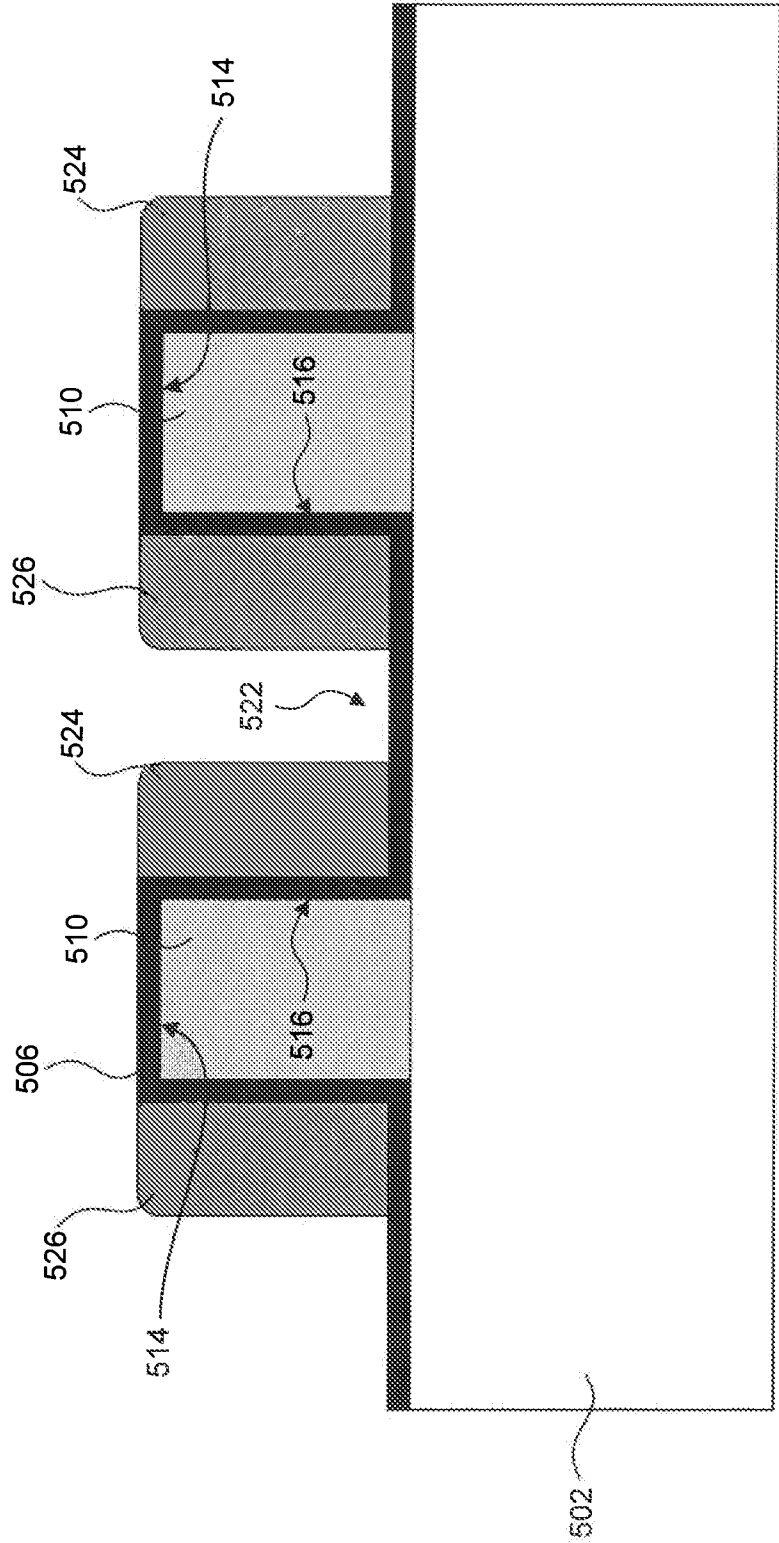


FIG. 5E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/074713**A. CLASSIFICATION OF SUBJECT MATTER****H01L 27/108(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/108; H01L 29/00; H01L 21/8246; H01L 27/105; H01L 21/30; H01L 21/8242

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: capacitors, conductors, separation region, side walls, surfaces, dielectric layer, capacitance, 3-dimension

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002-0146894 A1 (CEM BASCERI et al.) 10 October 2002 See paragraphs [0001]-[0006], [0038]-[0051]; and figure 18.	1-4, 7-10
A		5-6, 11-20
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Further documents are listed in the continuation of Box C.



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Date of the actual completion of the international search

27 March 2014 (27.03.2014)

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27 March 2014 (27.03.2014)

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