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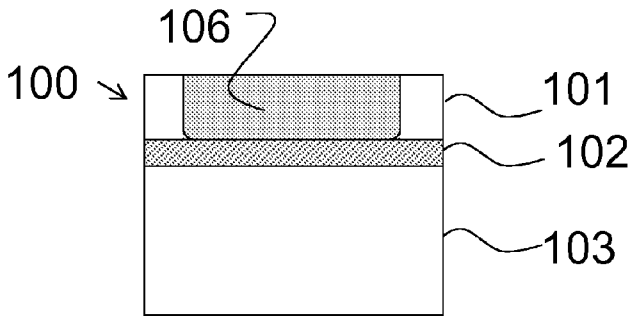

Fig. 8

(57) Abstract: The invention shows a doping method that can be used for doping of wafers. The method comprises making at least one ensemble of pores into a wafer matrix to be doped, depositing a vehicle layer on the substrate area of at least one said ensemble of pores and/or their walls, to form a vehicle layer as an interfacing surface for the dopant passage by diffusion. The deposition is followed by annealing said wafer in annealing specific conditions for enhancement of diffusion of said dopant from said vehicle layer via said interfacing surface into the wafer matrix to be doped. After the diffusion enhancement by annealing, the method comprises washing the vehicle layer away, by a washing agent for removal of the deposited dopant comprising material from the wafer surface and the pores. The doped porous structure of the wafer matrix comprising the dopant is then recrystallized, in a recrystallizing environment defined by recrystallizing parameters. The surface is finished and polished.

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A Method of Doping Wafers

Technical field

The invention is addressed to a wafer doping process in general. More specifically the invention concerns a wafer doping technique as defined in the pre-amble part of the independent claim concerning a method of doping wafers. The invention also concerns intermediate product of the method of doping, a wafer made by the method, and a power semiconductor component.

Background technology

In doping of wafers, it is important to have control of the concentration levels of dopant substances. Many times very insignificant looking departures from the desired dopant concentrations or levels thereof may lead to unexpected electro-mechanical behavior of the wafer material when used in semiconductor manufacturing, and/or in MEMS components.

Sometimes the departures cause variation in the quality, some components having not only different temperature behavior and/or electrical properties, but also mechanical properties, such as elasticity for example, which may be in key position in applications for switches and oscillators for instance. Especially in oscillator applications the temperature compensation to be gained may be very important measure of the oscillator stability, some applications being more tolerating temperature originating drifts than some other applications. Variation in properties, electric or mechanic, causes also losses, if manufactured materials have specifications with variations that are in an intolerable range, the range being too large and consequently the product pieces are not mutually sufficiently uniform.

Sometimes the crystalline structure sets unwanted limitations, when the crystals do not form when wanted into intended specifications range with the desired mono-crystalline structure but form poly crystals, whose properties differ from the mono crystal structure remarkably, often to the unwanted direction. Uniform crystals many times can be made from uniform materials, and the departures from the uniformity of starting materials cause problems to the crystal structure, which also influence to the electro-mechanical behavior.

One aspect is also process applicability to large scale manufacturing, taking into account the previous background-headed paragraphs in suitable part. Although some processes may be viable in lab conditions, they may be not applicable at all to mass production as such, although could solve doping related problems for a stable and sufficiently repeatable dopant concentration. Many times such techniques that work in lab are simply too slow for applicability to mass production, or need a special equipment for a manufacturing process step, or both ways. In addition although diversity could be controlled by selecting and testing the products followed by categorization in respect of quality, the loss of material and resources consumed to non-passed product handling increase the product prize and cuts its competitiveness.

Sometimes continuous process as such is desired, however such process may drift slowly apart from the parameterization at the beginning and it would be difficult to notice when the drift was occurring badly and which batches of products have acceptable composition of the wafer material. If the limits were detectable, also the variation of material grade may lead to variation in the amount of the product made from the material with the associated grade.

In electronics manufacturing, ultra-heavy phosphorous doping is in practice if not totally impossible at least extremely difficult during silicon ingot growth or during epitaxial layer growth of silicon in wafer manufacturing. Thermal diffusion of dopants after wafer fabrication is a slow process, although there is a need for a cost effective means to introduce dopants deep into silicon crystal lattice with uniform doping concentration in the whole device volume.

These difficulties are frequently met in the industry. But sometimes laboratory process operable as such has not been used in industry, as skilled persons know them as such but know them not viable in large scale, and nobody has noticed that such a process would be useful with a selected modification and/or combination into another known as such process or part thereof.

Summary of the invention

It is an object of the present invention to implement such a solution, that previously mentioned drawbacks of the prior art could be diminished. In particular, the invention is implied to solve how to improve the dopant uniformity of a processed wafer.

The objective of the invention is met by the features disclosed in the independent patent claim.

One objective of the invention is to improve high dopant concentration in a device layer of the wafer to be produced. The embodiments of the invention improve the dopant uniformity of the processed wafer. Consequently the crystalline structure is better of monocrystalline type, and consequently the electro-mechanical components have an improved quality.

The invention shows a novel cost effective industrially viable process how to produce extremely highly doped Si structures. In the following description of the embodiments of the invention the dopant concentration is above $1*10^{20}$ /cm^3.

A method of doping wafers according to the invention comprises:

- making at least one ensemble of pores into a wafer matrix to be doped,

- depositing a vehicle layer on the substrate area of at least one said ensemble of pores and/or their walls, to form an interfacing surface for the dopant passage by diffusion,

- annealing said wafer in annealing specific conditions for enhancement of diffusion of said dopant from said vehicle layer via said interfacing surface into the wafer matrix to be doped,

- washing the vehicle layer away, by a washing agent for removal of the deposited vehicle from the wafer surface and the pores,

- recrystallizing, the wafer matrix comprising the dopant, in a recrystallizing environment defined by recrystallizing parameters, and

- polishing a surface of said wafer on said area of the recrystallized material layer.

According to an embodiment recrystallization is made to close the pores and make the silicon matrix solid. According to an embodiment the recrystallization is made to modify the porous structure in a layer, to close the pores.

According to an embodiment of the invention the method comprises at least one of the following:

- defining the pore lithography,

- defining annealing-specific conditions, for the annealing environment

- defining recrystallizing environment,

- defining washing environment,

- defining washing agent composition,

- defining cooling with cooling parameters and

- defining finishing procedure with finishing details.

According to an embodiment of the invention the method comprises depositing a vehicle layer that comprises at least PSG oxide.

According to an embodiment of the invention the method comprises the doping made for a wafer that is a wafer with at least one buried layer in the wafer matrix.

According to an embodiment of the invention the method comprises such washing that is washing to reach an etch stop layer in contact with at least one buried layer or being a part of it, the etch stop layer arranged to stop washing and/or etching from the etching direction.

According to an embodiment of the invention the method comprises continuing the washing to focus into a buried layer in the wafer matrix for making a cavity under the doped matrix in the wafer, with a washing agent having an agent composition suitable to etch the buried layer but preserve the doped wafer matrix.

According to an embodiment of the invention the method comprises making of pores in said ensemble of pores comprising at least one pore, which is making such pores that have ensemble of pore-specific quantities as pore characteristic parameters.

According to an embodiment of the invention the method comprises washing further away of formed deposits of agents that formed the vehicle layer and/or a cap and/or other remaining agents.

According to an embodiment of the invention the method comprises making pores in at least one ensemble of pores uniform in respect of at least one parameter belonging to the pore characteristic parameters of the ensemble of pores. In this embodiment, the deposition would be more equal for the pores than if the pores were

very different from each other in respect of a key parameter associated to the pores as such.

According to an embodiment of the invention the method comprises utilization of one pore ensemble specific parameter as a process control parameter which is at least one of the following quantities: pore diameter, pore depth, other pore dimension, geometric form, volume, surface, surface roughness, surface material, fractal dimension of the pore, a derivative of said aforementioned parameters. In this embodiment the process can be controlled by a back loop signal to control process means to control the influencing quantity and/or material concentration.

According to an embodiment of the invention the method comprises making pores of different kinds on the same wafer so that pores in a first sub-ensemble of said ensemble are different than pores in a second sub-ensemble of said ensemble of pores, in respect of at least one ensemble specific quantity.

According to an embodiment of the invention the method comprises etching performed by means of electrochemical etching to make at least one ensemble of pores and/or a sub-ensemble of pores.

According to an embodiment of the invention the method comprises defining at least one sub-ensemble of pores lithographically and/or randomly.

According to an embodiment of the invention the method comprises defining said annealing specific conditions comprise defining at least one such parameter that is annealing specific parameter, which is at least one of the following:

- annealing temperature

- annealing pressure

- annealing chamber environmental composition

- at least one additional chemical agent

- a combination of the aforementioned parameters

- derivative of said aforementioned parameters or an ensemble of such.

Derivative means also in one embodiment mathematical derivative in respect of time and/or spatial location or another related process quantity.

According to an embodiment of the invention the method comprises selecting annealing specific parameter value to enhance diffusion of a dopant substance from the vehicle layer, and/or from the carrier material, if used in assistance and/or substitute to a vehicle, which carrier material in an embodiment can comprise a gaseous component to carry the dopant in a composition to be in contact with the pores and their walls.

According to an embodiment of the invention in the method, the dopant is selected from the group comprising P.

According to an alternative embodiment of the invention, use of the vehicle layer material can be substituted in suitable part if not totally, in a respective embodiment by another carrier material. According to an embodiment the carrier material comprises a gaseous component with a dopant in a hydrogen composition for the n-type semiconductor material to be produced. According to an embodiment the carrier material to be used to substitute the PSG-glass entirely or in suitable part to assist the doping, PH_3 is used as the dopant carrier material's gaseous component. For another n-type layer structure the dopant is selected from the nitrogen-group.

For the p-type semiconductor, the vehicle composition is selected accordingly, i.e. to comprise glass type to operate as a vehicle. According to an embodiment the carrier material comprises a gaseous component with a dopant in a hydrogen composition for the p-type semiconductor material to be produced.

According to an embodiment the carrier material to be used to substitute the BSG-glass entirely or in suitable part to assist the doping, a gaseous B-containing substance is used as the dopant carrier. For another p-type layer structure the dopant is selected from the Boron-group, to be used within a vehicle-layer and/or in a carrier material comprising gaseous component.

According to an embodiment of the invention the method comprises using such washing agent that comprises HF. According to a variant of the invention the HF is in gaseous form in the washing temperature and pressure. According to an embodiment, the washing temperatures and pressures are used in known as such regions.

According to an embodiment of the invention the method comprises removing remaining agents which can comprise nitrous and/or oxygen containing substances.

According to an embodiment of the invention the method comprises defining recrystallizing conditions for at least one such parameter that is recrystallizing specific parameter, which is at least one of the following:

- recrystallizing temperature,
- recrystallizing pressure,
- recrystallizing chamber atmosphere composition,
- concentration of at least one additional chemical agent,
- concentration component composition of said additional chemical agent,
- a combination of the aforementioned parameters
- derivative of said aforementioned parameters or an ensemble of such.

According to an embodiment of the invention the method comprises washing by a washing agent being continued to an etch-stop layer that stops the washing by the selected washing agent in a perpendicular direction to the pore length. In this way the pores lead the washing agent from the tubular pore to its radial direction in the buried layer until washing agent meets etch stop layer to stop the washing.

According to an embodiment of the invention the method comprises forming of a cavity between the pores containing layer and the etch-stop layer into a cavity forming layer by the washing agent used in washing for forming cavity in said layer. This way a structure with a cavity can be formed under the device layer of the wafer.

According to an embodiment of the invention the doping method further comprises bonding a wafer to the doped wafer according to an embodiment. According to an embodiment the wafer to be bonded is an oxidized layer comprising wafer. According to an embodiment of the invention the boding is made by fusion boding, which is in a variant followed by a thermal treatment.

An intermediate product according to an embodiment of the invention is made by at least one process step of an embodied method of the invention, to be made ready for a further step of the method.

A wafer according to an embodiment of the invention is manufactured by the doping method according to an embodiment of the invention.

A micro-mechanical device according to an embodiment of the invention is manufactured at least partly on the wafer according to an embodiment of the invention. According to an embodiment variant the micro mechanical device comprises at least one of the following:

MEMS-component, sensor, oscillator, semiconductor component, micro circuit, transistor, FET.

According to an embodiment of the invention a power semiconductor component comprising a semiconductor structure originating to a wafer manufactured according to an embodiment.

According to an embodiment of the invention, in the recrystallization environment the recrystallization occurs in a recrystallization temperature of 1000°C -1200°C. According to an embodiment of the invention the recrystallization atmosphere comprises Argon Ar, and/or Hydrogen H_2 in the recrystallization temperature.

According to an embodiment of the invention the dopant is selected for production of n-type semiconductor.

According to an embodiment of the invention such a dopant is an element of nitrogen-group of the periodic system. According to an embodiment of the invention the dopant is or comprises phosphorous P, according to a respective embodiment. According to an embodiment of the invention the dopant is specifically selected because of the mechanical contribution to the doped structure.

According to an embodiment of the invention the dopant is selected for production of p-type semiconductor.

According to an embodiment of the invention such a dopant is an element of boron-group of the periodic system. According to an embodiment of the invention the dopant is or comprises boron B, according to a respective embodiment. According to an embodiment of the invention the dopant is specifically selected because of the mechanical contribution to the doped structure, to be used alone or in combination with another doped structure comprising a specifically selected dopant.

Other embodiments are shown in the examples and in the Figs as well as in the description relating to the Figs. Embodiments of the invention are combinable in suitable part. The measures and dimensions in Figs are not necessarily in scale, or limiting the order and/or layout only to the shown illustrative examples.

Some preferable embodiments of the invention are described in the dependent claims.

Significant advantages can be achieved with the present invention when compared to the prior art solutions.

When considering doping of wafers, one starting point is a SOI wafer (Silicon On Insulator) or a derivative thereof. Also a bulk wafer may be used as a starting point for the substrate on which a more sophisticated structured topology is formed via several phases of etching and/or depositing.

Short description of the drawings

Same reference numerals are used to refer similar kind of objects in the figures from one to another, if specifically not otherwise defined. However, the objects do not necessarily need to be identical from one embodiment to another, but a skilled man in the art knows from the embodiments of the invention and the context the potential small differences, if any.

The doping method is explained further with reference to the wafer in the Fig 1 and in Figs 2 to 12B via them as intermediate products of the embodied doping method, except an aspect of Fig 9 to show a method flow for the process of an embodiment of the invention.

Next, the invention is described in more detail with reference to the appended drawings, in which

Fig 1 Illustrate a wafer to be processed porous according to an embodiment of the invention,

Fig 2 Illustrates a wafer with a porous pre-device layer in an embodied doping method example,

Fig 3 Illustrate microscopic cross sections of a porous wafer structure according to an embodiment of the invention,

Figs 4-8 Illustrate embodiments of the invention for the doping method and the related method step intermediate products,

Figs 6B-8B Illustrate ensemble of variant embodiments of the invention for the doping method variant and the related method step intermediate products,

Fig 9 Illustrate an embodiment of the invention, and

Figs 10A-12B Illustrate ensemble of variant embodiments of the invention for the doping method variant and the related method step intermediate products.

Detailed description of the embodiments

The scope of the invention is determined by the attached claims together with the equivalents thereof. The skilled persons will again appreciate the fact that the explicitly disclosed embodiments were constructed for illustrative purposes only, and the scope will cover further embodiments, embodiment combinations and equivalents that better suit each particular use case of the invention.

Starting point for getting a wafer doped can be a wafer illustrated in Fig 1. The wafer can be a SOI wafer 100 as in the example, or a bulk wafer to be further processed to have the structure suitable to the process start, i.e. a buried layer in the wafer structure with the etch stop layers to stop etching. These preparatory method steps are not explained further as a skilled man in the art knows how to make a SOI wafer as such, or, how to make suitable wafer as such with the appropriate etch stops, on the basis of the embodiments, a modified SOI wafer for a special embodiment of the invention if necessary for dedicated applications.

According to an embodiment of the invention, in the recrystallization environment the recrystallization occurs in a temperature of 1000°C -1200°C. According to an embodiment of the invention the recrystallization atmosphere comprises Argon Ar, and/or Hydrogen H_2 in the recrystallization temperature.

According to an embodiment of the invention the dopant is selected for production of n-type semiconductor.

According to an embodiment of the invention such a dopant is an element of nitrogen-group of the periodic system. According to an embodiment of the invention the dopant is or comprises phosphorous P, according to a respective embodiment. Ac-

cording to an embodiment of the invention the dopant is specifically selected because of the mechanical contribution to the doped structure.

According to an embodiment of the invention the dopant is selected for production of p-type semiconductor.

According to an embodiment of the invention such a dopant is an element of boron-group of the periodic system. According to an embodiment of the invention the dopant is or comprises boron B, according to a respective embodiment. According to an embodiment of the invention the dopant is specifically selected because of the mechanical contribution to the doped structure, to be used alone or in combination with another doped structure comprising a specifically selected dopant.

In Fig 1 the wafer 100 has a device layer forming layer 101, a buried layer 102, and a substrate layer 103. The layers can have a further composition and structure for application detail implementation for dedicated applications, where necessary.

In Fig 2, the device layer forming layer 101 of the wafer 100 has been made porous. The pores 104 are etched electrochemically to the buried layer, or such a part of it which comprises an etch stop layer in the buried layer 102. In the example the etching has stopped to the pore boundary, indicative of the etch stop layer position in the buried layer at the pore location.

Although the layer 101 has been used in the example for the pore 104 formation, skilled person in the art knows that the substrate layer 103 in the example can be used also for pore formation, but the parameters for the processing that side should be changed accordingly. The area on which the pores are placed can be whole wafer side or a part of it. The doped volume is then defined by the area of porous area and the pore length or depth. The doped volume defines the device layers of the wafer when ready. In an embodiment variant of the invention the wafer surface can be lithographically patterned to expose only certain parts of it to the electro-chemical etching.

Fig 3 illustrates as a microscope picture series a wafer structure of Fig 1 with the pores 104 in Fig 1.

Fig 4 illustrates wafer 100 in the process of doping method according to an embodiment of the invention, wherein the pores are filled with a dopant containing filling material, vehicle material or vehicle in the following, indicated with the black color. In the example the dopant containing filling material is PSG glass. The dopant in

the example is P. The pores 104 and the Si-matrix 101 in the device layer forming layer has been coated with the cap 105. The cap can be made of same material as the dopant carrying vehicle material, or can be in one embodiment be a composition of two or many layers. According to an embodiment of the invention the cap is made at least partly by silicon nitride Si_3N_4.

According to an embodiment closest layer of cap to layer 101 contains material that can accept impurities from the layer 101, when heated for diffusion enhancement.

In Fig 5 the gray area 106 of the cross section area of the wafer 100 indicates that the diffusion enhancement has occurred in the annealing phase of the process, so that the vehicle in the pores 104 has released dopant to the volume 106 for uniform doping. The cap is still there, until the removal of it.

Fig 6 is indicative of the wafer in the phase of the process to remove the cap and the other remaining material by etching agent. The washing/etching agent was in the example HF. According to the embodiment of the invention the HF was in anhydrous and gaseous form.

According to an embodiment the washing environment is in ambient conditions, with the temperature ramping to the washing temperature and atmosphere with the added HF. According to an embodiment the washing as such is made in a known washing temperature as such. According to an embodiment of the invention the washing temperature is limited by the reaction vessel tolerance of washing agent, for HF for example.

Fig 6B is indicative of an alternate wafer made with an embodiment phase, which continues from the illustrative situation of Fig 6. Etching further continues for a cavity 104C underneath the porous doped layer 106. The cavity embodied has a rectangular cross section, but a skilled person in the art knows that the form of the cavity can be pre-defined by the etch stop layer formation as its ceilings, floors and/or walls to define the cavity dimensions and form, for example when patterning the buried layer at the wafer manufacturing in an appropriate phase of the starting wafer manufacturing. The buried layer is drawn in the Fig 6B as a wider formation than in Fig 6 only for clarity reasons for the presentation, without any intention to restrict the dimensions to the shown example alone.

Fig 7 indicates the porous wafer 100 after the recrystallization phase of the embodied doping method. The layer 106 has become thinner, and the porous structure has been deformed to a uniform layer also in respect of the dopant concentration. The

recrystallization has been made in a recrystallization environment with a recrystallization temperature, in the embodiment example the selected temperature is 1150°C. According to an embodiment of the invention the recrystallization temperature is chosen to be the same as the annealing temperature, but is not always limited only that in embodiment variants.

For the thermal treatments of annealing and/or recrystallization the thermal rampings to elevate and decrease the temperature in the reactor vessel used in the processing of the wafer can be made according to the known techniques in suitable part as such.

The illustration in Fig 7B differs only with the structural matter of cavity 104C from the Fig 7 in that there is the cavity 104C formed into the wafer processed as Fig 7B indicate for the alternate embodiment branch of the doping method according to the embodiment of the invention. Pre-defined etch stop layers were used to stop the etching to the limited surfaces with the appearance of the cavity.

Fig 8 shows the wafer structure 100 as polished, and Fig 8B the wafer structure 100 with cavity 104C as polished too. Relating to the polishing, other finalizing phases can be made as normally are made for a wafer that is just manufactured.

Fig 9 illustrates a process flow according to an embodiment of the invention the doping method, in accordance of the figures 1 to 8B. Although some of the process steps may need preparatory actions, they are not shown in the figure 9 as skilled person in the art knows how to prepare from one step to another when read and understood the embodiments of the invention.

In the step 901 a wafer, for instance a SOI wafer (Fig 1) has been prepared to electrochemical etching (Fig 1 to Fig 2) for etching pores. PSG glass has been used as a vehicle for the dopant P in the example, for filling (Fig 2 to Fig 4) the pores with the vehicle material in the step 902. In the step 903, diffusion is enhanced in the annealing phase (Fig 4 to Fig 5). In step 904 the cap and the glass, the vehicle is removed (Fig 5 to Fig 6), and when cavity is desired underneath the layer 101, the process continues to step 904B for the cavity etch (Fig 5 to Fig 6B via Fig 6). The method step 905 continues with the recrystallization, without cavities (Fig 6 to Fig 7) or with cavities (Fig 6B to Fig 7B). The method step 906 finalizes the wafer by polishing (Fig 7 to Fig 8 without cavity, Fig 7B to Fig 8B with cavity) for example, illustrating also other finalizing works too.

According to a variant of embodiments, even further dopants can be used while repeating the method via the step 907, until the desired dopants have been doped. However, the line from box 905 to 907 is illustrated with a dashed line, indicative as an option, that may be as such available but potentially risky for losses per round if many cycles are performed before the taking the wafer out of the process and ending the process 908. The dashed arrows from the step indicative box 907 to steps 902 and 901 indicate optionality, to dope further via the pore-structure or mere surface with the specific dopant.

According to a variant of the embodied method, the Figs 10A to 12B illustrate a manufacturing example to implement a bonded structure with heavily or ultra-heavily doped crystalline structure. The bonding can be made with an oxide layer 1002 comprising wafer 1001 (Fig 10A). According to an alternative embodiment, the bonding can be made with such a bulk wafer that has not the oxide layer 1002, although shown in the Figs. The presentation media position does not limit the direction only to the indicated up or down, the bonding can be made also in an other geometry.

The wafer 1001 is oxidized to a desired thickness (at least on one of the sides of the wafer) of the layer 1002. According to an embodiment variant the wafer 1001 is a bulk wafer without the layer 1002. According to the method variant, the wafer (with or without the layer 1002) and the other wafer 100 are bonded together by fusion bonding and treated thermally (Fig 11A).

According to an embodiment of the invention the structural layer of the wafer 1001 is thinned to a desired thickness, as embodied in an example 10-20 μm. The top surface is polished and other routine such as rounding the edges are made, in an embodiment variant as in a normal way in SOI-manufacturing.

According to an embodiment, as manufactured within the method, the SOI-wafers with the ultra-high doped structure can be used in MEMS- or power semiconductor component manufacturing.

The Figs 10B to 12B, with the letter “B” is used to refer to a cavity in the structure, illustrate the same structure as with “A” except at least one cavity patterned into the structure according to an embodiment variant as in previously earlier cited Figs indicate, and/or another cavity 104CC is indicated in the wafer 1001 structure. According to an ensemble of embodiment variants, the layer 1002 can be in one type

of embodiment ensemble, but in another type of embodiment ensemble the layer 1002 is not present as a consequence of the bulk-wafer utilization in bonding.

Because the one with the dashed line surrounding illustrate in the example that the cavity 104CC is an optional embodiment, it is drawn with dashed line. In this embodiment the additional cavity 104CC so indicated can be manufactured in suitable part to the bonding wafer 1001, which is thus independently machinable/etchable cavity structure of the wafer 1001 as such, independently on the structure of the other wafer 100 to be bonded as such.

FURTHER EMBODIMENTS AS EXAMPLES

Extremely high doped Si comprising material can be manufactured according to an embodiment of the invention by doping wafer or similar structure with a suitable dopant.

The dopant concentration is selected in the example to $n_D > 1*10^{20}/cm^3$, on dopant atom number basis of the wafer area to be made porous. The process is made in a batch process way, which utilizes electrochemical etching, high temperature dopant diffusion, HF-vapor etching and high temperature recrystallization, and CMP. This way no polycrystalline deposition can be avoided and no need for plasma etching as such is present. Dopant can be brought to the Si structure from PSG donor-substance to be used as a vehicle. For another type of dopant, for example B doped P-structure, Boron containing glass (BSG or another suitable dopant comprising glass or compound) can be used as a vehicle to transport the dopant to the porous structure via the pore surfaces by the diffusion.

Starting point in one example can be a SOI wafer, or a pre-form of it to be used in the process according to an embodiment of the invention. Also a bulk wafer can be used in suitable part. In an example of embodiment, a wafer with a buried layer has been chosen, and a material layer of the wafer is made porous to the depth of the buried layer. According to an embodiment of the invention the buried layer comprises an etch stop layer, to stop the etching to the layer. According to an embodiment of the invention, not all the pores in the porous area are etched to the buried layer depth, i.e. some pores may be not necessarily etched through the layer. This perforation comprising phase to make pores can be made by using electrochemical etching. The pore locations can be lithographically defined, or allowed in random to be formed, over the whole wafer in an embodiment variant.

Skilled persons in the art know as such know how to control etching process as such for the porosity and the depth thereof, not to limit the form of pores in other embodiments, to get a pre-defined porosity parameters as such for the process step of an embodiment of the invention.

According to an embodiment of the invention, so pre-processed SOI wafer is the exposed to PSG oxide deposition, which at least partly fills pores in the porous area, so that at least some of the pores, if not all are full to the surface from which the etching was started. According to an embodiment, the porous area is sealed with a sealing material forming a cap. In an embodiment variant of the invention the cap is made of the deposited material for enhancement of diffusion to the surface of the wafer at the porous area, but in an another embodiment different material is used, in one variant of the invention above the same-species capping material, but in another embodiment variant directly on the porous wafer surface.

In a further variant of the invention, the capping can be formed of several layers from which one can be formed to pick unwanted impurities of the wafer surface into said layer by the diffusion.

According to an embodiment of the invention the capping layer is made either alone from Si_3N_4 or similar substance, or comprises a sub-layer of Si_3N_4 or a similar substance.

According to an embodiment, in a next step the porous surface is exposed to an annealing phase of in an annealing temperature and environment. A skilled person as such knows how to control the climate for the annealing environment of the processing chamber, to get a pre-defined thermal parameters as such for the process step of an embodiment of the invention. According to an embodiment of the invention the PSG contains P to be diffused into the Si-matrix in the inter-pore volume. According to an embodiment of the invention the temperature is selected to be 1150 °C. According to an embodiment of the invention the annealing is made during 10h annealing period. According to the corresponding variants of the invention, at least the raping up and/or down of the temperature are excluded from the 10 h annealing period.

According to an embodiment of the invention, the treatment temperature is selected to be between 800 °C and 1500 °C, preferably between 900 °C to 1400 °C, more preferably 1000 °C to 1300 °C and even more preferably essentially from 1100 °C to 1200 °C.

In a further process step, after the diffusion enhancement during the annealing and/or ramping to the suitable temperature of oxide (and/or nitrous remaining species) removal by HF-vapor in anhydrous form is performed. The glass remains are etched away, but the diffused substances in the inter-pore volume in the Si-matrix preserve beyond the etching.

According to a variant of the embodiment of the invention, the pores are allowed to act as feeding tunnels into the buried layer surface. Provided that the buried layer has the etch stop layer at the opposite side, the etching could be maintained in the buried layer in a transversal direction to the pore-length wise direction. For this embodiment, the buried layer has to be pre-defined for the material composition that can be etched by the HF for the desired depth. in such embodiment the etching can be stop be an etch stop layer in the buried layer, etching in the transversal direction by a wall of etch stop layer.

In one embodiment the buried layer can be pre-patterned to form cavities underneath the doped structure, when etched, by making etch stop walls to stop the etching to form the cavities into the form according to the form of the etch stop disclosure.

In a further process step in accordance with an embodiment of the invention, the device layer, doped layer of the wafer with the dopant in the inter-pore Si-matrix is exposed to recrystallization in a recrystallization environment. In the recrystallization event the surface Si atoms diffuse to minimize the energy of the system, the device layer gets thinner. The environment can be formed to comprise H_2 and/or Ar in the atmosphere of the processing chamber. According to an embodiment of the invention the temperature is essentially the same as in the diffusion enhancement phase.

According to an embodiment of the invention, the recrystallization temperature is selected to be between 800 °C and 1500 °C, preferably between 900 °C to 1400 °C, more preferably 1000 C to 1300 C and even more preferably essentially from 1100 °C to 1200°C. According to an embodiment of the invention, the recrystallization temperature is being selected to the same as the diffusion enhancement temperature in a previous phase, to allow the atomic structure to be treated in a similar manner.

In a further process step the thinner device layer and the Si-matrix outside the porous area are unequal in thickness. Thus the surface is polished with CMP, until suf-

ficiently smooth surface roughness is gained, in an embodiment example, for example to nm (rms) scale.

According to an embodiment the starting material in the device layer can be chosen to facilitate the etching with e-chem (electro-chemical) etch, or in another embodiment by another etching method.

Pre-selectively situating into the buried layer an etch stop layer as a sub-layer and/or an etch stop wall, the continuation of the etching can be controlled into the desired depth, and/or cavity formation form details with the patterning of the etch stop walls in to the buried layer.

According to an embodiment of the invention a series of dopants one by one can be brought into the device layer by repeating the process in a cyclic manner in which the PSG glass with P dopant is replaced by suitable dopant carrying material.

According to another embodiment of the invention also two or other number of dopants can be doped into the Si-matrix in such a crowd doping at a time, provided that the diffusion coefficients of the crowd doped dopants are closely the same for having uniform dopant concentration. However, presence of several dopants may influence on the device layer properties in mechanical and/or electrical way, which may limit the usability of the products accordingly.

According to an embodiment of the invention the annealing is made in annealing environment in such conditions in which the pressure is in the level of ambient air pressure, but in a variant of embodiments slightly above the ambient pressure, but below 10 bars, advantageously below 5 bars, even more preferably below 2 bars. According to an embodiment of the invention the atmosphere is inert. According to an embodiment of the invention the atmosphere comprises non-inert gaseous species, to be used as washing the surface in one phase of the annealing.

According to an embodiment of the invention the recrystallization is made in recrystallization environment in such conditions in which the pressure is in the level of ambient air pressure, but in a variant of embodiments slightly above the ambient pressure, but below 10 bars, advantageously below 5 bars, even more preferably below 2 bars. According to an embodiment of the invention the atmosphere comprises inert gaseous species. According to an embodiment of the invention the atmosphere comprises non-inert gaseous species, to be used as washing the surface in one phase of the annealing.

According to an alternative embodiment of invention the making of the pores by etching is made as a timer restricted process for such wafers that are used in the embodied process without the etch stop layer.

According to an embodiment of the invention the etching to make the pores is stopped as timed out even before to reach the etch stop layer. According to this embodiment the pore depth can be selected shallower than the distance to the etch stop layer by diffusion length of the dopant. In such a variant of the embodiment, the diffusion length of the embodied dopant is select so that the dopant reaches the structure to be doped down to the end via the pore-bottom parts because of the diffusion of the dopant from the vehicle layer, and/or from the carrier material in the use.

According to an embodiment HF is used as a washing agent, in an anhydrous gaseous form in suitable temperature to wash vehicle remains away, and/or to continue to a cavity etching phase.

The wafers manufactured according to embodiments of the invention can be used in manufacturing highly doped silicon resonators, a resonator material with near zero temperature coefficient of elasticity. In addition embodiments can be used also for MEMS, and/or semiconductor manufacturing, and also for production of such sensors that require a cavity presence in the structure for the sensing purposes.

A skilled person in the art knows many variants of the embodiments as such on the basis of the shown embodiments and examples after reading and understanding them from the specification above. However, these also fall into the scope of the invention limited only by the following claims.

CLAIMS

1. A method of doping wafers, comprising:
   - making at least one ensemble of pores into a wafer matrix to be doped,
   - depositing a vehicle layer on the substrate area of at least one said ensemble of pores and/or their walls, to form a vehicle layer as an interfacing surface for the dopant passage by diffusion,
   - annealing said wafer in annealing specific conditions for enhancement of diffusion of said dopant from said vehicle layer via said interfacing surface into the wafer matrix to be doped,
   - washing the vehicle layer away, by a washing agent for removal of the deposited dopant comprising material from the wafer surface and the pores,
   - recrystallizing, the wafer matrix comprising the dopant, in a recrystallizing environment defined by recrystallizing parameters, and
   - polishing a surface of said wafer on said area of the recrystallized material layer.

2. The doping method of claim 1, wherein the depositing comprises depositing a vehicle layer that comprises at least PSG oxide.

3. The doping method of claim 1 wherein the doping is made for a wafer that is a wafer with at least one buried layer in the wafer matrix.

4. The doping method of claim 3, wherein the washing/etching reaches an etch stop layer in contact with at least one buried layer or being a part of it, the etch stop layer arranged to stop washing and/or etching from the etching direction.

5. The doping method of claim 4, wherein the washing is continued to focused into a buried layer in the wafer matrix for making a cavity under the doped matrix in the wafer, with a washing agent having an agent composition suitable to etch the buried layer but preserve the doped wafer matrix.

6. The doping method of claim 1, wherein said making of pores in said ensemble of pores comprising at least one pore is making such pores that have ensemble of pore-specific quantities as pore characteristic parameters.

7. The doping method of claim 1, wherein the washing further comprises washing away of formed deposits of agents that formed the vehicle layer and/or a cap and/or other remaining agents.

8. The doping method of claim 1 wherein the method comprises making pores in at least one ensemble of pores uniform in respect of at least one parameter belonging to the pore characteristic parameters of the ensemble of pores.

9. The doping method of claim 8, wherein one parameter of said characteristic parameters comprises at least one of the following quantities to be used as a process control parameter: pore diameter, pore depth, other pore dimension, geometric form, volume, surface, surface roughness, surface material, fractal dimension of the pore, a derivative of said aforementioned parameters.

10. The doping method of claim 1, wherein pores in a first sub-ensemble of said ensemble are different than pores in a second sub-ensemble of said ensemble of pores, in respect of at least one ensemble specific quantity.

11. The doping method of claim 1, wherein at least one sub-ensemble of pores is made by means of electrochemical etching.

12. The doping method of claim 1, wherein at least one sub-ensemble of pores is defined lithographically and/or randomly.

13. The doping method of claim 1, wherein defining said annealing specific conditions comprise defining at least one such parameter that is annealing specific parameter, which is at least one of the following:

- annealing temperature
- annealing pressure
- annealing chamber environmental composition
- at least one additional chemical agent
- a combination of the aforementioned parameters, and
- derivative of said aforementioned parameters or an ensemble of such.

14. The doping method of claim 1, wherein a parameter value of an annealing specific condition is selected to enhance diffusion of a dopant substance from the vehicle layer.

15. The doping method of claim 1, wherein said dopant is selected from the group of elements comprising P.

16. The doping method of claim 1, wherein said washing agent comprises HF.

17. The doping method of claim 1, wherein said remaining agents comprise nitrous and/or oxygen containing substances.

18. The doping method of claim 1, wherein defining recrystallizing conditions comprise defining at least one such parameter that is recrystallizing specific parameter, which is at least one of the following:

- recrystallizing temperature,
- recrystallizing pressure,
- recrystallizing chamber atmosphere composition,
- concentration of at least one additional chemical agent,
- concentration component composition of said additional chemical agent,
- a combination of the aforementioned parameters, and
- derivative of said aforementioned parameters or an ensemble of such.

19. The doping method of claim 1, wherein the washing by a washing agent is continued to an etch-stop layer that stops the washing by the selected washing agent in a perpendicular direction to the pore length.

20. The doping method of claim 19, wherein method comprises forming of a cavity between the pores containing layer and the etch-stop layer into a cavity forming layer by the washing agent used in washing for forming cavity in said layer.

21. The doping method of claim 1, wherein the method further comprises bonding a wafer to the doped wafer.

22. The doping method of claim 1, wherein the dopant in the method is a p-type dopant to be doped with a help of a vehicle substance and/or another carrier material suitable to carry the dopant.

23. A wafer manufactured by the doping method according to any claim 1 to 22.

24. A power semiconductor component comprising a semiconductor structure originating to a wafer of claim 23.

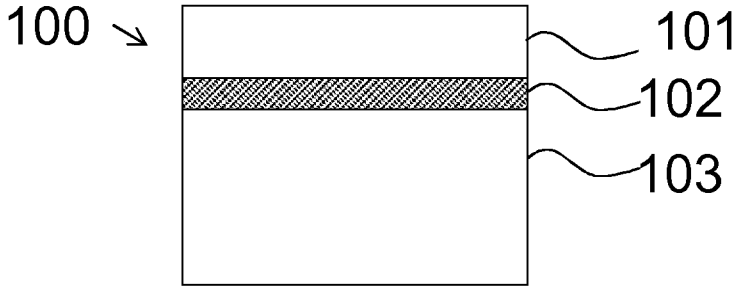

Fig. 1

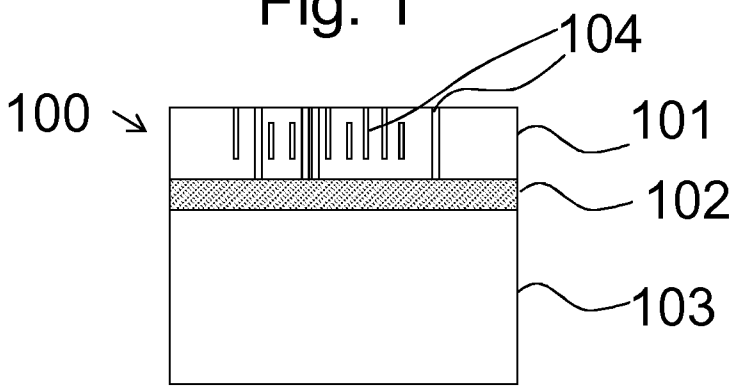

Fig. 2

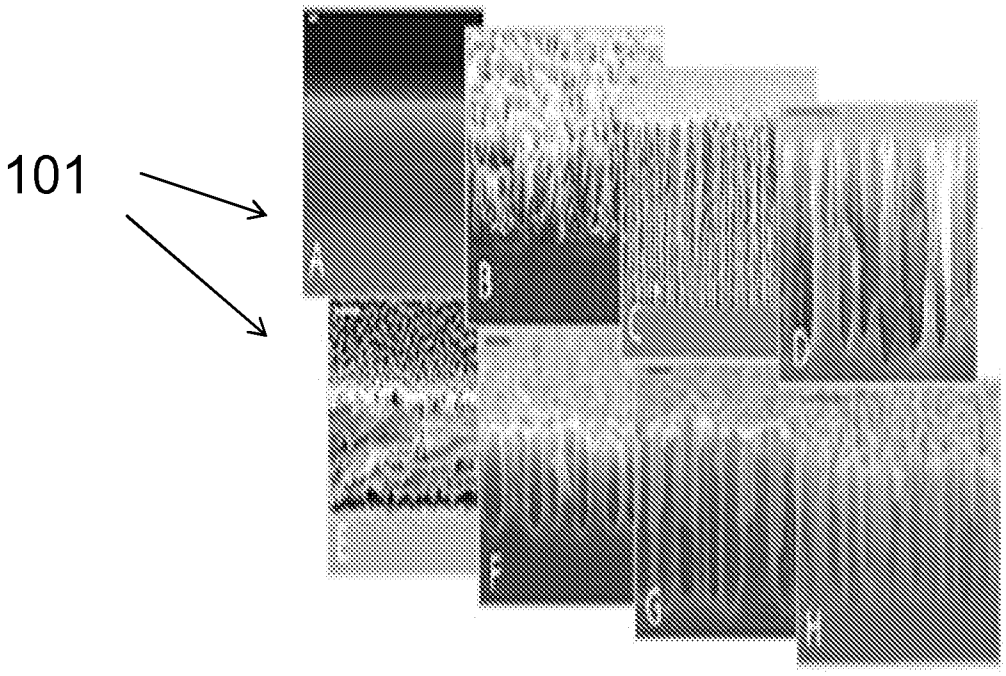

Fig. 3

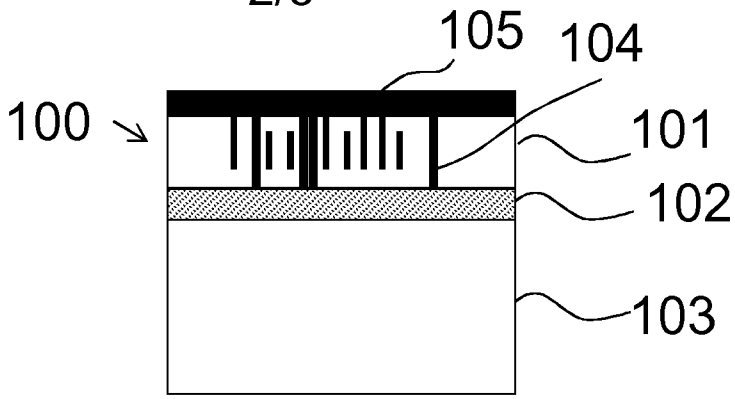

Fig. 4

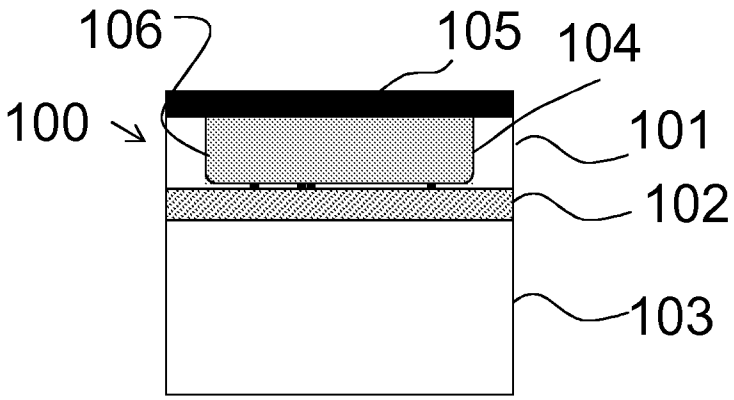

Fig. 5

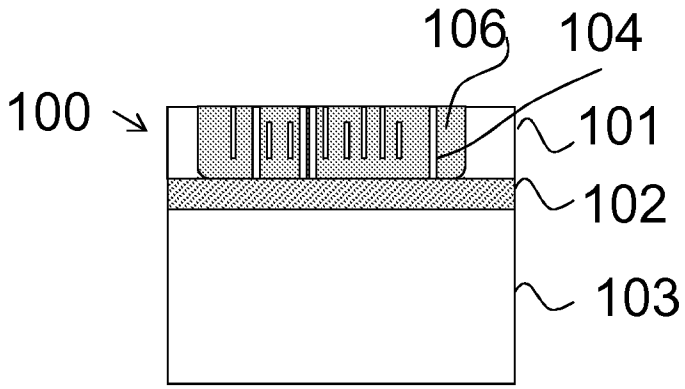

Fig. 6

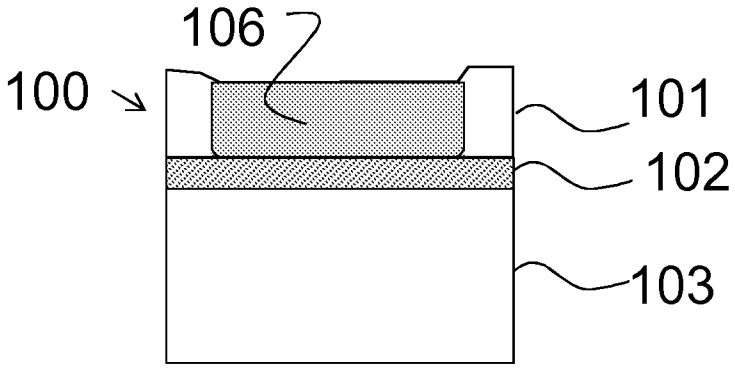

Fig. 7

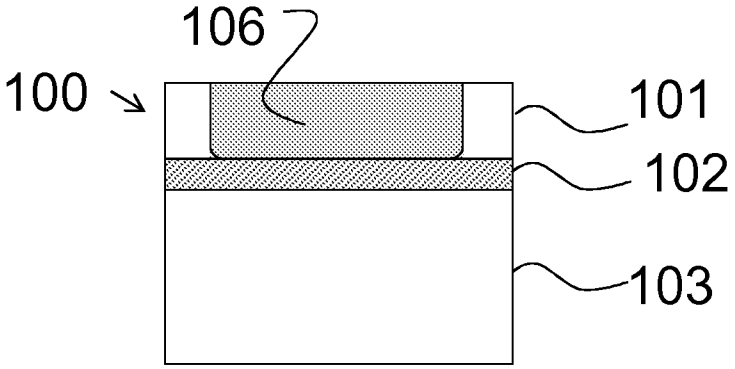

Fig. 8

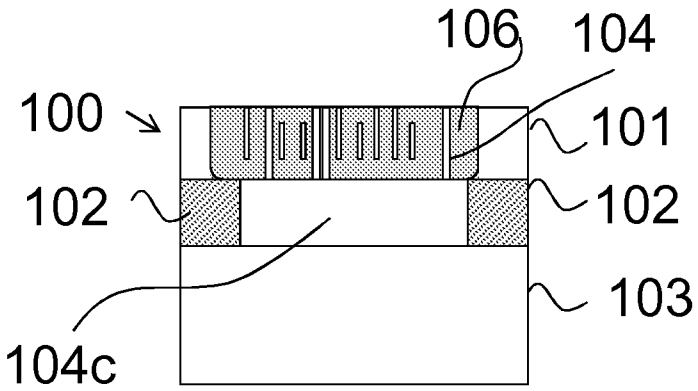

Fig. 6B

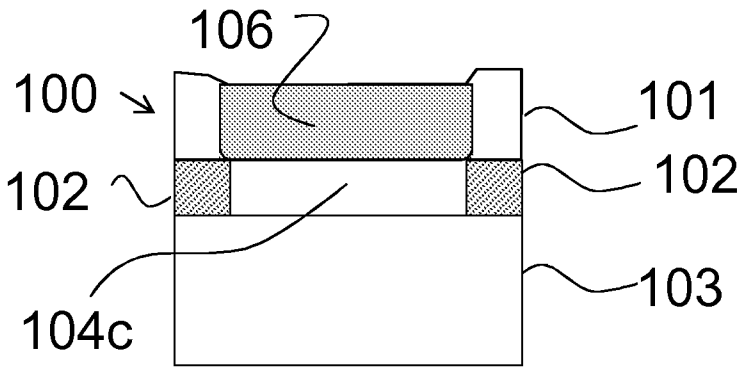

Fig. 7B

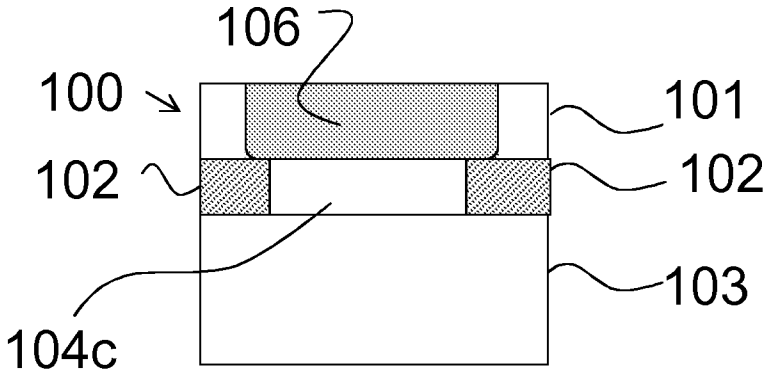

Fig. 8B

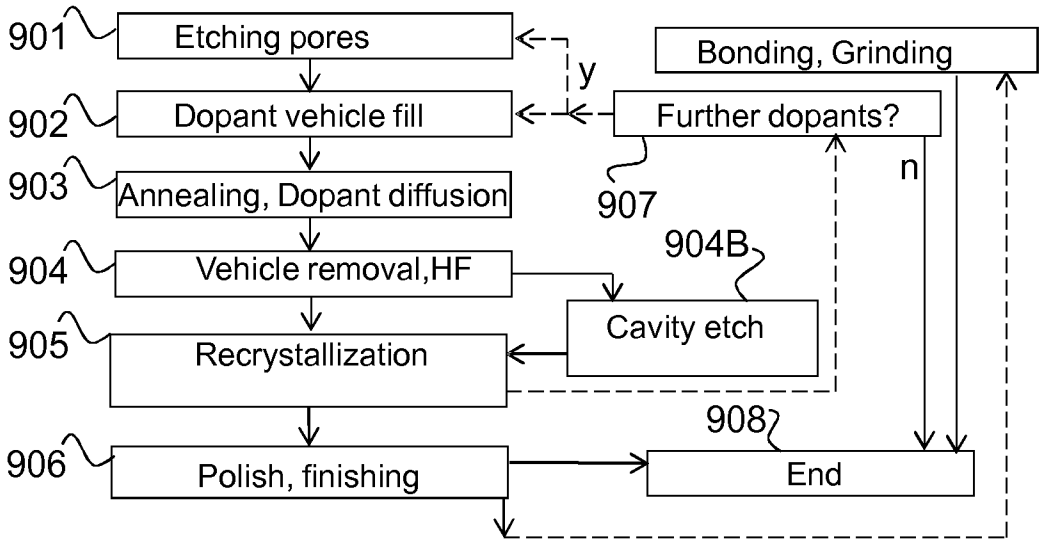

Fig. 9

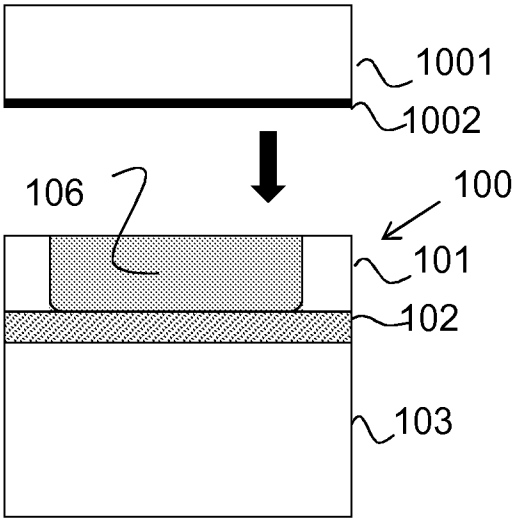

Fig. 10A

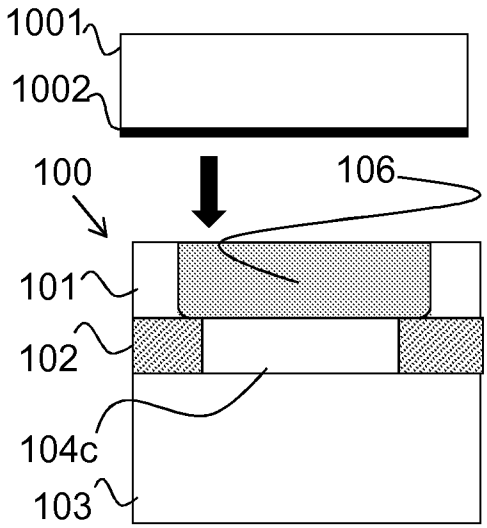

Fig. 10B

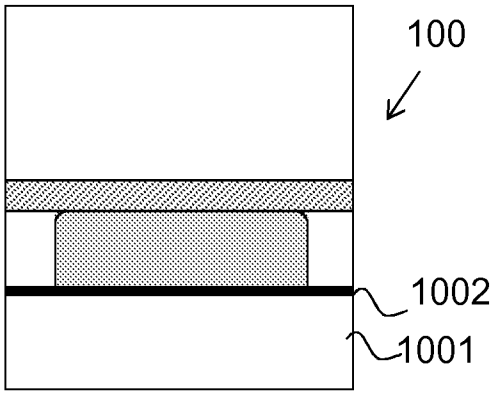

Fig. 11A

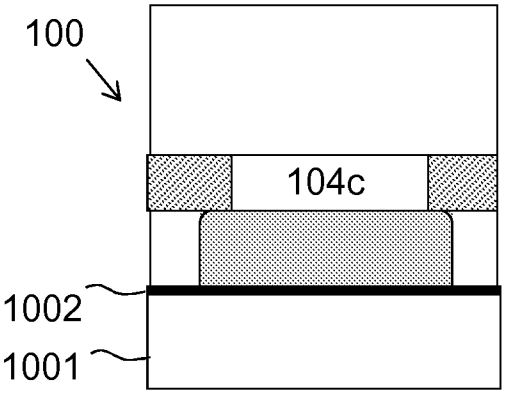

Fig. 11B

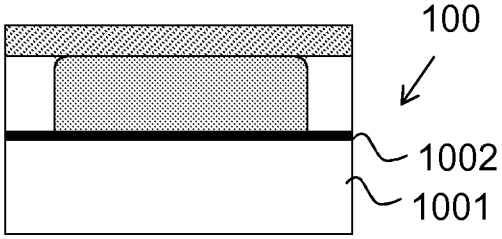

Fig. 12A

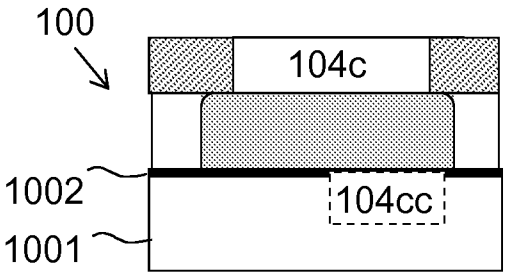

Fig. 12B

INTERNATIONAL SEARCH REPORT

International application No
PCT/FI2015/050929

A. CLASSIFICATION OF SUBJECT MATTER
INV. B81C1/00 H01L21/225
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B81C H01L B81B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	RINKE T J ET AL: "QUASI-MONOCRYSTALLINE SILICON FOR THIN-FILM DEVICES", APPLIED PHYSICS A: MATERIALS SCIENCE & PROCESSING, SPRINGER INTERNATIONAL, DE, vol. A68, 1 June 1999 (1999-06-01), pages 705-707, XP000937408, ISSN: 0947-8396, DOI: 10.1007/S003390050964	23,24
A	figure 2 section "1 Experimental" section "2 Results and discussion"	1-22

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 May 2016	27/05/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Meister, Martin

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/FI2015/050929

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EL-BAHAR A ET AL: "N-type porous silicon doping using phosphorous oxychloride (POCl 3)", IEEE ELECTRON DEVICE LETTERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 21, no. 9, 1 September 2000 (2000-09-01), pages 436-438, XP011430519, ISSN: 0741-3106, DOI: 10.1109/55.863102 page 426	1-22
A	DE 196 51 772 A1 (SAMSUNG DISPLAY DEVICES CO LTD [KR]) 3 July 1997 (1997-07-03) the whole document	1-24

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/FI2015/050929

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 19651772 A1	03-07-1997	DE 19651772 A1	03-07-1997
		GB 2308918 A	09-07-1997
		JP H09191127 A	22-07-1997
		US 5908303 A	01-06-1999