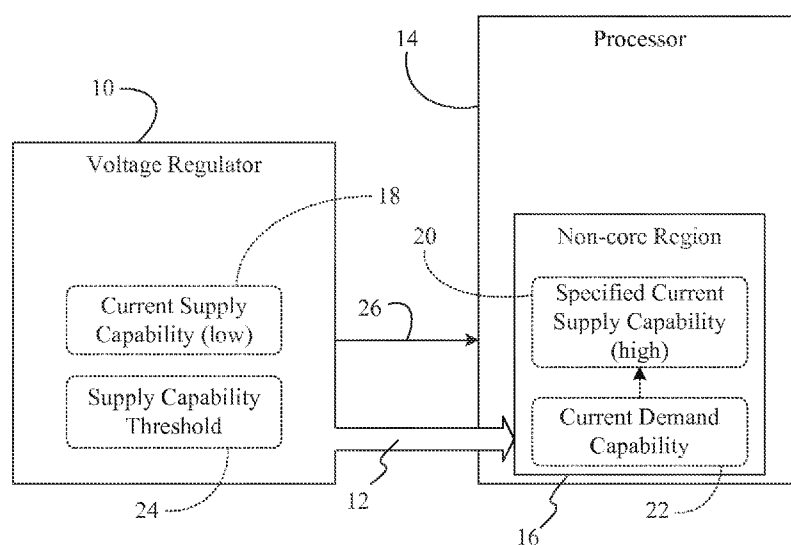




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- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
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(54) **Title:** MAXIMUM CURRENT THROTTLING

(57) **Abstract:** Systems and methods may provide for monitoring a current provided from a voltage regulator to a non-core region of a processor, and asserting a throttle signal to the non-core region of the processor if the current exceeds a supply capability threshold of the voltage regulator. In one example, a specified current supply capability of the non-core region is greater than a current supply capability of the voltage regulator, and the supply capability threshold is less than the specified current supply capability of the non-core region and an over current protection threshold of the non-core region.

MAXIMUM CURRENT THROTTLING

BACKGROUND

Technical Field

Embodiments generally relate to power management in computing platforms.
5 More particularly, embodiments relate to the selective throttling of non-core processor regions based on voltage regulator current levels.

Discussion

As computing platforms become smaller and more lightweight, a number of power management concerns may be encountered. For example, the ability to reduce platform
10 size can be limited by the size of the voltage regulator (VR) components that provide power to the various processors and other circuits of the platform. Moreover, VR component size may be a function of a specified maximum amount of current (e.g., I_{ccmax}) that VRs are expected to be capable of supplying. While computing platforms could be designed to have VRs with a current supplying capability that is less than the specified
15 amount, such an approach may increase the risk of VR shutdown or lifetime degradation. Indeed, downsizing VRs that supply non-core processor regions of the platform may be particularly problematic given a traditional lack of protection mechanisms in those regions.

BRIEF DESCRIPTION OF THE DRAWINGS

20 The various advantages of the embodiments of the present invention will become apparent to one skilled in the art by reading the following specification and appended claims, and by referencing the following drawings, in which:

FIG. 1 is a block diagram of an example of a throttling scheme according to an embodiment;

25 FIG. 2 is a flowchart of an example of a method of throttling a non-core region of a processor according to an embodiment; and

FIG. 3 is a block diagram of an example of a computing platform according to an embodiment.

DETAILED DESCRIPTION

30 Embodiments may include an apparatus having circuitry to monitor a current provided from a voltage regulator to logic of a processor. The circuitry may also assert a throttle signal to the logic of the processor if the current exceeds a supply capability threshold associated with the voltage regulator.

Embodiments may also include a non-transitory computer readable storage medium having a set of instructions which, if executed by a device, cause the device to monitor a current provided from a voltage regulator to logic of a processor. The instructions, if executed, may also cause the device to assert a throttle signal to the logic of the processor if the current exceeds a supply capability threshold associated with the voltage regulator.

Other embodiments may include a computer implemented method in which a current provided from a voltage regulator to logic of a processor is monitored. The method may also provide for asserting a throttle signal to the logic of the processor if the current exceeds a supply capability threshold associated with the voltage regulator.

Additionally, embodiments may include a system having a voltage regulator with an associated supply capability threshold, and a processor having logic coupled to the voltage regulator. The system can also include circuitry to monitor a current provided from the voltage regulator to the logic of the processor, and assert a throttle signal to the logic of the processor if the current exceeds the supply capability threshold associated with the voltage regulator, wherein the logic is to reduce a workload of the logic in response to the throttle signal.

Turning now to FIG. 1, a voltage regulator 10 is shown, wherein the voltage regulator 10 provides a power plane 12 (e.g., V_{cc}) to logic such as a non-core region 16 of a processor 14. The processor 14 may be, for example, a central processing unit (CPU), input output (IO) controller, memory controller, display controller, and so forth, of a computing platform, wherein the illustrated non-core region 16 (e.g., “un-core”) represents the elements in the processor 14 that are not used for computational tasks. As will be discussed in greater detail, the voltage regulator 10 may be sized to facilitate deployment of the voltage regulator 10 in a relatively small computing platform such as an “Ultrabook” computing system or other mobile device having a thin and/or small form factor. For example, relatively low rated inductors, FETs (field effect transistors) and other components may be used to construct the voltage regulator 10. The small size of the voltage regulator 10 may result in the voltage regulator 10 having an associated maximum current supply capability 18 (e.g., I_{ccmax_vr}) that is less than a maximum current supply capability 20 specified for the non-core region 16 (e.g., I_{ccmax}). In other words, the specified current supply capability 20, which may be a function of a current demand

capability 22 of the non-core region 16, exceeds the current supply capability 18 of the voltage regulator 10, in the example shown.

In order to obviate any concerns over shutdown or lifetime degradation due to such a supply capability mismatch, the illustrated voltage regulator 10 monitors the current/power provided from the voltage regulator 10 to the non-core region 16 (e.g., low side and/or high side FET current), and asserts a throttle signal 26 (e.g., $I_{ccmax_throttle}$) to the non-core region 16 if the current exceeds a supply capability threshold 24 associated with the voltage regulator 10. Assertion of the throttle signal 26 may be done very quickly (e.g., less than one micro-second). The supply capability threshold 24 may be less than the specified current supply capability 20 of the non-core region 16 as well as less than the current supply capability 18 of the voltage regulator 10. The supply capability threshold 24 may also be less than an over current protection (OCP) threshold (not shown) of the non-core region 16, wherein the gap between the supply capability threshold 24 and the OCP threshold may be selected based on the throttling response time of the non-core region 44.

In response to receiving the throttle signal 26, the non-core region 16 may reduce its internal workload, which can in turn reduce the current demand placed on the voltage regulator 10 by the non-core region 16. Thus, the illustrated throttle signal 26 enables the voltage regulator 10 to be downsized without risking shutdown or lifetime degradation. The throttle signal 26 may be provided either directly to the non-core region 16 (e.g., via a dedicated pin) or indirectly to the non-core region 16 via the processor 14, which may in turn control the workload of the non-core region 16.

FIG. 2 shows a method 28 of throttling a non-core region of a processor. The method 28 may be implemented as a set of logic instructions stored in a machine- or computer-readable storage medium such as random access memory (RAM), read only memory (ROM), programmable ROM (PROM), firmware, flash memory, etc., in configurable logic such as, for example, programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs), in fixed-functionality logic hardware using circuit technology such as, for example, application specific integrated circuit (ASIC), complementary metal oxide semiconductor (CMOS) or transistor-transistor logic (TTL) technology, or any combination thereof.

Illustrated processing block 30 provides for initializing a system having a voltage regulator that supplies power to a non-core region of a processor. The initialization

process may involve determining and/or setting a supply capability threshold of the voltage regulator (e.g., via accessing a register, memory location, etc.). In one example, the supply capability threshold is less than a specified current supply capability of non-core region, wherein the specified current supply capability of the non-core region is greater than a current supply capability of the voltage regulator. Block 30 may also provide for monitoring the current and/or power supplied by the voltage regulator to the non-core region. If it is determined at block 32 that the current exceeds the supply capability threshold, a throttle signal can be asserted to the non-core region at block 34 and the illustrated loop repeats. As already noted, the throttle signal may cause a reduction of the workload of the non-core region, which in turn may result in a reduction in the current demand placed on the voltage regulator by the non-core region.

If, on the other hand, the supply capability threshold is not exceeded, a determination may be made at block 36 as to whether a predetermined period of time (e.g., a “debouncing period”) has expired. The debouncing period may be used to reduce the likelihood of fluctuations and associated adjustments occurring around supply capability threshold. If the debouncing period has expired, illustrated block 38 de-asserts the throttle signal and the current monitoring continues.

Turning now to FIG. 3 a platform 40 is shown, wherein the platform 40 may be part of a device having computing functionality (e.g., personal digital assistant/PDA, laptop, smart tablet), communications functionality (e.g., wireless smart phone), imaging functionality, media playing functionality (e.g., smart television/TV), or any combination thereof (e.g., mobile Internet device/MID). In the illustrated example, a processor 42 has a non-core region 44 and a core region 46. The non-core region 44 may include, for example an integrated memory controller 52 that facilitates communication between the processor 42 and system memory 54, wherein the system memory 54 could include, for example, double data rate (DDR) synchronous dynamic random access memory (SDRAM, e.g., DDR3 SDRAM JEDEC Standard JESD79-3C, April 2008) modules. The modules of the system memory 76 may be incorporated into a single inline memory module (SIMM), dual inline memory module (DIMM), small outline DIMM (SODIMM), and so forth. Thus, the illustrated non-core region 44 does not perform computational operations. The core region 46, on the other hand, may have full computational functionality with instruction fetch units, instruction decoders, level one (L1) cache, execution units, and so forth.

In the illustrated example, the non-core region 44 receives power from a voltage regulator (VR) 48 and the core region 46 receives power from a different VR 50, wherein the VRs 48, 50 convert supply voltages received from a power supply 56 to voltages used by the respective circuits supported by the VRs 48, 50. The computing platform 40 may also include an input output (IO) module 58, network controller 60, display controller 62, solid state disk (SSD) 64, etc., to support off-platform communications, facilitate information storage, and enable the visual output of information. The IO module 58, network controller 60, display controller 62, and SSD 64, may also have non-core regions that receive power from platform VRs.

The VR 48 that supplies the non-core region 44 may have a current supply capability that is less than a specified current supply capability of the non-core region 44. Accordingly, the illustrated VR 48 has logic 66 configured to selectively assert a throttle signal to the non-core region 44 based on whether the current supplied to the non-core region 44 exceeds a supply capability threshold of the VR 48. In one example, the supply capability threshold is set to a value that is less than the specified current supply capability of the non-core region 44 in order to prevent shutdown and/or damage in the VR 48 during operation. The supply capability threshold may also be less than an over current protection threshold associated with the non-core region 44 to provide additional protection to the non-core region 44.

Techniques described herein may therefore use reduced I_{ccmax} design points for VRs to enable integration of the VRs with smaller components, lower cost, and higher efficiency. Closed loop detection and protection mechanisms can enable safe downsizing of non-core VRs on a platform having tight space requirements.

Embodiments of the present invention are applicable for use with all types of semiconductor integrated circuit ("IC") chips. Examples of these IC chips include but are not limited to processors, controllers, chipset components, programmable logic arrays (PLAs), memory chips, network chips, systems on chip (SoCs), SSD/NAND controller ASICs, and the like. In addition, in some of the drawings, signal conductor lines are represented with lines. Some may be different, to indicate more constituent signal paths, have a number label, to indicate a number of constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. This, however, should not be construed in a limiting manner. Rather, such added detail may be used in connection with one or more exemplary embodiments to facilitate easier understanding of

a circuit. Any represented signal lines, whether or not having additional information, may actually comprise one or more signals that may travel in multiple directions and may be implemented with any suitable type of signal scheme, e.g., digital or analog lines implemented with differential pairs, optical fiber lines, and/or single-ended lines.

5 Example sizes/models/values/ranges may have been given, although embodiments of the present invention are not limited to the same. As manufacturing techniques (e.g., photolithography) mature over time, it is expected that devices of smaller size could be manufactured. In addition, well known power/ground connections to IC chips and other components may or may not be shown within the figures, for simplicity of illustration and
10 discussion, and so as not to obscure certain aspects of the embodiments of the invention. Further, arrangements may be shown in block diagram form in order to avoid obscuring embodiments of the invention, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the embodiment is to be implemented, i.e., such specifics should be
15 well within purview of one skilled in the art. Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the invention, it should be apparent to one skilled in the art that embodiments of the invention can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

20 The term “coupled” may be used herein to refer to any type of relationship, direct or indirect, between the components in question, and may apply to electrical, mechanical, fluid, optical, electromagnetic, electromechanical or other connections. In addition, the terms “first”, “second”, etc. are used herein only to facilitate discussion, and carry no particular temporal or chronological significance unless otherwise indicated. Moreover,
25 any use of the terms “first”, “second”, etc., does not limit the embodiments discussed to the number of components listed.

 Those skilled in the art will appreciate from the foregoing description that the broad techniques of the embodiments of the present invention can be implemented in a variety of forms. Therefore, while the embodiments of this invention have been described
30 in connection with particular examples thereof, the true scope of the embodiments of the invention should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, specification, and following claims.

CLAIMS

We claim:

1. A system comprising:
a voltage regulator having a supply capability threshold;
5 a processor including a non-core region coupled to the voltage regulator; and
logic to,
monitor a current provided from the voltage regulator to the non-core
region of the processor, and
assert a throttle signal to the non-core region of the processor if the current
10 exceeds the supply capability threshold of the voltage regulator, wherein the non-
core region is to reduce a workload of the non-core region in response to the
throttle signal.
2. The system of claim 1, wherein the non-core region has a specified current
supply capability that is greater than a current supply capability of the voltage regulator,
15 and wherein the supply capability threshold is less than the specified current supply
capability of the non-core region.
3. The system of claim 1, wherein the logic is to de-assert the throttle signal if
the current does not exceed the supply capability threshold for a predetermined period of
time.
- 20 4. The system of claim 1, wherein the non-core region has an associated over
current protection threshold and the supply capability threshold is less than the over
current protection threshold.
5. The system of claim 1, wherein the processor includes an input output (IO)
controller.
- 25 6. The system of claim 1, wherein the processor includes a memory controller.
7. The system of claim 1, wherein the processor includes a display controller.
8. An apparatus comprising:
logic to,
monitor a current provided from a voltage regulator to a non-core region of
30 a processor, and
assert a throttle signal to the non-core region of the processor if the current
exceeds a supply capability threshold of the voltage regulator.

9. The apparatus of claim 8, wherein a specified current supply capability of the non-core region is to be greater than a current supply capability of the voltage regulator, and wherein the supply capability threshold is to be less than the specified current supply capability of the non-core region.

5 10. The apparatus of claim 8, wherein the logic is to de-assert the throttle signal if the current does not exceed the supply capability threshold for a predetermined period of time.

11. The apparatus of claim 8, wherein the supply capability threshold is to be less than an over current protection threshold associated with the non-core region of the
10 processor.

12. The apparatus of claim 8, wherein the throttle signal is to be asserted to an input output (IO) controller.

13. The apparatus of claim 8, wherein the throttle signal is to be asserted to a memory controller.

15 14. The apparatus of claim 8, wherein the throttle signal is to be asserted to a display controller.

15. A non-transitory computer readable storage medium comprising a set of instructions which, if executed by a device, cause the device to:

20 monitor a current provided from a voltage regulator to a non-core region of a processor; and

assert a throttle signal to the non-core region of the processor if the current exceeds a supply capability threshold of the voltage regulator.

16. The medium of claim 15, wherein a specified current supply capability of the non-core region is to be greater than a current supply capability of the voltage
25 regulator, and wherein the supply capability threshold is to be less than the specified current supply capability of the non-core region.

17. The medium of claim 15, wherein the instructions, if executed, cause a device to de-assert the throttle signal if the current does not exceed the supply capability threshold for a predetermined period of time.

30 18. The medium of claim 15, wherein the supply capability threshold is to be less than an over current protection threshold associated with the non-core region of the processor.

19. The medium of claim 15, wherein the throttle signal is to be asserted to an input output (IO) controller.

20. The medium of claim 15, wherein the throttle signal is to be asserted to a memory controller.

5 21. The medium of claim 15, wherein the throttle signal is to be asserted to a display controller.

22. A computer implemented method comprising:

monitoring a current provided from a voltage regulator to a non-core region of a processor; and

10 asserting a throttle signal to the non-core region of the processor if the current exceeds a supply capability threshold of the voltage regulator.

23. The method of claim 22, wherein a specified current supply capability of the non-core region is greater than a current supply capability of the voltage regulator, and wherein the supply capability threshold is less than the specified current supply capability
15 of the non-core region.

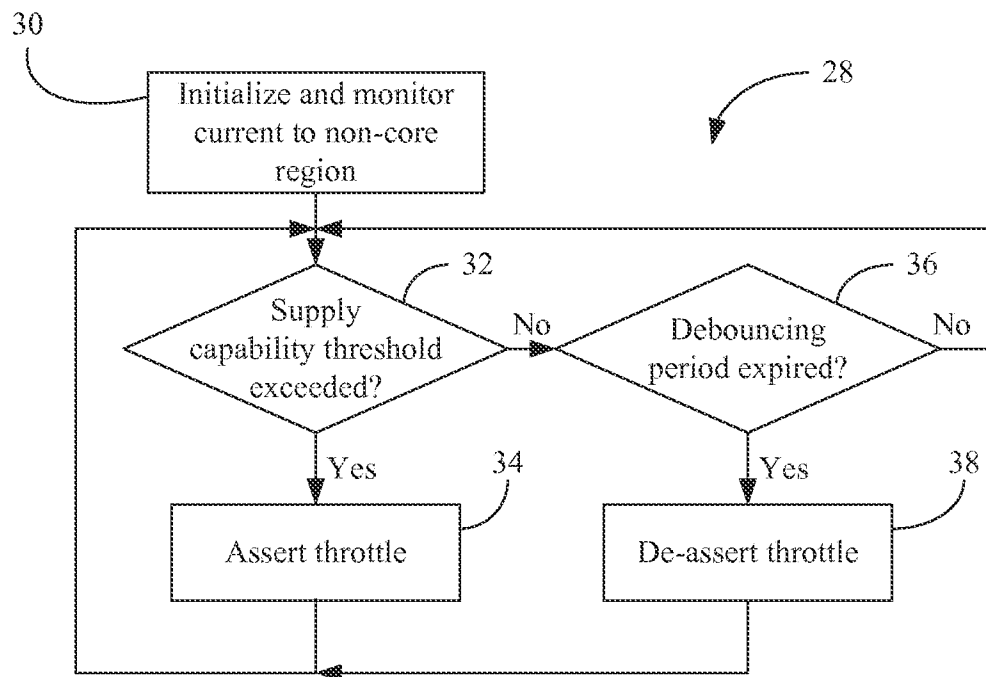
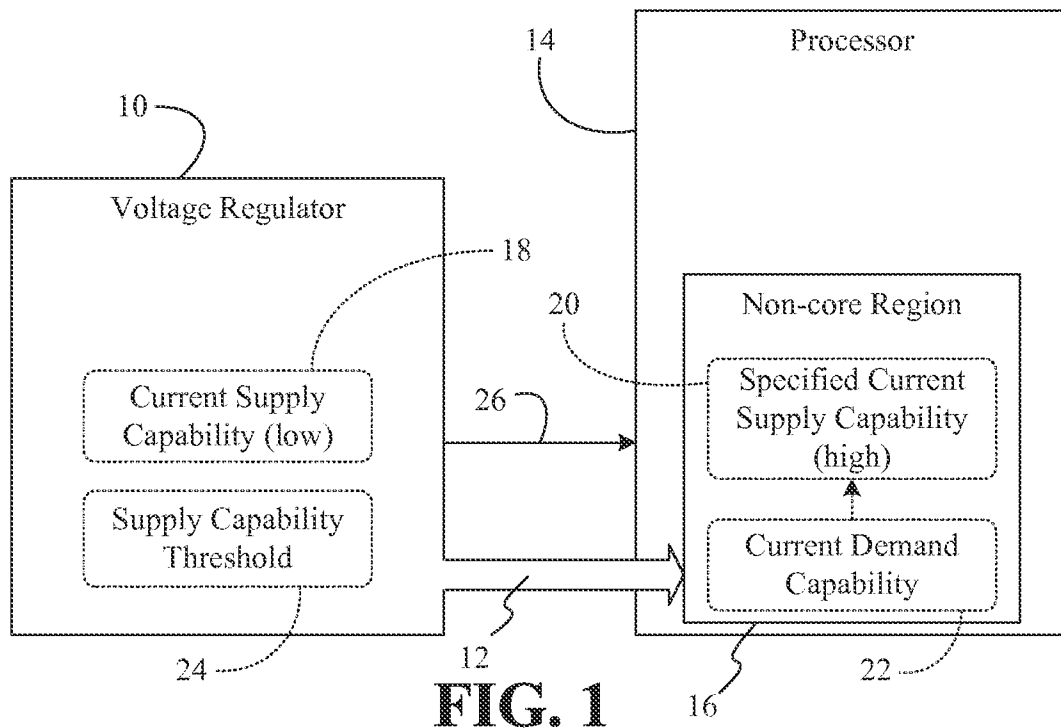
24. The method of claim 22, further including de-asserting the throttle signal if the current does not exceed the supply capability threshold for a predetermined period of time.

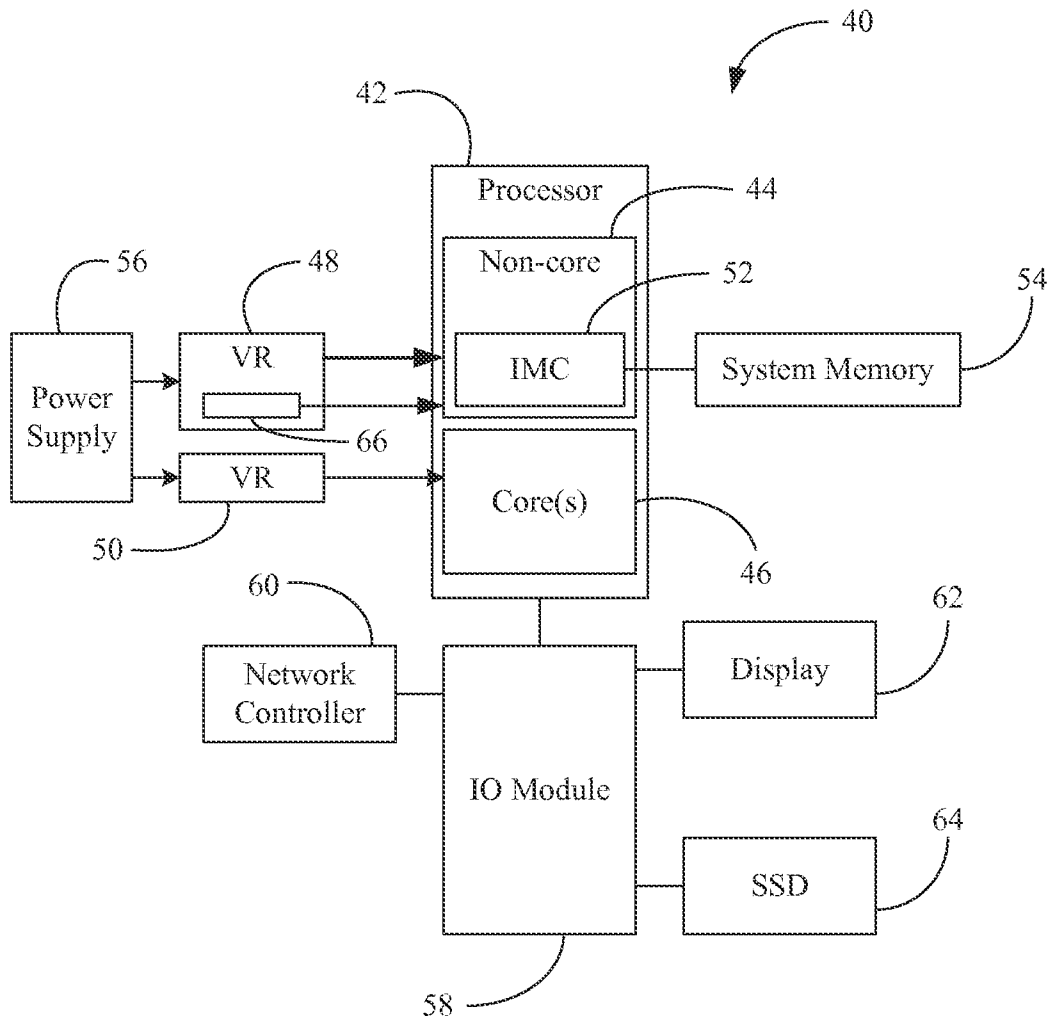
25. The method of claim 22, wherein the supply capability threshold is to be
20 less than an over current protection threshold associated with the non-core region of the processor.

26. The method of claim 22, wherein the throttle signal is asserted to an input output (IO) controller.

27. The method of claim 22, wherein the throttle signal is asserted to a memory
25 controller.

28. The method of claim 22, wherein the throttle signal is asserted to a display controller.

**FIG. 2**

**FIG. 3**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/047889**A. CLASSIFICATION OF SUBJECT MATTER****G06F 1/26(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/26; H04L 27/00; G06F 1/32; H04B 1/38; H02J 3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: processor, voltage, regulator, threshold, non-core, throttle, signal, current

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	KR 10-2005-0016645 A (INTEL CORP.) 21 February 2005 See page 2, line 20 - page 3, line 50; and figs. 1-4.	1-28



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

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08 October 2013 (08.10.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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