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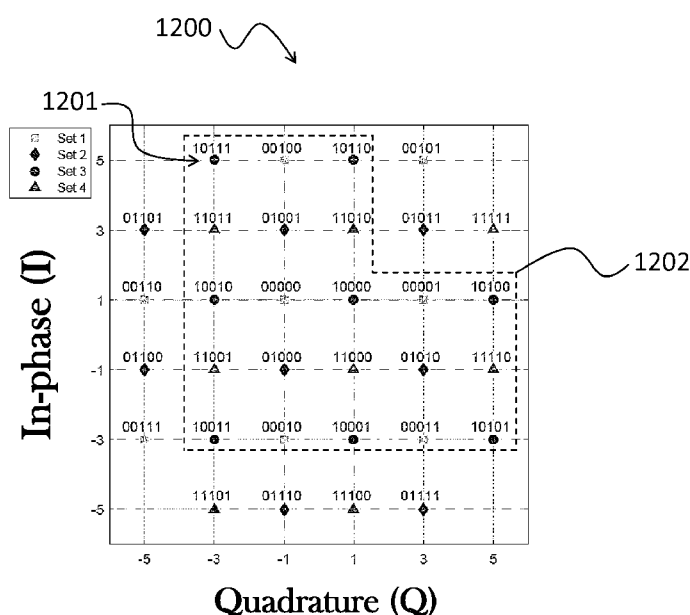


Fig. 12

(57) Abstract: The present invention provides a transmitter (200) for Delayed Bit-Interleaved Code Modulation, DBICM. The transmitter comprises a bit delay module (201) and a modulation module (202). The bit delay module (201) is configured to receive a plurality of parallel bit streams (203), delay at least one bit stream (204) of the parallel bit streams (203) to generate a plurality of realigned parallel bit streams (205), and provide the realigned parallel bit streams (205) to the modulation module (202). The modulation module (202) is configured to map the realigned parallel bit streams (205) to complex symbols (206), the complex symbols (206) corresponding to constellation points in a complex plane.

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TRANSMITTER AND RECEIVER FOR DELAYED BIT-INTERLEAVED CODE MODULATION

TECHNICAL FIELD

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The present invention relates to the field of coding and modulation schemes, in particular to Delayed Bit-Interleaved Code Modulation (DBICM). Specifically, the transmitter and receiver according to the present invention allow for improved mapping of complex symbols to constellation points by applying DBICM.

10

BACKGROUND

Bit-Interleaved Coded Modulation (BICM), as e.g. known from E. Zehavi, “8-PSK trellis codes for a Rayleigh channel”, in *IEEE Transactions on Communications*, vol. 40, no. 5, pp. 873-884, May 1992, or from G. Caire, G. Taricco and E. Biglieri, “Bit-interleaved coded modulation”, in *IEEE Transactions on Information Theory*, vol. 44, no. 3, pp. 927-946, May 1998, is a coding and modulation scheme, in which a bit-level interleaver is inserted between a channel encoder and a modulator. Since this approach of choosing three independent modules provides flexibility when designing a communication system, BICM has become a dominant coding and modulation scheme in communication systems of the prior art. Another prior art coding and modulation scheme, which was recently proposed in H. Ma, W. K. Leung, X. Yan, K. Law and M. Fossorier, “Delayed Bit Interleaved Coded Modulation”, in *Proceedings of 2016 9th International Symposium on Turbo Codes & Iterative Information Processing*, Brest, 2016, is conventional DBICM, which combines features from BICM and from multi-level coding (MLC), which is known from U. Wachsmann, R. F. H. Fischer and J. B. Huber, “Multilevel codes: theoretical concepts and practical design rules”, in *IEEE Transactions on Information Theory*, vol. 45, no. 5, pp. 1361-1391, July 1999.

As it is illustrated in Fig. 1, the main idea of a conventional DBICM scheme 100 is to delay a transmission of portions of information, so that consecutive transmission blocks 101, 102 comprise information coming from different forward error correction (FEC) codewords. In Fig. 1, this is illustrated e.g. in transmission block 101, which comprises information A from a first FEC code word, and which also comprises information B from a second FEC code word. In Fig. 1, the three rows labeled with b_0 , b_1 , b_2 , relate to the different portions (i.e. streams) of transmitted information, of which portion b_0 is delayed. In an 8-point constellation case,

conventional DBICM, as e.g. described in view of Fig. 1, offers significantly more performance than BICM. The 8-point constellation case thereby is as it is applied in quadrature amplitude modulation (QAM), a modulation scheme widely used in communication systems. In the field of QAM, 8-QAM relates to QAM which is associated with an 8-point constellation case, 16-QAM is associated with a 16-point constellation case and 32-QAM is associated with a 32-point constellation case, and so on.

In a communication system, which is based on conventional DBICM, labeling of constellation points, i.e. the way in which constellation points are derived from the transmission blocks 101, 102 as e.g. described in view of Fig. 1, has a significant impact on performance of the communication system, since the labelled constellation points correspond to complex symbols which are to be transmitted by the communication system. In order to achieve a desired performance of a communication system which is based on conventional DBICM, a structure in which portions of information are delayed to form transmission blocks, and a way according to which constellation points are labelled based on the transmission blocks need to be carefully designed. In an 8-point constellation case, it is possible to determine an appropriate combination of delay structure and labelling of constellation points by a brute-force approach, according to which all possible combinations are evaluated. However, for higher-order constellation cases, such as a 32-point constellation case, such a brute-force search is infeasible.

As a result, in the prior art there is a lack of a delay structure and a structure of labelling constellation points in a 32-point constellation case when using conventional DBICM.

SUMMARY

In view of the above-mentioned problems and disadvantages, the present invention aims to improve the conventional schemes and systems. The present invention thereby has the object to provide a transmitter, receiver and transceiver, in which an optimal combination of delay structure and labelling of constellation points is applied. This in particular allows for providing a communication system comprising the transmitter and the receiver according to the present invention, which facilitates higher performance, more efficient use of resources as well as more reliable transmission of information.

The object of the present invention is achieved by the solution provided in the enclosed independent claims. Advantageous implementations of the present inventions are further defined in the dependent claims.

- 5 In particular, the present invention proposes a solution that uses a mapping relationship between bits (which correspond to the transmission blocks 101, 102) and complex symbols I and Q (which correspond to labeled constellation points in a complex plane) in order to achieve optimal results of DBICM.
- 10 A first aspect of the present invention provides a transmitter for Delayed Bit-Interleaved Code Modulation, DBICM, comprising a bit delay module and a modulation module, wherein the bit delay module is configured to receive a plurality of parallel bit streams, delay at least one bit stream of the parallel bit streams to generate a plurality of realigned parallel bit streams, and provide the realigned parallel bit streams to the modulation module, wherein the modulation
- 15 module is configured to map the realigned parallel bit streams to complex symbols, the complex symbols corresponding to constellation points in a complex plane.

The transmitter of the first aspect uses a bit delay module to delay proportions of received bit streams, and a modulation module to map the delayed bit streams, which are partially delayed by

20 the delay module, to complex symbols. Since the complex symbols correspond to constellation points in a complex plane, the mapping of the delayed bit streams to the complex symbols corresponds to labelling of constellation points. The transmitter according to the first aspect advantageously allows precisely adjusting the manner according to which a portion of the parallel bit streams is delayed, and the manner according to which the delayed bit streams are

25 mapped to the complex symbols. As the complex symbols correspond to constellation points in a complex plane, the transmitter according to the first aspect allows efficiently labelling constellation points, even in higher-order constellation cases, such as 32-QAM. Further, the transmitter ensures that information can be transmitted with higher efficiency, and improved reliability and performance.

30 In a first implementation form of the transmitter according to the first aspect, the plurality of parallel bit streams can comprise five parallel bit streams, and the bit delay module can further be configured to delay two of the five parallel bit streams to generate the realigned parallel bit streams.

35

This ensures that delaying the parallel bit streams in the delay module can be performed according to an operating principle, which maximizes efficiency, reliability and performance of transmission.

5 In a second implementation form of the transmitter according to the first aspect as such or according to the first implementation form of the first aspect, the bit delay module can further be configured to delay each of the two bit streams by one time block to generate the realigned parallel bit streams.

10 Delaying each of the two bit streams by one time block each facilitates transmission with higher efficiency, reliability and performance.

In a third implementation form of the transmitter according to the first aspect as such or according to any previous implementation form of the first aspect, the constellation points are
15 constellation points according to 32-QAM.

This ensures that the modulation module of the transmitter according to the first aspect can map the realigned parallel bit streams to complex symbols in 32-point constellation cases according to 32-QAM.

20 In a fourth implementation form of the method according to the second aspect as such or according to any previous implementation form of the second aspect, the constellation points can comprise four groups of eight constellation points each.

25 This ensures that regularities in the constellation points can be exploited, in order to improve efficiency and performance of coding and modulating.

In a fifth implementation form of the transmitter according to the first aspect as such or according to any of the previous implementation forms of the first aspect, the realigned parallel
30 bit streams can be labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , and the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q , and the modulation module can be configured to map parallel bits of the realigned parallel bit streams to the complex symbols according to the following mapping relationship:

b₀	b₁	b₂	b₃	b₄	s_I	s_Q
A₀	A₁	0	0	0	-1	1
A₀	A₁	0	0	1	3	1
A₀	A₁	0	1	0	-1	-3
A₀	A₁	0	1	1	3	-3
A₀	A₁	1	0	0	-1	5
A₀	A₁	1	0	1	3	5
A₀	A₁	1	1	0	-5	1
A₀	A₁	1	1	1	-5	-3
B₀	B₁	0	0	0	-1	-1
B₀	B₁	0	0	1	-1	3
B₀	B₁	0	1	0	3	-1
B₀	B₁	0	1	1	3	3
B₀	B₁	1	0	0	-5	-1
B₀	B₁	1	0	1	-5	3
B₀	B₁	1	1	0	-1	-5
B₀	B₁	1	1	1	3	-5
C₀	C₁	0	0	0	1	1
C₀	C₁	0	0	1	1	-3
C₀	C₁	0	1	0	-3	1
C₀	C₁	0	1	1	-3	-3
C₀	C₁	1	0	0	5	1
C₀	C₁	1	0	1	5	-3
C₀	C₁	1	1	0	1	5
C₀	C₁	1	1	1	-3	5
D₀	D₁	0	0	0	1	-1
D₀	D₁	0	0	1	-3	-1
D₀	D₁	0	1	0	1	3
D₀	D₁	0	1	1	-3	3
D₀	D₁	1	0	0	1	-5
D₀	D₁	1	0	1	-3	-5
D₀	D₁	1	1	0	5	-1
D₀	D₁	1	1	1	5	3

wherein

- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
5 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
10 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
15 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
20 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
25 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$.

This ensures that the transmitter according to the first aspect is provided with a mapping
 relationship which defines a relationship of parallel bits (i.e. the parallel bits of the realigned
 30 parallel bit streams) and complex symbols, which are represented by constellation points. The
 mapping relationship thereby exploits regularities in the parallel bits of the realigned parallel bit
 streams in order to efficiently and flexibly modulate the processed information.

In a sixth implementation form of the transmitter according to the first aspect as such or
 35 according to any one of the previous implementation forms of the first aspect, the realigned

parallel bit streams can be labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q , and the modulation module can be configured to map parallel bits of the realigned parallel bit streams to complex symbols according to the following mapping relationship:

5

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
0	0	0	0	0	-1	1
0	0	0	0	1	3	1
0	0	0	1	0	-1	-3
0	0	0	1	1	3	-3
0	0	1	0	0	-1	5
0	0	1	0	1	3	5
0	0	1	1	0	-5	1
0	0	1	1	1	-5	-3
0	1	0	0	0	-1	-1
0	1	0	0	1	-1	3
0	1	0	1	0	3	-1
0	1	0	1	1	3	3
0	1	1	0	0	-5	-1
0	1	1	0	1	-5	3
0	1	1	1	0	-1	-5
0	1	1	1	1	3	-5
1	0	0	0	0	1	1
1	0	0	0	1	1	-3
1	0	0	1	0	-3	1
1	0	0	1	1	-3	-3
1	0	1	0	0	5	1
1	0	1	0	1	5	-3
1	0	1	1	0	1	5
1	0	1	1	1	-3	5
1	1	0	0	0	1	-1
1	1	0	0	1	-3	-1
1	1	0	1	0	1	3
1	1	0	1	1	-3	3

1	1	1	0	0	1	-5
1	1	1	0	1	-3	-5
1	1	1	1	0	5	-1
1	1	1	1	1	5	3

This ensures that the modulation module of the transmitter according to the first aspect is provided with a precise mapping relationship, which allows mapping of parallel bits of the realigned parallel bit streams to the complex symbols with high efficiency, reliability and performance.

A second aspect of the present invention provides a method for operating a transmitter for delayed bit-interleaved code modulation, DBICM, the method comprising the steps of: receiving, by a bit delay module, a plurality of parallel bit streams; delaying, by the bit delay module, at least one bit stream of the parallel bit streams to generate a plurality of realigned parallel bit streams; providing, by the bit delay module, the realigned parallel bit streams to a modulation module; mapping, by the modulation module, the realigned parallel bit streams to complex symbols, the complex symbols corresponding to constellation points in a complex plane.

In a first implementation form of the method according to the second aspect, the plurality of parallel bit streams can comprise five parallel bit streams and the method further can comprise the step of delaying, by the bit delay module, two of the five parallel bit streams to generate the realigned parallel bit streams.

In a second implementation form of the method according to the second aspect as such or according to the first implementation form of the second aspect, the method further can include the step of delaying, by the bit delay module, each of the two bit streams by one time block to generate the realigned parallel bit streams.

In a third implementation form of the method according to the second aspect as such or according to any previous implementation form of the second aspect, the constellation points can be constellation points according to 32-QAM.

In a fourth implementation form of the method according to the second aspect as such or according to any previous implementation form of the second aspect, the constellation points can comprise four groups of eight constellation points each.

In a fifth implementation form of the method according to the second aspect as such or according to any previous implementation form of the second aspect, the realigned parallel bit streams can be labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q , and the method can further comprise the step of mapping, by the modulation module parallel bits of the realigned parallel bit streams to the complex symbols according to the following mapping relationship:

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
A_0	A_1	0	0	0	-1	1
A_0	A_1	0	0	1	3	1
A_0	A_1	0	1	0	-1	-3
A_0	A_1	0	1	1	3	-3
A_0	A_1	1	0	0	-1	5
A_0	A_1	1	0	1	3	5
A_0	A_1	1	1	0	-5	1
A_0	A_1	1	1	1	-5	-3
B_0	B_1	0	0	0	-1	-1
B_0	B_1	0	0	1	-1	3
B_0	B_1	0	1	0	3	-1
B_0	B_1	0	1	1	3	3
B_0	B_1	1	0	0	-5	-1
B_0	B_1	1	0	1	-5	3
B_0	B_1	1	1	0	-1	-5
B_0	B_1	1	1	1	3	-5
C_0	C_1	0	0	0	1	1
C_0	C_1	0	0	1	1	-3
C_0	C_1	0	1	0	-3	1
C_0	C_1	0	1	1	-3	-3
C_0	C_1	1	0	0	5	1
C_0	C_1	1	0	1	5	-3
C_0	C_1	1	1	0	1	5
C_0	C_1	1	1	1	-3	5
D_0	D_1	0	0	0	1	-1
D_0	D_1	0	0	1	-3	-1

D₀	D₁	0	1	0	1	3
D₀	D₁	0	1	1	-3	3
D₀	D₁	1	0	0	1	-5
D₀	D₁	1	0	1	-3	-5
D₀	D₁	1	1	0	5	-1
D₀	D₁	1	1	1	5	3

wherein

- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
5 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
10 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
15 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
20 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
25 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$.

In a sixth implementation form of the method according to the second aspect as such or according to any previous implementation form of the second aspect, the realigned parallel bit streams can be labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q and the method further can comprise the step of mapping, by the modulation module, parallel bits of the realigned parallel bit streams to the complex symbols according to the following mapping relationship:

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
0	0	0	0	0	-1	1
0	0	0	0	1	3	1
0	0	0	1	0	-1	-3
0	0	0	1	1	3	-3
0	0	1	0	0	-1	5
0	0	1	0	1	3	5
0	0	1	1	0	-5	1
0	0	1	1	1	-5	-3
0	1	0	0	0	-1	-1
0	1	0	0	1	-1	3
0	1	0	1	0	3	-1
0	1	0	1	1	3	3
0	1	1	0	0	-5	-1
0	1	1	0	1	-5	3
0	1	1	1	0	-1	-5
0	1	1	1	1	3	-5
1	0	0	0	0	1	1
1	0	0	0	1	1	-3
1	0	0	1	0	-3	1
1	0	0	1	1	-3	-3
1	0	1	0	0	5	1
1	0	1	0	1	5	-3
1	0	1	1	0	1	5
1	0	1	1	1	-3	5
1	1	0	0	0	1	-1
1	1	0	0	1	-3	-1

1	1	0	1	0	1	3
1	1	0	1	1	-3	3
1	1	1	0	0	1	-5
1	1	1	0	1	-3	-5
1	1	1	1	0	5	-1
1	1	1	1	1	5	3

The method of the second aspect and its implementation forms achieve the same advantages as the system of the first aspect and its respective implementation forms.

- 5 A third aspect of the present invention provides a receiver for delayed bit-interleaved code modulation, DBICM, comprising a demodulation module and a bit delay module; wherein the demodulation module is configured to receive complex symbols corresponding to constellation points in a complex plane, map the complex symbols to a plurality of parallel bit streams and provide the parallel bit streams to the bit delay module; wherein the bit delay module is
10 configured to delay at least one bit stream of the parallel bit streams to generate a plurality of parallel bit streams.

The receiver of the first aspect uses a modulation module to map the complex symbols to bit streams, which are then partially delayed by the delay module. Since the complex symbols
15 correspond to constellation points in a complex plane, the mapping of the complex symbols to the bit streams corresponds to labelling of constellation points. The receiver according to the first aspect advantageously allows precisely adjusting the manner according to which complex symbols are mapped to bit streams, and the portion according to which the obtained bit streams are delayed. As the complex symbols correspond to constellation points in a complex plane, the
20 receiver according to the first aspect allows efficiently labelling constellation points, even in higher-order constellation cases, such as 32-QAM. Further, the receiver ensures that information can be received with high efficiency, reliability and performance.

In a first implementation form of the receiver according to the third aspect, the plurality of
25 parallel bit streams can comprise five parallel bit streams, and the bit delay module can further be configured to delay three of the five bit streams to generate the realigned parallel bit streams.

This ensures that delaying the parallel bit streams in the delay module can be performed according to an operating principle which maximizes efficiency, reliability and performance of transmission.

5 In a second implementation form of the receiver according to the third aspect as such or according to the first implementation form of the first aspect, the bit delay module can further be configured to delay each of the three bit streams by one time block to generate the realigned parallel bit streams.

10 Delaying each of the two bit streams by one time block each facilitates transmission with high efficiency, reliability and performance.

In a third implementation form of the receiver according to the third aspect as such or according to any previous implementation form of the third aspect, the constellation points can be
15 constellation points according to 32-QAM.

This ensures that the modulation module of the receiver according to the first aspect can map the realigned parallel bit streams to complex symbols in 32-point constellation cases according to
20 32-QAM.

In a fourth implementation form of the receiver according to the third aspect as such or according to any of the previous implementation form of the third aspect, the constellation points can comprise four groups of eight constellation points each.

25 This ensures that regularities in the constellation points can be exploited in order to improve efficiency and performance of coding and modulating.

In a fifth implementation form of the receiver according to the third aspect as such or according to any previous implementation form of the third aspect, the parallel bit streams can be labelled
30 as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q , and the demodulation module can be configured to map the complex symbols to parallel bits of the parallel bit streams according to the following mapping relationship:

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
A_0	A_1	0	0	0	-1	1
A_0	A_1	0	0	1	3	1
A_0	A_1	0	1	0	-1	-3
A_0	A_1	0	1	1	3	-3
A_0	A_1	1	0	0	-1	5
A_0	A_1	1	0	1	3	5
A_0	A_1	1	1	0	-5	1
A_0	A_1	1	1	1	-5	-3
B_0	B_1	0	0	0	-1	-1
B_0	B_1	0	0	1	-1	3
B_0	B_1	0	1	0	3	-1
B_0	B_1	0	1	1	3	3
B_0	B_1	1	0	0	-5	-1
B_0	B_1	1	0	1	-5	3
B_0	B_1	1	1	0	-1	-5
B_0	B_1	1	1	1	3	-5
C_0	C_1	0	0	0	1	1
C_0	C_1	0	0	1	1	-3
C_0	C_1	0	1	0	-3	1
C_0	C_1	0	1	1	-3	-3
C_0	C_1	1	0	0	5	1
C_0	C_1	1	0	1	5	-3
C_0	C_1	1	1	0	1	5
C_0	C_1	1	1	1	-3	5
D_0	D_1	0	0	0	1	-1
D_0	D_1	0	0	1	-3	-1
D_0	D_1	0	1	0	1	3
D_0	D_1	0	1	1	-3	3
D_0	D_1	1	0	0	1	-5
D_0	D_1	1	0	1	-3	-5
D_0	D_1	1	1	0	5	-1
D_0	D_1	1	1	1	5	3

wherein

- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
5 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
10 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
15 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
20 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
25 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$.

This ensures that the receiver according to the third aspect is provided with a mapping
30 relationship which defines a relationship of parallel bits (i.e. the parallel bits of the realigned
parallel bit streams) and complex symbols, which are represented by constellation points. The
mapping relationship of the fifth implementation form of the receiver according to the third
aspect thereby exploits regularities in the parallel bits of the realigned parallel bit streams in
order to efficiently modulate the processed information.

In a sixth implementation form of the receiver according to the third aspect as such or according to any previous implementation form of the third aspect, the parallel bit streams can be labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q , and the demodulation module can be configured to map the complex symbols to parallel bits of the parallel bit streams according to the following mapping relationship:

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
0	0	0	0	0	-1	1
0	0	0	0	1	3	1
0	0	0	1	0	-1	-3
0	0	0	1	1	3	-3
0	0	1	0	0	-1	5
0	0	1	0	1	3	5
0	0	1	1	0	-5	1
0	0	1	1	1	-5	-3
0	1	0	0	0	-1	-1
0	1	0	0	1	-1	3
0	1	0	1	0	3	-1
0	1	0	1	1	3	3
0	1	1	0	0	-5	-1
0	1	1	0	1	-5	3
0	1	1	1	0	-1	-5
0	1	1	1	1	3	-5
1	0	0	0	0	1	1
1	0	0	0	1	1	-3
1	0	0	1	0	-3	1
1	0	0	1	1	-3	-3
1	0	1	0	0	5	1
1	0	1	0	1	5	-3
1	0	1	1	0	1	5
1	0	1	1	1	-3	5
1	1	0	0	0	1	-1
1	1	0	0	1	-3	-1

1	1	0	1	0	1	3
1	1	0	1	1	-3	3
1	1	1	0	0	1	-5
1	1	1	0	1	-3	-5
1	1	1	1	0	5	-1
1	1	1	1	1	5	3

This ensures that the modulation module of the transmitter according to the first aspect is provided with a precise mapping relationship which allows mapping of parallel bits of the realigned parallel bit streams to the complex symbols with high efficiency, reliability and performance.

A fourth aspect of the present invention provides a method for operating a receiver for delayed bit-interleaved code modulation, DBICM, the method comprising the steps of: receiving, by a demodulation module of the receiver, complex symbols corresponding to constellation points in a complex plane; mapping, by the demodulation module, the complex symbols to a plurality of parallel bit streams; providing, by the demodulation module, the parallel bit streams to a bit delay module of the receiver; delaying, by the bit delay module, at least one bit stream of the parallel bit streams to generate a plurality of realigned parallel bit streams.

In a first implementation form of the method according to the fourth aspect, the plurality of parallel bit streams can comprise five parallel bit streams and the method further can comprise the step of delaying, by the bit delay module, three of the five bit streams to generate the realigned parallel bit streams.

In a second implementation form of the method according to the fourth aspect as such or according to the first implementation form of the fourth aspect, the method further can comprise the step of delaying, by the bit delay module, each of the three bit streams by one time block to generate the realigned parallel bit streams.

In a third implementation form of the method according to the fourth aspect as such or according to any previous implementation form of the fourth aspect, the constellation points can be constellation points according to 32-QAM.

In a fourth implementation form of the method according to the fourth aspect as such or according to any of the previous implementation forms of the fourth aspect, the constellation points can comprise four groups of eight constellation points each.

- 5 In a fifth implementation form of the method according to the fourth aspect as such or according to any previous implementation form of the fourth aspect, the parallel bit streams can be labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q , and the method can further comprise the step of mapping, by the demodulation module, the complex symbols to parallel bits of the parallel bit streams according to the following mapping relationship:
- 10

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
A_0	A_1	0	0	0	-1	1
A_0	A_1	0	0	1	3	1
A_0	A_1	0	1	0	-1	-3
A_0	A_1	0	1	1	3	-3
A_0	A_1	1	0	0	-1	5
A_0	A_1	1	0	1	3	5
A_0	A_1	1	1	0	-5	1
A_0	A_1	1	1	1	-5	-3
B_0	B_1	0	0	0	-1	-1
B_0	B_1	0	0	1	-1	3
B_0	B_1	0	1	0	3	-1
B_0	B_1	0	1	1	3	3
B_0	B_1	1	0	0	-5	-1
B_0	B_1	1	0	1	-5	3
B_0	B_1	1	1	0	-1	-5
B_0	B_1	1	1	1	3	-5
C_0	C_1	0	0	0	1	1
C_0	C_1	0	0	1	1	-3
C_0	C_1	0	1	0	-3	1
C_0	C_1	0	1	1	-3	-3
C_0	C_1	1	0	0	5	1
C_0	C_1	1	0	1	5	-3

C₀	C₁	1	1	0	1	5
C₀	C₁	1	1	1	-3	5
D₀	D₁	0	0	0	1	-1
D₀	D₁	0	0	1	-3	-1
D₀	D₁	0	1	0	1	3
D₀	D₁	0	1	1	-3	3
D₀	D₁	1	0	0	1	-5
D₀	D₁	1	0	1	-3	-5
D₀	D₁	1	1	0	5	-1
D₀	D₁	1	1	1	5	3

wherein

- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
5 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
10 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
15 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
20 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or

$A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or

$A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or

$A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$.

- 5 In a sixth implementation form of the method according to the fourth aspect as such or according to any previous implementation form of the fourth aspect, the parallel bit streams can be labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols can comprise an in-phase component s_I and a quadrature component s_Q , and the method further can comprise the step of mapping, by the demodulation module, the complex symbols to parallel bits of the parallel bit streams according to the following mapping relationship:
- 10

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
0	0	0	0	0	-1	1
0	0	0	0	1	3	1
0	0	0	1	0	-1	-3
0	0	0	1	1	3	-3
0	0	1	0	0	-1	5
0	0	1	0	1	3	5
0	0	1	1	0	-5	1
0	0	1	1	1	-5	-3
0	1	0	0	0	-1	-1
0	1	0	0	1	-1	3
0	1	0	1	0	3	-1
0	1	0	1	1	3	3
0	1	1	0	0	-5	-1
0	1	1	0	1	-5	3
0	1	1	1	0	-1	-5
0	1	1	1	1	3	-5
1	0	0	0	0	1	1
1	0	0	0	1	1	-3
1	0	0	1	0	-3	1
1	0	0	1	1	-3	-3
1	0	1	0	0	5	1
1	0	1	0	1	5	-3

1	0	1	1	0	1	5
1	0	1	1	1	-3	5
1	1	0	0	0	1	-1
1	1	0	0	1	-3	-1
1	1	0	1	0	1	3
1	1	0	1	1	-3	3
1	1	1	0	0	1	-5
1	1	1	0	1	-3	-5
1	1	1	1	0	5	-1
1	1	1	1	1	5	3

The method of the fourth aspect and its implementation forms achieve the same advantages as the receiver of the third aspect and its respective implementation forms.

- 5 A fifth aspect of the present invention provides a transceiver comprising the transmitter according to the first aspect as such or according to any implementation form of the first aspect, and the receiver according to the third aspect as such or any one of its implementation forms.

10 The transceiver of the fifth aspect achieves the same advantages as the transmitter of the first aspect and its respective implementation forms and the receiver of the third aspect and its respective implementation forms.

15 A sixth aspect of the present invention provides a method for operating the transceiver according to the fifth aspect, the method comprising the steps of the method according to the second aspect as such or any one of its implementation forms and the steps of the method according to the fourth aspect as such or any one of its implementation forms.

20 The method of the fifth aspect achieves the same advantages as the method of the second aspect as such and its respective implementation forms and as the method of the fourth aspect as such and its respective implementation forms.

It has to be noted that all devices, elements, units and means described in the present application could be implemented in the software or hardware elements or any kind of combination thereof. All steps which are performed by the various entities described in the present application as well

as the functionalities described to be performed by the various entities are intended to mean that the respective entity is adapted to or configured to perform the respective steps or functionalities. Even if, in the following description of specific embodiments, a specific functionality or a step to be performed by external entities is not reflected in the description of a specific detailed element of that entity which performs that specific step or functionality, it should be clear for a skilled person that these methods and functionalities can be implemented in respective software or hardware elements, or any kind of combination thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

The above described aspects and implementation forms of the present invention will be explained in the following description of specific embodiments in relation to the enclosed drawings, in which:

Fig 1 shows an example DBICM modulation scheme for 8-QAM according to the prior art.

Fig. 2 shows a schematic overview of a transmitter according to an embodiment of the present invention.

Fig. 3 shows a method according to an embodiment of the present invention.

Fig. 4 shows a schematic overview of a receiver according to an embodiment of the present invention.

Fig. 5 shows a method according to an embodiment of the present invention.

Fig. 6 shows a schematic overview of a transceiver according to an embodiment of the present invention.

Fig. 7 shows a method according to an embodiment of the present invention.

Fig. 8 shows another schematic overview of a transmitter and a receiver according to the present invention.

- Fig. 9 shows an operating principle of a bit delay module according to the present invention.
- Fig. 10 shows another operating principle of a bit delay module according to the present invention.
- Fig. 11 shows an operating principle of a modulation module according to the present invention.
- Fig. 12 shows a labelling scheme for DBICM with 32-QAM according to the present invention.
- Fig. 13 shows mapping relationships for DBICM with 32-QAM according to the present invention.
- Fig. 14 shows a semi-gray mapping for 32-QAM.
- Fig. 15 shows a spectral efficiency simulator.
- Fig. 16 shows a bit error rate simulator for DBICM.
- Fig. 17 shows spectral efficiency of DBICM and BICM.
- Fig. 18 shows spectral efficiency of DBICM and BICM.
- Fig. 19 shows bit error rates of DBICM and BICM.

DETAILED DESCRIPTION OF THE EMBODIMENTS

- Fig. 2 shows a transmitter 200 according to an embodiment of the present invention. The transmitter 200 is particularly suited for DBICM. The transmitter 200 comprises a bit delay module 201 and a modulation module 202. The bit delay module 201 is configured to receive a plurality of parallel bit streams 203 and to delay at least one bit stream 204 of the plurality of received parallel bit streams 203. Delaying the at least one bit stream 204 is illustrated in Fig. 2 by the dashed line within the bit delay module 201 which comprises longer dashes compared to

the remaining four dashed lines in the bit delay module 201. Although it is also only illustrated in Fig. 2 that one bit stream 204 is delayed, it is to be noted that the bit delay module 201 can be configured to delay an arbitrary number of received parallel bit streams 203, for example, one, two, three or four bit streams of the received parallel bit streams 203 can be delayed. By delaying at least one bit stream 204 in the received plurality of parallel bit streams 203, the bit delay module 201 is able to provide a plurality of realigned parallel bit streams 205. The realigned parallel bit streams 205 can subsequently be provided to the modulation module 202. After receiving the realigned parallel bit streams 205, the modulation module 202 maps the realigned parallel bit streams 205 to complex symbols 206. Therefore, the modulation module 202 uses a pre-configured mapping relationship, which is pre-stored in the modulation module 202. The complex symbols 206, which are generated based on the realigned parallel bit streams 205, correspond to constellation points in a complex plane.

In particular, the plurality of parallel bit streams 203 optionally can comprise five parallel bit streams, and the bit delay module 201 optionally can be configured to delay two of the five parallel bit streams to generate the realigned parallel bit streams 205. More specifically, the bit delay module 201 can further optionally be configured to delay each of the two bit streams by one time block each to generate the realigned parallel bit streams 205. In particular, the time block can have the same length as one of the transmission blocks 101, 102 as described in view of Fig. 1.

Further optionally, the constellation points can be constellation points according to 32-QAM. Further optionally, the constellation points can comprise four groups of eight constellation points each. The constellation points according to 32-QAM and the four groups of eight constellation points each are going to be described in detail in view of Fig. 12 below.

A more detailed description of the transmitter 200 and in particular of the bit delay module 201 and the modulation module 202 is going to be provided in view of Figs. 8 to 11 below. The features, which are going to be described in view of Figs. 8 to 11 below are optional features.

Fig. 3 shows a method 300 according to an embodiment of the present invention. The method 300 corresponds to the transmitter 200 of Fig. 2 and is accordingly for operating the transmitter 200 for DBICM.

The method 300 comprises a step of receiving S301, by a bit delay module 201 of a transmitter 200, a plurality of parallel bit streams 203. Further, the method 300 comprises a step of delaying S302, by the bit delay module 201, at least one bit stream 204 of the parallel bit streams 203 to generate a plurality of realigned parallel bit streams 205. The method 300 comprises another step of providing S303, by the bit delay module 201, the realigned parallel bit streams 205 to a modulation module 202 of the transmitter 200. Finally, the method 300 comprises a step of mapping S304, by the modulation module 202, the realigned parallel bit streams 205 to complex symbols 206, the complex symbols 206 corresponding to constellation points in a complex plane.

Fig. 4 shows a receiver 400 according to an embodiment of the present invention. The receiver 400 is in particular suited for DBICM. The receiver 400 comprises a demodulation module 401 and a bit delay module 402. The demodulation module 401 is configured to receive complex symbols 403 corresponding to constellation points in a complex plane. The complex symbols 403, which can be received by the demodulation module 401 can in particular be provided to the receiver 400 by the transmitter 200 as described in view of Fig. 2.

After receiving the complex symbols 403, the demodulation module 401 maps the complex symbols 403 to a plurality of parallel bit streams 404. Therefore, the demodulation module 401 uses a pre-configured mapping relationship, which is pre-stored in the demodulation module 401. The bit delay module 402 is configured to receive the plurality of parallel bit streams 404 and to delay at least one bit stream 405 of the plurality of received parallel bit streams 404.

Delaying the at least one bit stream 405 is illustrated in Fig. 4 by the dashed line within the bit delay module 402 which comprises longer dashes compared to the remaining four dashed lines in the bit delay module 402. Although it is illustrated in Fig. 4 that only one bit stream 405 is delayed, it is to be noted that the bit delay module 402 can be configured to delay an arbitrary number of received parallel bit streams 404, for example, one, two, three or four bit streams of the received parallel bit streams 404 can be delayed. By delaying at least one bit stream 405 in the received plurality of parallel bit streams 405, the bit delay module 402 is able to provide a plurality of realigned parallel bit streams 406.

It is to be noted that the bit delay module 402 specifically can be configured to delay those bit streams in the received parallel bit streams 404, which have not been delayed in the realigned parallel bit streams 205 that were generated by the bit delay module 201 by processing the parallel bit streams 203 in the transmitter 200. More specifically, the realigned parallel bit

streams 205 are used to generate the complex symbols 206 which are transmitted from the transmitter 200 to the receiver 400, where they are received as complex symbols 403, based on which the parallel bit streams 404 are generated.

- 5 In particular, the plurality of parallel bit streams 404 optionally can comprise five parallel bit streams, and the bit delay module 402 optionally can be configured to delay three of the five parallel bit streams to generate the realigned parallel bit streams 406. More specifically, the bit delay module 402 can further optionally be configured to delay each of the two bit streams by one time block each to generate the realigned parallel bit streams 406. In particular, the time
10 block can have the same length as one of the transmission blocks 101, 102 as described in view of Fig. 1.

Further optionally, the constellation points can be constellation points according to 32-QAM. Further optionally, the constellation points can comprise four groups of eight constellation points
15 each. The constellation points according to 32-QAM and the four groups of eight constellation points each are going to be described in detail in view of Fig. 12 below.

A more detailed description of the receiver 400 and in particular of the bit delay module 402 and the modulation module 401 is going to be provided in view of Figs. 8 to 11 below. The features,
20 which are going to be described in view of Figs. 8 to 11 below are optional features.

Fig. 5 shows a method 500 according to an embodiment of the present invention. The method 500 corresponds to the receiver 400 of Fig. 4, and is accordingly for operating the receiver 400 for DBICM.

25 The method 400 comprises a step of receiving S501, by a demodulation module 401 of a receiver 400, complex symbols 403 corresponding to constellation points in a complex plane. Further, the method 500 comprises a step of mapping S502, by the demodulation module 401, the complex symbols 403 to a plurality of parallel bit streams 404. The method 500 comprises another step of
30 providing S503, by the demodulation module 401, the parallel bit streams 404 to a bit delay module 402 of the receiver 400. Finally, the method 500 comprises a step of delaying S504, by the bit delay module 402, at least one bit stream 405 of the parallel bit streams 404 to generate a plurality of realigned parallel bit streams 406.

Fig. 6 shows a transceiver 600 according to an embodiment of the present invention. The transceiver 600 is particularly suited for DBICM. The transceiver 600 comprises the transmitter 200 as described in view of Fig. 2 and the receiver 400 as described in view of Fig. 4. The transmitter 200 and the receiver 400 as included in the transceiver 600 can also include the optional features as described in view of Figs. 8 to 13 below. The transmitter 200 and the receiver 400 as included in the transceiver 600 include the same features and functionality of the transmitter 200 and the receiver 400 as described in view of Figs. 2 and 4 above. As a result, in Fig. 6, features which are identical to features described in view of Fig. 2 or Fig. 4 are labelled with identical reference signs as used in Fig. 2 or Fig. 4. In the transceiver 600, features provided and operations performed by the transmitter 200 as well as the receiver 400 can be simultaneously implemented in a shared module or unit. It is to be noted that the transceiver 600 simultaneously contains the transmitter 200 and the receiver 400 to be able to send or receive information at the same time, which is received or transmitted by another transmitter or receiver.

Fig. 7 shows a method 700 according to an embodiment of the present invention. The method 700 corresponds to the transceiver 600 of Fig. 6 and is accordingly for operating the transceiver 600 for DBICM.

The method 700 comprises all steps of the method 300 as described in view of Fig. 3 and all steps of the method 500 as described in view of Fig. 5. In order to operate the transceiver 600, method steps which result from method 300 can be performed sequentially before or after method steps that result from method 500 are sequentially performed. However, it is also possible that, when executing all steps of the method 700, at least one step is executed from the method 300 or the method 500 alternatively. When executing the method 700, the method steps which result from the method 300 and the method steps which result from the method 500 can be executed by a shared module or unit. . It is to be noted that the method 700 is in particular adapted to operate the transceiver 600 that simultaneously contains the transmitter 200 and the receiver 400 to send or receive information at the same time, which is received or transmitted by another transmitter or receiver.

Fig. 8 shows a transmitter 200 and a receiver 400 according to the present invention in more detail. In Fig. 8, in particular the operating manner of the bit delay modules 201, 402, the modulation module 202 and the demodulation module 401 are described in more detail. Although the transmitter 200 and the receiver 400 are described in view of a single figure, their corresponding functionalities relate to separate embodiments. The blocks labelled π and π^{-1} are

the interleaver and deinterleaver, respectively. Interleaving is usually used in digital communication systems with channel coding to improve the performance of FEC codes. Both interleaver and deinterleaver are present in a BICM system, which was used as prior art for DBICM. Their presence in Fig. 8 serves only for completeness of the solution (a complete communications system), but is not directly relevant to the invention.

The description of the transmitter 200 and the receiver 400 refers to the transmission of complex symbols that correspond to constellation points according to 32-QAM. In this case, each transmitted complex symbol is formed by a mapping of five bits (which can be called a five-bit-string) to a complex number.

In the transmitter 200 of Fig. 8, a codeword that is provided by an encoder ENC of the transmitter 200 is identified as vector $\vec{c}(t)$. The index t identifies the position of a given codeword in a sequence of transmitted codewords. The length of the vector $\vec{c}(t)$ is here $N=5M$ bits (N and M being positive integers), wherein the vector $\vec{c}(t)$ is defined as $\vec{c}(t) = [c_1(t) \cdots c_M(t) c_{M+1}(t) \cdots c_{2M}(t) c_{2M+1}(t) \cdots c_{3M}(t) c_{3M+1}(t) \cdots c_{4M}(t) c_{4M+1}(t) \cdots c_{5M}(t)]$

In a next step, the vector $\vec{c}(t)$ is processed in a serial/parallel converter S/P. At the output side of the serial/parallel converter S/P, $\vec{c}(t)$ is divided into five parallel streams of bits: $\vec{b}_0(t), \dots, \vec{b}_4(t)$, i.e. into the plurality of parallel bit streams 203.

These five parallel bit streams 203 are realigned at the bit delay module 201, in which two streams of the five parallel streams are here exemplarily delayed by one time block each, and then transformed in the modulation module 202 into complex symbols 206 that compose a vector $\vec{s}(t)$.

In the receiver 400, inverse operations are applied to a vector of received complex symbols $\vec{y}(t)$ (which may correspond to the vector $\vec{s}(t)$), with the object of estimating the codeword $\vec{c}(t-1)$ at time instant t . The demodulation module 401 at time instant t demodulates the first two bits in each symbol, generating $\vec{l}_0(t-1)$ and $\vec{l}_1(t-1)$. With this information, the codeword $\vec{c}(t-1)$ is decoded in a decoder DEC with optional error correction. Information of the first two bits in each symbol is then fed back to the demodulation module 401, and this information is used to demodulate the three remaining bits for each symbol at time instant $t+1$, generating $\vec{l}_0(t)$ and $\vec{l}_1(t)$ that will be used to estimate $\vec{c}(t)$.

In the bit delay module 402, the parallel bit streams 404 obtained by the demodulation module 401 can be realigned, in particular by delaying here exemplarily three bit streams of the obtained parallel bit streams 404. An output of the bit delay module 402 (i.e. the realigned bit streams 406) is forwarded to a parallel/serial converter P/S, where $\vec{c}(t)$ is obtained before it is provided to a decoder DEC.

In order to obtain the complex symbols 206 from the parallel bit streams 203, the following processes are performed by the bit delay module 201 and the modulation module 202 in the transmitter 200:

- 1) Realignment of the parallel bit streams 203 is performed in the bit delay module 201 according to preferably a 2+3 DBICM scheme with a delay of 1 time block.
 - a. In this scheme, the streams $\vec{b}_2(t)$, $\vec{b}_3(t)$ and $\vec{b}_4(t)$ are integrated with streams $\vec{b}_0(t-1)$ and $\vec{b}_1(t-1)$, coming from a preceding codeword.
 - b. Also, the streams $\vec{b}_0(t)$ and $\vec{b}_1(t)$ are delayed to be integrated with subsequent streams $\vec{b}_2(t+1)$, $\vec{b}_3(t+1)$ and $\vec{b}_4(t+1)$.
 - c. This realignment occurs with all generated codewords.
- 2) The specific mapping of each set of five bits in the modulation module 202 to complex symbols 206, is going to be described in detail below.
- 3) At the receiver, inverse operations relating to items 1 and 2 above are performed in the bit delay module 402 and the demodulation module 401.

Fig. 9 shows an operating principle of a bit delay module 201 according to the present invention. Fig. 9 in particular illustrates the process of realigning a codeword $\vec{c}(t)$ (which is processed as parallel bit streams 203 in the bit delay module 201 after it was processed in the serial/parallel converter S/P) to codeblocks (i.e. the realigned bit streams 205) that in turn can be input to the modulation module 202.

Fig. 10 shows another operating principle of a bit delay module 201 according to the present invention. Fig. 10 in particular illustrates a sequence of three consecutive codeblocks at times t , $t+1$ and $t+2$, respectively, which are output as realigned parallel bit streams 205 by the bit delay module 201, and which can be provided to the modulation module 202.

Fig. 11 shows an operating principle of the modulation module 202 according to the present invention. After determining the realigned parallel bit streams 205 by the bit delay module 201, the realigned parallel bit streams 205 can subsequently be provided to the modulation module 202. The realigned parallel bit streams 205 can be labelled as $\vec{d}_0(t)$, $\vec{d}_1(t)$, $\vec{d}_2(t)$, $\vec{d}_3(t)$, and $\vec{d}_4(t)$, as it is illustrated in Fig. 11. After receiving the realigned parallel bit streams 205, the modulation module 202 (modulator) maps the realigned parallel bit streams 205 to complex symbols 206 that compose the vector $\vec{s}(t)$. Therefore, the modulation module 202 preferably uses a pre-configured mapping relationship, which is pre-stored in the modulation module 202, and which is described in detail in view of Figs. 12 and 13 below. In particular, the modulation module 202 processes five parallel bits $d_0(t)$, $d_1(t)$, $d_2(t)$, $d_3(t)$, and $d_4(t)$ at time t to obtain a complex symbol (which comprises an in-phase component s_I and a quadrature component s_Q), wherein each bit of the five parallel bits $d_0(t)$, $d_1(t)$, $d_2(t)$, $d_3(t)$, and $d_4(t)$ is a bit that is obtained at time t from a corresponding stream of the five realigned parallel bit streams 205 that are labelled $\vec{d}_0(t)$, $\vec{d}_1(t)$, $\vec{d}_2(t)$, $\vec{d}_3(t)$, and $\vec{d}_4(t)$.

Fig. 12 shows a labelling scheme (which also can be called mapping relationship 1200) for DBICM with 32-QAM according to the present invention. Fig. 12 in particular shows the mapping relationship 1200 according to which the modulation module 202 maps parallel bits of the realigned parallel bit streams 205 (i.e. $\vec{d}_0(t)$, $\vec{d}_1(t)$, $\vec{d}_2(t)$, $\vec{d}_3(t)$, and $\vec{d}_4(t)$) to the complex symbols 206 – by specifying an in-phase component s_I and a quadrature component s_Q that correspond to five parallel bits (i.e. the 5-bit-string), wherein a bit is obtained from one of the realigned parallel bit streams 205 each at a given time t – and according to which the demodulation module 401 maps the complex symbols 403 to parallel bits of the parallel bit streams 404 (i.e. $\vec{d}_0(t)$, $\vec{d}_1(t)$, $\vec{d}_2(t)$, $\vec{d}_3(t)$, and $\vec{d}_4(t)$) – by specifying five parallel bits of the parallel bit streams 404 that correspond to an in-phase component s_I and a quadrature component s_Q .

In Fig. 12, an example of one mapping of the mapping relationship 1200 is marked in which the five bits “10111” are mapped to a complex symbol that corresponds to a constellation point 1201 with an in-phase component of 5 and quadrature component of -3.

The advantageous effect of the present invention is in particular achieved if the mapping relationship 1200 of Fig. 12 is used in the transmitter 200 in combination with the realignment principle of the parallel bit streams 203 as it is performed in the bit delay module 201 according

to the preferred 2+3 DBICM scheme as described above, in particular as described in view of Fig. 8. The same applies for the corresponding parts in the receiver 400.

The constellation points which are shown in the mapping relationship 1200 in particular can be constellation points according to 32-QAM. The mapping relationship 1200 in particular achieves its beneficial effect when applied in the field of 32-QAM.

More specifically, the constellation points can comprise four groups (i.e. Set 1, Set 2, Set 3 and Set 4, as illustrated on the top-left side of Fig. 12) of eight constellation points each. In Fig. 12, each label of a group (i.e. the rectangle, the rhombus, the circle and the triangle) represents a different group of eight constellation points. Inside each set, a quasi-gray mapping can be applied.

When separately looking at the eight constellation points of each of the four groups, it can be seen that the eight constellation points form an L-shape in the complex plane. In Fig. 12 this is exemplary illustrated for the constellation points that belong to the group “Set 3” by means of an L-shape 1202 that is drawn in dashed lines. For each group, the L-shape can be rotated in a different way.

Each of the four groups contains constellation points, whose corresponding 5-bit-strings are identical in the first two bits of the 5-bit-string. For example, the constellation points which correspond to the group “Set 3” in Fig. 12 are all labelled with 5-bit-strings that star with “10” and only differ in the last three bits. These regularities can be exploited by the mapping relationship 1200 in order to improve performance and efficiency of the transmitter 200 or the receiver 400.

Fig. 13 shows mapping relationships 1300 for DBICM with 32-QAM according to the present invention. The different mapping relationships 1300 are provided in tables 1301 and 1302. In each line of a table 1301, 1302, a mapping of parallel bits (i.e. parallel bits of the five parallel bit streams 205, 404 at a predefined time t , that is, the 5-bit-string) $d_0(t)$, $d_1(t)$, $d_2(t)$, $d_3(t)$, and $d_4(t)$ to an in-phase component s_I and a quadrature component s_Q of a complex symbol 206, 403 is provided.

In order to improve performance and efficiency of the transmitter 200 or the receiver 400, as well as flexibility of mapping, by exploiting the regularities in the mapping relationships 1300,

in table 1301 of Fig. 13, predefined fields are labelled with variables A_0 , A_1 , B_0 , B_1 , C_0 , C_1 , D_0 , D_1 . These variables can be assigned with a set of values according to one of the 24 lines below, wherein each possible mapping relationship resulting from table 1301 being filled with a set of values according to one of the 24 lines below represents a valid operating configuration of the transmitter 200 or the receiver 400.

The 24 sets of values can be as follows:

- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
- 10 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
- 15 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
- $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
- $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
- $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
- $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
- 20 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
- $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
- $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
- $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
- $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
- 25 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
- $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
- $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
- $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
- $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
- 30 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
- $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
- $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$.

A possible mapping relationship provided in table 1301 can correspond to the constellation points as shown in Fig. 12 and achieves the advantageous effect of improving reliability,

efficiency and performance of the transmitter 200 and the receiver 400 according to the present invention.

More preferably, the mapping relationship as shown in table 1302 provides a precise mapping of parallel bits (i.e. parallel bits of the five parallel bit streams at a predefined time t) $d_0(t)$, $d_1(t)$, $d_2(t)$, $d_3(t)$, and $d_4(t)$ to an in-phase component s_I and a quadrature component s_Q of a complex symbol 206, 403. The mapping relationship provided in table 1302 corresponds precisely to the constellation points as shown in Fig. 12 and achieves the advantageous effect of improving reliability, efficiency and performance of the transmitter 200 and the receiver 400 according to the present invention.

The mapping relationships for DBICM according to the present invention in particular improve conventional DBICM, but also are improved compared to BICM, a prior art technique for coded modulation. The advantageous effect of the mapping relationship for DBICM according to the present invention is in particular based on the mapping of bits to constellation points as e.g. described in view of Figs. 12 and 13. Thus, a performance analysis is provided in the following, which proves the advantageous effects. For comparison of performance results of the mapping relationships for DBICM according to the present invention, we use a quasi-gray labelling of a 32-QAM cross constellation with a BICM scheme, which is known to be an optimal labelling for BICM.

Fig. 14 shows a semi-gray mapping for 32-QAM 1400 which is used for comparison with the results of the mapping relationships for DBICM according to the present invention.

To show performance gains of the mapping relationships for DBICM according to the present invention in comparison to a baseline BICM scheme in a 32-QAM quasi gray system, a spectral efficiency analysis and bit error rate (BER) curves are provided in the following.

Fig. 15 shows a schematic overview of a spectral efficiency simulator 1500 that can be used for performance tests of mapping relationships for DBICM according to the present invention as well as for performance tests of conventional DBICM and BICM.

Fig. 16 shows a schematic overview of a bit error rate simulator 1600 that can be used for performance tests of mapping relationships for DBICM according to the present invention as well as for performance tests of conventional DBICM and BICM.

Figs. 17 and 18 show spectral efficiency 1700, 1800 of mapping relationships for DBICM according to the present invention and BICM. The spectral efficiency 1700, 1800 of the competing schemes is based on an additive white Gaussian noise (AWGN) channel. The preferred 2+3 DBICM scheme with delay of one time block according to the invention
5 approximates a constellation capacity at a high signal-to-noise ratio SNR. Looking at an operation point of 4 bits/symbol, a gain of 0.3 dB in relation to BICM is notable.

To obtain BER results, a tested DBICM system (which comprises a transmitter 200 and a receiver 400) is implemented in a coded system. In this case, a Low-Density-Parity-Check
10 (LDPC) encoder/decoder with rate of 0.8 and blocks with length of 15303 bits of information is implemented.

Fig. 19 shows bit error rates 1900 of mapping relationships for DBICM according to the present invention and BICM. Fig. 19 in particular shows BER curves comparing the DBICM scheme
15 according to the invention and a baseline BICM scheme. To obtain this result, in the DBICM scheme case, it is assumed that bits used in a decoding process are known. As it can be noticed in Fig. 19, the DBICM scheme according to the invention improves performance over BICM, as expected from the spectral efficiency analysis. The result as illustrated in Fig. 19 shows a gain of 0.2 dB of the DBICM scheme according to the invention in relation to baseline quasi-gray 32-
20 QAM BICM.

All performance results which are shown in view of Figs. 17 to 19 that compare DBICM according to the present invention and BICM can also be used to compare DBICM according to the present invention and conventional DBICM.

The present invention has been described in conjunction with various embodiments as examples as well as implementations. However, other variations can be understood and effected by those persons skilled in the art and practicing the claimed invention, from the studies of the drawings, this disclosure and the independent claims. In the claims as well as in the description the word
30 “comprising” does not exclude other elements or steps and the indefinite article “a” or “an” does not exclude a plurality. A single element or other unit may fulfill the functions of several entities or items recited in the claims. The mere fact that certain measures are recited in the mutual different dependent claims does not indicate that a combination of these measures cannot be used in an advantageous implementation.

CLAIMS

1. A transmitter (200) for Delayed Bit-Interleaved Code Modulation, DBICM, comprising a bit delay module (201) and a modulation module (202);

5 wherein the bit delay module (201) is configured to receive a plurality of parallel bit streams (203), delay at least one bit stream (204) of the parallel bit streams (203) to generate a plurality of realigned parallel bit streams (205), and provide the realigned parallel bit streams (205) to the modulation module (202);

10 wherein the modulation module (202) is configured to map the realigned parallel bit streams (205) to complex symbols (206), the complex symbols (206) corresponding to constellation points in a complex plane.

2. The transmitter (200) according to claim 1, wherein the plurality of parallel bit streams (203) comprises five parallel bit streams, and
15 the bit delay module (201) is further configured to delay two of the five parallel bit streams to generate the realigned parallel bit streams (205).

3. The transmitter (200) according to claim 2, wherein the bit delay module (201) is further configured to delay each of the two bit streams by
20 one time block to generate the realigned parallel bit streams (205).

4. The transmitter (200) according to any one of the preceding claims, wherein the constellation points are constellation points according to 32 quadrature amplitude modulation, 32-QAM.

5. The transmitter (200) according to any one of the preceding claims, wherein the constellation points comprise four groups of eight constellation points each.

6. The transmitter (200) according to any one of claims 1 to 5, wherein
30 the realigned parallel bit streams (205) are labelled as b_0 , b_1 , b_2 , b_3 , and b_4 , the complex symbols (206) comprise an in-phase component s_I and a quadrature component s_Q , and

the modulation module (202) is configured to map parallel bits of the realigned parallel bit streams (205) to the complex symbols (206) according to the following mapping relationship:

b₀	b₁	b₂	b₃	b₄	s_I	s_Q
A₀	A₁	0	0	0	-1	1
A₀	A₁	0	0	1	3	1
A₀	A₁	0	1	0	-1	-3
A₀	A₁	0	1	1	3	-3
A₀	A₁	1	0	0	-1	5
A₀	A₁	1	0	1	3	5
A₀	A₁	1	1	0	-5	1
A₀	A₁	1	1	1	-5	-3
B₀	B₁	0	0	0	-1	-1
B₀	B₁	0	0	1	-1	3
B₀	B₁	0	1	0	3	-1
B₀	B₁	0	1	1	3	3
B₀	B₁	1	0	0	-5	-1
B₀	B₁	1	0	1	-5	3
B₀	B₁	1	1	0	-1	-5
B₀	B₁	1	1	1	3	-5
C₀	C₁	0	0	0	1	1
C₀	C₁	0	0	1	1	-3
C₀	C₁	0	1	0	-3	1
C₀	C₁	0	1	1	-3	-3
C₀	C₁	1	0	0	5	1
C₀	C₁	1	0	1	5	-3
C₀	C₁	1	1	0	1	5
C₀	C₁	1	1	1	-3	5
D₀	D₁	0	0	0	1	-1
D₀	D₁	0	0	1	-3	-1
D₀	D₁	0	1	0	1	3
D₀	D₁	0	1	1	-3	3
D₀	D₁	1	0	0	1	-5
D₀	D₁	1	0	1	-3	-5
D₀	D₁	1	1	0	5	-1
D₀	D₁	1	1	1	5	3

wherein

- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
5 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
10 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or

- $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
5 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
10 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
15 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$.

7. The transmitter (200) according to any one of claims 1 to 5, wherein
the realigned parallel bit streams (205) are labelled as b_0 , b_1 , b_2 , b_3 , and b_4 ,
the complex symbols (206) comprise an in-phase component s_I and a quadrature
20 component s_Q , and
the modulation module (202) is configured to map parallel bits of the realigned parallel
bit streams (205) to the complex symbols (206) according to the following mapping relationship:

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
0	0	0	0	0	-1	1
0	0	0	0	1	3	1
0	0	0	1	0	-1	-3
0	0	0	1	1	3	-3
0	0	1	0	0	-1	5
0	0	1	0	1	3	5
0	0	1	1	0	-5	1
0	0	1	1	1	-5	-3
0	1	0	0	0	-1	-1
0	1	0	0	1	-1	3
0	1	0	1	0	3	-1
0	1	0	1	1	3	3
0	1	1	0	0	-5	-1
0	1	1	0	1	-5	3
0	1	1	1	0	-1	-5
0	1	1	1	1	3	-5

1	0	0	0	0	1	1
1	0	0	0	1	1	-3
1	0	0	1	0	-3	1
1	0	0	1	1	-3	-3
1	0	1	0	0	5	1
1	0	1	0	1	5	-3
1	0	1	1	0	1	5
1	0	1	1	1	-3	5
1	1	0	0	0	1	-1
1	1	0	0	1	-3	-1
1	1	0	1	0	1	3
1	1	0	1	1	-3	3
1	1	1	0	0	1	-5
1	1	1	0	1	-3	-5
1	1	1	1	0	5	-1
1	1	1	1	1	5	3

8. A receiver (400) for Delayed Bit-Interleaved Code Modulation, DBICM, comprising a demodulation module (401) and a bit delay module (402);

wherein the demodulation module (401) is configured to receive complex symbols (403) corresponding to constellation points in a complex plane, map the complex symbols (403) to a plurality of parallel bit streams (404), and provide the parallel bit streams (404) to the bit delay module (402);

wherein the bit delay module (402) is configured to delay at least one bit stream (405) of the parallel bit streams (404) to generate a plurality of realigned parallel bit streams (406).

9. The receiver (400) according to claim 8, wherein

the plurality of parallel bit streams (404) comprises five parallel bit streams, and

the bit delay module (402) is further configured to delay three of the five bit streams to generate the realigned parallel bit streams (406).

10. The receiver (400) according to claim 9, wherein

the bit delay module (402) is further configured to delay each of the three bit streams by one time block to generate the realigned parallel bit streams (406).

11. The receiver (400) according to any one of claims 8 to 10, wherein

the constellation points are constellation points according to 32 quadrature amplitude modulation, 32-QAM.

12. The receiver (400) according to any one of claims 8 to 11, wherein

the constellation points comprise four groups of eight constellation points each.

13. The transmitter (400) according to any one of claims 8 to 12, wherein

the parallel bit streams (404) are labelled as b_0 , b_1 , b_2 , b_3 , and b_4 ,

5 the complex symbols (403) comprise an in-phase component s_I and a quadrature component s_Q , and

the demodulation (401) module is configured to map the complex symbols (403) to parallel bits of the parallel bit streams (404) according to the following mapping relationship:

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
A_0	A_1	0	0	0	-1	1
A_0	A_1	0	0	1	3	1
A_0	A_1	0	1	0	-1	-3
A_0	A_1	0	1	1	3	-3
A_0	A_1	1	0	0	-1	5
A_0	A_1	1	0	1	3	5
A_0	A_1	1	1	0	-5	1
A_0	A_1	1	1	1	-5	-3
B_0	B_1	0	0	0	-1	-1
B_0	B_1	0	0	1	-1	3
B_0	B_1	0	1	0	3	-1
B_0	B_1	0	1	1	3	3
B_0	B_1	1	0	0	-5	-1
B_0	B_1	1	0	1	-5	3
B_0	B_1	1	1	0	-1	-5
B_0	B_1	1	1	1	3	-5
C_0	C_1	0	0	0	1	1
C_0	C_1	0	0	1	1	-3
C_0	C_1	0	1	0	-3	1
C_0	C_1	0	1	1	-3	-3
C_0	C_1	1	0	0	5	1
C_0	C_1	1	0	1	5	-3
C_0	C_1	1	1	0	1	5
C_0	C_1	1	1	1	-3	5
D_0	D_1	0	0	0	1	-1
D_0	D_1	0	0	1	-3	-1
D_0	D_1	0	1	0	1	3
D_0	D_1	0	1	1	-3	3
D_0	D_1	1	0	0	1	-5
D_0	D_1	1	0	1	-3	-5
D_0	D_1	1	1	0	5	-1
D_0	D_1	1	1	1	5	3

10

Wherein

- $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
5 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
10 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 0$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 1$, or
15 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 0$ and $B_0 = 1$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 1$ and $D_1 = 0$, or
20 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 0$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 1$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 0$ and $B_1 = 1$ and $C_0 = 1$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 0$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 0$ and $D_0 = 0$ and $D_1 = 1$, or
 $A_0 = 1$ and $A_1 = 1$ and $B_0 = 1$ and $B_1 = 0$ and $C_0 = 0$ and $C_1 = 1$ and $D_0 = 0$ and $D_1 = 0$.

25

14. The receiver (400) according to any one of claims 8 to 13, wherein
 the parallel bit streams (404) are labelled as b_0 , b_1 , b_2 , b_3 , and b_4 ,
 the complex symbols (403) comprise an in-phase component s_I and a quadrature
 component s_Q , and

- 30 the demodulation module (401) is configured to map the complex symbols (403) to
 parallel bits of the parallel bit streams (404) according to the following mapping relationship:

b_0	b_1	b_2	b_3	b_4	s_I	s_Q
0	0	0	0	0	-1	1
0	0	0	0	1	3	1
0	0	0	1	0	-1	-3

0	0	0	1	1	3	-3
0	0	1	0	0	-1	5
0	0	1	0	1	3	5
0	0	1	1	0	-5	1
0	0	1	1	1	-5	-3
0	1	0	0	0	-1	-1
0	1	0	0	1	-1	3
0	1	0	1	0	3	-1
0	1	0	1	1	3	3
0	1	1	0	0	-5	-1
0	1	1	0	1	-5	3
0	1	1	1	0	-1	-5
0	1	1	1	1	3	-5
1	0	0	0	0	1	1
1	0	0	0	1	1	-3
1	0	0	1	0	-3	1
1	0	0	1	1	-3	-3
1	0	1	0	0	5	1
1	0	1	0	1	5	-3
1	0	1	1	0	1	5
1	0	1	1	1	-3	5
1	1	0	0	0	1	-1
1	1	0	0	1	-3	-1
1	1	0	1	0	1	3
1	1	0	1	1	-3	3
1	1	1	0	0	1	-5
1	1	1	0	1	-3	-5
1	1	1	1	0	5	-1
1	1	1	1	1	5	3

15. A transceiver (600) comprising the transmitter (200) according to any one of claims 1 to 7 and the receiver (400) according to any one of claims 8 to 14.

100 

	101						102					
	1	2	...	n/3	1	2	...	n/3	1	2	...	n/3
b_0	X	X	...	X	A	A	...	A	B	B	...	C
b_1	A	A	...	A	B	B	...	B	C	C	...	
b_2	A	A	...	A	B	B	...	B	C	C	...	

Fig. 1

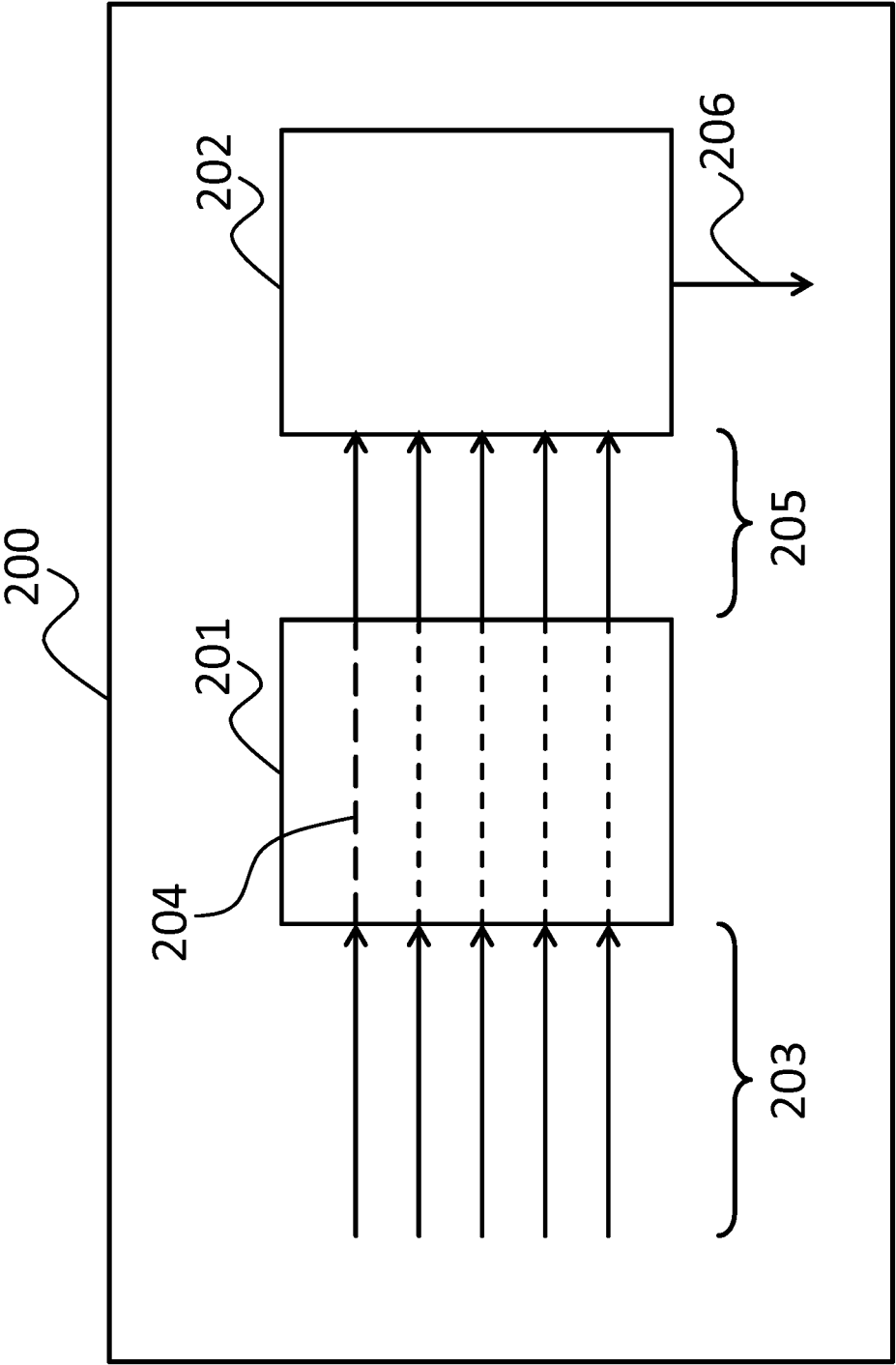


Fig. 2

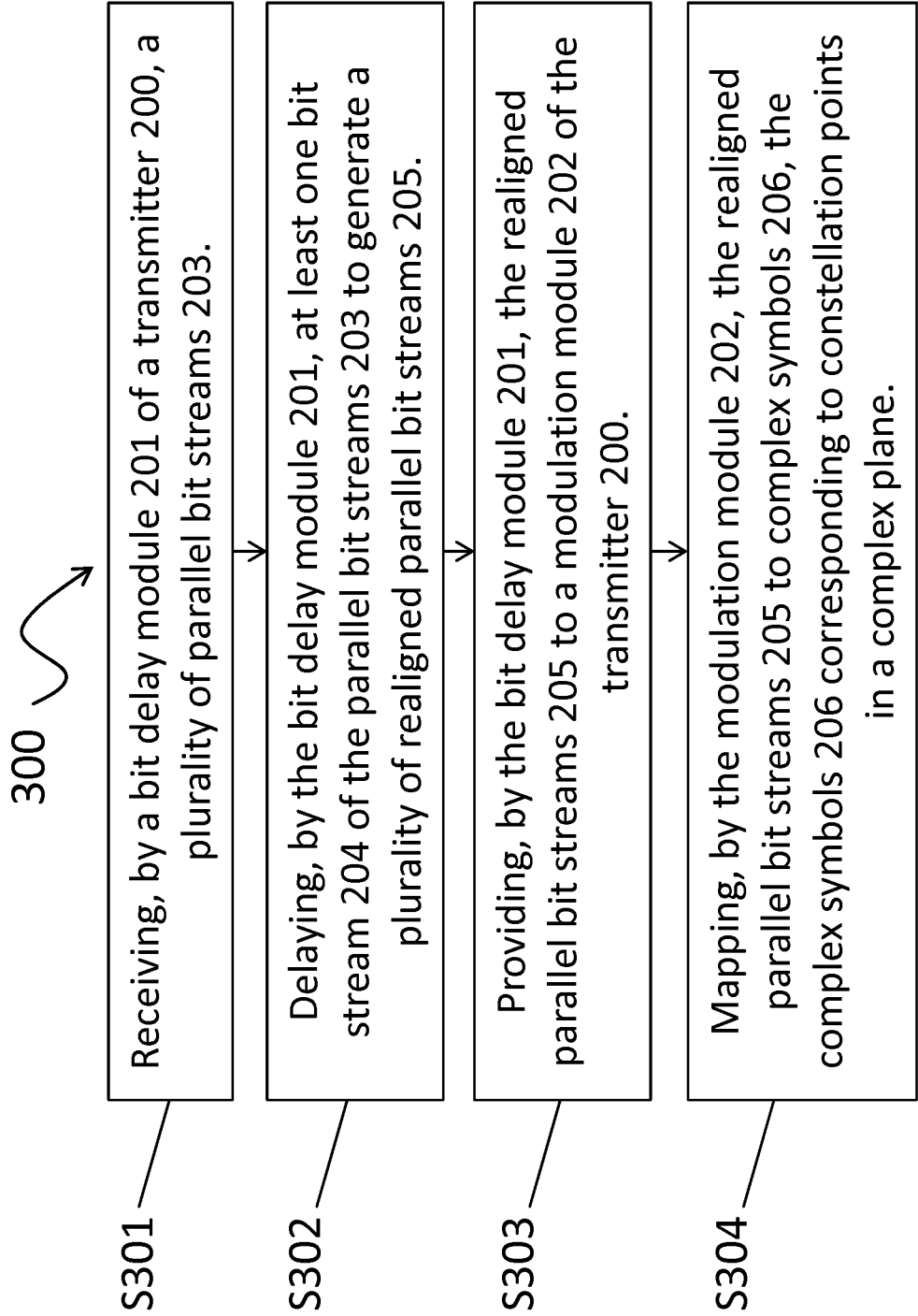


Fig. 3

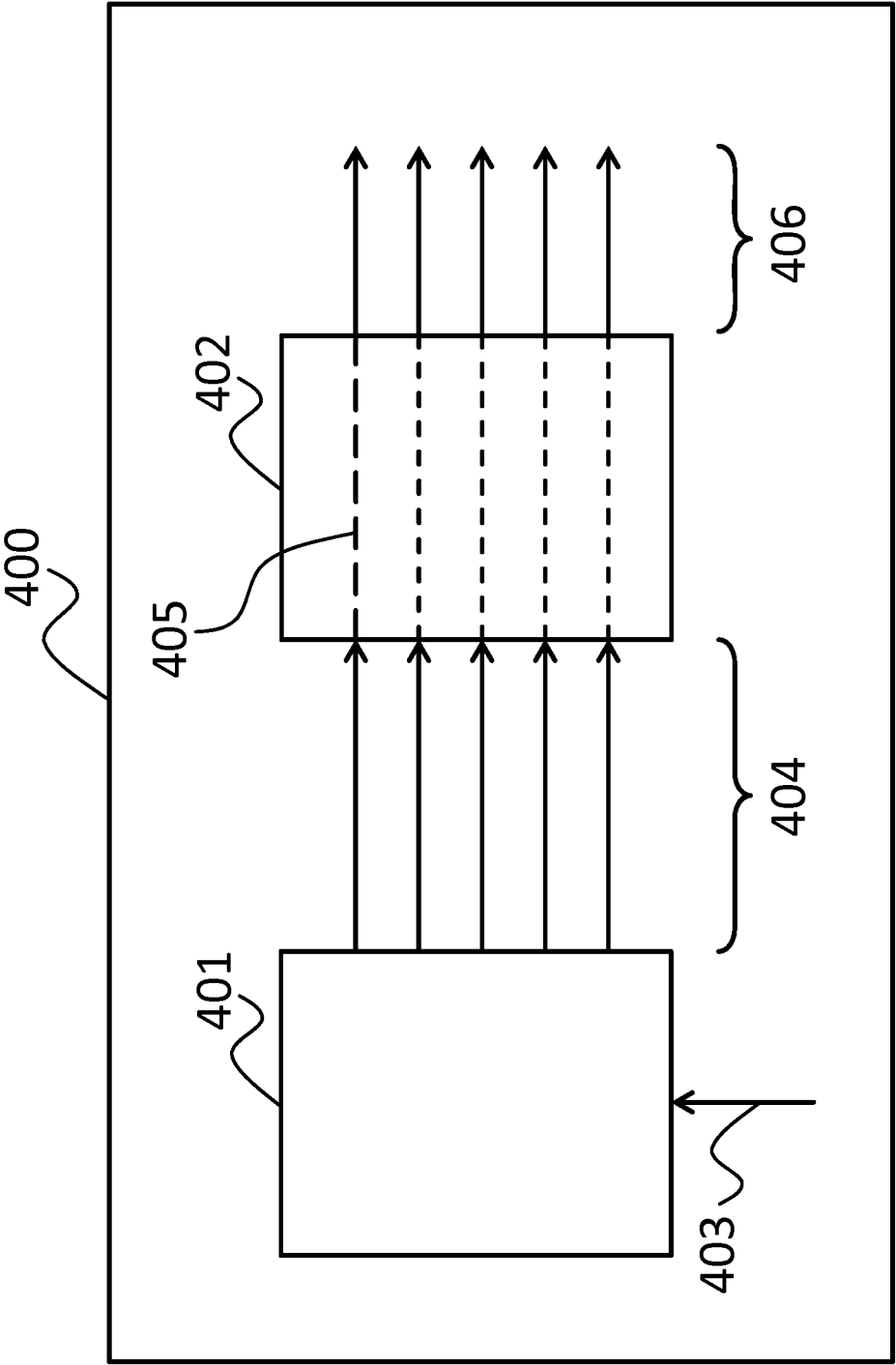


Fig. 4

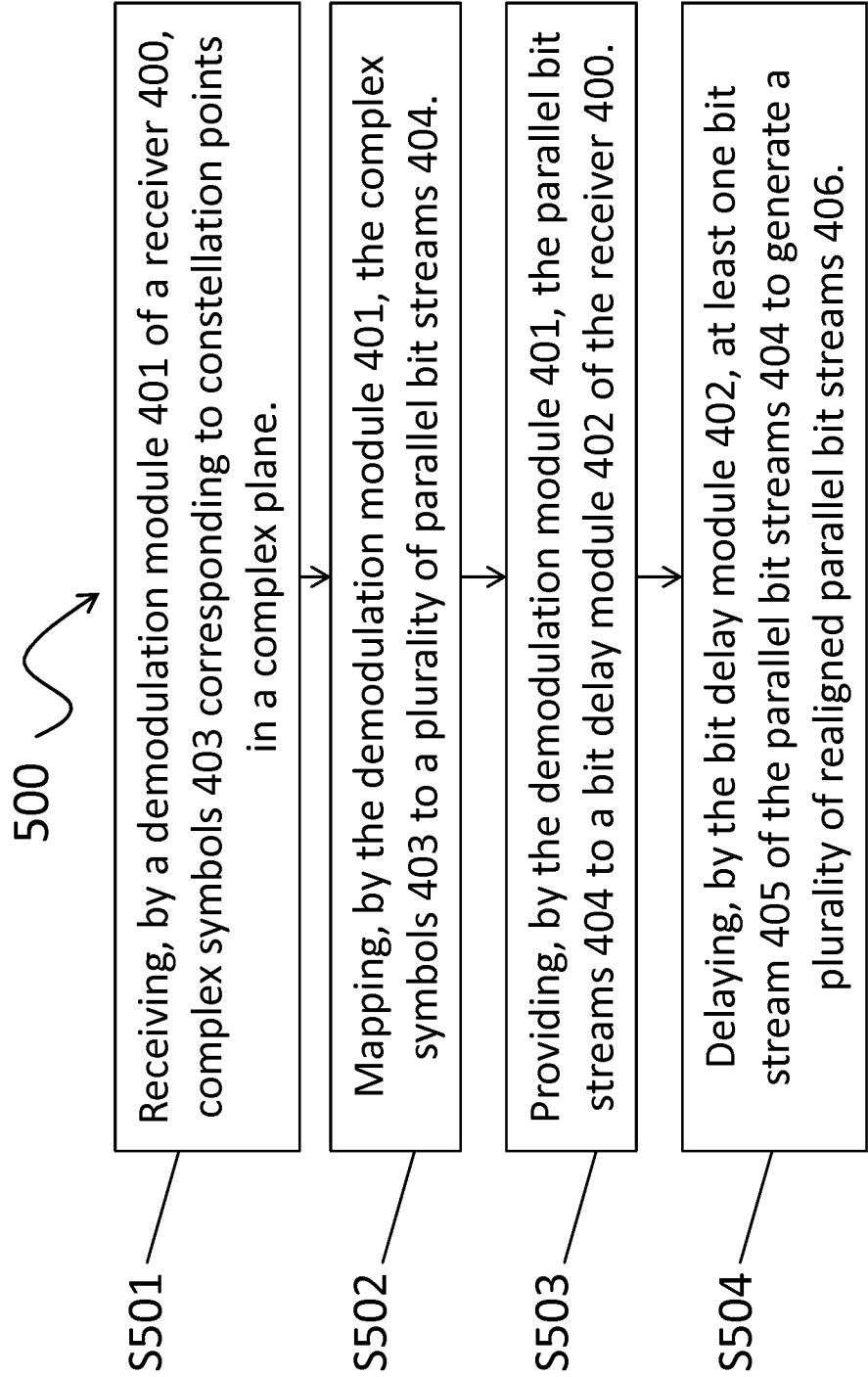


Fig. 5

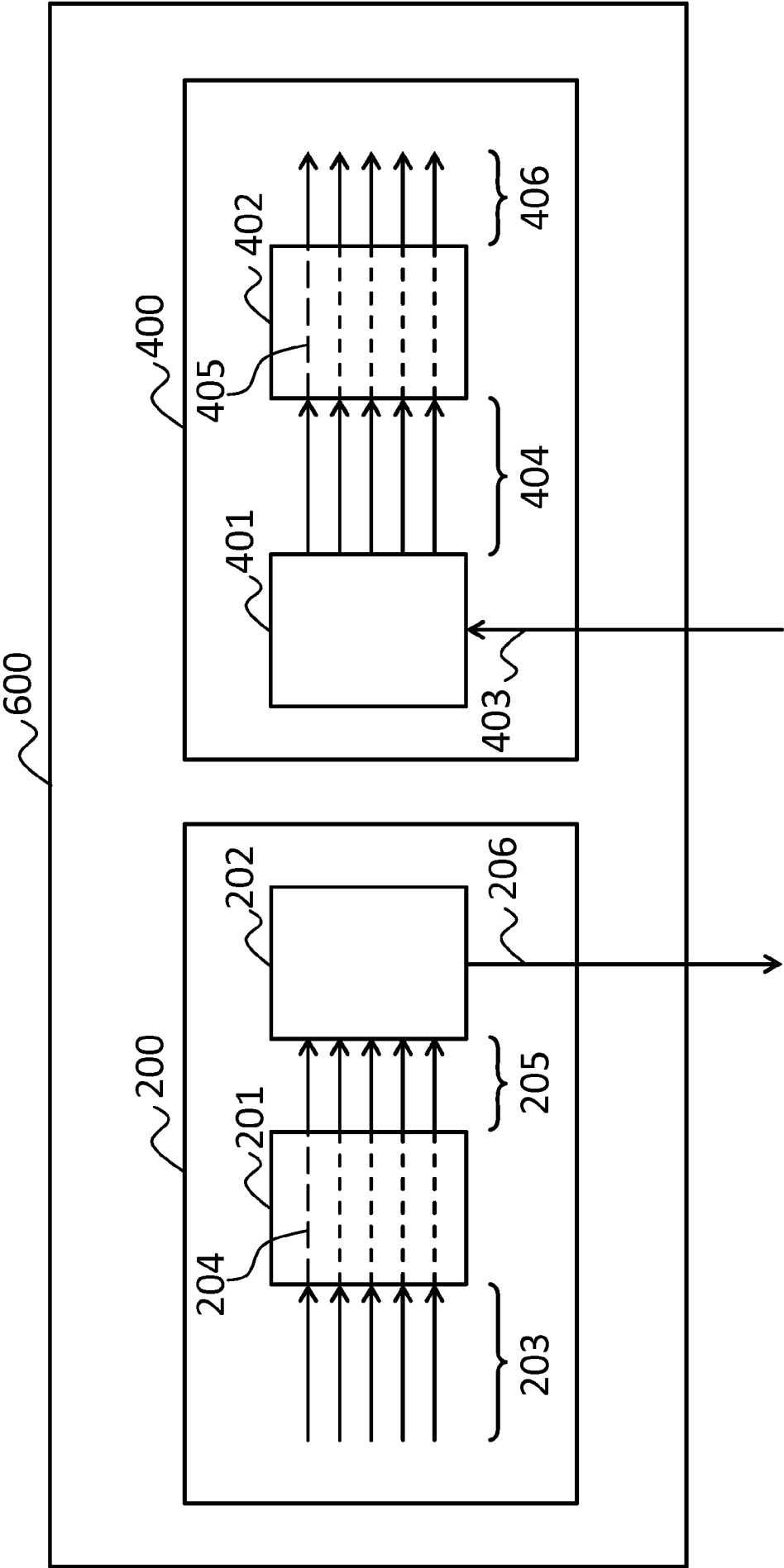


Fig. 6

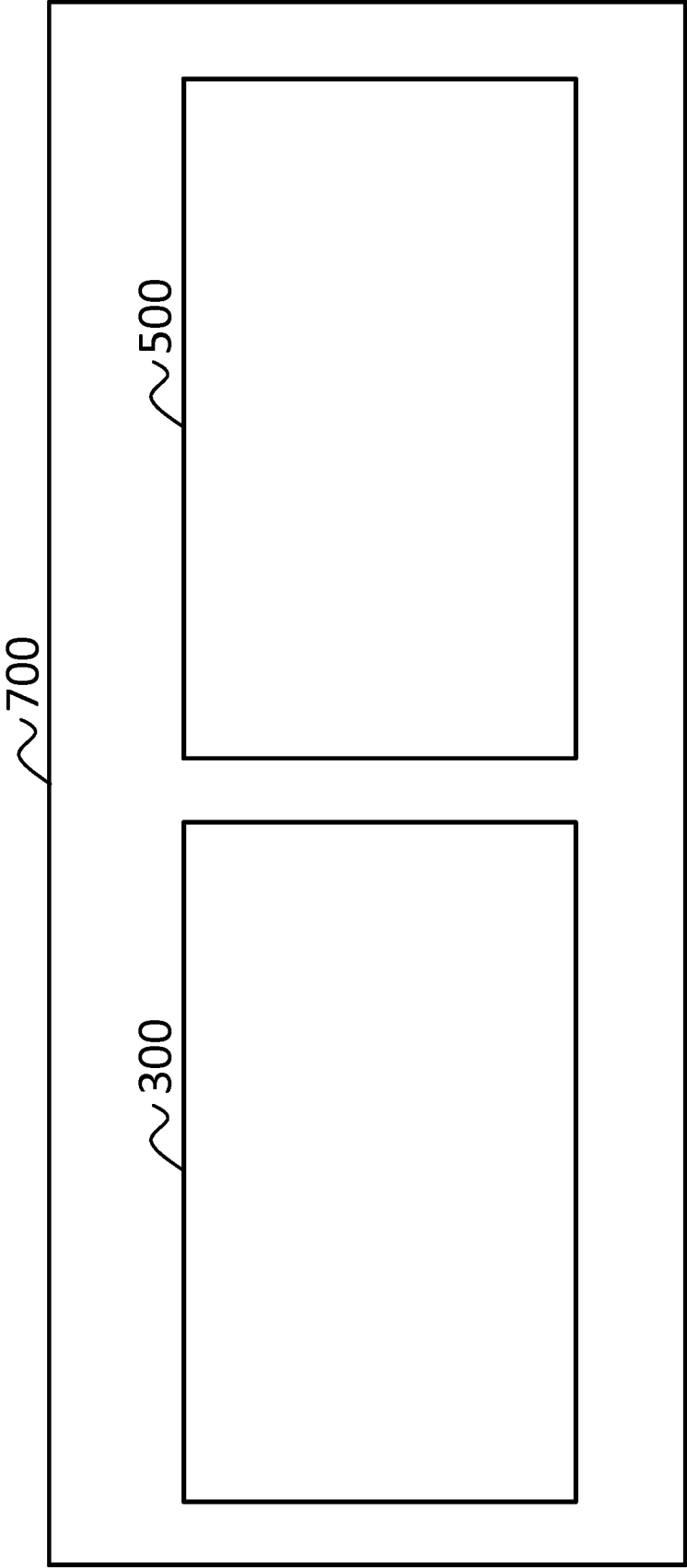


Fig. 7

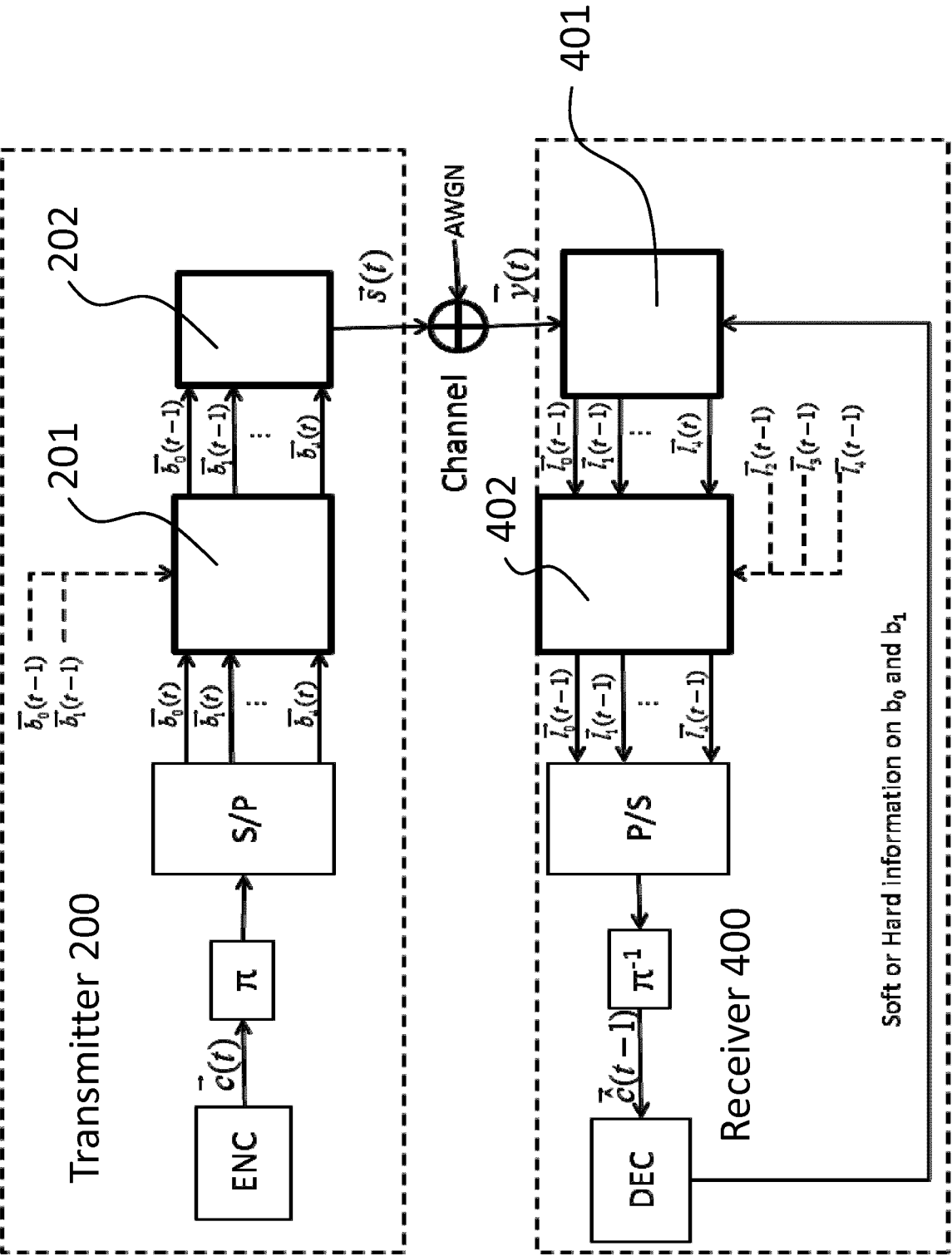


Fig. 8

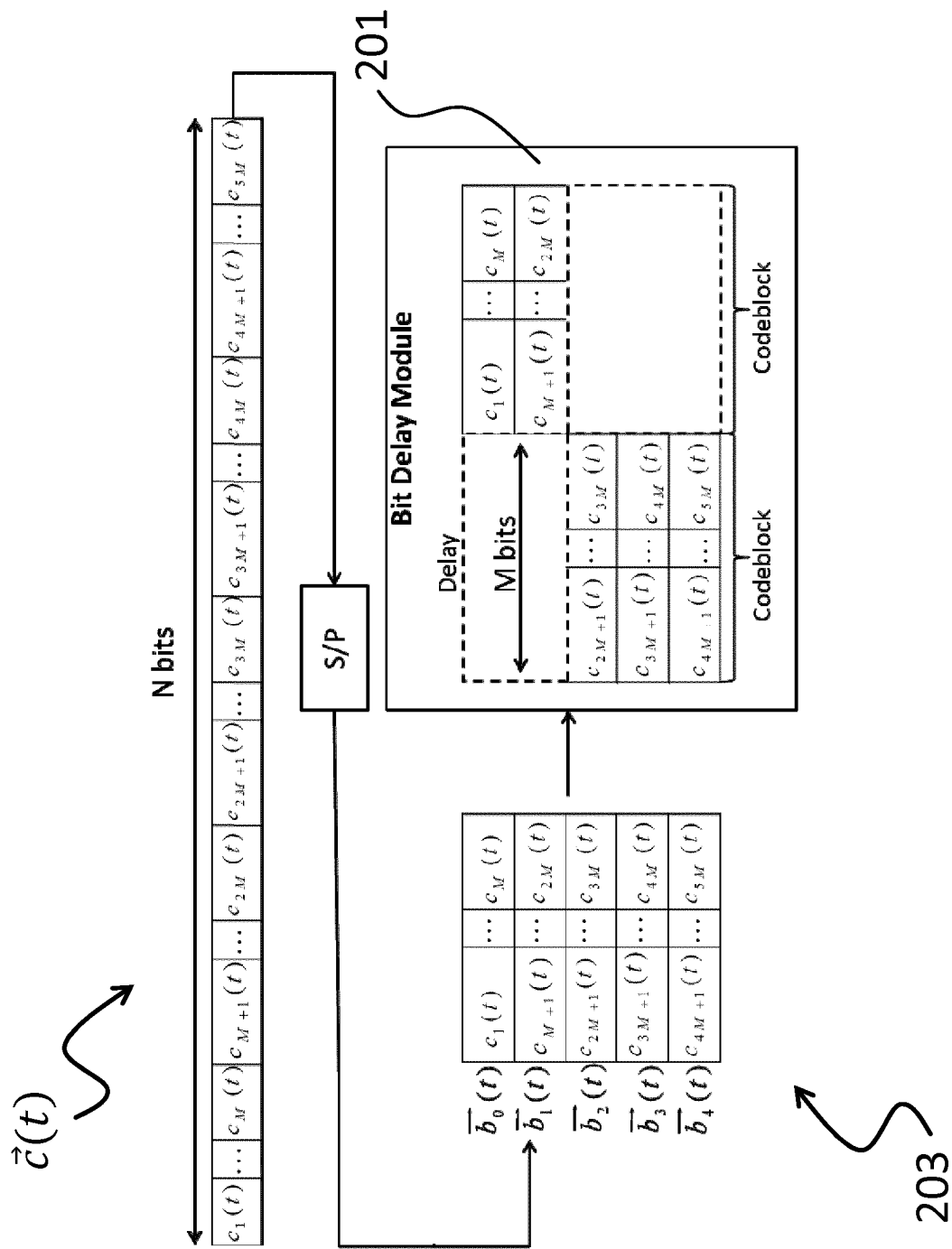


Fig. 9

$c_1(t-1)$	$\dots$	$c_M(t-1)$	$c_1(t)$	$\dots$	$c_M(t)$	$c_1(t+1)$	$\dots$	$c_M(t+1)$
$c_{M+1}(t-1)$	$\dots$	$c_{2M}(t-1)$	$c_{M+1}(t)$	$\dots$	$c_{2M}(t)$	$c_{M+1}(t+1)$	$\dots$	$c_{2M}(t+1)$
$c_{2M+1}(t)$	$\dots$	$c_{3M}(t)$	$c_{2M+1}(t+1)$	$\dots$	$c_{3M}(t+1)$	$c_{2M+1}(t+2)$	$\dots$	$c_{3M}(t+2)$
$c_{3M+1}(t)$	$\dots$	$c_{4M}(t)$	$c_{3M+1}(t+1)$	$\dots$	$c_{4M}(t+1)$	$c_{3M+1}(t+2)$	$\dots$	$c_{4M}(t+2)$
$c_{4M+1}(t)$	$\dots$	$c_{5M}(t)$	$c_{4M+1}(t+1)$	$\dots$	$c_{5M}(t+1)$	$c_{4M+1}(t+2)$	$\dots$	$c_{5M}(t+2)$
Codeblock at time t			Codeblock at time t+1			Codeblock at time t+2		

Fig. 10

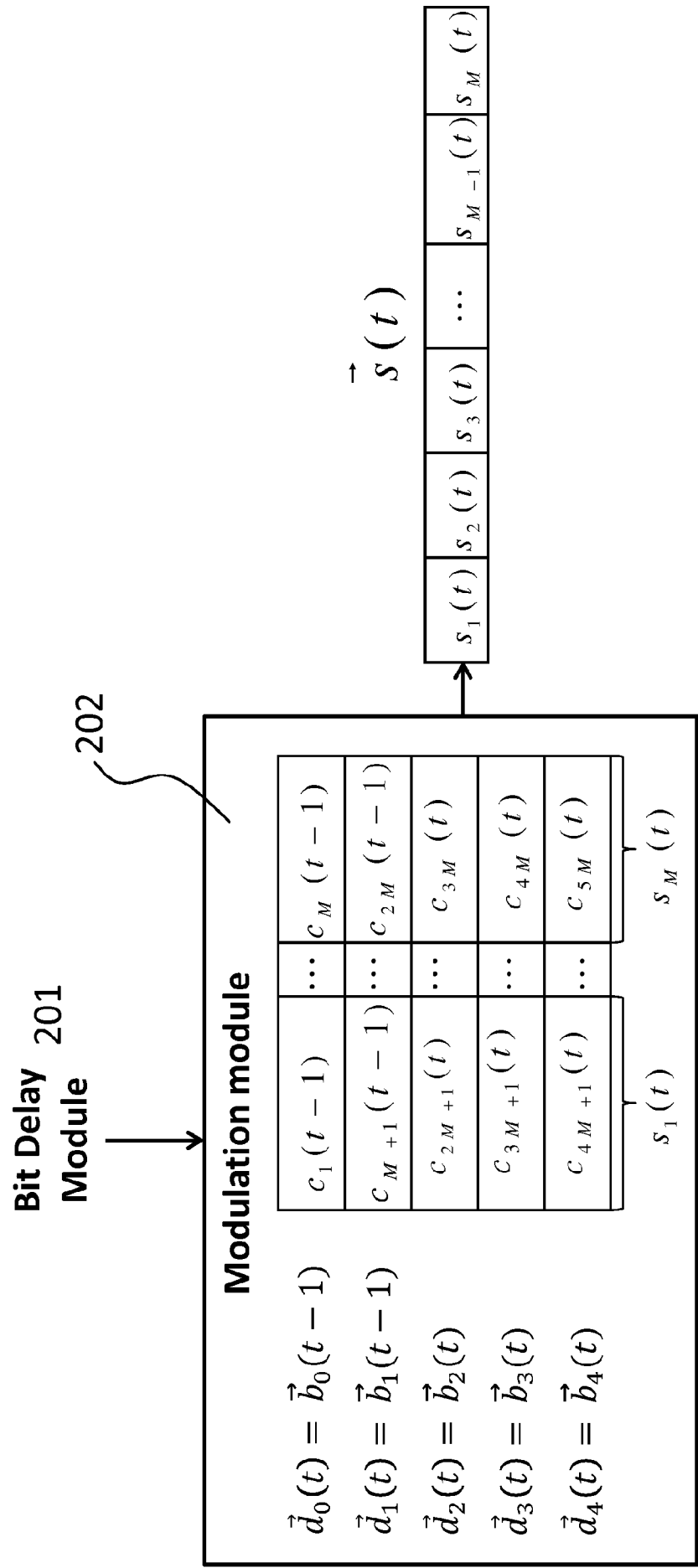


Fig. 11

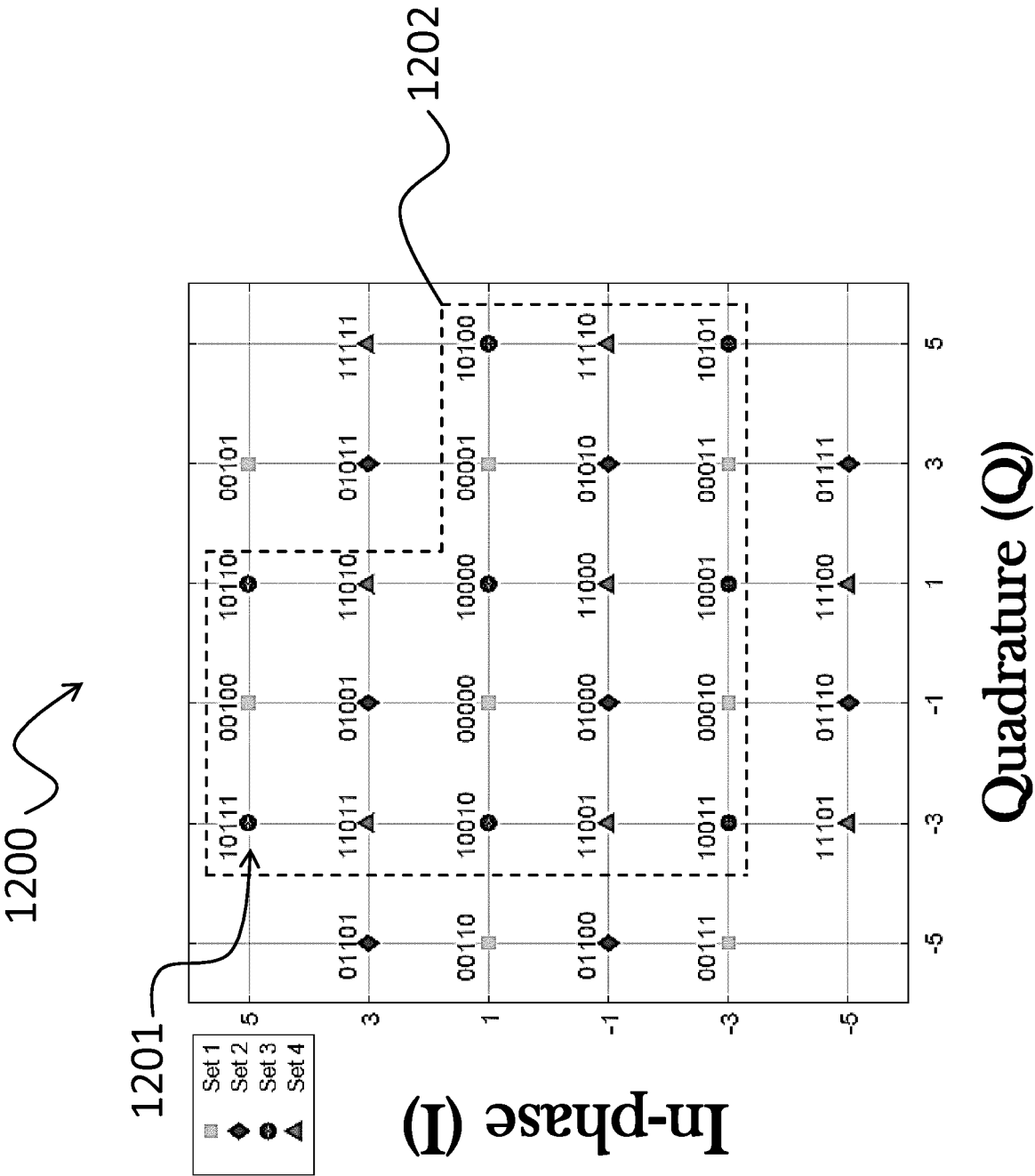


Fig. 12

1302

1300

d_0	d_1	d_2	d_3	d_4	s_1	s_0
A_0	A_1	0	0	0	-1	1
A_0	A_1	0	0	1	3	1
A_0	A_1	0	1	0	-1	-3
A_0	A_1	0	1	1	3	-3
A_0	A_1	1	0	0	-1	5
A_0	A_1	1	0	1	3	5
A_0	A_1	1	1	0	-5	1
A_0	A_1	1	1	1	-5	-3
B_0	B_1	0	0	0	-1	-1
B_0	B_1	0	0	1	-1	3
B_0	B_1	0	1	0	3	-1
B_0	B_1	0	1	1	3	3
B_0	B_1	1	0	0	-5	-1
B_0	B_1	1	0	1	-5	3
B_0	B_1	1	1	0	-1	-5
B_0	B_1	1	1	1	3	-5
C_0	C_1	0	0	0	1	1
C_0	C_1	0	0	1	1	-3
C_0	C_1	0	1	0	-3	1
C_0	C_1	0	1	1	-3	-3
C_0	C_1	1	0	0	5	1
C_0	C_1	1	0	1	5	-3
C_0	C_1	1	1	0	1	5
C_0	C_1	1	1	1	-3	5
D_0	D_1	0	0	0	1	-1
D_0	D_1	0	0	1	-3	-1
D_0	D_1	0	1	0	1	3
D_0	D_1	0	1	1	-3	3
D_0	D_1	1	0	0	1	-5
D_0	D_1	1	0	1	-3	-5
D_0	D_1	1	1	0	5	-1
D_0	D_1	1	1	1	5	3

1301

d_0	d_1	d_2	d_3	d_4	s_1	s_0
0	0	0	0	0	-1	1
0	0	0	0	1	3	1
0	0	0	1	0	-1	-3
0	0	0	1	1	3	-3
0	0	1	0	0	-1	5
0	0	1	0	1	3	5
0	0	1	1	0	-5	1
0	0	1	1	1	-5	-3
0	1	0	0	0	-1	-1
0	1	0	0	1	-1	3
0	1	0	1	0	3	-1
0	1	0	1	1	3	3
0	1	1	0	0	-5	-1
0	1	1	0	1	-5	3
0	1	1	1	0	-1	-5
0	1	1	1	1	3	-5
1	0	0	0	0	1	1
1	0	0	0	1	1	-3
1	0	0	1	0	-3	1
1	0	0	1	1	-3	-3
1	0	1	0	0	5	1
1	0	1	0	1	5	-3
1	0	1	1	0	1	5
1	0	1	1	1	-3	5
1	1	0	0	0	1	-1
1	1	0	0	1	-3	-1
1	1	0	1	0	1	3
1	1	0	1	1	-3	3
1	1	1	0	0	1	-5
1	1	1	0	1	-3	-5
1	1	1	1	0	5	-1
1	1	1	1	1	5	3

Fig. 13

1400 ↗

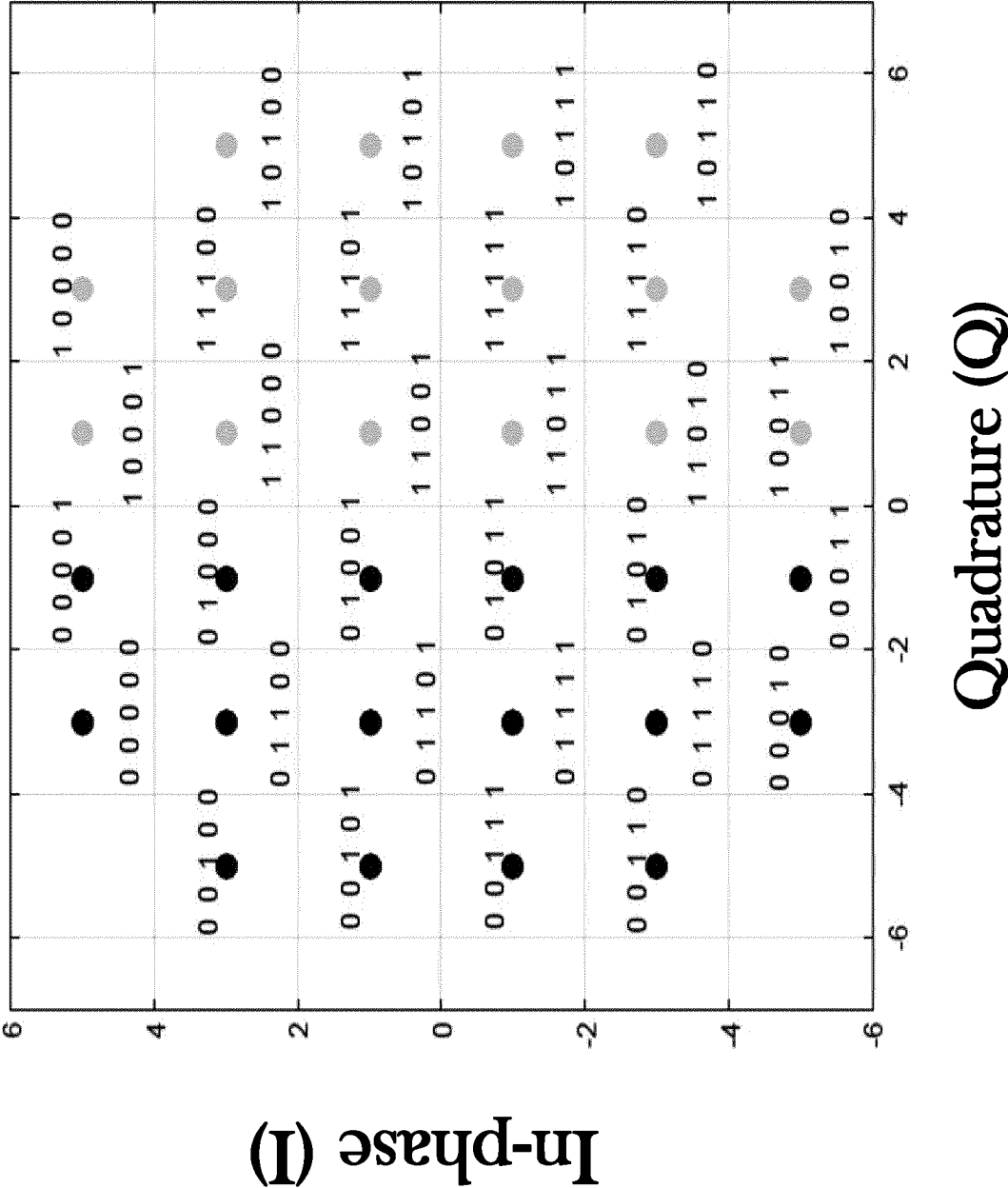


Fig. 14

1500 ↗

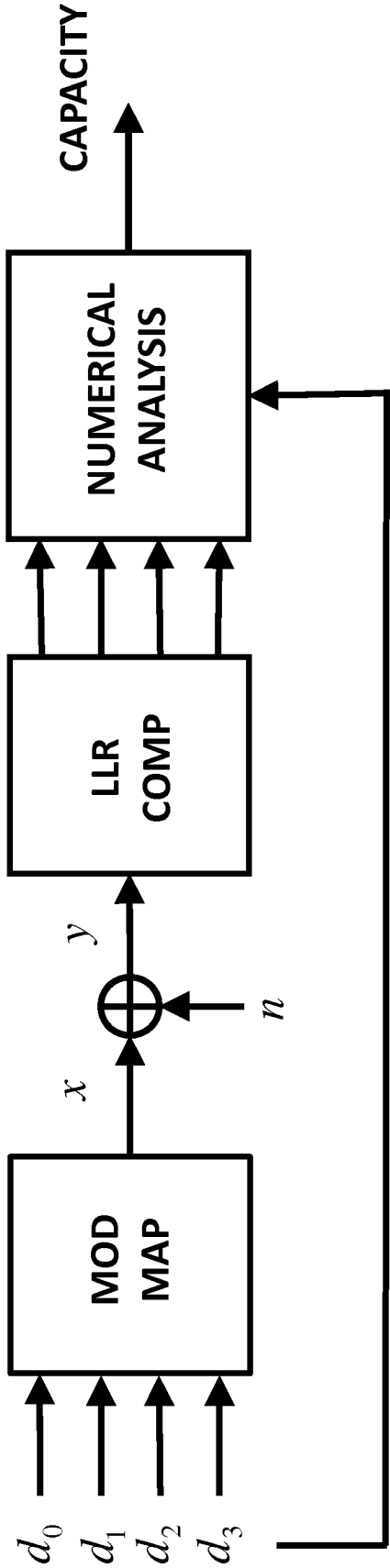


Fig. 15

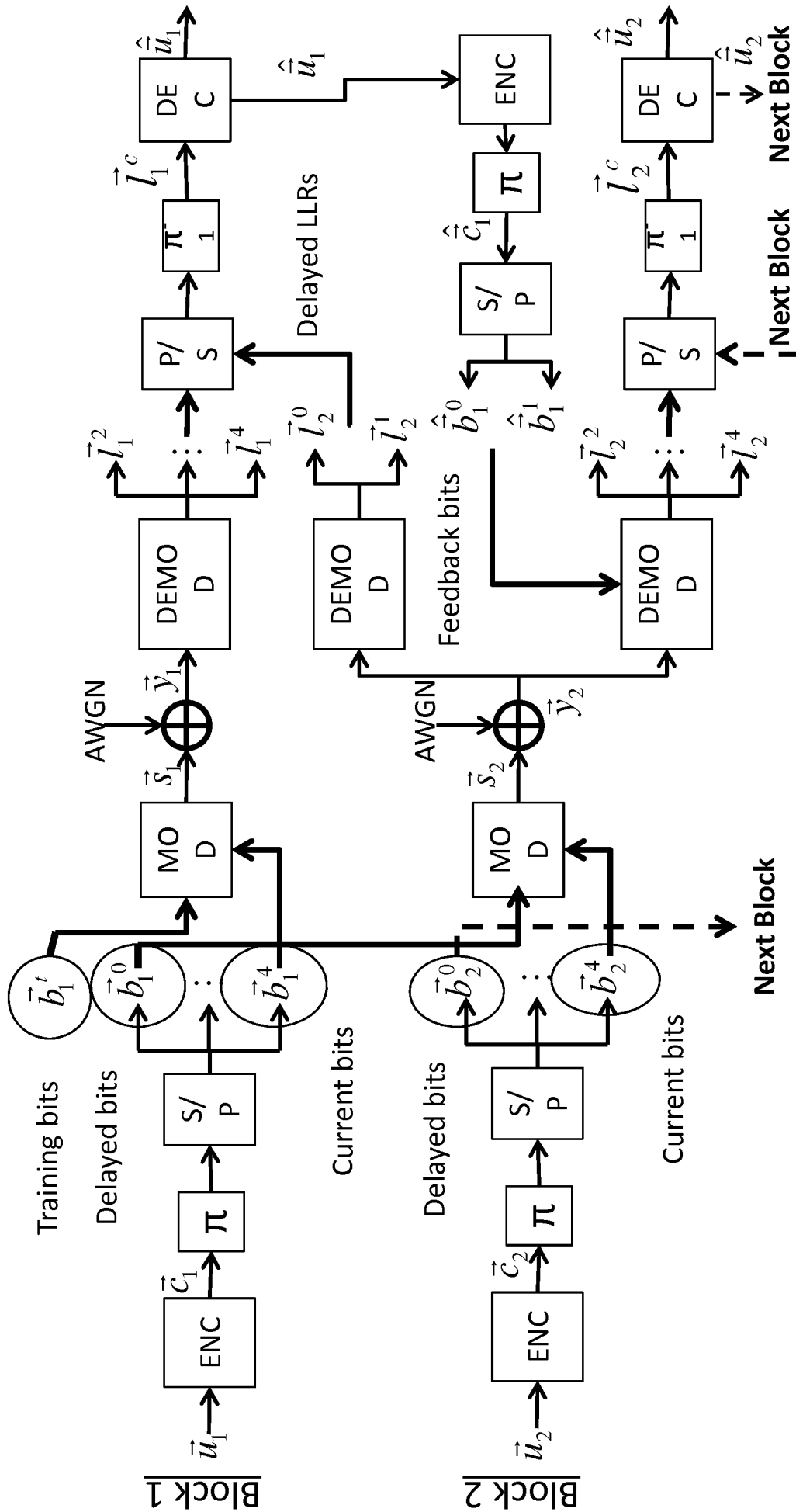


Fig. 16

1700 ↗

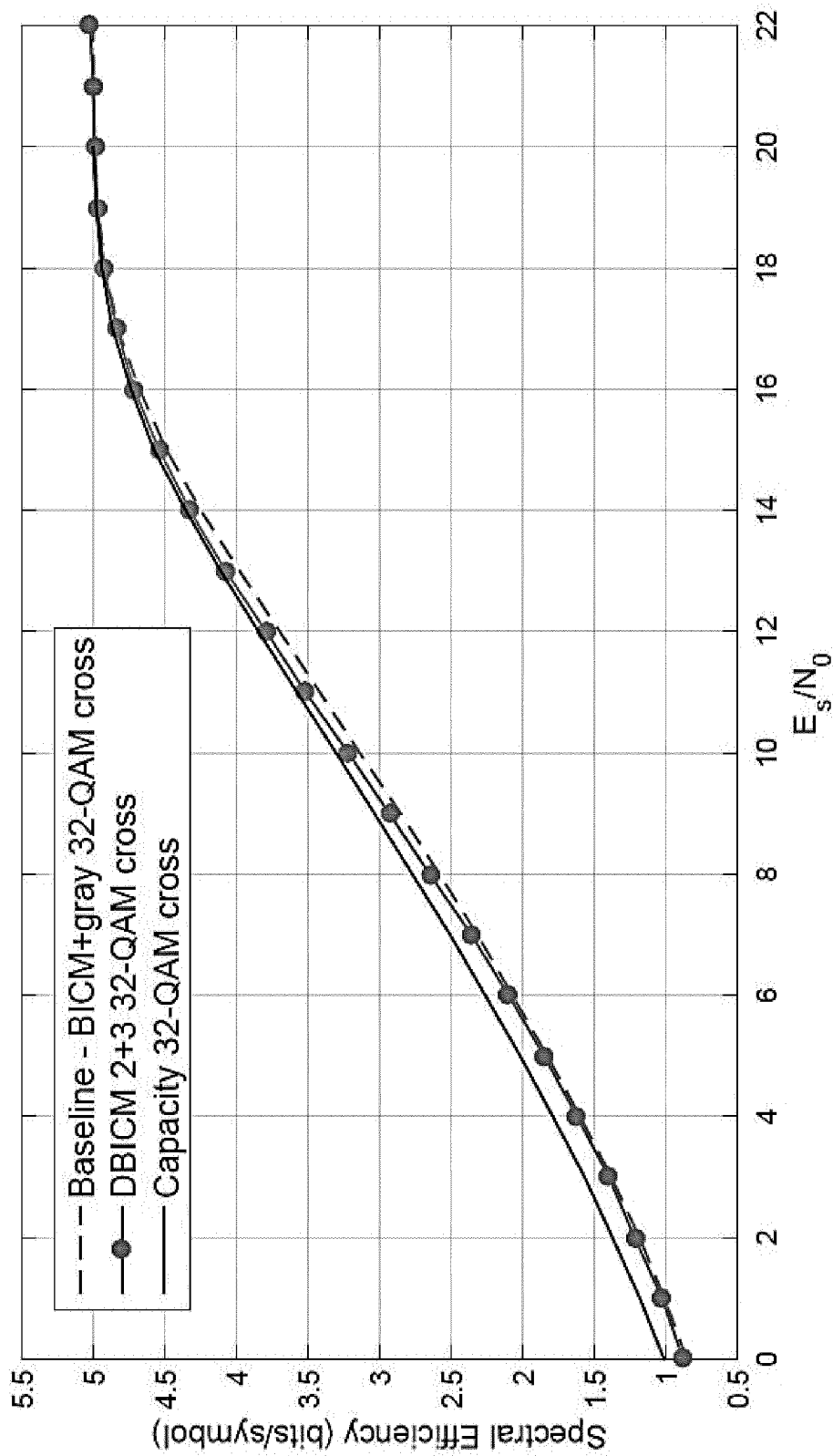


Fig. 17

1800 ↗

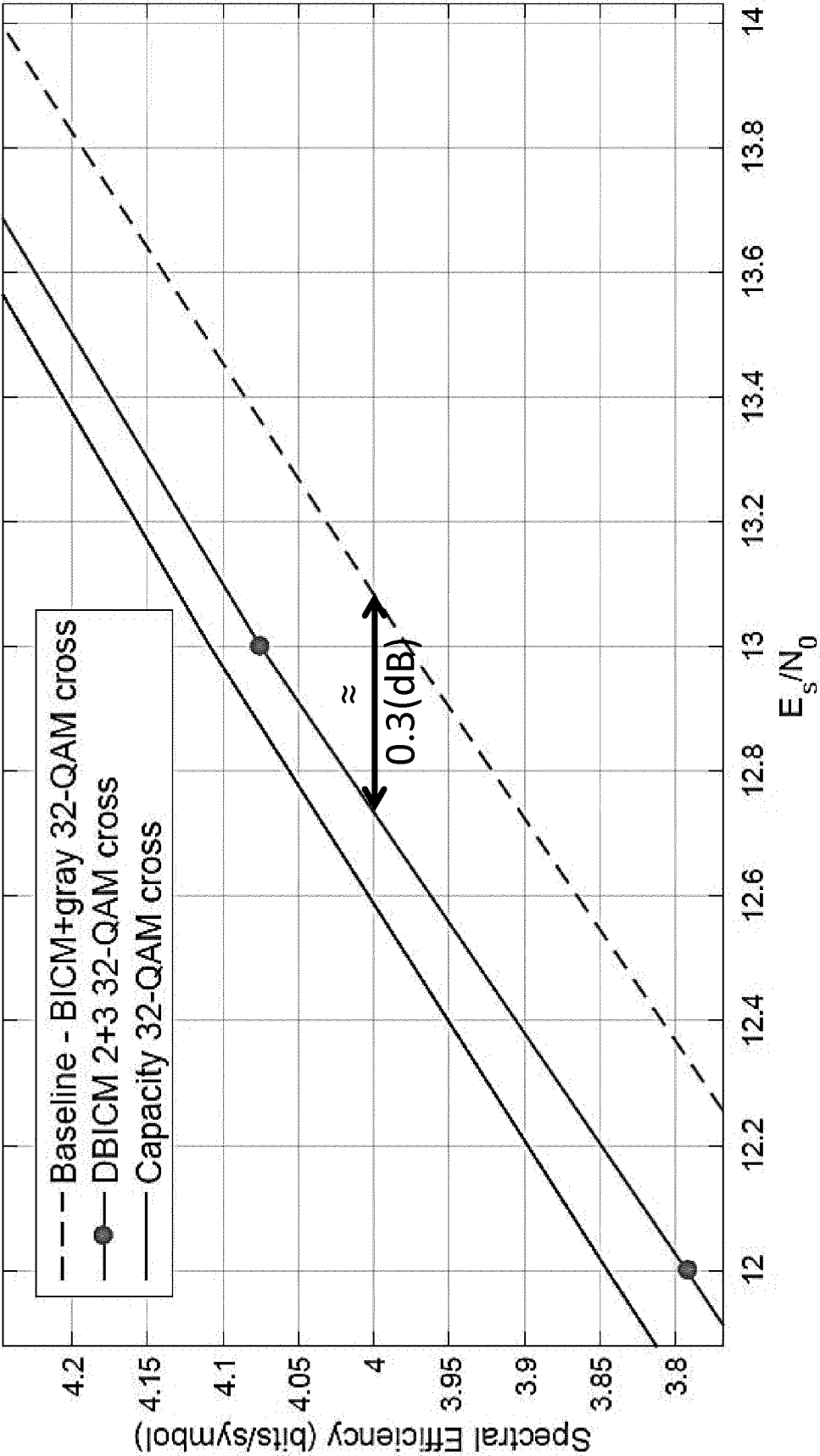


Fig. 18

1900 ↗

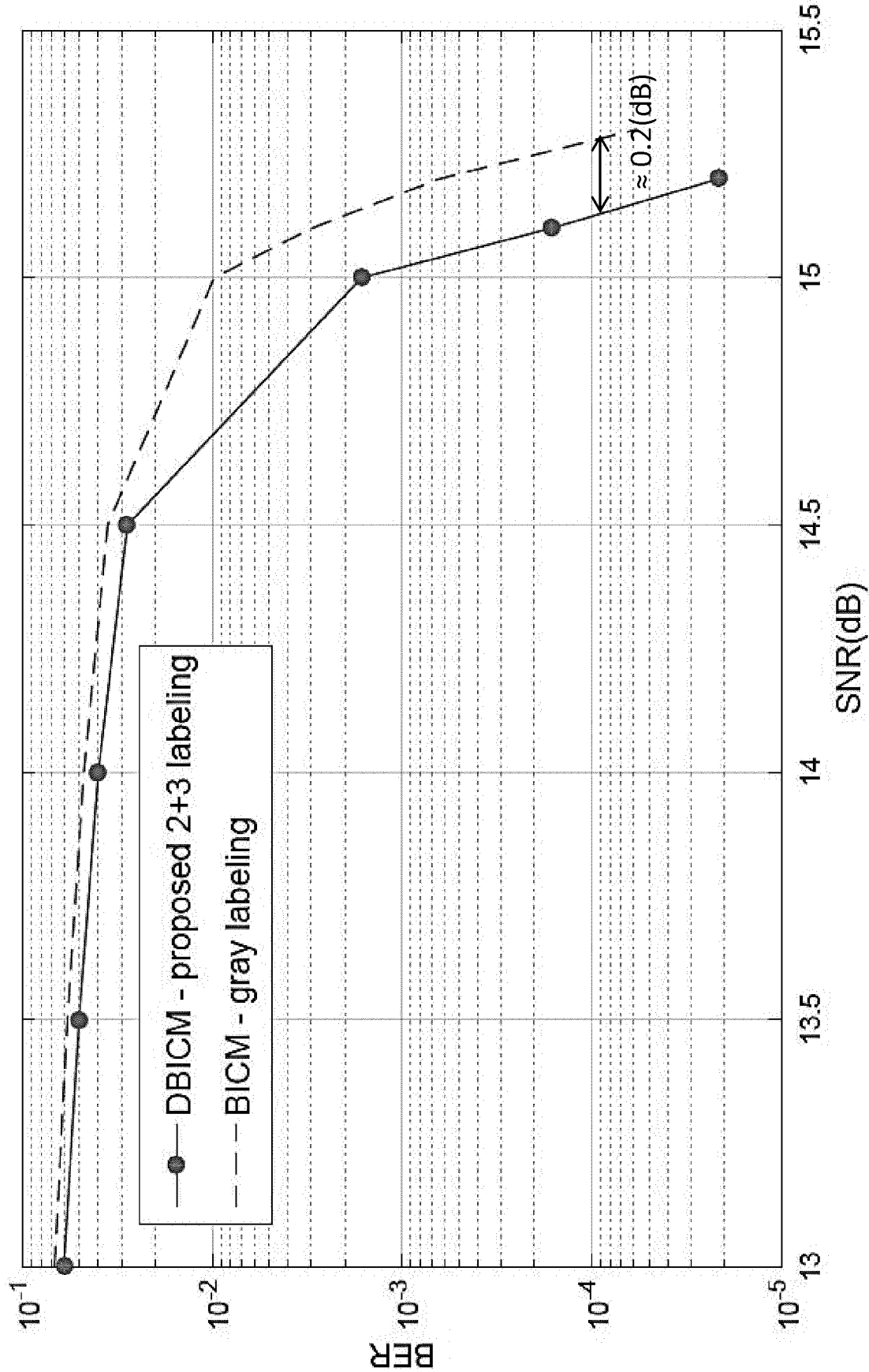


Fig. 19

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/060045

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L1/00 H04L27/34
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MA HUIXIAO ET AL: "Delayed bit interleaved coded modulation", 2016 9TH INTERNATIONAL SYMPOSIUM ON TURBO CODES AND ITERATIVE INFORMATION PROCESSING (ISTC), IEEE, 5 September 2016 (2016-09-05), pages 86-90, XP032981270, DOI: 10.1109/ISTC.2016.7593082 [retrieved on 2016-10-17] cited in the application	1-5, 8-12,15
A	abstract * section II * * sub-section III-B * figures 1-3 ----- -/--	6,7,13, 14



Further documents are listed in the continuation of Box C.



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Date of the actual completion of the international search

12 January 2018

Date of mailing of the international search report

26/01/2018

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Authorized officer

Garrammone, Giuliano

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2017/060045

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	YEONG-LUH UENG ET AL: "Concatenated space-time block coding with trellis coded modulation using a delay processor", IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 6, no. 12, 1 December 2007 (2007-12-01), pages 4452-4463, XP011198742, ISSN: 1536-1276, DOI: 10.1109/TWC.2007.060314	1-5, 8-12,15
A	abstract * section IV * figure 2 -----	6,7,13, 14
A	US 2014/119458 A1 (LIMBERG ALLEN LEROY [US]) 1 May 2014 (2014-05-01) abstract figure 13 -----	1-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2017/060045

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014119458	A1	01-05-2014	NONE
