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(54) SEMICONDUCTOR MEMORY WITH VERTICAL CHARGE-TRAPPING MEMORY CELLS AND FABRICATION

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(57) **ABSTRACT**

A semiconductor device is formed by forming a plurality of trenches in a semiconductor body. The trenches alternate between active trenches and isolation trenches with the isolation trenches being deeper than the active trenches. The semiconductor body is doped so that a top surface of the semiconductor body adjacent each active trench and a floor of each active trench is doped. Memory cell components are formed in each active trench. The memory cell components include a gate electrode and a charge-trapping layer disposed between the gate electrode and a sidewall of the trench. The charge-trapping layer includes a memory layer disposed between first and second limiting layers. Bitlines are formed over the semiconductor body and electrically coupled doped regions adjacent to the top surface of the semiconductor body adjacent the active trenches. Bitline contacts are coupled to the bitlines.

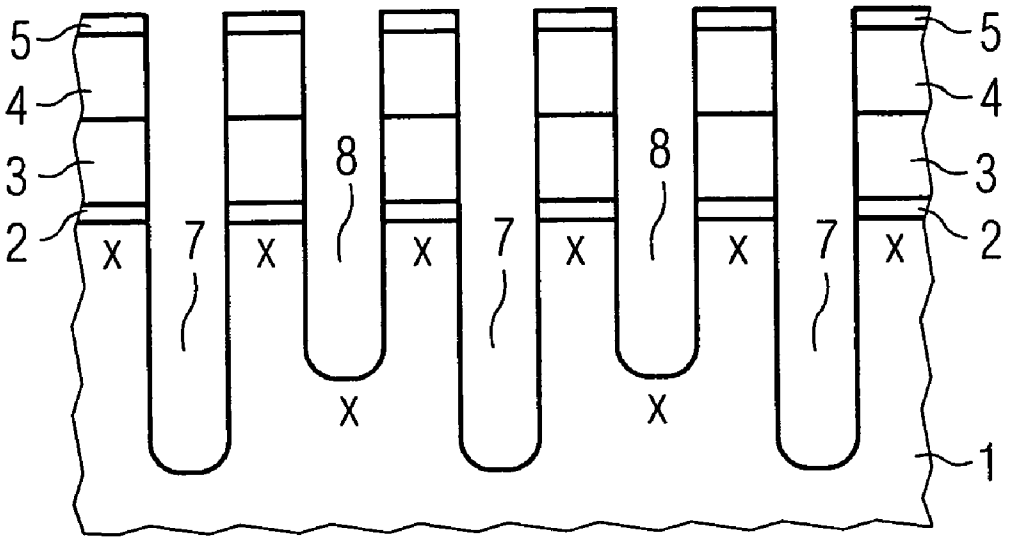


FIG 1

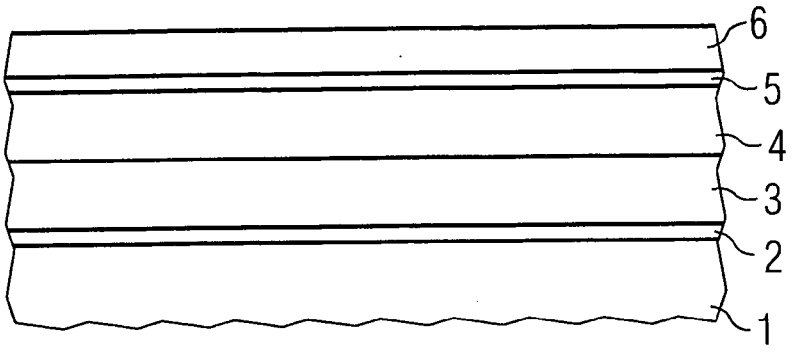


FIG 2

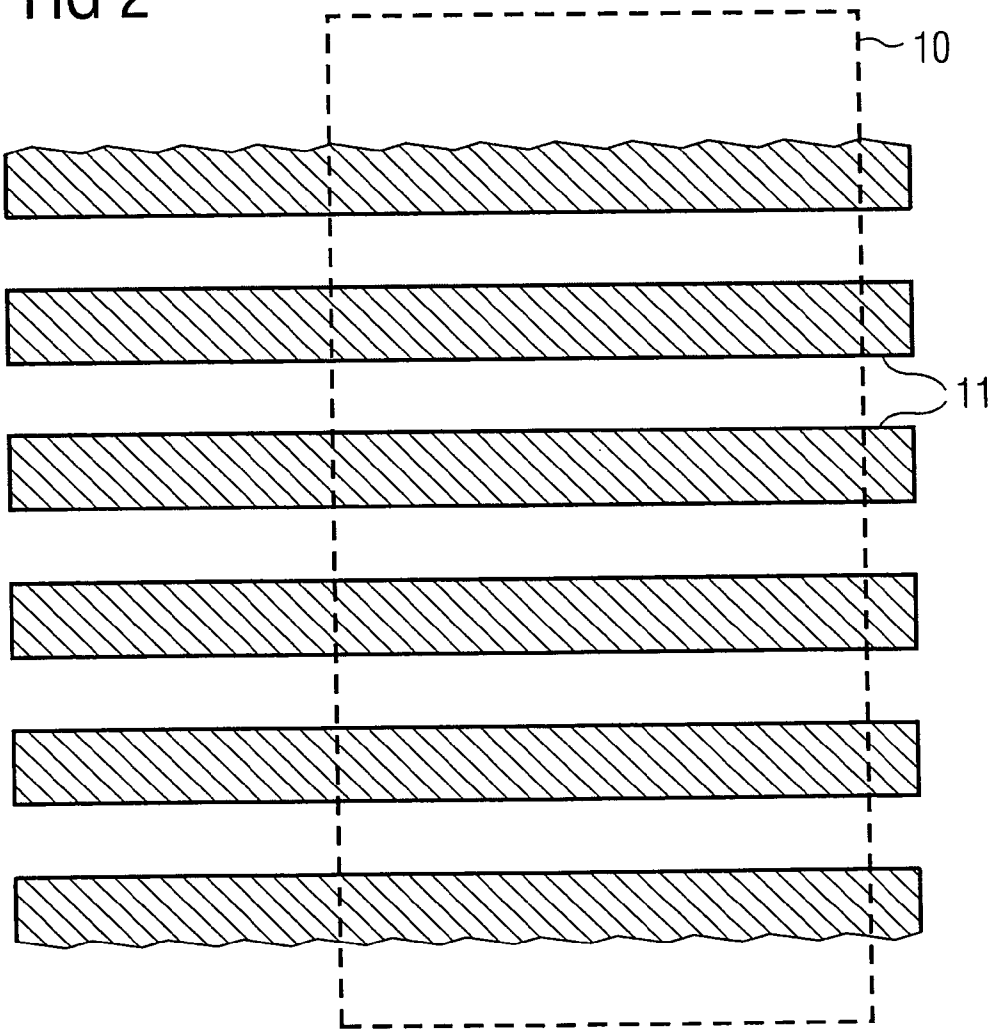


FIG 3

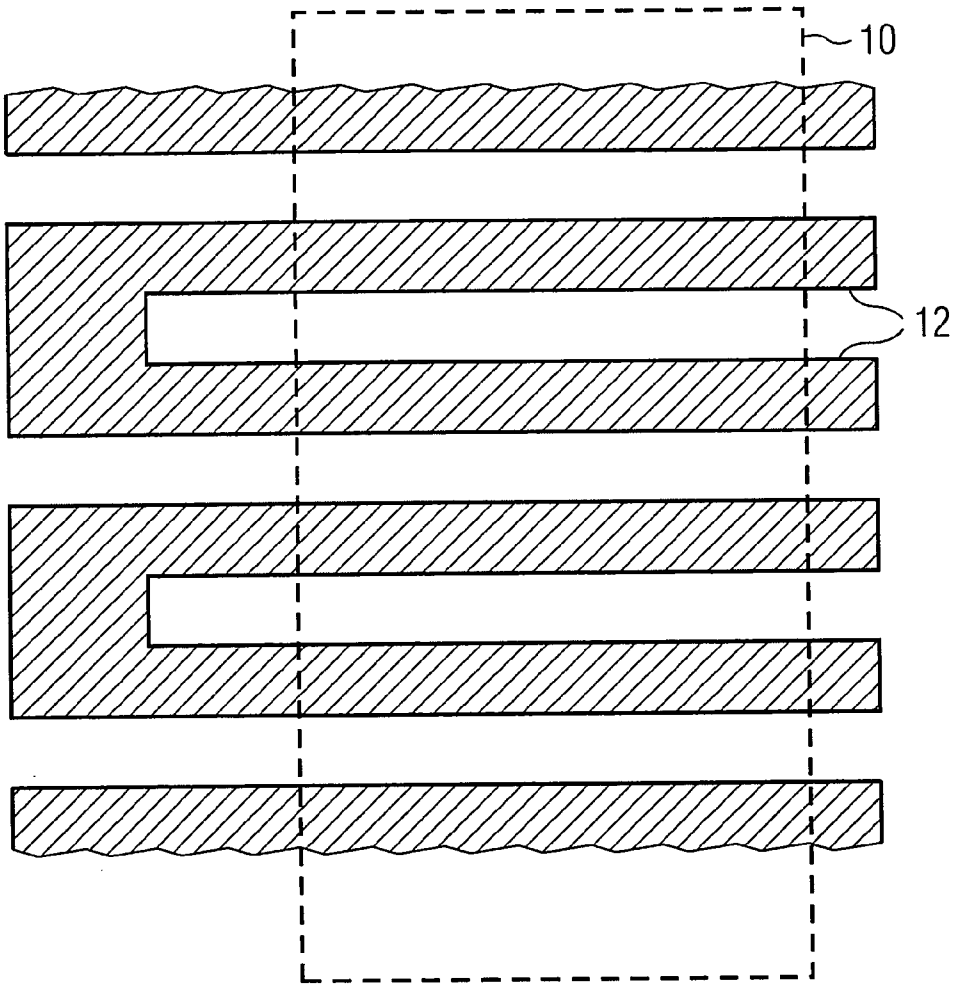


FIG 4

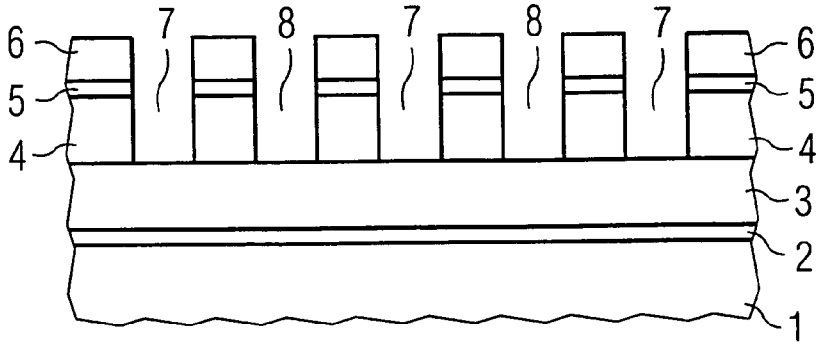


FIG 5

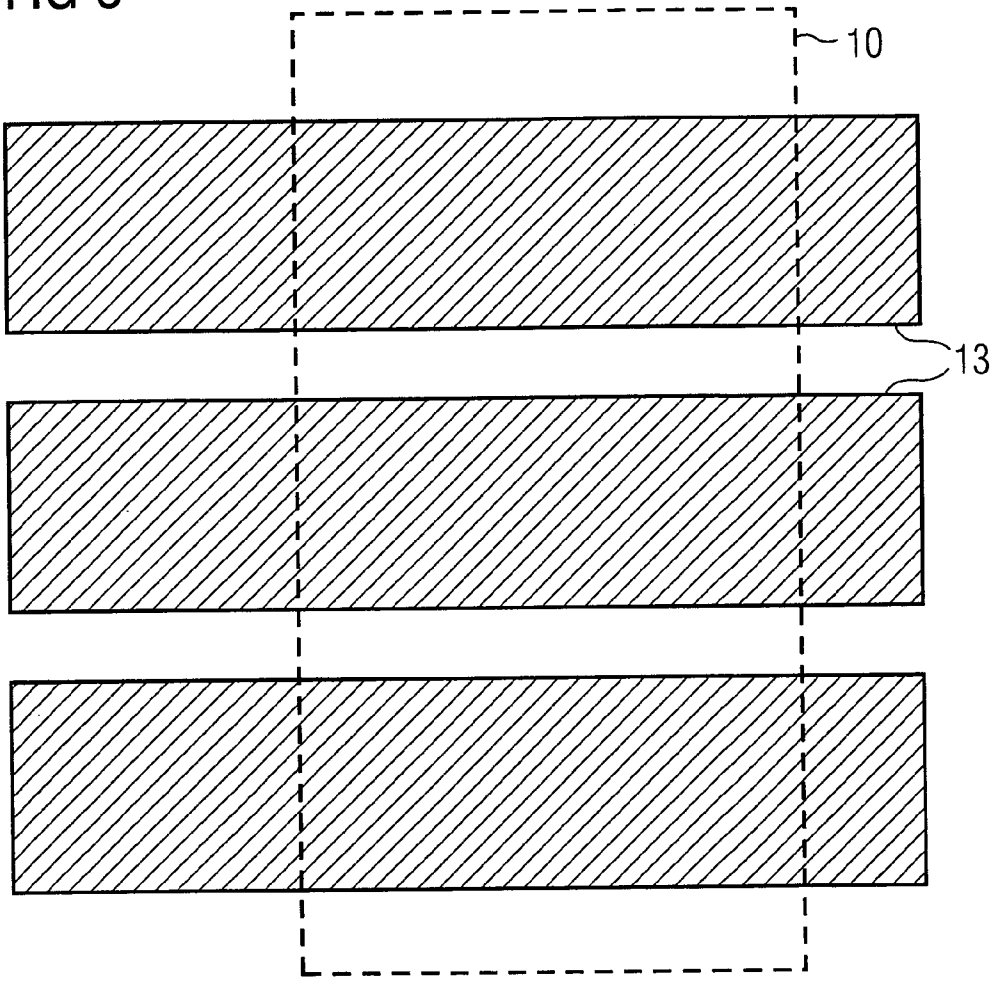


FIG 6

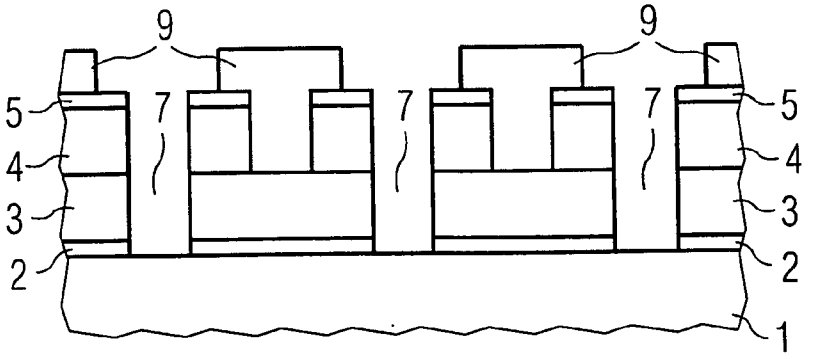


FIG 7

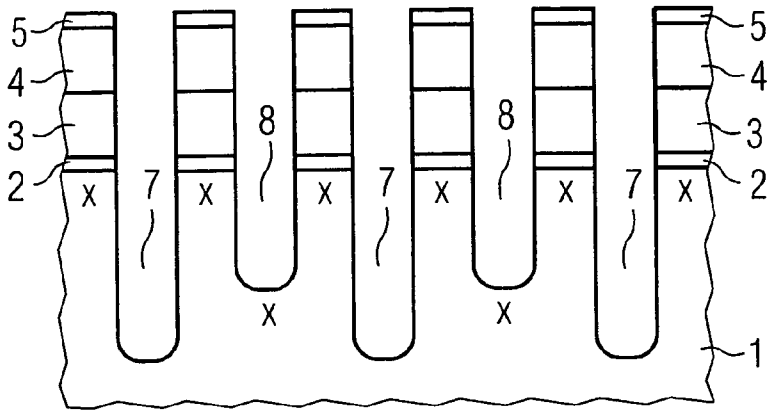


FIG 8

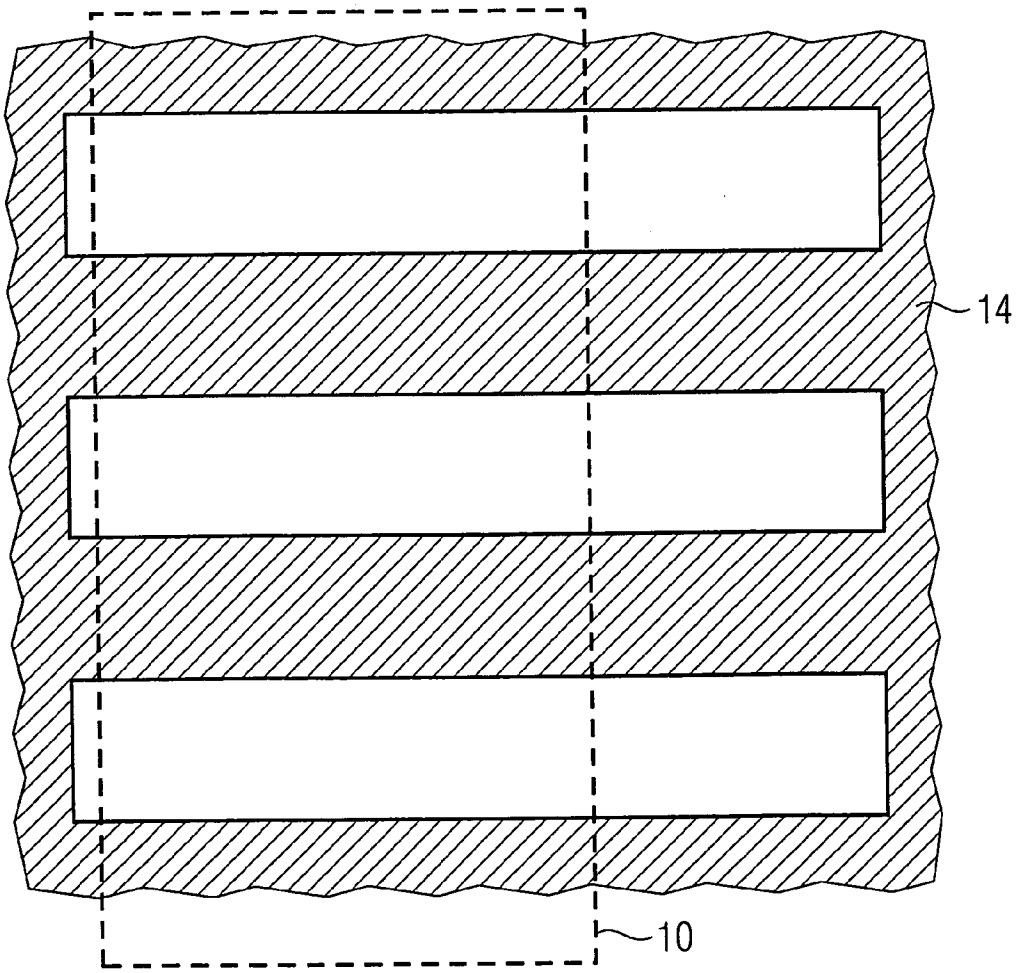
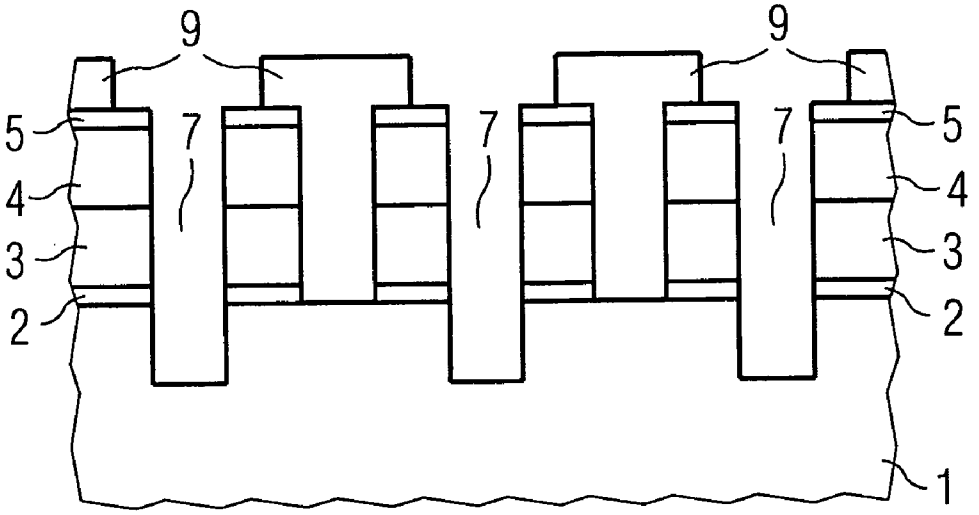


FIG 9



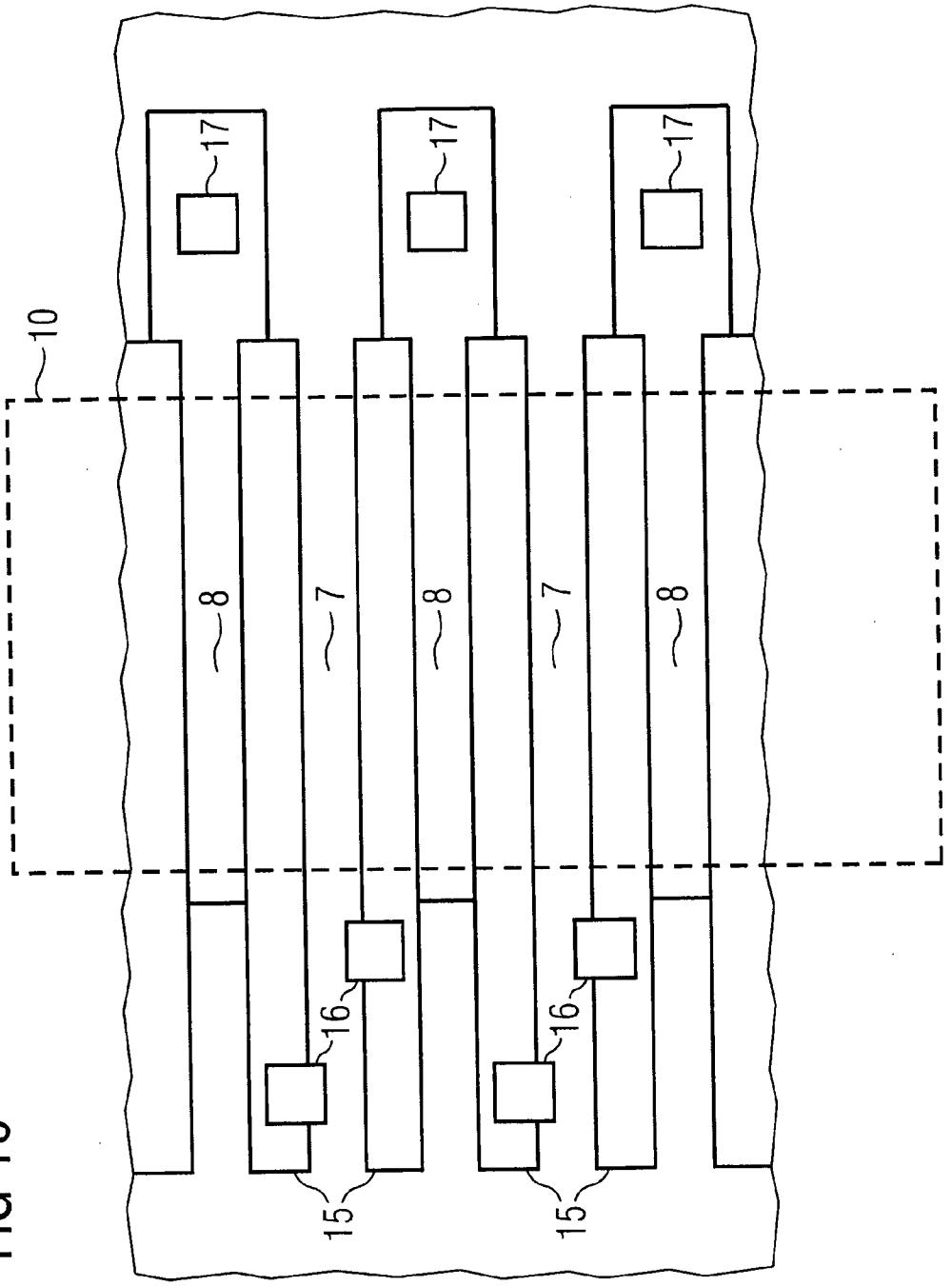


FIG 10

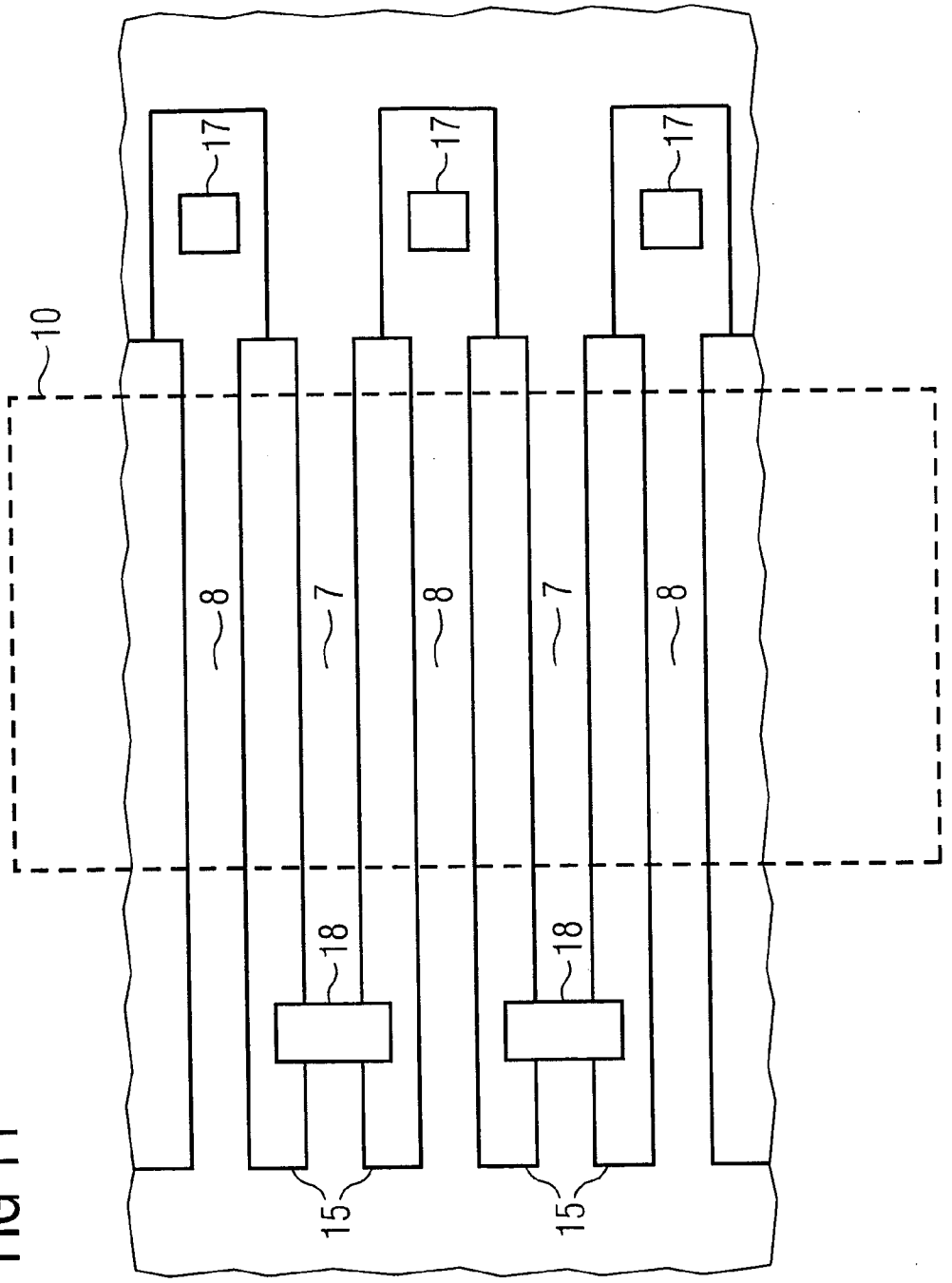


FIG 11

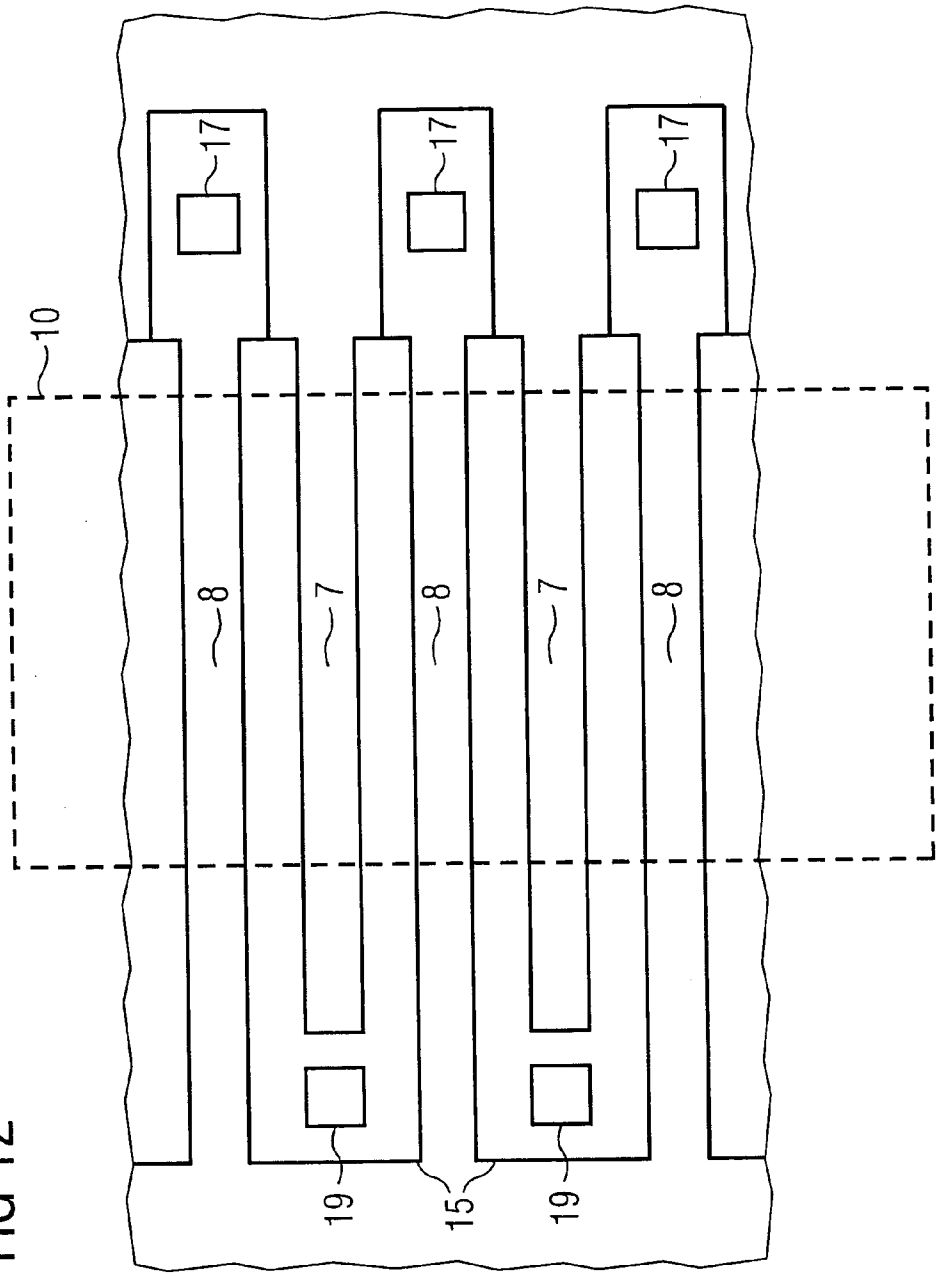


FIG 12

SEMICONDUCTOR MEMORY WITH VERTICAL CHARGE-TRAPPING MEMORY CELLS AND FABRICATION

[0001] This application is a divisional of patent application Ser. No. 10/741,970, entitled "Semiconductor Memory with Vertical Charge-Trapping Memory Cells and Fabrication," filed on Dec. 19, 2003, which application is incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices and, more particularly, to a semiconductor memory with vertical charge-trapping memory cells and a method of fabricating the same.

BACKGROUND

[0003] For further miniaturization of charge-trapping memory cells, especially of NROM (nitride read only memory) memory cells, memory transistors can be arranged on the walls of trenches etched into a semiconductor material. This arrangement significantly reduces the strong dependence of the necessary chip surface area on the thickness of the gate oxide and the channel length of the transistors, as is typical for two-dimensional components. One such semiconductor memory with vertical charge-trapping memory cells consists of a comb-like structure of the semiconductor body or substrate with channel regions in the trench walls. The channel regions are located between source/drain regions that are located at the surface on the edge of the trenches and at the base of the trenches.

[0004] Here, it is difficult to connect the bit line in the trench base. A connection must contact the bit line in the trench base and connect vertically to one of the metallization layers provided for wiring. Within the cell field, the trench for such a contact is too narrow.

SUMMARY OF THE INVENTION

[0005] In one aspect, the present invention discloses a layout for a semiconductor memory with vertical charge-trapping memory cells, which enables economical contacting of the bit lines at the trench base.

[0006] For the semiconductor memory of one embodiment, a comb-like structure is formed on a top side of a semiconductor body or substrate, in which parallel trenches are arranged at intervals to each other. These trenches are alternately isolation trenches and active trenches, wherein the isolation trenches are arranged between the lower bit lines on the trench bases and the active trenches are provided for the memory transistors. Outside a memory cell field, bit-line contacts are present on the top bit lines and additional bit-line contacts are present on the lower bit lines and are each connected in an electrically conductive way to a metallization layer provided for wiring. Further, the bit-line contacts for the upper bit lines and the additional bit-line contacts for the lower bit lines are mounted on opposing sides of the memory cell field and portions of the isolation trenches are arranged between the additional bit-line contacts.

[0007] These isolation trenches can be generated together with the isolation trenches in the core and in the periphery of the memory chip. This is performed in a known way like the method of STI (shallow trench isolation). During fabrication, lithography masks are used for structuring the isolation trenches and the active trenches and also for structuring the regions provided for the bit-line contacts. The STI trenches in the core and in the periphery of the chip are generated simultaneously.

[0008] Nitride read only memory (NROM) devices are disclosed in a number of prior art references. For example, U.S. Pat. No. 5,966,603 ('603) teaches a method of fabricating an NROM chip. U.S. Pat. No. 6,583,079 ('079) discloses a non-volatile read only memory transistor that includes a substantially vertically oriented channel fabricated in a trench formed in a substrate. The '603 and '079 patents are incorporated herein by reference.

[0009] U.S. Pat. No. 6,486,028, which is incorporated herein by reference, discloses a method for fabricating a nitride read only device. A trench is formed in a semiconductor substrate. An ion implantation is performed to form a first source/drain region and a second source/drain region within the substrate in the upper corners of the trench, and to form a common source/drain region within the substrate at a bottom of the trench. Next, a trapping layer is formed over the substrate and the trench and a gate conducting layer is formed over the substrate and filling the trench.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] In the following, a more detailed description of examples of the semiconductor memory and the fabrication method is given with reference to **FIGS. 1-12**.

[0011] **FIG. 1** shows a first intermediate product in cross section.

[0012] **FIG. 2** shows the structure of a first lithography mask in a top view.

[0013] **FIG. 3** shows an alternative example of the first lithography mask in a top view.

[0014] **FIG. 4** shows a second intermediate product in cross section.

[0015] **FIG. 5** shows the structure of a second lithography mask in a top view.

[0016] **FIG. 6** shows a third intermediate product in cross section.

[0017] **FIG. 7** shows a fourth intermediate product in cross section.

[0018] **FIG. 8** shows the structure of a third lithography mask in a top view.

[0019] **FIG. 9** shows the intermediate product from **FIG. 6** for an alternative configuration of the method in cross section.

[0020] **FIG. 10** shows a schematic of a first embodiment of the memory chip in a top view.

[0021] **FIG. 11** shows a schematic of a second embodiment of the memory chip in a top view.

[0022] **FIG. 12** shows a schematic of a third embodiment of the memory chip in a top view.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0023] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0024] In **FIG. 1**, a semiconductor body **1**, e.g., a substrate, is shown in cross section with a pad oxide layer **2** deposited on this body, a pad nitride layer **3** deposited on the oxide layer **2**, a hard mask layer **4** deposited on the nitride layer **3**, an anti-reflex layer **5** (e.g., anti-reflection coating or ARC layer) deposited on this mask layer **4**, and a photoresist layer **6** deposited on the anti-reflex layer **5**. The material of the hard mask layer **4** is, e.g., an oxide deposited by the decomposition of TEOS (tetraethylorthosilicate). The anti-reflex layer **5** is used to simplify the subsequent photolithography.

[0025] This lithography is performed by means of a first lithography mask **11**, which is shown schematically in **FIG. 2** in a top view and which has the structure indicated in **FIG. 2** so that a photoresist mask produced with this method covers the cross-hatched regions. The cross-hatched regions extend at the sides beyond the provided memory cell field **10**. Therefore, with this first lithography mask **11**, strip-like regions in the area of the memory cell field and also large surface-area regions at the periphery are removed by the photoresist layer **6**. According to whether a positive or a negative photoresist is used, i.e., whether the illuminated portions are to be removed or preserved, the first lithography mask **11** has openings in the cross-hatched regions or a complementary structure.

[0026] **FIG. 3** shows an alternative configuration of the first lithography mask **12**, for which the cross-hatched regions, which are covered by the produced photoresist layer, are combined in pairs outside the memory cell field **10**. This configuration is especially suitable for the fabrication of flash memory cells.

[0027] **FIG. 4** shows in cross section how the structured photoresist layer **6** is used to etch parallel, strip-like openings arranged at intervals to each other in the anti-reflex layer **5** and the hard mask layer **4**. Here, openings for isolation trenches **7** and openings for active trenches **8** are provided. Here, the term "active trench" means that the relevant trench is provided for the arrangement of vertical memory transistors. As illustrated in **FIG. 6**, the photoresist layer **6** is then removed. The anti-reflex layer **5** can also be removed at this time. Then another photoresist layer **9** is deposited, wherein, if necessary, the anti-reflex layer **5** is renewed.

[0028] The second lithography mask **13** corresponding to the top view of **FIG. 5** is then used to structure the other photoresist layer so that the regions that are cross-hatched in **FIG. 5** are covered. As can be seen here with reference to the borders of the memory cell field **10** drawn for orientation, this second lithography mask **13** is provided for the purpose of structuring the other photoresist layer so that only the already produced openings, which are provided for the isolation trenches **7**, are exposed. Here, the mask also covers in particular the connection regions for the bit lines in the active trenches.

[0029] **FIG. 6** shows this other intermediate product in cross section. The other photoresist layer **9** now still has only strip-like portions, which close the openings for the active trenches **8** and expose the openings for the isolation trenches **7**. The pad nitride layer **3** and the pad oxide layer **2**, and, if necessary, also a portion farther into the semiconductor body **1** or the substrate, are then etched in these openings. Here, the structured hard mask layer **4** is likewise used as a mask. Then the other photoresist layer **9** is removed.

[0030] **FIG. 7** shows the cross section of an intermediate product after another etching step, in which the pad nitride layer **3** and the pad oxide layer **2** are also etched in the openings, which are provided for the active trenches **8**. In the remaining openings for the isolation trenches **7**, semiconductor material of the semiconductor body **1** (e.g., substrate) is also already removed. This etching step continues into the semiconductor material **1** until the structure of **FIG. 7** is produced. The deeper trenches manufactured in this way are provided for the isolation trenches **7**, while the flatter trenches are provided as active trenches **8** and the flat region adjacent to the flat trenches is provided as a contact region for contacting the bit lines in the active trenches. The trenches can then be filled with a high-temperature oxide (e.g., high density plasma or HDP oxide), which is made level with the surface, e.g., by means of CMP (chemical-mechanical polish). Another photoresist layer is then deposited.

[0031] By means of a third lithography mask **14**, which is shown in a top view in **FIG. 8**, the other photoresist layer is structured so that the regions that are cross-hatched in **FIG. 8** remain covered. Under the use of this structured additional photoresist layer, the oxide in the active trenches **8** is then removed. From the position of the memory cell field **10** marked in **FIG. 8**, it can be seen that the openings of this photoresist mask extend beyond the memory cell field on the right side in **FIG. 8** and there the openings have a width, with which sufficiently wide recesses can be etched for later attachment of the bit-line contacts.

[0032] **FIG. 9** shows in cross section an intermediate product of an alternative method, in which the hard mask layer **4**, the pad nitride layer **3** and the pad oxide layer **2** are already structured. Under the use of the additional photoresist layer **9** structured with the second lithography mask **13**, the openings, which are provided for the isolation trenches **7**, are already etched into the semiconductor material of the semiconductor body **1** or substrate. In additional processing steps, in principle the same structure as shown in **FIG. 7** is obtained.

[0033] Then impurities are implanted in order to form source/drain regions on the surface at the sides of the active trenches **8** and at the bases of the active trenches **8** by introducing dopants, whose positions are marked in **FIG. 7** with X's. Vertical memory transistors are formed in the active trenches **8**. These memory transistors each have on one wall of an active trench **8** a channel region, which is separated from a gate electrode arranged in the trench by a gate dielectric. Such a channel region is defined by the doped regions of source and drain, which are adjacent to the trench at the floor of the associated trench and the surface of the semiconductor body.

[0034] At least between the gate electrode and a source-side or drain-side end of an associated channel region, there is a dielectric memory layer sequence made from a first limiting layer, a memory layer, and a second limiting layer, especially an oxide-nitride-oxide layer sequence, which is provided for programming the memory cell by trapping hot electrons from the channel region (channel hot electrons or CHE). The source/drain regions on the surface of the semiconductor body or substrate are each connected to each other between two trenches **7**, **8** adjacent to each other by upper bit lines running parallel to the trenches, while the source/drain regions on the bases of the trenches are connected to each other along the same trench by lower bit lines formed (buried) as doped regions running in the semiconductor body or substrate.

[0035] **FIG. 10** shows a layout of such a memory chip in a top view. Here, the isolation trenches **7** and the active trenches **8** are in an alternating arrangement. In-between, there are the comb-like structures of the semiconductor body or substrate, which form on the surface the upper bit lines **15**. On the upper bit lines **15**, bit-line contacts **16** are deposited on one side of the memory cell field **10**, with which the upper bit lines **15** are connected in an electrically conductive way to one of the metallization layers of the surface wiring. In the example shown in **FIG. 10**, separate bit-line contacts **16** for forming EEPROM memory cells are provided for all upper bit lines **15**.

[0036] The lower bit lines in the active trenches **8** are contacted with additional bit-line contacts **17** on the opposite side next to the memory cell field **10** and connected in an electrically conductive way to a metallization layer, wherein, for the additional bit-line contacts **17**, wider recesses are provided here than corresponds to the width of the active trenches. These wide recesses between the material of the isolation trenches **7** are fabricated under the use of the third lithographic mask **14** from **FIG. 8**.

[0037] **FIG. 11** shows another layout of the memory chip in a top view corresponding to **FIG. 10**. Here, the bit-line contacts **18** are deposited so that every two adjacent upper bit lines, which are separated from each other by an isolation trench **7**, have a common bit-line contact **18**.

[0038] **FIG. 12** shows a third embodiment of the layout, corresponding to **FIG. 10** in a top view, for which every two adjacent upper bit lines **15**, which are separated from each other by an isolation trench **7**, have a cross connection outside the memory cell field **10** in the semiconductor material. The bit-line contact **19** can thus be deposited in the shown way on this cross connection.

[0039] The fabrication of STI isolation trenches for the core and periphery can be combined with the fabrication process for the isolation trenches **7**. For this purpose, the lithography masks are designed accordingly. The second lithography mask can be open or closed at the positions provided for the STI trenches of the core and periphery, so that the trenches produced at the periphery are etched more or less deeply. Less deep trenches have the advantage that the process for making the oxide planar is simplified. If deeper isolation trenches are fabricated at the periphery, a thicker oxide layer may also be deposited there in order to fill the trenches with oxide. This is because the trenches provided for the core and periphery are typically significantly wider than the isolation trenches of the memory cell field.

[0040] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A method of forming a semiconductor device, the method comprising:

forming a plurality of trenches in a semiconductor body, wherein the trenches alternate between active trenches and isolation trenches, the isolation trenches being deeper than the active trenches;

doping the semiconductor body so that a top surface of the semiconductor body adjacent each active trench and a floor of each active trench is doped;

forming memory cell components in each active trench, the memory cell components comprising a gate electrode and a charge-trapping layer disposed between the gate electrode and a sidewall of the trench;

forming bitlines over the semiconductor body and electrically coupling doped regions adjacent to the top surface of the semiconductor body adjacent the active trenches; and

forming bitline contacts coupled to the bitlines.

2. The method of forming the semiconductor device of claim 1, wherein the charge-trapping layer comprises a memory layer disposed between first and second limiting layers.

3. The method of forming the semiconductor device of claim 2, wherein forming a plurality of trenches comprises forming parallel strip-like trenches.

4. The method of forming the semiconductor device of claim 2, further comprising, prior to forming a plurality of trenches, forming a region of material over the semiconductor body.

5. The method of forming the semiconductor device of claim 4, wherein forming a plurality of trenches comprises:

forming openings through the region of material over the isolation trenches; and

etching the region of material and the semiconductor body so that the semiconductor body is etched to a greater depth at the isolation trenches.

6. The method of forming the semiconductor device of claim 4, wherein forming a region of material comprises:

forming a pad oxide over the semiconductor body;

forming a pad nitride over the pad oxide; and

forming a hard mask over the pad nitride.

7. The method of forming the semiconductor device of claim 1, wherein the charge-trapping layer comprises a dielectric memory layer sequence.

8. The method of forming the semiconductor device of claim 7, wherein the dielectric memory layer sequence comprises a memory layer disposed between a first limiting layer and a second limiting layer.

9. The method of forming the semiconductor device of claim 8, wherein the memory layer comprises a nitride layer and wherein the first and second limiting layers comprise oxide layers.

10. The method of forming the semiconductor device of claim 8, wherein the dielectric memory layer sequence is provided for programming by trapping hot electrons from a channel region.

11. The method of forming the semiconductor device of claim 1, wherein the semiconductor body comprises a semiconductor substrate.

12. A method for fabricating a semiconductor memory with vertical charge-trapping memory cells, the method comprising:

in a first step, a hard mask layer is deposited on a surface of a semiconductor body and a photoresist layer is deposited on this mask layer;

in a second step, the photoresist layer is provided with a plurality of parallel, strip-like openings arranged at intervals to each other under the use of a first lithography mask, the first lithography mask being formed so that the photoresist layer covers regions on a first side adjacent to a provided memory cell field, which are provided for attachment of bit-line contacts;

in a third step, the hard mask layer is structured under the use of the photoresist layer;

in a fourth step, the photoresist layer is replaced by a full-surface, additional photoresist layer;

in a fifth step, the additional photoresist layer is structured under the use of a second lithography mask so that in the series of strip-like openings formed in the hard mask layer, every second opening is exposed so that remaining openings remain covered by the additional photoresist layer, wherein the second lithography mask is formed so that the additional photoresist layer covers regions on a second side that is opposite the first side adjacent to the provided memory cell field, where these regions are provided for attaching additional bit-line contacts;

in a sixth step, under the use of the hard mask layer and the additional photoresist layer as a mask, a material present under the hard mask layer is removed in the region of the exposed openings in a direction perpendicular to the hard mask layer;

in a seventh step, the additional photoresist layer is removed and additional material is removed in the region of the openings of the hard mask layer in a direction perpendicular to the hard mask layer in order to fabricate trenches;

in an eighth step, the trenches produced in the seventh step are filled with an oxide and the hard mask layer is removed;

in a ninth step, another photoresist layer is deposited and is structured under the use of a third lithography mask, wherein openings are generated above the trenches in corresponding regions, which remain covered by the photoresist layer structured in the fifth step, wherein the third lithography mask is formed so that the openings of the additional photoresist layer expose regions extending over the regions of the trenches on the second side adjacent to the provided memory cell field, which are provided for the additional bit-line contacts; and

in a tenth step, under the use of the photoresist layer structured in the ninth step the oxide is removed from the corresponding trenches, which are provided for the memory transistors.

13. The method for fabricating the semiconductor memory of claim 12, and further comprising a subsequent eleventh step wherein bit-line contacts are formed in the regions that remain covered in the second step to the sides adjacent to the provided memory cell field, and additional bit-line contacts are formed in the regions that were exposed in the ninth step to the sides adjacent to the provided memory cell field.

14. The method for fabricating the semiconductor memory of claim 13, for which in the eleventh step the bit-line contacts are formed for forming flash memory cells so that two adjacent bit lines, which are arranged between the trenches, are coupled to a common bit-line contact.

15. A method of making a semiconductor memory with vertical charge-trapping memory cells, the method comprising:

forming a plurality of parallel trenches arranged at intervals to each other with corresponding walls and floors formed on a surface of a semiconductor body;

forming a memory transistor in a memory cell field on the surface of the semiconductor body, the memory transistor having on one wall of one of the trenches a channel region, which is separated from a gate electrode arranged in the trench by a gate dielectric, the channel region limited by doped regions, which are adjacent to the trench at the floor of the associated trench and at the surface of the semiconductor body and which are provided as source/drain regions;

forming a dielectric memory layer sequence disposed at least between an appropriate gate electrode and a source-side or a drain-side end of an associated channel region, the dielectric memory layer sequence being made from a first limiting layer, a memory layer, and a second limiting layer, the dielectric memory layer sequence being provided for programming by trapping hot electrons from the channel region;

forming upper bit lines running parallel to the trenches, wherein the source/drain regions are coupled to each other at the surface of the semiconductor body between two adjacent trenches by the upper bit lines; and

forming lower bit lines formed as doped regions in the semiconductor body, wherein the source/drain regions are connected to each other at the floors of the trenches along the same trench by the lower bit lines;

wherein the trenches are alternating isolation trenches and active trenches, wherein the isolation trenches are also present between the lower bit lines and the active trenches are provided for the memory transistors, and outside the memory cell field there are bit-line contacts on the upper bit lines and other bit-line contacts are provided on the lower bit lines and are connected in an electrically conductive way to a metallization layer provided for wiring, wherein the bit-line contacts and the other bit-line contacts are mounted on opposite

sides of the memory cell field and portions of the isolation trenches are arranged between the other bit-line contacts.

16. The method of making the semiconductor memory according to claim 15, wherein the upper bit lines are each provided separately with the bit-line contact.

17. The method of making the semiconductor memory according to claim 15, for which every two adjacent upper bit lines, which are separated from each other by an isolation trench, have a common bit-line contact.

18. The method of making the semiconductor memory according to claim 17, for which every two adjacent upper bit lines, which are separated from each other by an isolation trench, have a cross connection in the semiconductor material of the semiconductor body outside the memory cell field.

19. The method of forming the semiconductor memory according to claim 15, wherein forming a dielectric memory layer sequence comprises forming a memory layer disposed between a first limiting layer and a second limiting layer.

20. The method of forming the semiconductor memory according to claim 19, wherein the memory layer comprises a nitride layer and wherein the first and second limiting layers comprise oxide layers.

* * * * *