United States Patent [19]

Pottebaum

[11] **3,832,628**

[45] **Aug. 27, 1974**

[54] **ENGINE TIMER**

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[73] Assignee: **Production Measurements Corporation,** Hilliard, Ohio

[22] Filed: **Dec. 8, 1972**

[21] Appl. No.: **313,484**

[52] **U.S. Cl.**..... **324/16 R,** 324/83 A, 324/83 D

[51] **Int. Cl.**..... **F02p 17/00**

[58] **Field of Search**..... 324/15, 16 R, 16 T, 83 A, 324/83 D; 73/116–119

[56] **References Cited**

UNITED STATES PATENTS

3,697,865 10/1972 Smith ..... 324/16 T

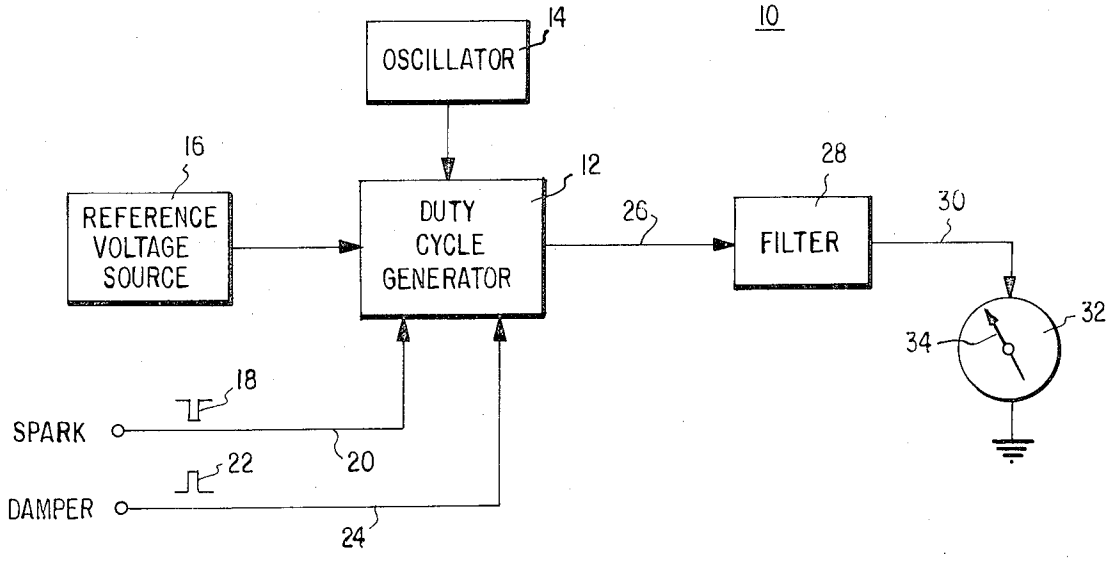
Primary Examiner—Michael J. Lynch

Attorney, Agent, or Firm—LeBlanc & Shur

[57] **ABSTRACT**

Disclosed is a timer for indicating the average timing of an internal combustion engine. The timer includes a duty cycle generator which produces a series of pulses whose duty cycle varies with the average timing of the engine. These pulses are fed through a filter to produce an analog signal for display by a conventional voltmeter or ammeter.

18 Claims, 9 Drawing Figures



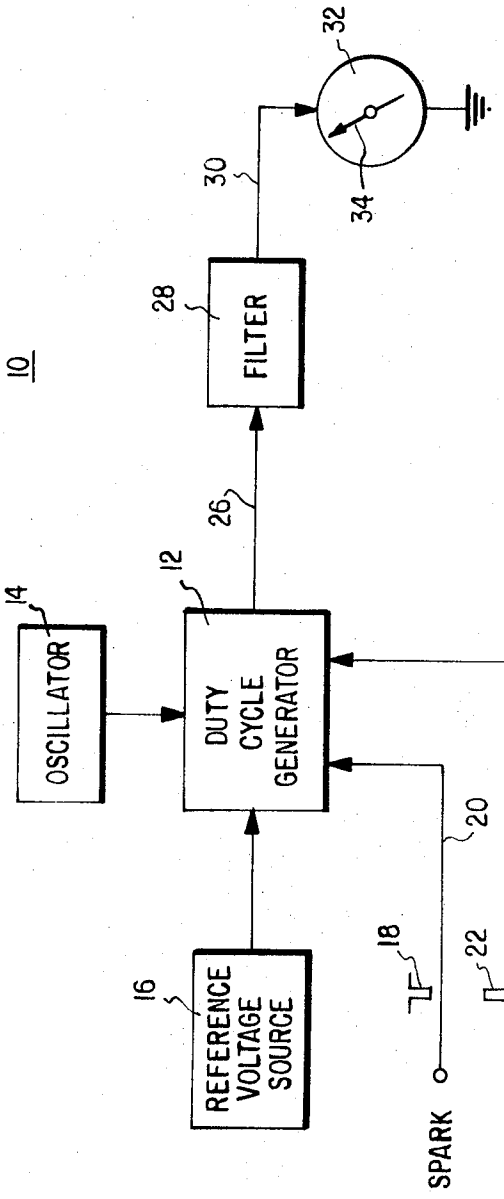

10
OSCILLATOR
14
DUTY CYCLE GENERATOR
12
REFERENCE VOLTAGE SOURCE
16
FILTER
28
26
30
32
34
18
20
22
24
SPARK
DAMPER

FIG. 1

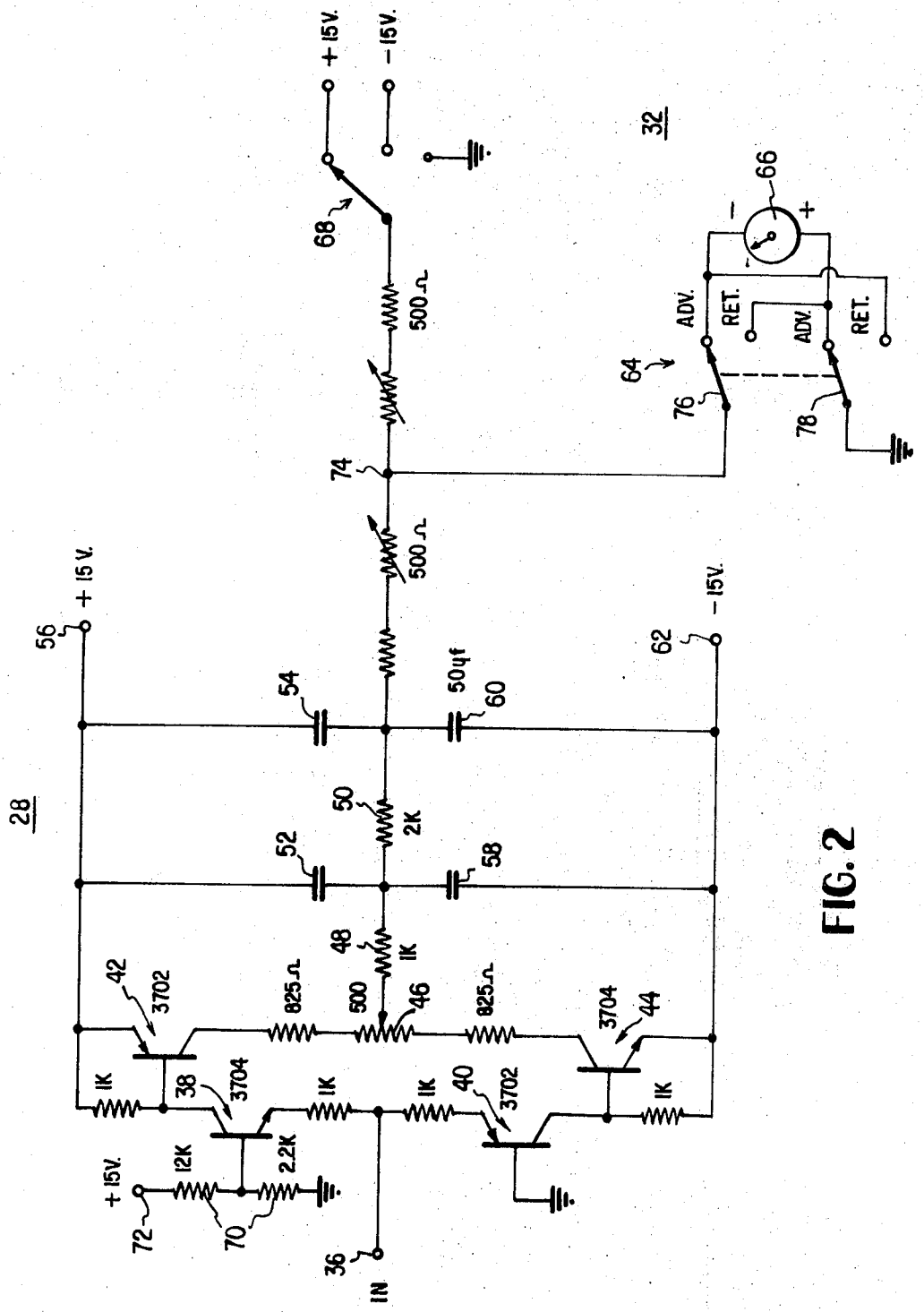

+15V.
-15V.
68
500Ω
74
500Ω
32
66
ADV.
RET.
ADV.
RET.
64
76
78
+15V.
56
54
50μf
60
62
-15V.
28
50
2K
52
58
48
1K
42
3702
825Ω
500
46
825Ω
3704
44
1K
38
3704
1K
1K
40
3702
1K
+15V.
12K
2.2K
72
70
36
IN

FIG. 2

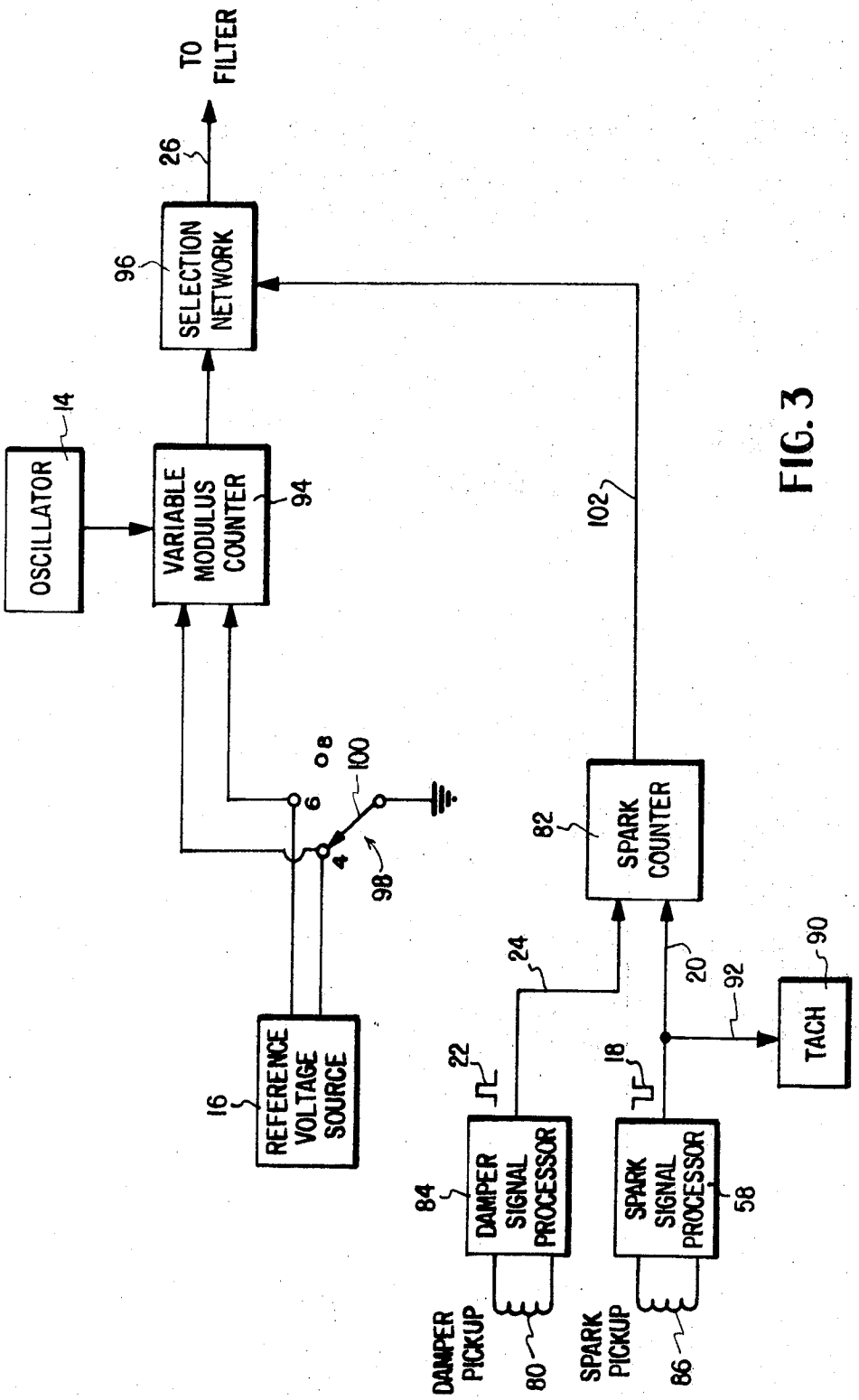

TO FILTER
26
SELECTION NETWORK
96
OSCILLATOR
14
VARIABLE MODULUS COUNTER
94
102
6
8
4
100
98
SPARK COUNTER
82
24
20
92
TACH
90
16
REFERENCE VOLTAGE SOURCE
22
18
84
DAMPER SIGNAL PROCESSOR
SPARK SIGNAL PROCESSOR
58
DAMPER PICKUP
80
SPARK PICKUP
86

FIG. 3

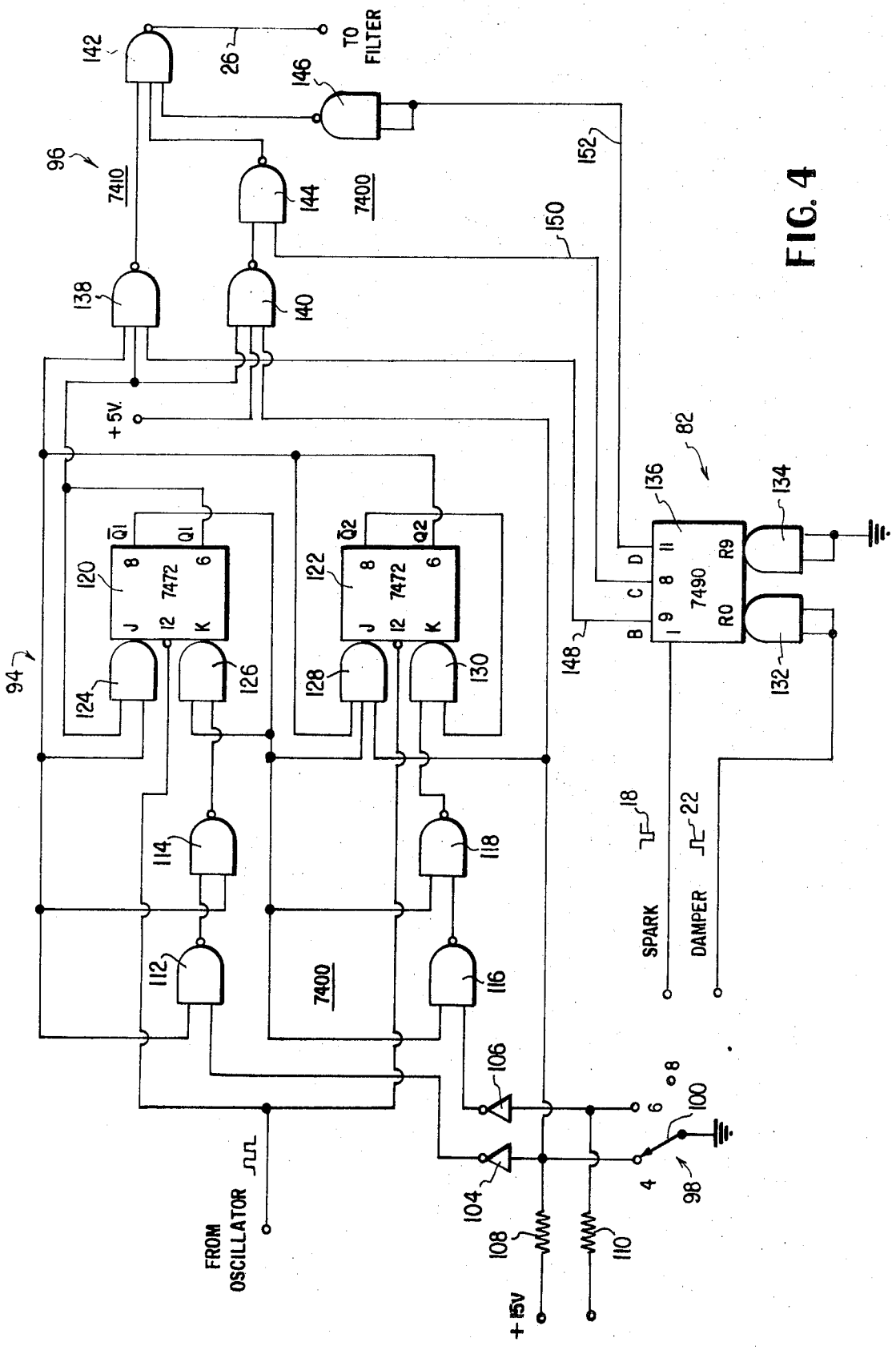

142
26
TO FILTER
146
96
7410
144
7400
152
150
138
140
+5V
82
136
134
120
122
7472
124
126
128
130
94
148
132
18
22
SPARK
DAMPER
114
118
112
116
106
100
104
108
110
98
FROM OSCILLATOR
+15V

FIG. 4

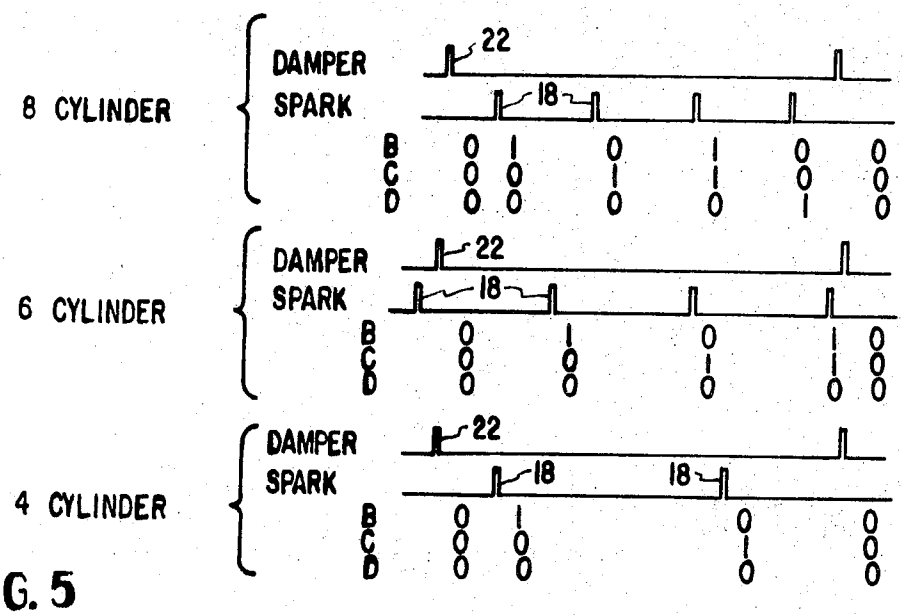


FIG. 5

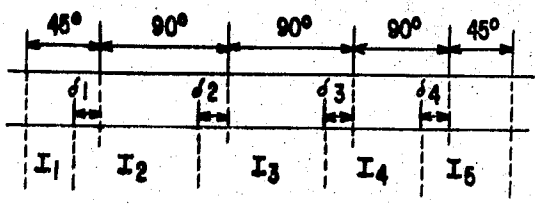


FIG. 6A

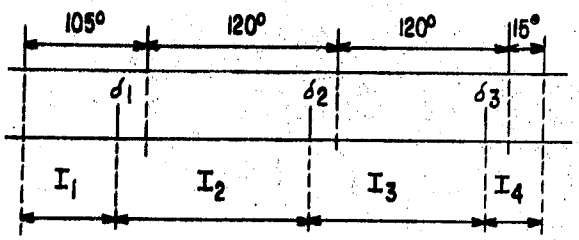


FIG. 6B

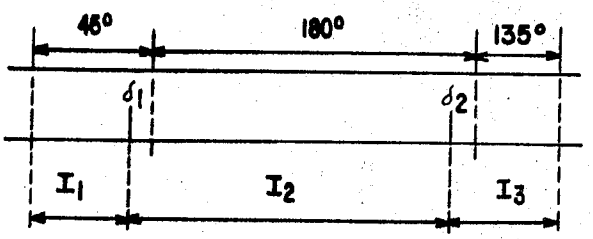
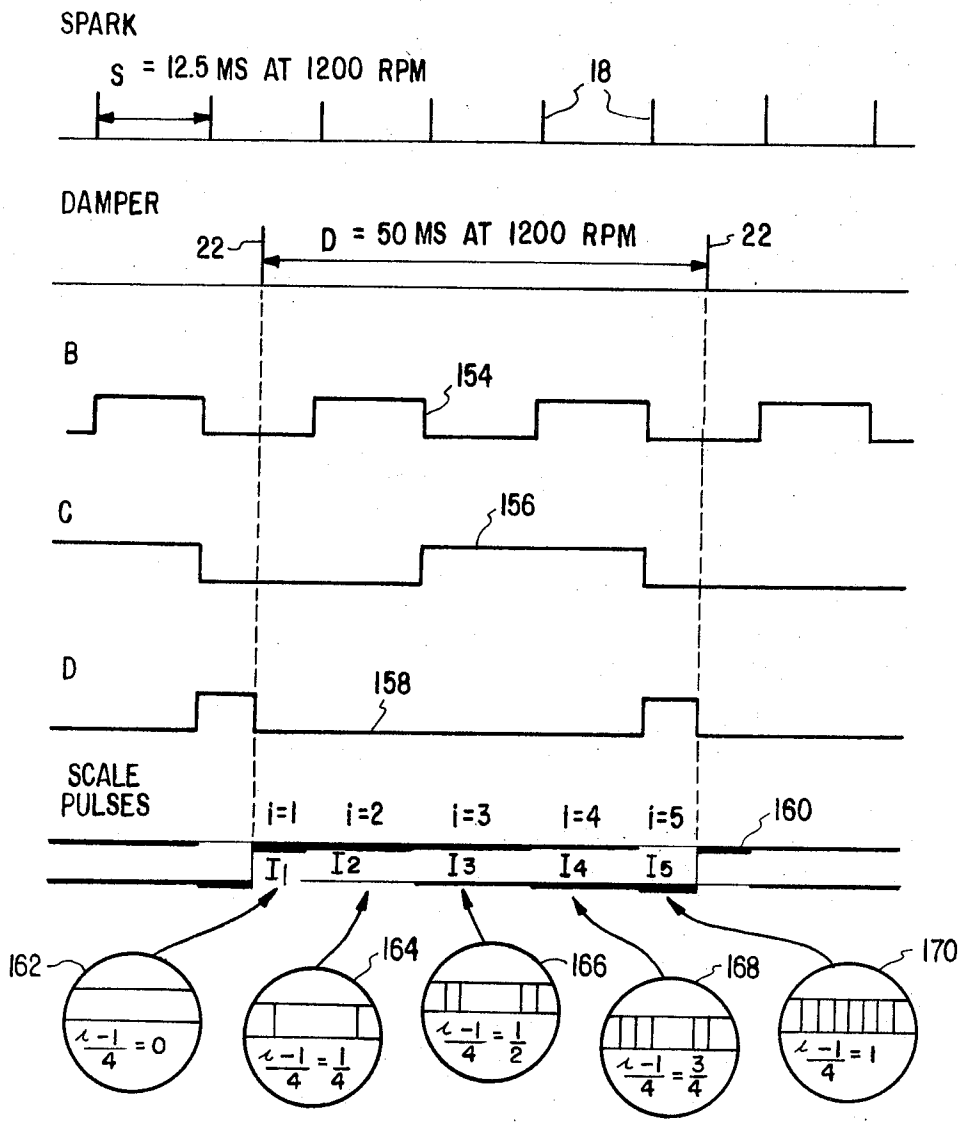


FIG. 6C

FIG. 7


SPARK
S = 12.5 MS AT 1200 RPM
18
DAMPER
22
D = 50 MS AT 1200 RPM
22
B
154
C
156
D
158
SCALE PULSES
i=1
i=2
i=3
i=4
i=5
160
I1
I2
I3
I4
I5
162
164
166
168
170
i-1/4 = 0
i-1/4 = 1/4
i-1/4 = 1/2
i-1/4 = 3/4
i-1/4 = 1

ENGINE TIMER

This invention relates to an internal combustion engine timer and more particularly to an average timer for improving the timing of internal combustion engines such as automobile engines. It provides a relatively simplified and inexpensive timer particularly adapted for use by automotive dealers and repair shops where the investment of substantial sums of money in more complicated equipment is not warranted.

In a four-cycle engine of the type customarily employed in automobiles each cylinder fires once for every two revolutions of the crank shaft. In most engines, a spark is provided for each cylinder slightly prior to the top dead-center position for the piston on its compression stroke, although engines are occasionally designed to fire after the top dead-center position.

Firing is controlled by a timing system. This includes a distributor having a rotating shaft coupled to the crank shaft by a 2:1 gearing mechanism whereby the distributor shaft makes one complete rotation for every two crank shaft rotations. The distributor shaft carries a multi-lobe cam (one lobe for each cylinder) which engages with a follower to operate a set of breaker points. These are shunted by a capacitor in a primary circuit of a spark coil connected to the battery. Opening of the points as the timing cam rotates provides rapid magnetic field changes in the secondary of the spark coil with resulting high voltage across the coil secondary. The high voltage pulses are coupled to individual spark plugs by a rotating contact member carried by the distributor shaft and engaging with a series of fixed contacts in the distributor, each connected to one of the spark plugs.

Timing is normally adjusted in relation to the top dead-center position of the No. 1 piston by rotating a plate carrying the cam follower and breaker points in relation to the cam on the distributor shaft.

Accurate engine timing is extremely important because an improperly timed engine operates inefficiently and with less than optimum power and also because timing errors increase the octane requirement of the fuel. Also of increasing importance is the fact that an improperly timed engine produces high exhaust emissions and consequent air pollution.

The normal procedure employed in engine timing utilizes a timing light which has a stroboscopic lamp fired by discharge of the No. 1 spark plug. Firing of the lamp illuminates a pointer mounted on the engine in relation to a dial on the rotating damper pulley. The recurring momentary illumination of the pointer and dial indicates the relationship between the firing of the No. 1 cylinder and the top dead-center position of its piston, ordinarily in terms of degrees before (or after) top-dead center.

The foregoing system possesses several disadvantages. First, because of the positioning of the various measuring components, there can be substantial and unpredictable parallax in reading of the pointer and markings on the damper pulley, thereby rendering the measurement inaccurate. Moreover, the stroboscopic timing equipment itself possesses inherent inaccuracies, due to the dynamic nature of the operation, and the visual nature of the observations. Further, measurements have been made with reference to a single cylinder on the assumption that each cylinder actually fires

in precisely fixed relationship to the No. 1 cylinder. However, inperfections in the timing gears, the cam and elsewhere in the timing mechanism can cause deviations as much as ± 3° from the designed values. Thus, if the cam surface for cylinder No. 1 is inaccurate, the resulting offset may completely invalidate the timing reading. Even if the No. 1 cylinder is adjusted to fire exactly as specified, for example at 6° before top dead-center, adjustment of the timing for the No. 1 cylinder to achieve this ordinarily results in firing the remaining cylinders anywhere between 3° and 9° before top dead-center. This is totally unacceptable, particularly in view of increasing demand for reduced exhaust emissions.

In order to overcome these and other disadvantages there is disclosed in assignee's copending U.S. Pat. application Ser. No. 219,416, filed Jan. 20, 1972, a method and apparatus for measuring the average timing of internal combustion engines. In that application there is disclosed a digital technique for producing a series of pulses whose number is representative of average engine timing and counting the number of pulses during a timing interval to give an indication of engine timing.

The present invention is directed to an average engine timer of the same general type as that disclosed in the above-mentioned copending application but one that is of more simplified and less expensive construction. In the present invention pulses derived from a spark coil pickup and a damper pickup are applied to a duty cycle generator. The duty cycle generator varies the duty cycle of pulses from a relatively high frequency oscillator in proportion to engine timing as determined by the angular distance between the spark and damper pulses. These high frequency pulses having a duty cycle representative of average engine timing are applied to a filter to produce an analog voltage or current used to drive an analog display in the form of a conventional voltmeter or ammeter. The output from the duty cycle generator is substantially independent of frequency and therefore of engine speed so that in the present invention it is not necessary to accurately control engine rpm in order to provide an accurate output reading. The result is an accurate and yet simplified and inexpensive device which does not require a large investment of time and money to operate and is suitable for use by automotive dealers, repair shops and others who may not wish to make a large investment in engine timing equipment.

It is therefore one object of the present invention to provide an improved internal combustion engine timer.

Another object of the present invention is to provide a simplified and less expensive average timer for internal combustion engines.

Another object of the present invention is to provide an average timer for internal combustion engines incorporated an analog display.

Another object of the present invention is to provide an improved and simplified average timer particularly adapted for timing automotive engines.

Another object of the present invention is to provide an average timer for internal combustion engines which eliminates the necessity for closely controlling engine speed in order to provide an accurate reading of engine timing.

Another object of the present invention is to provide an average timer for internal combustion engines in

which the duty cycle of a relatively high frequency electrical signal is varied in accordance with engine timing.

Another object of the present invention is to provide an improved method of obtaining average engine timing.

These and further objects and advantages of the invention will be more apparent upon reference to the following specification, claims and appended drawings wherein:

FIG. 1 is a simplified block diagram of an average timer constructed in accordance with the present invention;

FIG. 2 is a detailed circuit diagram of the filter and meter forming the analog display portion of the average timer of FIG. 1;

FIG. 3 is a more detailed block diagram of the digital portion of the timer of FIG. 1;

FIG. 4 is an overall circuit diagram of the digital portion of the timer illustrated in FIG. 3;

FIG. 5 is a wave form diagram showing the count pattern of the spark counter of FIGS. 3 and 4;

FIGS. 6A, 6B and 6C illustrate the interval definition of timing angles in accordance with the present invention for eight-cylinder, six-cylinder, and four-cylinder engines, respectively; and

FIG. 7 shows a wave form chart for an eight-cylinder engine illustrating some of the features of the present invention.

Referring to the drawings, FIG. 1 is a simplified block diagram of an average engine timer constructed in accordance with the present invention. The engine timer generally indicated at 10 comprises a duty cycle generator 12 receiving relatively high frequency electrical oscillations from an oscillator 14 and a reference voltage or current from a DC reference source such as reference source 16. By way of example only, oscillator 14 may be a free-running multi-vibrator supplying continuous square wave pulses to the duty cycle generator preferably at a frequency of about 40 kHz. Reference voltage source 16 is preferably a regulated DC power supply and has taps providing both plus and minus 15 volts DC as well as plus 5 volts DC for other portions of the circuit. Spark pulses such as indicated at 18 are supplied to duty cycle generator 12 by way of lead 20 and damper pulses such as that indicated at 22 are supplied to the duty cycle generator over lead 24. The output from duty cycle generator 12 on lead 26 is a train of 40 kHz pulses which have been scaled to have a duty cycle representative of average engine timing as determined by the time of the spark pulses 18 in relation to the damper pulses 22. These variable duty cycle pulses on lead 26 are supplied through a low pass RC filter 28 to produce an analog voltage on lead 30 applied to meter 32 so that the deflection of the meter pointer 34 is an indication of average timing for the engine from which the spark pulses 18 and damper pulses 22 are derived. The meter reading is $(K + \delta_{AVE})1/360° \times V$ (or I) where K is a constant offset, δ_{AVE} is average timing and V is the voltage (or current I) of source 16.

FIG. 2 is a detailed circuit diagram showing the filter 28 and the meter 32. The output from the duty cycle generator on lead 26 of FIG. 1 is applied as a series of scaling pulses to the input terminal 36 of the filter 28 of FIG. 2. The circuit comprises a first pair of series connected transistors comprising NPN junction transistor 38 and PNP junction transistor 40. Connected to the collectors of those two transistors are the respective bases of a PNP junction transistor 42 and a NPN junction transistor 44. A potentiometer 46 connects the output of the transistors to an RC filter network comprising series resistors 48 and 50 and shunt capacitors 52 and 54 connected to a positive 15 volt power supply terminal 56 and similar shunt capacitors 58 and 60 connected to a minus 15 volt DC power supply terminal 62. Connected between the output of the filter and ground by a four-pole double-throw switch 64 is a meter 66. By way of example only, meter 66 may be a 500 microammeter having 0°–20° full scale deflection of the type manufactured by Modutec Inc. of Norwalk, Conn. and identified as Model No. 2S-DUA-500-NL. Other equivalent voltmeters or ammeters may be utilized. Finally, the filter output is also connected to a positive or negative 15 volt DC power supply through a normalizing switch 68.

In operation of the circuit of FIG. 2, transistor 38 is normally biased on by having its base connected to an intermediate point on voltage divider 70 in turn coupled to the positive 15 volt DC power supply terminal 72. Conduction of a transistor 38 forward biases transistor 42 causing this latter transistor to turn "hard" on. With the reception of a positive pulse at input terminal 36 this positive pulse turns on transistor 40 in turn turning transistor 44 hard on. The turn on of transistor 44 causes transistor 38 to be reversed biased turning it off along with its associated transistor 42. When the positive pulse at the input terminal 36 disappears transistors 40 and 44 turn off and transistors 38 and 42 turn back on to assume the initial condition. The hard saturated switching transistors 42 and 44 apply sharp pulses to the low pass filter comprising series resistors 48 and 50 and the shunt capacitors each of which, by way of example only, may have a relatively large capacity of about 50 microfarrads. The filter converts the pulses into a varying DC or analog signal which is applied across meter 66 between terminal 74 and ground. Switch 68 connects terminal 74 either to + 15 volts, −15 volts, or to ground, as desired.

As previously indicated most automotive engines are timed in the advance mode; that is, they are timed to fire approximately 6° before the top dead-center of the piston. However, some engines are operated in a retard mode where the engine fires after the piston has crossed the top deadcenter position. Switch 64 makes it possible to operate meter 66 in either an advance or retard mode by reversing the connections to the meter by movement of the ganged switch blades 76 and 78 between the advance and retard contacts as illustrated in FIG. 2.

FIG. 3 is a more detailed block diagram of the portions of the average timer 10 of the present invention associated with the duty cycle generator 12. Like parts in FIG. 3 bear like reference numerals. A damper pickup illustrated at 80 passes electrical damper signals 22 to a spark counter 82 by way of a damper signal processer 84. Similarly, a spark signal pickup illustrated at 86 passes spark pulses 18 to the spark counter 82 by way of a spark signal processer 88. If desired, a tachometer 90 may be coupled to the output of the spark signal processer 88 by a lead 92. The tachometer 90 is provided to indicate engine rpm. By way of example only, the two pickups and the two signal processers along with the tachometer 90 may be of the type more fully shown and described in assignee's copending ap-

plication Ser. No. 219,416 filed Jan. 20, 1972. Pickups **80** and **86** may be constructed in any suitable fashion. Damper pickup **80** is preferably an eddy-current or other magnetic field sensitive device while spark pickup **86** is either a magnetic field or electric field sensitive (capacitive) device as desired. The damper pickup operates as a proximity sensor to produce an output signal once per revolution of the damper as a notch cut in its periphery passes through the pickup field of view. To this end, there is advantageously provided a mounting fixture (not shown) on the engine to support the pickup in suitable relation to the damper so that the pickup senses the notch as the damper rotates. The mounting fixture may be of any suitable construction and does not constitute part of this invention as such. However, it will be realized that placement of the fixture depends on the availability of an accessible mounting space. Any suitable mounting position may be employed.

Damper signal processer **84** converts the pickup output into a narrow pulse defining the center of the damper notch thereby providing a precise reference for generation of damper pulses from which timing measurement is made. Spark pickup **86** operates to provide a signal representing the magnetic field pattern associated with the spark coil output. In one preferred construction, the spark pickup is attached around the spark coil output wire, in the manner of a "clip on" type ammeter, but other constructions may be employed if desired.

Spark signal processer **88** responds to the pickup output to generate a pulse in precise time relationship with the opening of the distributor points. This signal is supplied to the spark counter **82** and to tachometer **90** which produces an analog signal representative of the frequency of the spark pickup output. Analog signal generation in the tachometer is accomplished by integrating a series of pulses produced by spark signal processer **88.** The tachometer is preferably provided with a three-position switch (not shown) to provide for an eight-, six- and four-cylinder engine respectively in which the number of sparks per revolution of the engine are different.

The duty cycle generator **12** of FIG. **1** is made up of the spark counter **82,** a variable modulous counter **94,** a selection network **96,** and a three-position switch **98,** having four-, six-, and eight-cylinder contacts. The wiper **100** of switch **98** is moved to the appropriate contact manually in accordance with whether a four-, six-, or eight-cylinder engine is under test. Spark counter **82** is a decade counter which is triggered with each spark signal **18** and which is reset by each damper signal **22.** That is, spark counter **18** produces an output which is representative of the number of spark signals **18** between damper signals **22.** As previously indicated, on an eight-cylinder engine there are normally four spark signals per damper signal, for a six-cylinder engine there are normally three spark signals per damper signal, and for a four-cylinder engine there are normally two spark signals per damper signal. Variable modulous counter **94** is a divider which divides the signals from oscillator **14** by a variable amount depending upon the position of switch **98.** When the wiper **100** of switch **98** is on the four-cylinder contact, variable modulous counter **94** divides by two. When switch **98** is set to the six-cylinder contact variable modulous counter **94** divides by three, and when switch **98** is manually set to the eight-cylinder contact variable modulous counter **94** divides by four. Selection network **96** is a variable gating network which passes only certain ones of the high frequency pulses from the variable modulous counter **94.** Selection network **96** provides scaling factors to the pulse output supplied to the filter in accordance with the count of spark counter **82.** These scaling factors are based upon the definition of average timing more fully described below.

FIG. **4** is a more detailed block diagram of the portions of the circuit associated with the variable duty cycle generator **12.** Again, like parts bear like reference numerals in FIG. **4.** In FIG. **4** the three-position switch **98** is connected to the variable modulous counter **94** by a pair of invertors **104** and **106.** The four-cylinder contact of the switch is connected to the regulated + 15 volt DC power supply through a resistor **108** and the six-cylinder contact of the switch is similarly connected to the + 15 volt DC power supply through a resistor **110.** When movable contact **100** is moved to the four-cylinder contact, the input of invertor **104** is grounded. Similarly, when switch blade **100** is moved to the six-cylinder contact, the input of invertor **106** is grounded. When the switch is moved to the eight-cylinder contact, neither invertor input is grounded.

Variable modulous counter **94** comprises four NAND gates formed from a 7400 integrated circuit and labeled **112, 114, 116** and **118.** The NAND gates are connected to a pair of JK flip-flops **120** and **122** through AND gates **124, 126, 128** and **130** formed from a 7472 integrated circuit as illustrated. Spark counter **82** comprises a binary counter formed from a 7490 integrated circuit and is connected to the spark and damper processers to receive the spark signal **18** and the damper signal **22,** the latter through a pair of AND gates **132** and **134.** The binary counter is illustrated by the box **136.**

Selection network **96** is a logic network formed from a 7410 and a 7400 integrated circuit. It comprises NAND gates **138, 140, 142, 144** and **146.** These gates are connected to the output of the variable modulous counter **94** and receive signals from spark counter **82** by way of three leads **148, 150** and **152** labeled B, C and D, respectively, at the outputs of counter **136.**

The operation of the timer of the present invention is based upon the following mathematical description of average timing.

Assume the engine rotation is divided into sections where N = the number of pistons in the engine (4, 6, 8). If "top dead-center" piston is defined as 0°, then the section lines fall at $L(360)°/N/2\ L = 0, 1 \ldots (N\text{-}1)$, i.e.,

4 = 0°	180°		
6 = 0°	120°	240°	
8 = 0°	90°	180°	270°

If the deviation from these section lines of the appropriate piston firings is defined as δ_M, M = 1 . . . N; then the average timing is

$$(\Delta_{AVE}) = \sum_{M=1}^{N} \frac{\delta M}{N}. \qquad (1)$$

As previously indicated, the spark counter **82** is a decade counter (7490) which counts on the leading edge

of each synchronized spark pulse **18** and returns to 000 on the synchronized damper pulse **22.** FIG. **5** shows the timing relationship between the spark and damper pulses for eight-, six- and four-cylinder engines. For ease of understanding the spark and damper pulses are illustrated with the same polarity, it being understood that the damper pulse is conventionally a positive going pulse and the spark pulses are negative going pulses. As illustrated in FIG. **5** for an eight-cylinder engine there are customarily four spark pulses **18** for each damper pulse **22**; for a six-cylinder engine there are customarily three spark pulses **18** for each damper pulse **22,** and for a four-cylinder engine there are customarily two spark pulses **18** for each damper pulse **22.** The count pattern for spark counter **82** is illustrated beneath each of the wave forms in FIG. **5** with the outputs B, C and D of the counter of FIG. **4** illustrated after each damper pulse and after each spark pulse. For example, referring to the diagram in FIG. **5** for the eight-cylinder engine, after the damper pulse **22** the outputs B, C and D are all zero. After the first spark pulse the outputs are 100 indicating a binary 1. After the second spark pulse **18,** output B is 0, output C is 1, and output D is 0, indicating a binary 2. After the third spark pulse, output B is 1, output C is 1, and output D is zero, indicating a binary 3. After the fourth spark pulse output B is zero, output C is zero, and output D is 1, indicating the binary 4. After the second damper pulse the outputs are all reset to zero. The B, C and D outputs of the spark counter for the six-cylinder and four-cylinder engines follow the same binary numerical order. The highest number counted for an eight-cylinder engine is binary 100 or a decimal 4, for a six-cylinder engine binary 011 or decimal 3, and for a four-cylinder engine binary 010 or decimal 2. The least significant bit is output B, the next significant bit is output C, and the most significant bit is output D.

Variable modulous counter **94** and selection network **96** constitute scaling circuits for modifying the number of output pulses passed from oscillator **14.** The scaling logic is based on a modified mathematical definition of average timing in which the engine or damper revolution is divided into angular intervals. For an eight-cylinder engine a revolution is divided into five intervals labeled I_1 through I_5. For a six-cylinder engine one revolution is divided into four intervals labeled I_1 through I_4, and for a four-cylinder engine a revolution is divided into three angular intervals, labeled I_1 through I_3. The scaling logic is based on the modified mathematical definition of an average timing in which:

$$\delta_{AVE}=\sum_{M=1}^{X}\frac{\delta M}{X} \qquad (2)$$

where

δ_{AVE} = average timing M = timing with respect to cylinder M X = number of cylinders ÷ 2.

FIG. **6A** illustrates the interval definition of timing angles for an eight-cylinder engine, FIG. **6B** for a six-cylinder engine, and FIG. **6C** for a four-cylinder engine. Referring to FIG. **6A** for the eight-cylinder engine, a revolution is divided into five intervals; namely, a first interval of approximately 45°; second, third and fourth intervals of approximately 90°, and a fifth interval of approximately 45°. The intervals I_1 through I_5 differ from 45° and 90°, respectively, in that they are modified by the spark firing deviations δ_1 through δ_4. Thus, the intervals for an eight-cylinder engine are exactly defined as follows:

$$I_1 = 45° - \delta_1$$
$$I_2 = 90° + \delta_1 - \delta_2$$
$$I_3 = 90° + \delta_2 - \delta_3$$
$$I_4 = 90° + \delta_3 - \delta_4$$
$$I_5 = 45° + \delta_4.$$

If these intervals are scaled by the formula

$$N_8=\sum_{1=1}^{5}\frac{(i-1)}{4}I_i, \qquad (3)$$

then $N_8 = 0\ (45-\delta_1)+¼(90+\delta_1-\delta_2)+½(90+\delta_2-\delta_3)+¾(90+\delta_3-\delta_4)+1(45+\delta_4)$
or $N_8 = 180°+¼(\delta_1+\delta_2+\delta_3+\delta_4)$
or

$$N_8=180°+\frac{1}{4}\sum_{n=1}^{4}\delta m$$

$\therefore N_8=180°+\delta_{AVE}$

where

N_8 = degree count δAVE = average timing angle 4.

Equivalent reasoning is used in the cases of six-cylinder and four-cylinder engines in which the interval definition of timing angles are illustrated in FIGS. **6B** and **6C**, respectively, for six- and four-cylinders. In FIG. **6B** the intervals are defined as follows:

$$I_1 = 105° - \delta_1$$
$$I_2 = 120° - \delta_1 - \delta_2$$
$$I_3 = 120° + \delta_2 - \delta_3$$
$$I_4 = 15° + \delta_4$$

$$N_6=\sum^{4}\frac{i-1}{3}Ii$$

$$\therefore N_6 = 135° + \delta_{AVE}$$

5.

For a four-cylinder engine and referring to FIG. **6C** the intervals are defined as follows:

$$I_1 = 45° - \delta_1$$
$$I_2 = 180° + \delta_1 - \delta_2$$
$$I_3 = 135° + \delta_2$$

$$N_4=\sum^{3}\frac{i-1}{2}Ii$$

$$\therefore N_4 = 225° + \delta_{AVE}$$

6.

The scaling logic consists of the variable modulous counter including JK flip-flops **120** and **122** and the associated gates as well as the selection circuit **96** incorporating the selector logic gates. The variable modulous counter divides by four in the eight-cylinder mode for the integral multiplication factors of $i_1/4$ in the equation

$$N_8=\sum_{i=1}^{3}\frac{i-1}{4}Ii$$

(equation 3 above). Likewise the counter divides by three for a six-cylinder engine (equation 5 above) and divides by two for a four-cylinder engine (equation 6 above). The modulous of the counter is controlled by the gating to the J and K inputs of flip-flops **120** and **122.** The selection gates **96** scale the outputs Q_1 and Q_2 from flip-flops **120** and **122.** This scaling is based upon the outputs B, C and D from the spark counter **82.** The selection gates obtain the (*i*-1) factors in equations 3, 5 and 6 above.

The following table gives the scaling logic variables at the modulous counter outputs Q_1 and Q_2 for an eight-cylinder engine (divide by 4), for a six-cylinder engine (divide by 3), and for a four-cylinder engine (divide by 2):

TABLE

8 Cylinder		6 Cylinder		4 Cylinder	
Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
0	0	0	0	0	0
1	0	1	0	1	0
1	1	1	1	0	0
0	1	0	0		
0	0				

For an eight-cylinder engine before the first pulse from oscillator **14** Q_1 and Q_2 are both zero. After the first pulse Q_1 is at the one level and Q_2 is zero. After the second oscillator pulse both outputs are at the one level. After the third pulse Q_1 is zero and Q_2 is **1.** After the fourth oscillator pulse both outputs are again at zero. Similar counting cycles are given in the table for the six-cylinder and four-cylinder modes.

FIG. **7** is a wave form chart for eight-cylinder engine operation. The spark pulses are shown at **18** and the damper pulses at **22.** Again, both set of pulses are shown with positive polarity for the sake of comparison, it being understood that the spark pulses are negative going pulses as previously indicated. The spacing γ_S between successive spark pulses for an eight-cylinder engine at 1,200 rpm and 0.0° timing is 12.5 miliseconds. The spacing γ_0 between damper pulses is 50 miliseconds under these same conditions. The next wave form illustrated at **154** in FIG. **7** is the B output on lead **148** from spark counder **82.** Wave form **156** is the C output on lead **150** and wave form **158** is the D output on lead **152** of FIG. **4.** Wave form **160** is an oscilloscope trace of the scale pulses appearing on output lead **26** as supplied to the filter and this trace is expanded in the circles **162, 164, 166, 168** and **170** for the five intervals I_1 through I_5 for eight-cylinder operation. During the first Interval I_1 illustrated at **162** no scale pulses are passed to the filter whereas during the succeeding four intervals correspondingly increased numbers of scale pulses are passed through gate **96** until the fifth interval in which $i-1/4=1$ and all scale pulses pass to the filter. It is apparent that corresponding conditions apply for the four and three intervals of the revolution of the engine for the six- and four-cylinder engine operations.

It is apparent from the above, that the present invention provides an improved average engine timer and particularly one that is of simplified and inexpensive construction and which may be used with a small initial investment in average engine timing equipment. Important features of the present invention include the provision of a variable duty cycle generator for varying the duty cycle of relatively high frequency pulses in accordance with average engine timing. These variable duty cycle pulses are applied through a filter to create an analog signal which may be used to drive an analog indicator such as a conventional voltmeter or ammeter. Also incorporated in the system is a tachometer for indicating engine rpm although it is apparent that the timer of the present invention is substantially independent of speed and there is no necessity for closely controlling engine rpm in order to obtain an accurate reading of average engine timing. The timer may be manually switched so that it operates to indicate average timing for either a four-cylinder, six-cylinder, or an eight-cylinder engine. In addition, the timer incorporates an advance-retard switch so that average engine timing may be indicated either in the advance or retard mode. If desired, the output from filter **28** may be applied through an analog to digital converter to a digital counter or the like to provide a digital display of engine timing.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiment is therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

I claim:

1. An average timer for multicylinder internal combustion engines comprising a first input terminal for receiving a signal indicative of a predetermined angular position of the engine crankshaft during each revolution of an engine under test, a second input terminal for receiving a signal indicative of the time of firing of each spark plug of an engine under test, two successive signals at said first input terminal defining a first longer time interval, the successive signals at said second input terminal within said first time interval defining in combination with said successive signals at said first input terminal a series of shorter time intervals within each longer time interval, an oscillator, a duty cycle generator coupled to both said input terminals and to said oscillator, said duty cycle generator modifying the oscillator signals to produce an electrical output which has a different duty cycle for each of said shorter time intervals in a longer time interval, a detector coupled to said duty cycle generator for producing an analog signal representative of the duty cycle of the output from said generator, and means for coupling a display to the output of said detector.

2. A timer according to claim **1** wherein said detector comprises a low pass filter.

3. A timer according to claim **2** wherein said duty cycle generator comprises a variable modulus counter and a selection network including a plurality of logic gates for gating the pulses passed from said variable modulus counter to said filter.

4. A timer according to claim **3** wherein said counter includes means for dividing by four, means for dividing by three and means for dividing by two.

5. A timer according to claim 3 wherein said duty cycle generator further comprises a spark counter coupled between said terminals and said selection network for controlling said selection network in accordance with the time difference between the signals received at said terminals.

6. A timer according to claim 5 wherein said spark counter supplies a different signal to said selection network with the receipt of each signal from either one of said terminals during a revolution of an engine under test.

7. A timer according to claim 6 wherein said spark counter is triggered by the signal from said second terminal and reset by the signal from said first terminal.

8. An average timer for multicylinder internal combustion engines comprising a damper pick up for producing impulses indicative of a predetermined angular position of the engine crankshaft during each revolution of an engine under test, a spark pick up for producing impulses indicative of the firing of each spark plug of an engine under test, a pulse oscillator, a divider coupled to the output of said oscillator, said divider including means for dividing the number of output pulses from said oscillator by a factor dependent upon the number of cylinders in an engine under test, a selection network including a plurality of logic gates coupled to the output of said divider for passing selected pulses from said divider, a spark counter coupling said damper and spark pickups to said selection network for controlling said selection network in accordance with the time relationship between the impulses from said pickups, a low pass filter coupled to the output of said selection network, and display means coupled to the output of said filter.

9. A timer according to claim 8 wherein said display means comprises an analog display.

10. A timer according to claim 9 wherein said display comprises a meter with a movable pointer.

11. A timer according to claim 10 wherein said meter is coupled to said filter by an advance-retard switch whereby either advance or retard engine firing may be displayed on said meter.

12. A timer according to claim 8 wherein said spark counter supplies a first output to said selection network for a first interval between a damper impulse and the first spark impulse of an engine revolution, a different output for each interval between successive spark impulses of said engine revolution, and a still different output for the interval between the last spark impulse of said revolution and the next damper impulse.

13. A timer according to claim 12 wherein said selection network passes increasing proportions of the pulses from said divider with each of the successive intervals of said revolution.

14. A timer according to claim 13 wherein said selection network passes no pulses from said divider during the first interval of said revolution and all the pulses from said divider during the last interval of said revolution.

15. A method of determining average engine timing in a multicylinder engine comprising generating a series of pulses, detecting each engine damper and spark impulse for each revolution of an engine under test, scaling the series of pulses to produce an output having a different duty cycle for each time interval between successive damper and spark impulses in a single revolution of the engine, and producing an analog signal proportional to the duty cycle of the scaled pulses.

16. A method according to claim 15 wherein said pulses are also scaled in accordance with the number of cylinders in the engine under test.

17. A method according to claim 16 wherein said pulses are scaled according to the formula:

$$\delta_{AVE}=\sum_{n=1}^{x}\frac{\delta m}{x}$$

where

δ_{AVE} = average timing δ_M = timing with respect to cylinder M X = number of engine cylinders ÷ 2.

18. A method according to claim 17 wherein X may have any of the values selected from the group consisting of two, three and four.

* * * * *

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,832,628 Dated August 27, 1974

Inventor(s) Joseph R. Pottebaum

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Col. 2, line 2, "inperfections" should read --imperfections--.

In Col. 8, line 23, (formula 4, bottom line), "n = 1" should read --m = 1--.

In Col. 12, line 34, (formula, bottom line), "n = 1" should read --m = 1--.

Signed and sealed this 5th day of November 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSAHLL DANN
Commissioner of Patents