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(54) Title: HIGH PERFORMANCE POLYCRYSTALLINE TRANSISTORS

(57) Abstract: The invention teaches new uses for a class of polycrystalline semiconductors and highly defected semiconductors, particularly in the channel region of a thin-film field-effect transistor (TFT). The invention also discloses methods used to design and fabricate high performance electronic devices using semiconductors from said class.

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Title:

High Performance Polycrystalline Transistors

Cross-Reference to Related Application:

This application claims priority from U.S. Provisional Patent Application No. 60/475,337, filed 2 June 2003 (our docket No. L3176-014), with the title: "Polycrystalline Microelectronic Devices."

Field of the Invention:

This invention relates generally to the field of thin-film transistors, particularly to the design, structure, and fabrication of high-performance thin-film transistors using polycrystalline compound semiconductors, and also to designs, structures, and fabrication methods of polycrystalline compound semiconductors in high-performance thin-film transistors.

Background of the Invention and Limitations of the Prior Art

State-of-the-art thin-film transistors (TFTs) generally suffer low performance because of the poor electric properties of polycrystalline or amorphous thin-film semiconductors. In particular,

• The mobility (μ) is lowered by the scattering of charge carriers at grain boundaries (J Levinson, FR Shepherd, PJ Scanlon, WD Westwood, G Este, and M Rider, "Conductivity behavior in polycrystalline semiconductor thin-film transistors," *J. Appl. Phys.* v. **53**, p. 1193 (1982)) and other crystalline defects absent in single-crystal (monocrystalline) forms of the same semiconductor material. Lower mobility means lower performance transistors, since $v = \mu \times E$ where v is carrier velocity in the channel (related to frequency response) and E is the electric field in the channel. Though it is sometimes possible to increase the carrier velocity by increasing the electric field, this costs higher operating voltage and power dissipation, and risks breakdown.

• Carrier velocity is further limited by the saturated drift velocity in the thin-film semiconductor, which may also be degraded in polycrystalline material. Lower saturated drift velocity also follows from scattering at grain boundaries and dislocations, resulting in lower frequency response by way of increased the transit time (τ) through the FET channel.

• Limitations on processing technology for TFTs heavily penalize minimum feature sizes smaller than 1 μm, and usually smaller than 2 μm. Transistor uniformity constraints can further limit the minimum feature size by requiring each transistor element to incorporate a minimum number of grains. Large feature sizes necessitate large gate widths and source-to-drain spacing (L), resulting in lower speed performance (f_T).

• TFTs are often deposited on low-cost glass or flexible polymeric substrates, which can withstand only modest processing temperatures. Low processing temperatures generally produce higher defect densities and small grains, hence losses and more grain boundary scattering. Glass and most flexible substrates also have low thermal conductivity, meaning poor heat dissipation properties, limiting the power density of devices and circuits.

Prior art approaches raising TFT performance have focused primarily on polycrystalline silicon (polysilicon) which is easy to deposit amorphously, anneal to achieve a desired grain size (including rapid thermal annealing, laser annealing, and other approaches), passivate to reduce scattering at grain boundaries, coat (additively or by growth) with oxides and nitrides for the gate dielectric and passivation, and back-end process to define

transistors and other electronic devices. Much of the success of polysilicon TFTs follows from knowledge about, and techniques for, passivating their grain boundaries and the oxide-semiconductor (or insulator-semiconductor) interface.

Despite these advantages, polysilicon suffers from low mobilities and low saturated drift velocities, limiting the modulation frequency of polysilicon TFTs with L >1 μm to f_T <1 GHz.

Compound semiconductors have been considered as alternatives to polysilicon for TFTs with L >1 μm, particularly in applications requiring f_T >1 GHz, such as wireless communications, radar, and high performance computing. One straightforward approach is to incorporate Ge or C into conventional polysilicon, creating polycrystalline SiGe, SiC, or SiGeC. Such approaches yield performance within a factor of only about twice that of polysilicon.

ZnO TFTs have been fabricated by S Masuda, K Kitamura, Y Okumura, S Miyatake, H Tabata, and T Kawai, "Transparent thin-film transistors using ZnO as an active channel layer and their electric properties," *J. Applied Physics,* v. **93**, p. 1624, Feb. 2003. These TFTs exhibited a mobility below 1 $cm^2V^{-1}s^{-1}$, which leads to very low modulation frequency performance. Similarly, CdSe has been considered as a TFT semiconductor, achieving TFT channel mobilities as high as 180 $cm^2V^{-1}s^{-1}$, which remains lower than that achieved by polysilicon TFTs.

GaAs is also a candidate semiconductor for TFTs because it exhibits high mobilities and high saturated drift velocities when used in a single-crystal form. However, surface states at grain boundaries in GaAs lower its mobility to <10 $cm^2V^{-1}s^{-1}$, ruining TFT performance. (F Greuter and G Blatter, "Electric properties of grain boundaries in polycrystalline compound semiconductors," *Semicond. Sci. Technol.* v. **5**, p. 111, 1990. Also, JJJ Yang, PD Dapkus, RD Dupuis, and RD Yingling, "Electric properties of polycrystalline GaAs films," *J. Appl. Phys.* v. **51**, p. 3794, 1980, and U.S. Patent No. 5,481,120).

When these materials are used in a FET such as a TFT, a high density of surface states at the top (and/or bottom) interface of the channel region ordinarily degrades performance. Furthermore, the density of such surface states is not well controlled, and differences in the density of surface states from device to device often results in significant shifts in the threshold voltage of different FET devices. Additionally, if surface states exist with trapping time constants comparable to the FET's cycle time or

longer, the states will act as a time-dependent charge, further degrading the performance of the TFT.

The InAs TFT and InN polycrystalline materials are promising, but have failed to achieve commercial success for a number of reasons. Polycrystalline InN layers have shown mobilities as high as 2700. (AG Bhuiyan, A Hashimoto, and A Yamamoto, "Indium nitride: A review on growth, characterization, and properties," *J. Applied Physics*, **94**, p.2779, (2003). Also TL Tansley and CP Foley, "Electron Mobility in Indium Nitride," *Electron Lett.* **20** 1066-1068, (1984).) Furthermore, free InN surfaces exhibit a high density of surface states acting as shallow donors, pinning the Fermi level deep into the conduction band with a surface state density as high as 2×10^{13} cm^{-3} (I Mahboob, TD Veal, CF McConville, H Lu and WJ Schaff, *Phys. Rev. Lett.* **92**, p. 036804, (2004). Even though free InN surfaces exhibit such a high surface state density, surface states acting as shallow donors means electrons accumulate at free surfaces and can form a high conductivity surface channel. Where such an accumulation layer is achieved at grain boundaries in polycrystalline material, its free charges screen the ionized surface charges, and band bending at the interface results in only a narrow potential *well*. These effects greatly reduce carrier scattering a grain boundaries. This situation differs from the more common case of a wide potential *barrier* at grain boundaries observed in most semiconductors, including Si and GaAs. Reduced scattering at grain boundaries in InN suffices to explain the high mobilities observed in polycrystalline InN.

Thin films of InAs also achieve very high channel mobilities (D Scott, M Urteaga, N Parthasarathy, JH English, and M Rodwell, "Molecular Beam Deposition of Low-Resistance Polycrystalline InAs," Lester Eastman Conference, University of Delaware, Newark. (August 6 - 8, 2002)), demonstrating Hall mobilities up to 886 $cm^2V^{-1}s^{-1}$. Field-effect mobilities as high as 3000 have been observed in a thin-film MOSFET structure grown on a glass substrate. (HE Kunig, "Analysis of An InAs Thin-film Transistor," *Solid-State Electronics*, **11**, p. 355. (1968)). InAs exhibits a strong similarity to InN insofar as its electrons accumulate of at free surfaces due to oxidation and/or passivation. (L Canali, JWG. Wildöer, O Kerkhof, LP Kouwenhove, "Low-temperature STM on InAs (110) accumulation surfaces," *Appl. Phys. A*, v. **66**, p. 5113, 1998).

Nevertheless, prior art TFTs using InAs and InN have proven commercially unsuccessful. First, thermal instability of the InAs layers has been misunderstood, such as by K Kano, and H Kunig, "Effect of Thermal

Instability on Ultra-High Frequency Performance of Insulated-Gate Field-Effect Transistors," *Solid-State Electronics*, **12**, p. 719. (1969), and was attributed to the high transconductance of the InAs TFT, low thermal conductivity of the glass substrate, and narrow band gap of the InAs. However, their analysis incorrectly treated the scaling of L_g and current densities, which now allow smaller devices to operate at lower power densities, avoiding thermal instability at high f_T. Second, metal-oxide semiconductor (MOS) and metal-insulator semiconductor (MIS) structures on InAs and other III-V compound semiconductors exhibit a high surface-state density (DA Baglee, DK Ferry, CW Wilmsen, and HH Wideer, "Inversion layer transport and properties of oxides on InAs," *J. Vac. Sci. Technol.*, **17**, p. 1032, and HH Wieder, "Perspectives on III-V compound MIS structures," *J. Vac Sci. Technol.*, **15**, p. 1498, 1978, HA Washburn, JR Sites, and HH Wieder, "Electronic profile of n-InAs on semi-insulating GaAs," J. Appl. Phys. v. 50, p. 4872 1979). Typical surface-state densities in InAs, 10^{12} cm^{-2}, degrade TFT performance significantly.

Undoped polycrystalline InAs exhibits a high sheet electron density. Its free electron concentration partly depends on its density of surfaces, including top and bottom surfaces of the channel, as well as the grain boundaries within the channel. Depletion of an InAs or InN channel with a high sheet electron density consequently requires a high gate voltage, hence a high resistivity, high dielectric-strength gate insulator to prevent breakdown. In the prior art, thick InAs films have been preferred to achieve high mobilities and low background carrier concentrations, but a thick InAs channel is difficult to fully modulate with the field effect due to the high intrinsic background doping from self-doping by surface states at grain boundaries which screens the applied electric field. Unless full modulation is achieved, a parasitic channel exists, lowering f_T and raising the power dissipation and operating temperature.

The use of lattice-matched, wider band gap polycrystalline semiconductors (such as AlGaSb, AlAsSb or AlGaAsSb on InAs) to passivate the InAs channel surface states and act as a barrier layer for metal semiconductor field effect transistors (MESFETs) is not expected to provide a suitably low gate currents, because parasitic conduction channels around grain boundaries is expected to results in excessive gate leakage currents. (MJ Cohen, MD Paul, DL Miller, JR Waldrop, and JS Harris, Jr., "Schottky barrier behavior in polycrystal GaAs," *J. Vac. Sci. Technol.*, **17**, p. 899. (1980).)

Consequently, there is a need for TFTs exhibiting high mobility not degraded by surface states and gate insulator properties. Recently, Asif Khan, et. al (US Patent No. 6,690,042, US Patent Application No. 2002/0052076, US Patent Application No. US 2004/0036086) have developed the concept of the metal oxide semiconductor heterostructure field effect transistor (MOSHFET) using GaN and related compound semiconductors. They describe a method to "prevent current-voltage characteristic collapse at high drain biases due to the large density of interface states" in heterostructure field effect transistors (HFET) by simultaneously lowering the surface state density of a FET's channel region while increasing the insulating property of the gate, by combining heterojunction confinement of the channel with a high performance gate insulator. The MOSHFET design would enable high performance FET operation if the surface state density were *lower* than the sheet carrier concentration in the channel, enabling high performance despite high dielectric-semiconductor interface state densities. For example, the '042 Patent states, "The surface charge density in SiO_2 layer, n_s is estimated to be about 1×10^{12} cm^{-2}. This is one order of magnitude less than the sheet carrier density (of free carriers) in the 2D electron gas channel of the MOSHFET, thereby indicating a high quality for the SiO_2/AlGaN interface."

Similar MOSHFET structures have been investigated for single cyrstal GaAs FET devices (M Passlack, JK Abrokwah, R Droopad, Z Yu, C Overgaard, S In Yi, M Hale, J Sexton, and A Kummel, "Self-Aligned GaAs *p*-Channel Enhancement Mode MOS Heterostructure Field-Effect Transistor," *IEEE Electron Device Letters*, v. **23**, p. 508, 2002), where advances in the dielectric-semiconductor interface have lead to a low density of surface states, hence good MOSFET characteristics, including inversion mode devices.

However, the prior art MOSHFET approaches fail to understand or teach that the confinement of carriers in a channel can advantageously be used to substantially eliminate performance degradation due to the interface states at the semiconductor-dielectric interface, especially regarding high frequency performance of polycrystalline compound semiconductors. Confinement of carriers in the channel region can be achieved not only by using heterojunction confinement, but may also incorporate a spatial profile of ionized donors (or acceptors) that confine the channel carriers to a specific region of the device and away from the semiconductor-dielectric interface. The use of a means for confining charge carriers in the channel — such as a heterostructure, a doping profile, or both — to create potential barrier making it energetically unfavorable for charge carriers to leave the channel,

enables TFTs to be created with dramatically lower sensitivity to surface states at the dielectric-semiconductor interface. They transfer the surface state density from the dielectric-semiconductor interface to the confinement means. Due to the fact that heterojunction confinement in compound semiconductors can achieve lower interface state densities than compound semiconductor-dielectric interfaces, this trade-off is advantageous. The confinement means enables high performance polycrystalline metal insulator field effect transistors (MISFETs) to be achieved without prior art failures of high gate leakage currents or high semiconductor/insulator interface state densities.

While certain compound semiconductors with greater than 20% atomic concentration of indium (e.g. InAs, InN, $In_{0.5}Ga_{0.5}As$) can be made with excellent mobilities in thin-film polycrystalline forms, such materials have not been suitable for TFTs because surface states and surface scattering have prevented effective gate modulation of the conductivity using the field effect. An important embodiment of the present invention employs channel confinement with a thin-film polycrystalline compound semiconductor containing at least 20% atomic concentration of indium to enable thin-film transistors (TFTs) with performance far exceeding that of polysilicon TFTs.

Objects of the Invention:

An object of the invention is to create high performance polycrystalline TFTs by employing certain high mobility, III-V compound semiconductors a with higher sheet carrier concentrations than surface state densities. Another object is to form the channel of a thin-film MOSHFET in such materials, particularly with sheet carrier concentration > 10^{11} cm^{-2}. Another object of the invention is to employ high quality dielectrics such as SiO_2 or Si_3N_4 to reduce the gate leakage and surface state density. Another object is to reduce costs by depositing a gate dielectric using evaporation, sputtering, chemical vapor deposition (CVD), pulsed laser deposition (PLD), jet vapor deposition (JVD), molecular beam epitaxy (MBE), vapor transport (VT), or related low-cost techniques. Another object is to improve the gate dielectric by forming an amorphous oxide by anodic oxidation of a semiconductor surface. Another object is to improve the gate dielectric by forming a high quality non-amorphous material, such as polycrystalline GaP. Another object is to use thin-film compound semiconductors with high indium concentrations in the channel regions of the device, such as InAs, InGaAs,

InAsP, InAlAs, InSb, InGaSb, InN, InGaN, and related alloys. Another object is to improve surface passivation of the upper and lower planes of the channel region (not to be confused with passivating the grain boundaries) using lattice-matched heterojunction layers. Another object is to improve surface passivation of the channel region by including pseudomorphic heterojunction layers, especially where the pseudomorphic thickness of the polycrystalline material may differ from the pseudomorphic thickness of monocrystalline material. Another object is to produce a high sheet carrier concentration in the channel region by modulation doping. Another object is to produce a high sheet carrier concentration in the channel region by "self-doping" by means of surface states at grain boundaries. Another object is to employ conventional doping in the channel region itself via Si, Sn, or other *n*-type dopants. Another object is an apparatus using a semiconductor thin film formed from a semiconductor material exhibiting high mobilities even in the presence of a high density of grain boundaries and dislocations, such as polycrystalline (or amorphous) compound semiconductors including InAs, InN, InGaAs, InAsP, InAlAs, InSb, InGaSb, InGaN, InGaAlN and other alloys of these materials, especially when possessing an indium concentration above 20%. Another object is an apparatus using a semiconductor thin film formed from a semiconductor material exhibiting a high sheet carrier concentration in the channel, typically above 1×10^{11} cm^{-2}. Another object of the invention is control of the effective doping concentration, such that extrinsic or intrinsic donors are located in or near the channel and away from the semiconductor-dielectric interface. A further object of the invention is to employ modulation doping as a means of producing the high sheet carrier concentration in the channel region, by providing dopants in the upper heterojunction confinement layer, the lower heterojunction confinement layer, or within the channel itself using modulation doping of a super-lattice structure, where alternating layers of semiconductors provide alternating barrier and channel regions, with the doping confined to the barrier regions. Another object is a heterojunction confinement layer providing a low surface state density at the interface between the confinement layer and the channel and a potential barrier blocking the majority of carriers in the channel from reaching the insulator/semiconductor interface. A further object of this invention is to provide heterostructure passivation beneath the channel region and/or above the channel region. Another object is a high quality dielectric gate insulator layer such as SiO_2, Si_3N_4 or amorphous GaP, located adjacent to the heterostructure confinement layer, and providing a barrier to

electron flow between the gate and the channel layer. A further object of the invention is a high quality dielectric gate insulator layer formed from crystalline materials, such as polycrystalline GaP or polycrystalline Al_2O_3, provided such layers achieve suitable insulating properties with low surface, fixed, and mobile charge densities. .

Summary of the Figures:

Figures 1A, 1B and **1C** show the band diagram of various polycrystalline semiconductors, showing the barriers to transport across grain boundaries.

Figure 2 shows the layer structure of an InAs thin film deposited on SiO_2.

Figure 3A shows the layer structure of a metamorphic InGaAs on GaP FET layer structure with a high density of dislocations.

Figure 3B shows the cross sectional geometry of a FET fabricated using the metamorphic InGaAs on GaP FET layer structure

Figure 3C shows an overhead view of the geometry of a FET fabricated using the metamorphic InGaAs on GaP FET layer structure

Figure 3D shows the current-voltage characteristics of the gate diode used to modulate the conductivity of the InGaAs on GaP FET.

Figure 3E shows the common source characteristics of the InGaAs on GaP FET

Figure 4A shows the layer structure of the preferred embodiment.

Figure 4B shows the cross sectional geometry of a FET fabricated from the preferred embodiment.

Figure 4C shows an overhead view of the geometry of a FET fabricated from the preferred embodiment.

Figure 4D shows a plot of the charge density as a function of vertical depth into the device.

Figure 5A shows the layer structure of alternative embodiments.

Figure 5B shows the cross-sectional geometry of a FET fabricated from the alternative embodiment.

Figure 5C shows an overhead view of the geometry of a FET fabricated from the alternative embodiment.

Detailed Description of the Figures:

Reference is now made to **Figure 1A** showing the band diagram of a semiconductor that exhibits strong Fermi level pinning at grain boundaries. Strong Fermi level pinning is observed for many of the commonly used semiconductors, including Si, Ge, and GaAs. The band diagram plots energy **198** as a function of lateral position **199**. The conduction band **101A**, valence band **103A** and Fermi level **102A** are shown in the figure. Grain boundaries **105A** normally exhibit a high density of surface states **106A**. The surface states may be distributed in energy throughout the forbidden gap of the semiconductor (as shown in the diagram) or may be tightly concentrated at certain energy levels in the forbidden gap. The surface states **106A** trap free carriers from the surrounding semiconductor region, resulting in a wide depletion region surrounding the grain boundaries **105A**. The depletion region surrounding the grain boundaries **105A** cause localized band bending in region **110A**, and result in a barrier of energy height **111A** to carrier transport across the grain boundaries **105A**. This barrier acts to block carrier transport across grain boundaries **105A**, as well as causing a significant of scattering and thereby severely lowered carrier mobility.

Reference is now made to **Figure 1B**, showing the band diagram of a semiconductor that exhibits weak Fermi level pinning at grain boundaries. Weak Fermi level pinning is observed for some semiconductors such as InP. The band diagram plots energy **198** as a function of lateral position **199**. The conduction band **101B**, valence band **103B** and Fermi level **102B** are shown in the figure. Grain boundaries **105B** exhibit only a low density of surface states **106B**. The surface states **106B** may be distributed in energy throughout the forbidden gap of the semiconductor (as shown in the diagram) or may be tightly concentrated at certain energy levels in the forbidden gap. This low density of surface states **106B** only trap a small fraction of free carriers from the surrounding semiconductor, resulting in a narrow depletion region surrounding the grain boundaries **105B**. The depletion region surrounding the grain boundaries **105B** cause localized band bending in region **110B**, and result in a low barrier of height **111B** to carrier transport across the grain boundaries **105B**. This barrier acts to only slightly block carrier transport across grain boundaries **105B**, causing some carrier scattering and hence only a moderate degradation in carrier mobility.

Reference is now made to **Figure 1C**, showing the band diagram of a semiconductor that exhibits Fermi level pinning within the conduction band. Fermi level pinning at or within the conduction band is observed for some

alloys of InAs and InN. The band diagram plots energy **198** as a function of lateral position **199**. The conduction band **101C**, valence band **103C** and Fermi level **102C** are shown in the figure. Grain boundaries **105C** exhibit the majority of surface states with energies near the conduction band edge **101C**, such that a high fraction of the surface states are ionized at the operating temperature and act as shallow donors rather than the deep level defects shown in Figures 1A and 1B. This concentration of surface state **106C** energies near the conduction band **101C** results in an accumulation of majority carriers at the grain boundaries **105C**. The accumulation region surrounding the grain boundaries **105B** cause a reverse band bending in region **110C**, and result in a negative barrier of height **111C** to carrier transport across the grain boundaries **105C** and an accumulation of majority carriers around grain boundaries **105C**. However, the reverse band bending in regions **110C** and discontinuity across grain boundaries **105C** may cause some carrier scattering due to quantum mechanical reflections, causing a small amount of degradation in carrier mobility.

Semiconductors that exhibit either a low surface state density as shown in **Figure 1B** or surface states concentrated at energy levels near the band edge (within $2k_BT$ - $5k_BT$ of the band edge) as shown in **Figure 1C** are expected to be excellent candidates for thin film transistors, with the key performance parameter being their low field mobility. Semiconductors that exhibit a high density of surface states in the forbidden band gap as shown in **Figure 1A** are not expected to be suitable for TFTs, unless some sort of surface passivation technique can be developed to lower the density of surface states. Indeed, surface state passivation is one technique used to improve the properties of polysilicon TFTs.

Reference is now made to **Figure 2**, showing the layer structure of a thin film of InAs deposited on SiO_2. A thermal oxide **203** of thickness **213** of 300 nm is first grown using conventional oxidation techniques on top of a <100> *p*-type silicon substrate **201** of thickness **211** between 500 and 550 μm. The wafer is introduced into a MBE machine, where InAs layer **205** is grown to a thickness **215** of 50 nm. The undoped InAs layer is grown under slightly arsenic rich conditions at a substrate temperature of 350 °C. Upon completion of the growth of layer **205**, the wafer is removed from the MBE and JVD is used to deposit a silicon nitride layer **207** to a thickness **217** of 10 nm (TP Ma, "Making Silicon Nitride Film a Viable Gate Dielectric," *IEEE Trans. Electron. Dev.*, v. **45**, p. 680, 1998).

Upon completion of the deposition of layer **207**, The wafer can be cut into several pieces and annealed to various temperatures using rapid thermal annealing. The resulting mobility as a function of annealing temperature is shown in Table I. As can be clearly seen in the table, high mobilities are achieved, with a significant improvement in mobility observed for higher temperature anneals, which is likely due to a reduction of the defects in the InAs layer **205**. The high carrier concentrations are likely a direct result of self doping through the surface states at grain boundaries and dislocations (V Gopal, E-H Chen, EP Kvam, and JM Woodall, "Behavior of a new ordered structural dopant source in In/(001) GaP Heterostructures," *J. Vac. Sci. Technol.* **B**. 17, p. 1767, 1999), as well as at the top surface **225A** and bottom surface **225B** of the InAs layer **205**.

Table I. Hall effect measurements of the layer structure shown in Figure 2. As a function of annealing. Note that the high observed electron concentrations are likely a direct result of self-doping via interface states at both the grain boundaries and top interface 225A and bottom surface 225B.

Anneal temperature	Electron concentration (cm^{-3})	Mobility ($cm^2V^{-1}s^{-1}$)
500 °C, 30 sec	8.7×10^{18}	201
600 °C, 30 sec	5.5×10^{18}	571
700 °C, 30 sec*	6.1×10^{18}	687
800 °C, 30 sec*	8.8×10^{18}	396

* Increased surface roughness indicates that a reaction at the Si_3N_4 / InAs interface may be occurring, causing an increase in the carrier concentration and eventual decrease in mobility.

Reference is now made to **Figure 3A** depicting the layer structure of an FET grown on a *n*-type *crystalline* GaP substrate **301** with a thickness **311** of 500 μm. All layers are grown using conventional MBE techniques at substrate temperatures between 300 and 400 °C. An undoped $In_{0.75}Al_{0.25}As$ buffer layer **303** is grown on top of the crystalline GaP substrate **301**. Due to the large lattice mismatch between GaP and $In_{0.75}Al_{0.25}As$, a high density of dislocations **325** is generated to relieve the strain. The $In_{0.75}Al_{0.25}As$ layer **303** is grown to a thickness **313** of 1.0 μm, which provides a buffer between the GaAs substrate **301** and the channel region **305**. On top of the buffer layer **303** is grown an undoped $In_{0.75}Ga_{0.25}As$ channel layer **305**, grown to a thickness **315** of 100 nm. Based on our previous measurements of similar lattice mismatched growth (H Tsukamoto, E-H Chen, JM Woodall, V Gopal, "Correlation of defect profiles with carrier profiles of InAs epilayers on GaP," *Appl. Phys. Lett.*, v. **78**, p.

952, 2001), we expect the dislocation density in the channel layer **305** to be in the range of $1 \times 10^8 - 1 \times 10^9$ cm^{-2}. On top of channel layer **305** is grown a pseudomorphic $Al_{0.5}Ga_{0.5}As$ gate insulator layer **307** to a thickness **317** of 10 nm.

Reference is now made to **Figure 3B**, which shows a cross sectional view of the geometry of FETs fabricated from the layer structure shown in **Figure 3A**. First, gate contact layer **321** is deposited on top of gate insulator layer **307** through a liftoff mask that defines the gate dimensions. The lateral dimension of the gate is **331**, which is commonly referred to as the gate length. The gate metal **321** is a combination of Ti, deposited directly on top of the gate insulator **307**, followed by Au deposited directly on top of the Ti layer. The gate metal **321** is expected to form a Schottky diode with a significant barrier height to the gate insulator layer **307**. A photolithographic liftoff mask is used to define the source contact **322** and the drain contact **323**. Since the liftoff mask is absent in the regions where the source and drain contacts are to be formed, the liftoff mask may be used to etch through the gate insulator layer **307** and exposing the channel region **305** in order to facilitate ohmic contacts. Source contact **322** and drain contact **323** are deposited directly on top of the channel region **305**. Ohmic source and drain contacts are readily achieved to $In_{0.75}Ga_{0.25}As$ because it is a low band gap material with native Fermi level pinning near the conduction band edge. The source **322** and drain **323** contacts are formed by depositing Ti directly on top of the channel layer **305**, followed by Au on top of the Ti layer using a liftoff mask to define the contact geometry. The source contact length is **333A** and the drain contact length is **333B**. The spacing between the source and the gate is **332A**, while the spacing between the gate and the drain is **332B**. Mesa **327** is used to isolate adjacent devices, with a mesa length of **335**.

Reference is now made to **Figure 3C**, which depicts an overhead top view of the geometry of the same FET shown in the cross sectional view in **Figure 3B**. The transverse width of source contact **322** is **343A**. The transverse width of drain contact **323** is **343B**. The transverse width of gate metal **321** is **341**. The transverse width of mesa **327** is **345**. Since the effective gate width is determined by the width of mesa **327**, the effective gate width is **345**.

Reference is now made to **Figure 3D**, which shows the dependence of the gate current **351** on the gate-to-source bias **352**. Curve **353** shows the measured Schottky diode characteristics of a gate with a 5 μm gate length **331** and an effective gate width of 140 μm. Curve **353** shows rectifying characteristics, as expected, however, the reverse leakage current for negative gate bias

voltages **352** is larger than desirable (absolute value of the gate current exceeds 100 μA at -5V reverse bias). This excessive gate current is attributed to the presence of defects at the interface between the gate **321** and the gate insulator layer **307**, such a threading dislocation **325**.

Reference is now made to **Figure 3E**, which shows the drain current **361** as a function of the drain bias **362** in the common source configuration (source grounded). Curves **371**, **372**, **373**, **374**, **375**, **376**, **377**, **378**, and **379** are measured drain current curves for gate bias voltages of 0, -0.1, -0.2, -0.3, -0.4, -0.5, -0.6, -0.7, and -0.8 V respectively. Hall measurements of the channel indicate a Hall mobility of 1500 $cm^2V^{-1}s^{-1}$ and a channel carrier concentration of 1×10^{17} cm^{-3}. These results indicate that good mobilities can be achieved despite a high density of dislocations in the channel region of a FET, but also indicate that excessive gate leakage current cause by dislocations in the gate insulator layer are problematic, and are the primary cause of the high drain current observed for high reverse gate voltages, such as that observed in curve **379**.

Reference is now made to **Figure 4A**, showing the layer structure of the preferred embodiment of the invention. Substrate **401** is a single crystal silicon substrate of thickness **411**. A silicon substrate was chosen because of its wide availability, low cost, smooth flat surface, and compatibility with MBE. On top of substrate **401** is grown a thermal oxide **402** to a thickness **412** of 1.0 μm using conventional thermal oxidation techniques. The oxide **402** preferably exhibits a smooth, flat surface with a root-mean-squared surface roughness no larger than one-tenth of the thickness **417** of the channel layer **407**, to ensure that channel layer **407** is continuous and relatively smooth. Layers **403**, **405**, **407**, **409** are deposited using MBE under arsenic-stabilized growth conditions with the arsenic atomic flux to group three atomic flux ratio held to approximately 1.5 (i.e. approximately 1.5 times more arsenic atoms than group III atoms are incident on the substrate). The nominal MBE deposition rate is about 1.0 μm per hour and the nominal substrate temperature is 400 °C. On top of oxide layer **401** is grown an undoped $Al_{0.75}Ga_{0.25}As$ buffer layer **403** deposited to a thickness **413** of 10 nm. This $Al_{0.75}Ga_{0.25}As$ buffer layer **403** will exhibit a good adhesion to the thermal oxide layer **402**, and will exhibit a high resistivity compared to channel layer **407**, ensuring that no significant parasitic conduction channel exists through the buffer layer **403**. Next, an undoped $In_{0.75}Al_{0.25}As$ lower heterostructure confinement layer **405** is deposited to a thickness **405** of 50 nm. Next, an undoped InAs channel layer **407** is deposited to a thickness **417**

of 50 nm. The interface between the channel layer **407** and the lower heterostructure confinement layer **405** is **493**. Next, an undoped $In_{0.75}Al_{0.25}As$ upper heterostructure confinement layer **409** is deposited on top of the InAs channel layer **407**. After the deposition of 6 nm of $In_{0.75}Al_{0.25}As$, the growth is interrupted by shuttering the group III fluxes (cutting off both the In and Al beams), and a silicon flux is introduced to create a silicon delta doping layer **499**, until a delta doping density of 1×10^{12} cm^{-2} is achieved. Next, the remainder of $In_{0.75}Al_{0.25}As$ upper heterostructure confinement layer **409** is deposited to a total thickness **419** of 20 nm. The delta doping layer **499** is spaced 6 nm from the interface **492** between the channel layer **407** and the upper heterostructure confinement layer **409**. Upon completion of the deposition of layer **409**, the group III beam fluxes are again shut off, the arsenic flux is held constant, and the substrate temperature **401** is increased to 600 °C to anneal the layer structure for 10 minutes.

The substrate **401** with layers **403**, **405**, **407**, and **409** is removed from the MBE machine and transferred under vacuum to a JVD system for the deposition of the gate insulator layer **410**. The JVD system is used to deposit SiO_2 as the gate insulator layer **410** to a total thickness **420** of 10 nm.

TFTs can now be fabricated from the layer structure shown in **Figure 4A**. Reference is now made to **Figure 4B**, showing the cross-sectional geometry of a TFT in accordance with the preferred embodiment of the invention. Aluminum gate metal **421** is deposited directly on top of the gate insulator layer **410**, and the gate dimensions are defined using standard photolithographic processing techniques. The lateral gate length is **431**. Source **422** and drain **423** contacts are achieved by first defining a liftoff mask with the photo resist removed from the regions where the source and drain contacts are to be formed. This liftoff mask is used as an etch mask to allow complete removal of the gate insulator layer **410** using a standard buffered oxide etch. Next, the source and drain ohmic contacts are deposited across the whole device structure, and liftoff is used to remove any metal outside the source and drain contact areas. The source and drain metal uses conventional AuGeNi/Ti/Au alloyed contacts and annealing at 370 °C for 30 seconds is used to alloy the contacts through the upper heterostructure confinement layer **409**, allowing direct ohmic contact to channel **407** to be achieved. The lateral length of source contact **422** is **433A**, and the source contact **422** is laterally spaced a distance **432A** from the gate contact **421**. The lateral length of drain contact **423** is **433**, and the drain contact **423** is laterally spaced a distance

of **432B** from the gate contact **421**. Mesa isolation is used to isolate adjacent devices, with mesa **427** having a lateral mesa dimension of **435**.

Reference is now made to **Figure 4C**, which shows an overhead top view of a TFT fabricated in accordance with the preferred embodiment of the invention. The source contact **422** has a transverse width of **433A**, and the drain contact **423** has a transverse width of **443B**. The transverse width of the gate contact is **441**, and the effective transverse width of the channel is defined by the transverse width **445** of mesa **427**.

Reference is now made to **Figure 4D**, which illustrates the various sheet charges that may be present in a device produced according to the invention. In **Figure 4D**, the charge density **401** plotted against the sample depth **402**. Sheet charge **495** is caused by interface states at the interface **491** between the gate insulator layer **410** and the upper heterostructure confinement layer **409**. Sheet charge **496** is caused by the delta doping layer **499** used to provide free carriers to channel **407**. Sheet charge **496** is located at a distance **417** from the upper gate insulator layer **410** and a distance **418** from the channel layer **407**. Sheet charge **497** is caused by the interface **492** between the upper heterostructure confinement layer **409** and the channel layer **407**. Sheet charge **498** is caused by the interface **493** between the lower heterostructure confinement layer **405** and the channel layer **407**.

A numerical example clarifies the dependence of the TFT on sheet charges. Assume the sheet charge density **495** is 5×10^{11} cm^{-2}, the sheet charge density **496** is 1×10^{12} cm^{-2}, the sheet charge density **497** is 1×10^{10} cm^{-2}, the sheet charge density **498** is 1×10^{10} cm^{-2}, the thickness **420** of gate insulator layer **410** is 10 nm, the thickness **419** of the upper heterostructure confinement layer **409** is 20 nm, the thickness **417** of the channel layer is 50 nm, the distance **417** is 14 nm, the distance **418** is 6 nm, the dielectric constant of layer 410 is 3.9 (i.e. equivalent to the dielectric constant of SiO_2), the dielectric constant of layers **407** and **409** is 12.3 (approximately the dielectric constant of InAs based compound semiconductors), the capacitance of layer **410** (i.e. the capacitance between the gate and charge **495**) is about 3.5×10^{-7} F/cm^2, the capacitance of layer **410** plus the thickness **417** of layer **409** (i.e. the capacitance between the gate and charge **496**) is about 2.4×10^{-7} F/cm^2, the capacitance of layer **410** plus the entire thickness of layer **409** (i.e. the capacitance between the gate and charge **497**) is about 2.1×10^{-7} F/cm^2, the capacitance of layer **410** plus the entire thickness of layer **409** plus the entire thickness of layer **407** is 1.1×10^{7}

F/cm^2. The differential gate voltage associated with the sheet charge can be calculated from $q \times N_S / C$, where q is the electron charge, N_s is the sheet charge, and C is the capacitance. The voltage shifts associated with the interface charges are shown in Table II. As is evident in the table, the threshold voltage of the device will be dominated by the sheet charge **496**, which is desirable, because sheet charge **496** is intentionally produced by the doping, and therefore the voltage properties of the device are dominated by the intentional doping, and not by the parasitic interface charges **495**, **497**, and **498**. In particular, the variation in the threshold voltage shift due to variations in the sheet charge density **495** cause by processing variation is not expected to cause significant variation in gate threshold voltages.

Table II. Calculated gate voltage shifts necessary fully deplete the sheet charges **495**, **496**, **497**, and **498** for the example sheet charge densities and layer capacitances.

Figure 4D ID number	Sheet Charge density (cm^{-2})	Capacitance (F/cm^{-2})	Gate voltage shift (V)
495	5×10^{11}	3.5×10^{-7}	0.23
496	1×10^{12}	2.4×10^{-7}	0.67
497	1×10^{10}	2.1×10^{-7}	0.01
498	1×10^{10}	1.1×10^{-7}	0.01

This structure satisfies the objects of the invention listed above. The preferred embodiment of the invention is embodied as a high performance polycrystalline TFT employing a high mobility, III-V compound semiconductor in the channel region **407** a with higher sheet carrier concentration than surface state density **495** in the channel using a thin-film, confined channel structure. It advantageously uses a thin film of polycrystalline compound semiconductor material with high indium concentration in the TFT's channel region **407**, resulting in high electron mobility and high saturated drift velocity despite the presence of a high density of grain boundaries. It employs high quality dielectric layer **410** to reduce both the gate leakage current and surface state density **495**. It advantageously confines the upper and lower surfaces **492** and **493** respectively of the channel region **407** using lattice-matched and pseudomorphic heterojunction confinement layers with low interface state densities between the confinement layers and the channel region at surfaces **492** and **493**. The lower $In_{0.75}Al_{0.25}As$ confinement layer **405** is mostly lattice-matched to the $In_{0.75}Ga_{0.25}As$ channel **407**. The upper $In_{0.50}Al_{0.50}As$ confinement layer **409** exhibits a significant amount of strain with respect to the $In_{0.75}Ga_{0.25}As$ channel layer **407**, but grown to a thickness

419 that is expected to be less than the critical thickness for strain relaxation and therefore layer 409 is a pseudomorphic strained layer (note that it is polycrystalline, but within single grains, layer 409 is pseudomorphic with respect to layer 407 and does not result in the generate a significant amount of additional dislocations due to strain at the interface inside a single grain. Advantageously, a high sheet carrier concentration is produced in the channel region 407 by modulation doping 499. The combination of the confinement layers 405 and 409, and the modulation doping 499 result in a very effective confinement of the channel layer 407, with the FET channel 407 separated from surface 491 with a potential barrier that substantially blocks electron transport between the channel 407 and surface states at 491, and hence these surface states do not substantially degrade the high frequency performance of the transistor.

Reference is now made to **Figure 5A**, showing the layer structure of several alternative embodiments of the invention. The thin film semiconductor layers 503, 505, 507, 509, and 510 are deposited on a substrate 501 of thickness 511. Thin films of these compound semiconductors may be produced using conventional deposition techniques such as evaporation, sputtering, chemical vapor deposition (CVD), molecular beam epitaxy (MBE), pulsed laser deposition (PLD), close-spaced vapor transport (CSVT), hot wire deposition, or any other well-known or future thin film deposition technique. The thin films may be deposited in either polycrystalline or amorphous form, and annealing may be used to modify the crystalline structure to achieve grain sizes that support high mobility in these polycrystalline TFTs. Substrate 501 may be any compatible material, including polymers, glass, metal foil, sapphire, or crystalline silicon. On top of substrate 501 is deposited an optional buffer layer 503 to a thickness 513. Buffer layer 503 should exhibit a high resistivity compared to channel layer 507 to ensure that no significant parasitic conduction channel exists through the buffer layer 503. Buffer layer 503 may be an amorphous layer such as amorphous GaAs, amorphous GaP, amorphous silicon, amorphous SiO_2, or amorphous Si_3N_4. Buffer layer 503 may also be a crystalline layer (including nano-crystalline, polycrystalline, micro-micro-cryatalline, or single crystal) that is compatible with the channel layer 507, including polycrystalline germanium, polycrystalline silicon, polycrystalline GaAs, polycrystalline GaP, polycrystalline InP, polycrystalline $In_xAl_{1-x}As$ ($0 < x < 1$), single crystalline GaP, etc. On top of layer 503 is deposited an optional lower heterostructure confinement layer 505 with a thickness 515. Layer 505 preferably exhibits a larger band gap

than channel layer **507**, providing heterojunction confinement of layer **507**. Lower heterostructure confinement layer **505** can be formed from any suitable semiconductor, such as $In_xAl_{1-x}As$ ($0 < x < 1$), InP, $In_xGa_{1-x}P$ ($0 < x < 1$), $InAs_xP_{1-x}$ ($0 < x < 1$), $In_xGa_{1-x}In_xGa_{1-x}As$ ($0 < x < 1$), silicon, and so forth. Layer **505** may optionally include a doping plane **598** (delta doping), or may be doped with any arbitrary doping profile such that donor ions are incorporated into layer **505**, with substantially all of the free electrons generated by said donor ions being captured by the channel layer **507** due to the potential well created by the heterojunction between the lower heterostructure confinement layer **505** and the channel layer **507**. On top of doping layer **505** is deposited the semiconducting channel layer **507** with a thickness **517**. Channel layer **507** preferably exhibits a lower band gap than layers **505** and **509**, and exhibits suitably high mobilities and saturated drift velocities to enable high TFT performance. Channel layer **507** is preferably formed from compound semiconductors containing at least 20% In, including InAs, InN, InP, InSb, $In_xGa_{1-x}As$ ($0.5 < x < 1.0$), $InAs_xP_{1-x}$ ($0 < x < 1.0$), $InAs_xN_{1-x}$ ($0 < x < 1.0$), $In_xGa_{1-x}Sb$ ($0.5 < x < 1.0$), and other combinations of III-V semiconductors with at least 20% of the atoms are In. On top of channel layer **507** is deposited the upper heterostructure confinement layer **509** with a thickness **519**. Upper heterostructure confinement layer **509** preferably exhibits a larger band gap than the channel layer **507**, and provides a significant barrier to block the electrons in the channel layer **507** from escaping to surface **591**. In addition, upper heterostructure confinement layer **509** preferably exhibits a low interface state density to the channel layer **507** at interface **592**. Upper heterostructure confinement layer **509** can be formed from any suitable semiconductor, such as $In_xAl_{1-x}As$ ($0 < x < 1$), InP, $In_xGa_{1-x}P$ ($0 < x < 1$), $InAs_xP_{1-x}$ ($0 < x < 1$), $In_xGa_{1-x}As$ ($0 < x < 1$), silicon, etc. Layer **509** may optionally include a doping plane **599** (delta doping), or may be doped with any arbitrary doping profile such that donor ions are incorporated into layer **509**, with substantially all of the free electrons generated by said donor ions being captured by the channel layer **507** due to the potential well created by the heterojunction between the upper heterostructure confinement layer **509** and the channel layer **507**. On top of the channel confinement layer **509** is deposited the gate insulator layer **510**, with a thickness **520**. The gate insulator layer **510** is preferably a material that is highly insulating with low fixed and mobile charge, and provides a low density of surface states at surface **591**. The gate insulator layer **510** may be formed from amorphous layers such as SiO_2, Si_3N_4, Al_2O_3, Ga_2O_3, or may be

formed from crystalline layers such as GaP or SiC. The gate insulator layer **510** can advantageously be deposited using evaporation, sputtering, chemical vapor deposition (CVD), pulsed laser deposition (PLD), jet vapor deposition (JVD), molecular beam epitaxy (MBE), vapor transport (VT), or related low-cost techniques; or by forming an amorphous oxide by anodic oxidation of a semiconductor surface; or by forming a high quality non-amorphous material, such as polycrystalline GaP. The gate insulator layer **510** may be formed from multiple layers of materials, such as from an anodic Ga_2O_3 and As_2O_3 passivation layer grown directly on top of channel confinement layer **509**, followed by deposition of a high quality insulator layer such as SiO_2. The gate insulator layer **510** may be deposited by a wide range of techniques, including MBE, MOCVD, plasma enhanced chemical vapor deposition (PECVD), sputtering, PLD, CSVT, JVD, and liquid phase deposition (MP Houng, CJ Huang, YH Wang, NF Wang, and WJ Chang, "Extremely low temperature formation of silicon dioxide on gallium arsenide," *J. Appl. Phys.*, v. **82**, p. 5788, 1997). Note that the deposition method for layers **501**, **503**, **505**, **507**, **509**, and **510** may use different techniques, and intermediate processing steps such as annealing may be performed at any time during or between the deposition of each layer. The layer structure presented in Figure 5A is obviously illustrative, and those skilled in the art will recognize that additional layers can be inserted anywhere in the structure to achieve desired goals such as doping control, voltage threshold control, band gap engineering of the channel region, or engineering of the properties of the gate insulator layer.

Reference is now made to **Figure 5B**, which shows a cross sectional view of a TFT fabricated using the alternative embodiment of **Figure 5A** in accordance with the invention. The gate contact **521** is deposited directly on top of the gate insulator layer **510**, and the gate dimensions are defined using standard photolithographic processing techniques. The lateral gate length is **531**. Source **522** and drain **523** contacts are achieved by first defining a liftoff mask, using the liftoff mask to etch through the gate insulator layer **510**, and the gate blocking layer **509**, depositing the source and drain metal contact layer across the whole device structure, and using liftoff to define the source and drain contact areas. The lateral length of source contact **522** is **533A**, and the source contact **522** is laterally spaced a distance **532A** from the gate contact **521**. The lateral length of drain contact **523** is **533**, and the drain contact **523** is laterally spaced a distance of **532B** from the gate contact **521**. Mesa isolation is used to isolate adjacent devices, with mesa **527** having a lateral mesa length of **535**.

Reference is now made to **Figure 5C**, which shows an overhead top view of a TFT fabricated using the alternative embodiment of **Figure 5A** in accordance with the invention. The source contact **522** has a transverse width of **533A**, and the drain contact **523** has a transverse width of **543B**. The transverse width of the gate contact is **541**, and the effective transverse width of the channel is defined by the transverse width **545** of mesa **527**.

Also note that the geometrical definition of the FET devices (shown in **Figures 5B** and **5C**) can proceed in any order, with geometrical definition of some of the lower layers proceeding prior to the deposition of some of the upper layers. For example, layers **501**, **503**, **505**, **507**, and **509** could all be deposited, followed by geometrical fabrication of the source contact **522** and drain contacts **523**, as well as mesa isolation of the FETs, followed by deposition (or growth) of layer **510**, followed by deposition of the gate contact **521**.

The applicants intend to seek, and ultimately receive, claims to all aspects, features and applications of the current invention, both through the present application and through continuing applications, as permitted by 35 U.S.C. §120, etc. Accordingly, no inference should be drawn that applicants have surrendered, or intend to surrender, any potentially patentable subject matter disclosed in this application, but not presently claimed. In this regard, potential infringers should specifically understand that applicants may have one or more additional applications pending, that such additional applications may contain similar, different, narrower or broader claims, and that one or more of such additional applications may be designated as not for publication prior to grant.

A TFT in accordance with **Figure 5** advantageously uses a polycrystalline thin film channel region **507** formed from a semiconductor material exhibiting high mobilities in spite of a high density of grain boundaries and dislocations. Notable polycrystalline (or amorphous) compound semiconductors suitable for demonstrating this property in the channel region of a device typically include InAs, InN, InGaAs, InAsP, InAlAs, InSb, InGaSb, InGaN, InGaAlN and other alloys of these materials. These films typically possess an indium concentration above 20%.

A heterojunction confinement layer **509** advantageously provides a low surface state density at the interface **592** between the confinement layer and the channel **507** and provides a potential barrier blocking the majority of the free carriers in the channel **507** from reaching the insulator-semiconductor interface **591**. Spatial separation of the channel electrons from the

semiconductor-dielectric interface **591** can also be employed advantageously to reduced scattering due to roughness and surface states at interface **591**. Heterojunction confinement layers include lattice-matched layers with a lattice constant matched to less than one percent of the underlying thin-film semiconductor channel. Lattice-matched heterojunction confinement layers are expected to provide excellent passivation of surface states at the interface between the channel region and the heterojunction confinement layer, similar to the passivation of such states achieved using single-crystal heterojunction confinement. For example, InAlAs can be used to passivate an InGaAs channel region, since the lattice constant of the InAlAs can be made sufficiently similar to the lattice constant of the InGaAs that strain across the interface is negligible. Heterojunction confinement layers also include strained pseudomorphic heterojunction layers with more than 1% lattice-mismatched that may provide improved passivation of the surface states at the interface **592** between the heterojunction confinement layer and the channel region. For example, thin pseudomorphic InP layers can be used to passivate an $InAs_{0.5}P_{0.5}$ channel region. Note that the pseudomorphic thickness for polycrystalline material may be different from the pseudomorphic thickness for single crystal material, because the small size of the grains can more readily relieve the strain associated with the lattice mismatch. Heterojunction confinement layers also include lattice-mismatched heterojunctions such that the lattice constant of the heterojunction confinement layer differs greatly from the lattice constant of the channel layer, and both said layers are substantially relaxed with the lattice mismatch accommodated through the generation of dislocations in either the heterojunction confinement layer or the channel layer or both. Such a lattice-mismatched heterojunction is only suitable for heterojunction confinement layer if it provides a means of substantially passivating the surface states at interface **592**.

The heterojunction confinement layer may be chosen to simultaneously provide high quality confinement of free carriers in the channel layer **507** with a low interface state density at interface **592**, and provide a low interface state density at interface **591** to the dielectric layer **510**.

A polycrystalline TFT in accordance with **Figure 5** advantageously uses a thin film formed from a semiconductor material exhibiting a high sheet carrier concentration in the channel **507**, typically above 1×10^{11} cm^{-2}. A high sheet carrier concentration in channel **507** brings several benefits, including

increased transconductance, improved spatial confinement of the channel electrons, and increased tolerance of surface charge at interface **591**.

It is advantageous to provide modulation doping as one means of producing the high sheet carrier concentration in the channel region **507**. Modulation doing is achieved by providing layers with a given density of donor atoms adjacent to the channel layer **507**, with the free carriers generated by the doping being captured by the potential well of the channel layer, allowing the free carriers to be spatially separated from their associated donor atoms. Such spatial separation leads to higher mobility through reduced scattering between the free carriers and the ionized dopant atoms. Modulation doping may advantageously be achieved by providing doping in the upper heterojunction confinement layer **509**, the lower heterojunction confinement layer **505**, or within the channel layer **507** itself using modulation doping of a super-lattice structure, where alternating layers of semiconductors provide alternating barrier and channel regions, with the doping confined to the barrier regions.

Alternatively, "self-doping" via surface states at grain boundaries can be used as a means to produce a high sheet carrier concentration in the channel region **507**. Grain boundaries in these materials can be effectively used to provide doping for the channel region since surface states in semiconductors such as InAs and InN act as shallow donors and result in an accumulation of electrons around such surfaces. Alternatively, conventional doping in the channel region **507** can be achieved via doping Si, Sn, and any other *n*-type dopants.

It is advantageous to control the effective doping concentration, so that extrinsic or intrinsic donors are located in or near the channel **507** and away from the semiconductor-dielectric interface **591**. Electrons in the channel **507** can be confined to the channel region by the heterojunction barrier, as noted above, and can also be confined by their electrostatic attraction to the ionized donor atoms (or donor sites in the case of defect doping). This confinement can be advantageously used to keep channel electrons separated from interface states at the dielectric/semiconductor interface **591**. This substantially reduces the degradation of FET performance due to surface states at the semiconductor/insulator interface **591**.

A high quality dielectric gate insulator layer **510**, must achieve a suitably low surface state density at interface **591**, low fixed charge density in layer **510**, and low mobile charge density in layer **510**, as is commonly necessary for all FET devices. It is advantageous for the dielectric-

semiconductor interface **591** to achieve a low surface state density to keep threshold voltage shifts low. In general, that density should be less than the sheet carrier concentration in the channel; such that the normal processing variation in surface state density does not cause an unacceptable threshold voltage shift. The gate insulator layer **510** must provide low leakage currents between the gate **521** and the channel **507** of the TFT. Low leakage current is generally achieved using an insulator with a relatively wide band gap, high resistivity, and high breakdown filed. The amorphous gate dielectric may be deposited using conventional CVD, PLD, jet vapor deposition (JVD), liquid phase deposition (LPD) or evaporation techniques, as well as anodic oxidation of a deposited layer, or any other suitable deposition or oxidation technique. High quality gate insulators also include crystalline layers, such as polycrystalline GaP or polycrystalline Al_2O_3, provided such layers achieve suitable insulating

The preferred embodiment combines heterojunction confinement to confine channel electrons away from the surface with a high quality dielectric insulator to allow effective modulation of the channel conductivity without being dominated by surface states at interface **591**. This combination can be produced in several ways, not necessarily distinct:

Physical separation of the channel charge from the interface **591** reduces interaction between channel electrons and the interface states at interface **591**. The heterojunction confinement between layer **507** and **509** allows the channel region **507** to be separated from the semiconductor-dielectric interface **591**, reducing the sensitivity of the channel electrons to surface states.

Modulation doping, commonly used for high electron mobility transistors, results in the incorporation of dopant atoms in the heterojunction confinement layer **509** or layer **505** while associated free electrons are captured by the channel region **507** of the device. This modulation doping can be used to further confine the channel electrons away from the interface **591**. Furthermore depletion mode, *n*-channel HFETs generally operate with negative bias voltages on gate **521** (with respect to the bias on the source **522** & the bias on the drain **523**), which will also act to push electrons away from the interface **591**. Enhancement mode, *n*-channel HFETs generally operate with similar electrical field profiles to depletion mode devices, using the built-in Schottky diode voltage of the gate diode to fully deplete the channel under zero bias, and therefore allow operation with positive gate biases. As long as the positive bias on gate **521** is kept

reasonably low, the internal electrical field in the device (resulting from the Schottky barrier voltage and the ionized donors) will act to keep channel electrons away from the semiconductor-dielectric interface. Operation of both enhancement mode and depletion mode devices at high positive biases is feasible, but should be avoided for TFTs since this would result in the possibility of channel electrons being attracted to the semiconductor-dielectric interface **591**, resulting in enhanced interaction with surface states at interface **591**.

The combination of a gate dielectric **510** with a heterostructure confinement layer **509** allows the relative contribution of the semiconductor-dielectric interface charge at interface **591** to be reduced. Due to the fact that the gate insulator includes both the dielectric layer **510** and the semiconductor heterostructure confinement layer **509** (which will be fully depleted), the semiconductor-dielectric charge at interface **591** is closer to the gate **521** than to the channel **507**. Therefore, the relative threshold voltage shift due to interface charge is lower (i.e. charge close to the gate results in a lower voltage shift than charge further from the gate because the capacitance is higher for charge closer to the gate).

We Claim:

1. A field-effect transistor including a channel region with a first semiconductor material made of a polycrystalline compound semiconductor, a second semiconductor region, a dielectric region, and a gate region, wherein said channel region further includes a confinement means located in or near said channel region to keep charge carriers predominantly within said channel region.

2. The transistor of claim 1, further including a source region and drain region.

3. The transistor of claim 1, wherein the average grain diameter of said first material is less than 100 nm, or amorphous.

4. The transistor of claim 1, wherein the average grain diameter of said first material is between 100 nm and 10 μm.

5. The transistor of claim 1, wherein at least 20% of the atoms in said first material are indium.

6. The transistor of claim 1, wherein said first material further includes at least 1% gallium or aluminum.

7. The transistor of claim 1, wherein said first material further includes at least 1% arsenic, antimony, nitrogen, or phosphorous.

8. The transistor of claim 1 wherein said confinement means employs a potential barrier formed by a heterostructure of said first material and said second semiconductor region.

9. The transistor of claim 1 wherein said confinement means employs a doping profile in or near said channel region which acts as a potential barrier.

10. The transistor of claim 9, further including a source of free charge carriers in or near said channel region, wherein said charge carriers are preferentially kept within said channel region by said confinement means.

11. The transistor of claim 1, wherein the maximum charge density of said

channel region is greater than 10^{11} cm^{-3}.

12. The transistor of claim 1, wherein the resistivity of said dielectric region is greater than 10^{12} ohm-cm.

13. The transistor of claim 1 further including a second surface on said channel region, a second gate suitable for modulating the conductivity of said channel region, a second confinement means located at or near said second surface of said channel region and suitable for keeping charge carriers predominately within said channel region, a third semiconductor material, and a second dielectric region located between said second gate and said third semiconductor material.

14. The transistor of claim 1, wherein said transistor is a thin-film transistor (TFT).

15. The transistor of claim 1, further including a substrate material with a lattice constant, wherein the lattice constants of said substrate and said channel region differ by more than 3%.

16. A thin-film transistor, including a first region, a second region located near said first region, a dielectric material located near said second region, a gate suitable for modulating the conductivity of said first region, and a source of free charge carriers located in or near said first region, wherein said first region includes a polycrystalline or amorphous compound semiconductor material and acts as the channel of a field-effect transistor, and said second region includes a semiconductor material.

17. A method for enhancing the confinement of charge carriers to the channel region of a thin-film transistor, said transistor including a channel region and a confinement region, constituting applying a voltage between the gate and said channel which is lower than the potential barrier of a confinement region.

18. A method for forming a field-effect transistor, said method including steps, not necessarily in sequence, of forming a channel region including a compound semiconductor and a surface, forming a confinement layer at or near said surface, forming a gate insulator, and forming a gate, wherein the potential barrier formed by said confinement layer makes it energetically

unfavorable for charge carriers to leave said channel region.

19. The method of claim 19 wherein said confinement layer instead, or additionally, makes it energetically unfavorable for charge carriers to enter said channel region.

20. A method of confining charge carriers to the channel region of a TFT comprising the act of using a potential barrier between said channel region and a gate insulator to make the loss of charge carriers from the channel region be energetically unfavorable.

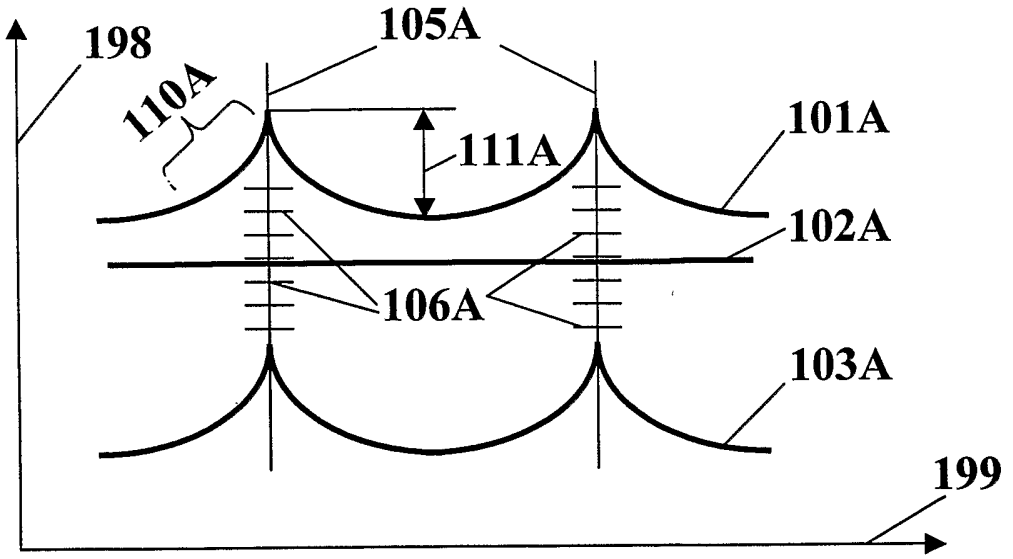


Figure 1A

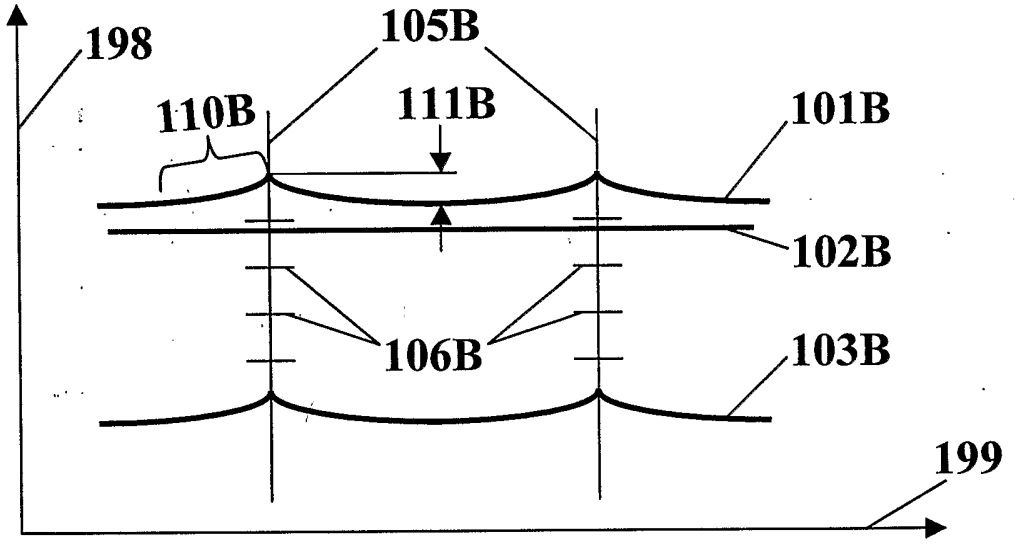


Figure 1B

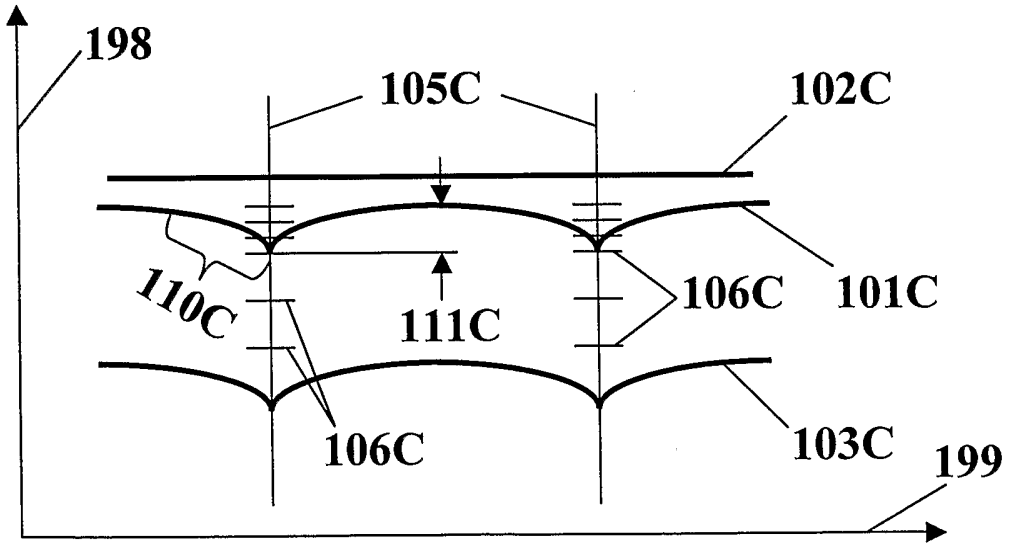


Figure 1C

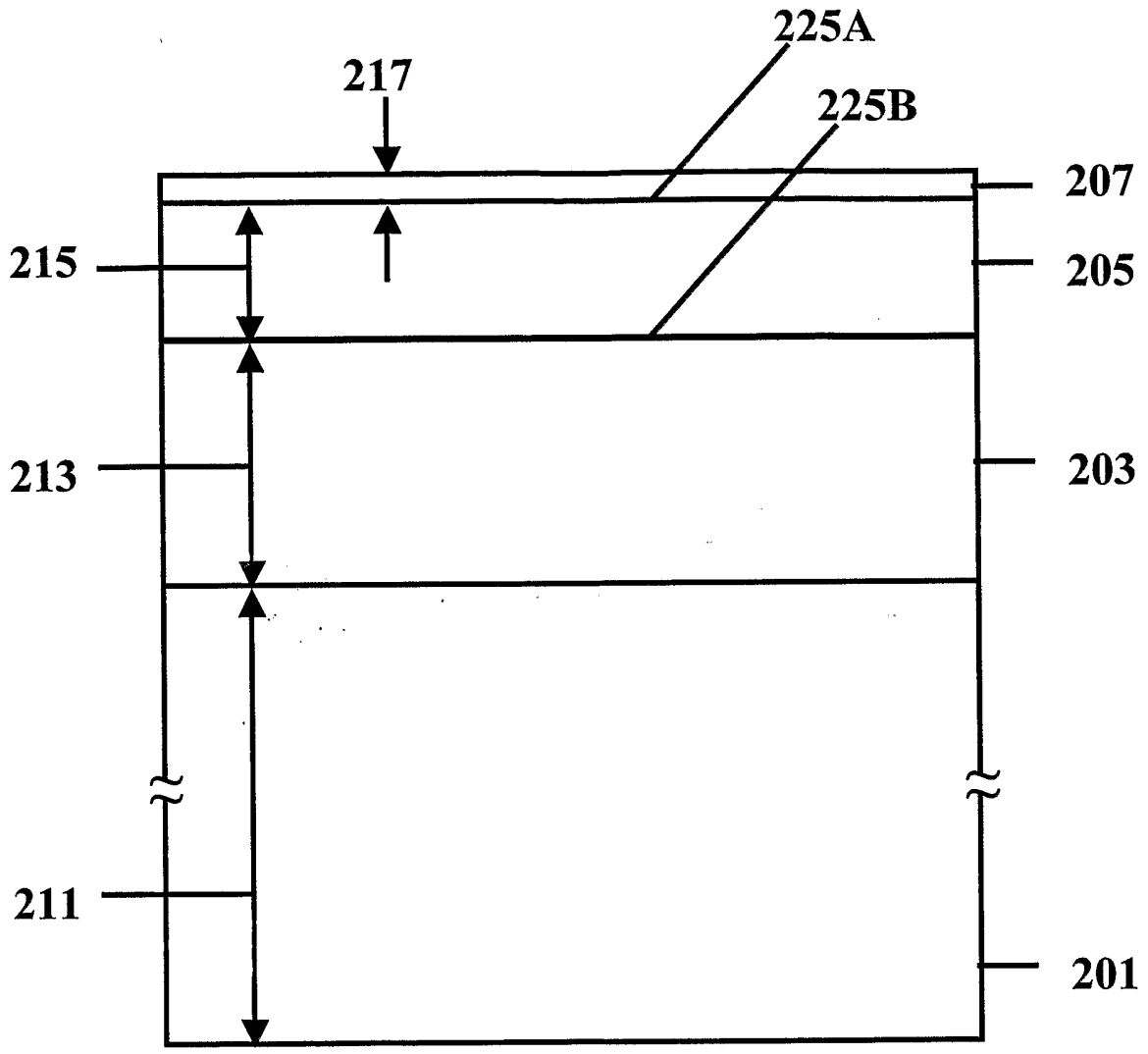


Figure 2

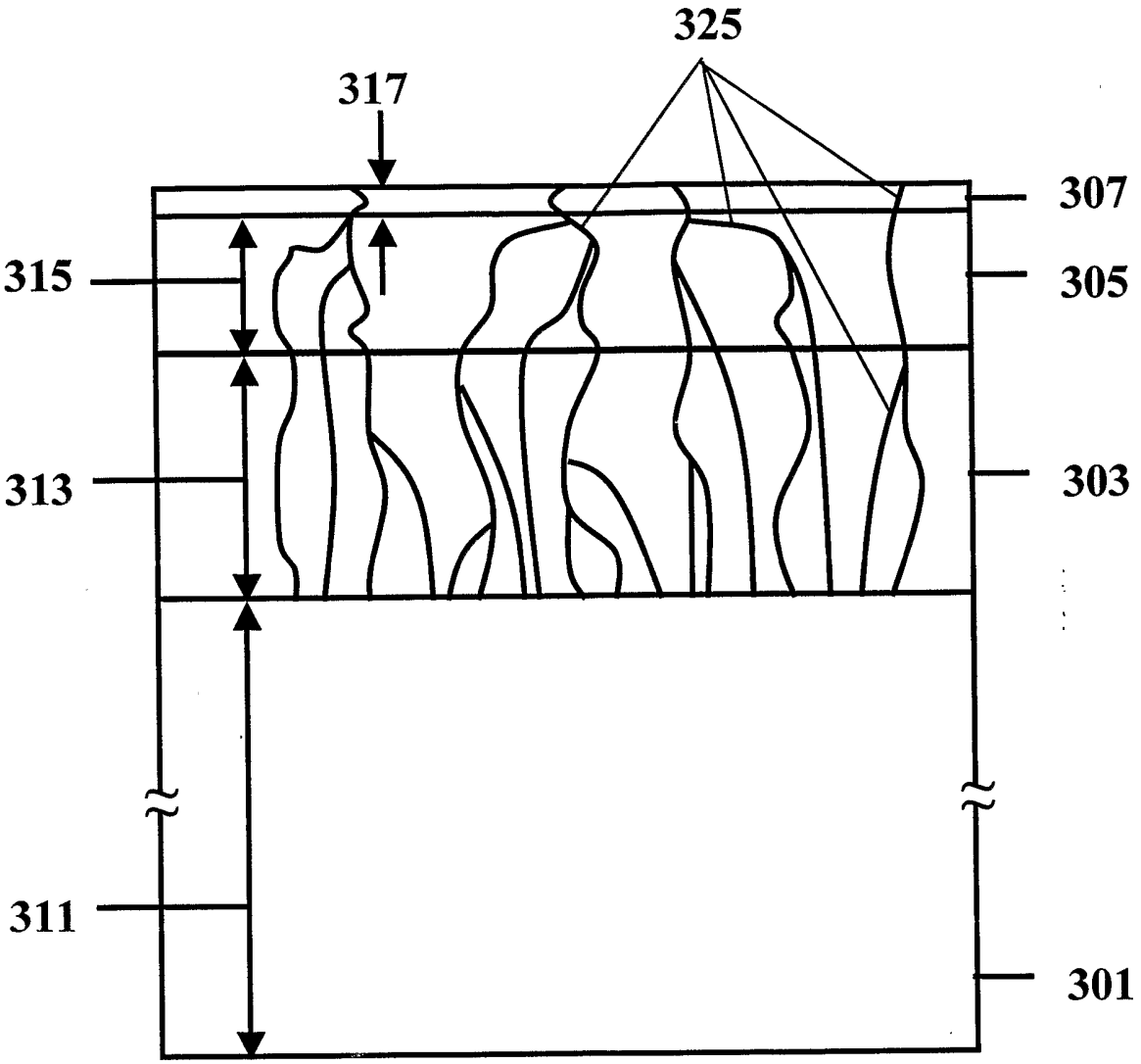


Figure 3A

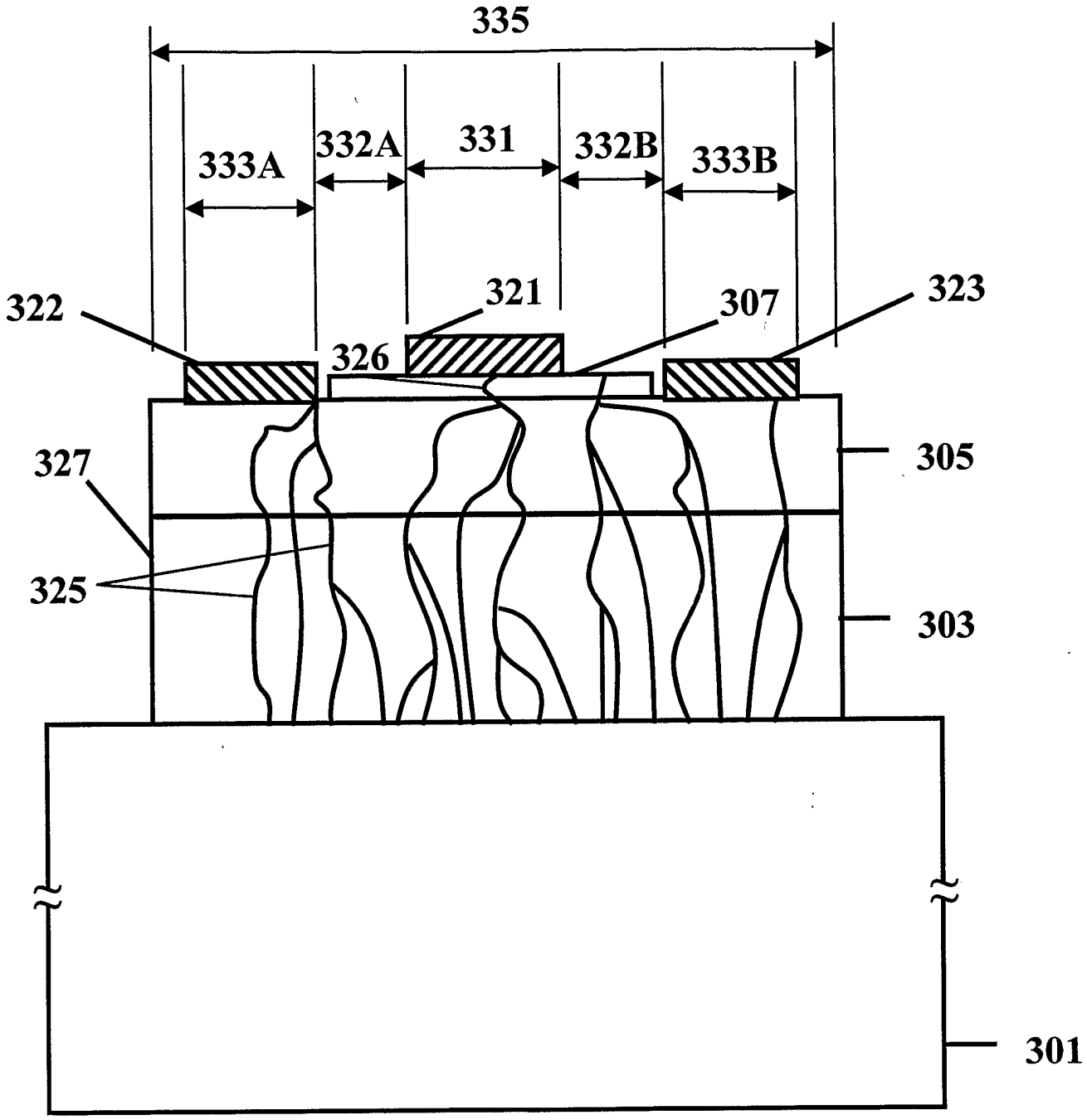

335
333A
332A
331
332B
333B
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325
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Figure 3B

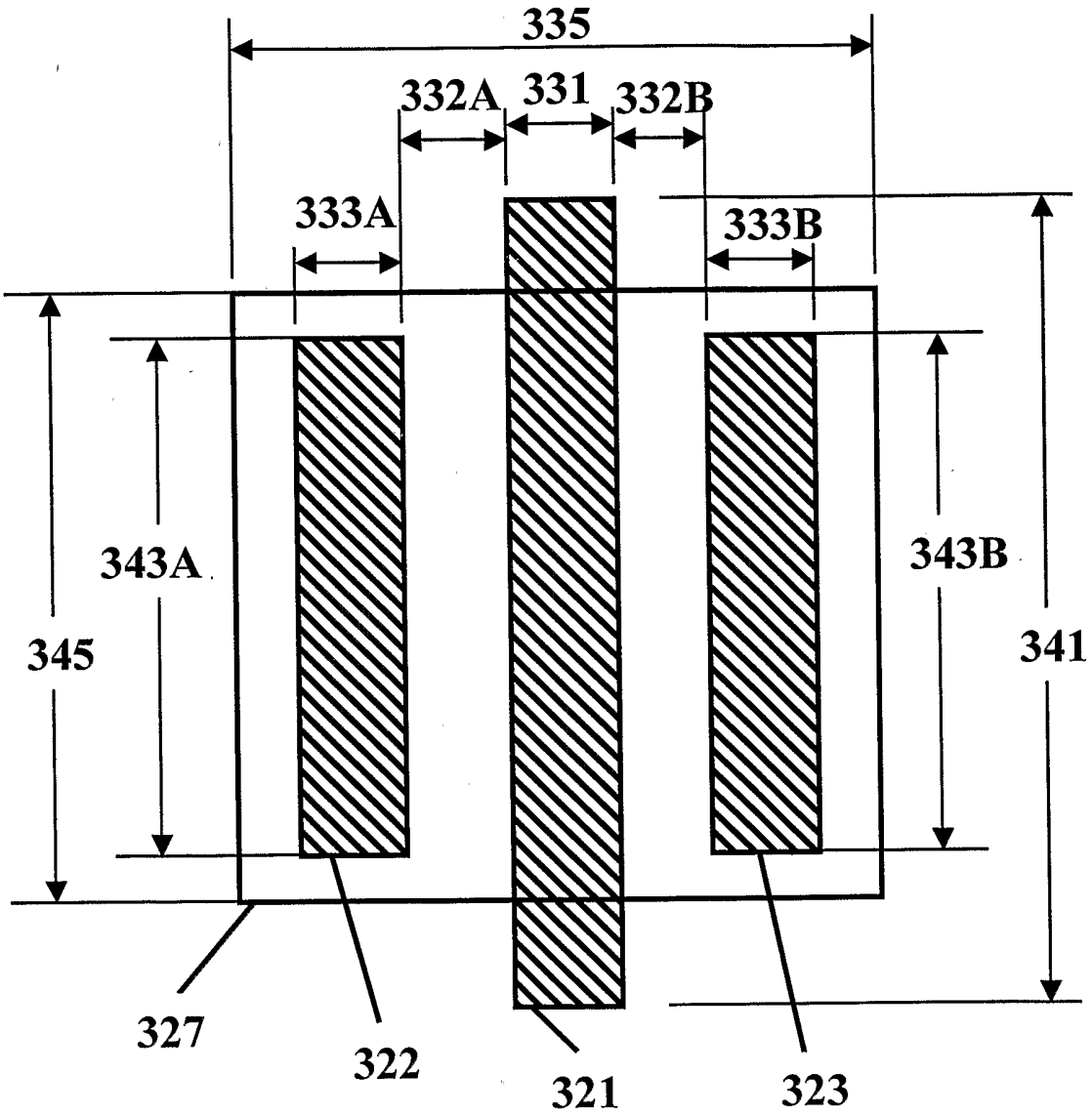


Figure 3C

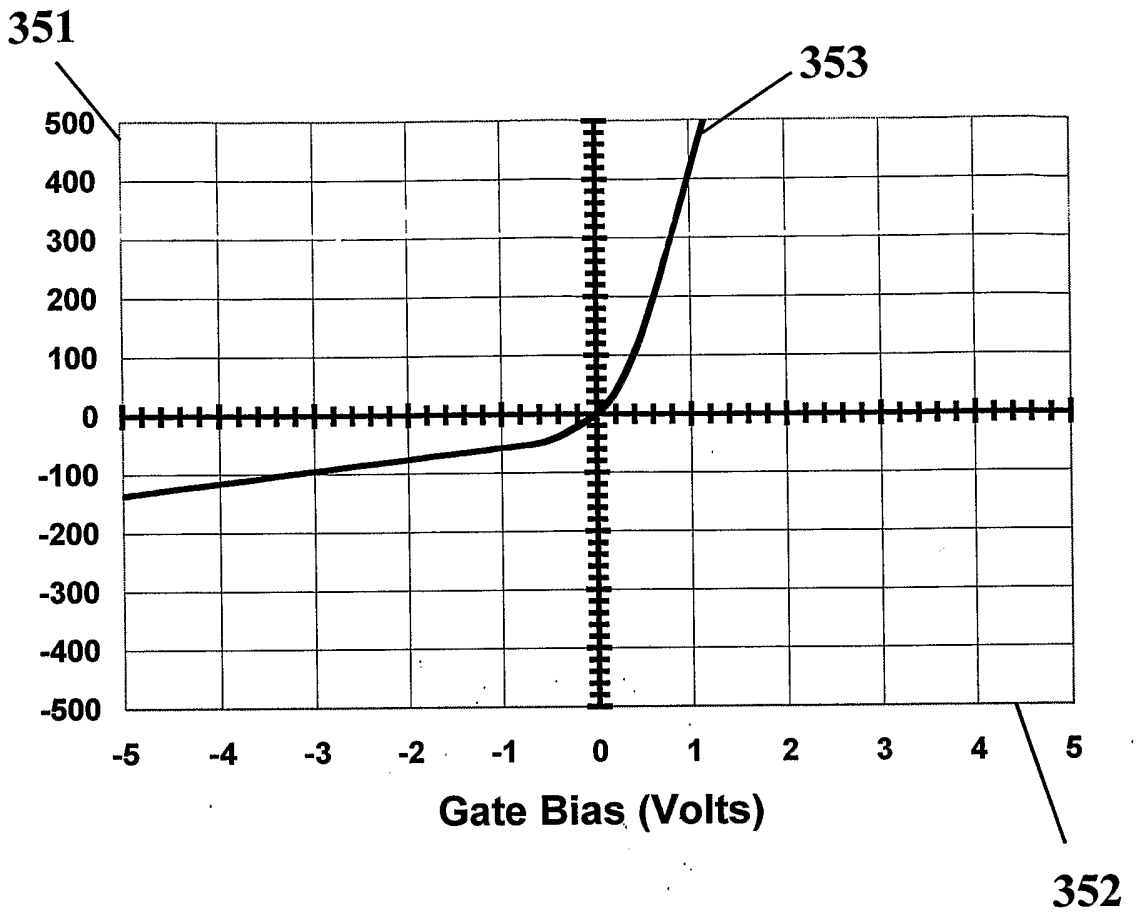

351
353
500
400
300
200
100
0
-100
-200
-300
-400
-500
-5
-4
-3
-2
-1
0
1
2
3
4
5
Gate Bias (Volts)
352

Figure 3D

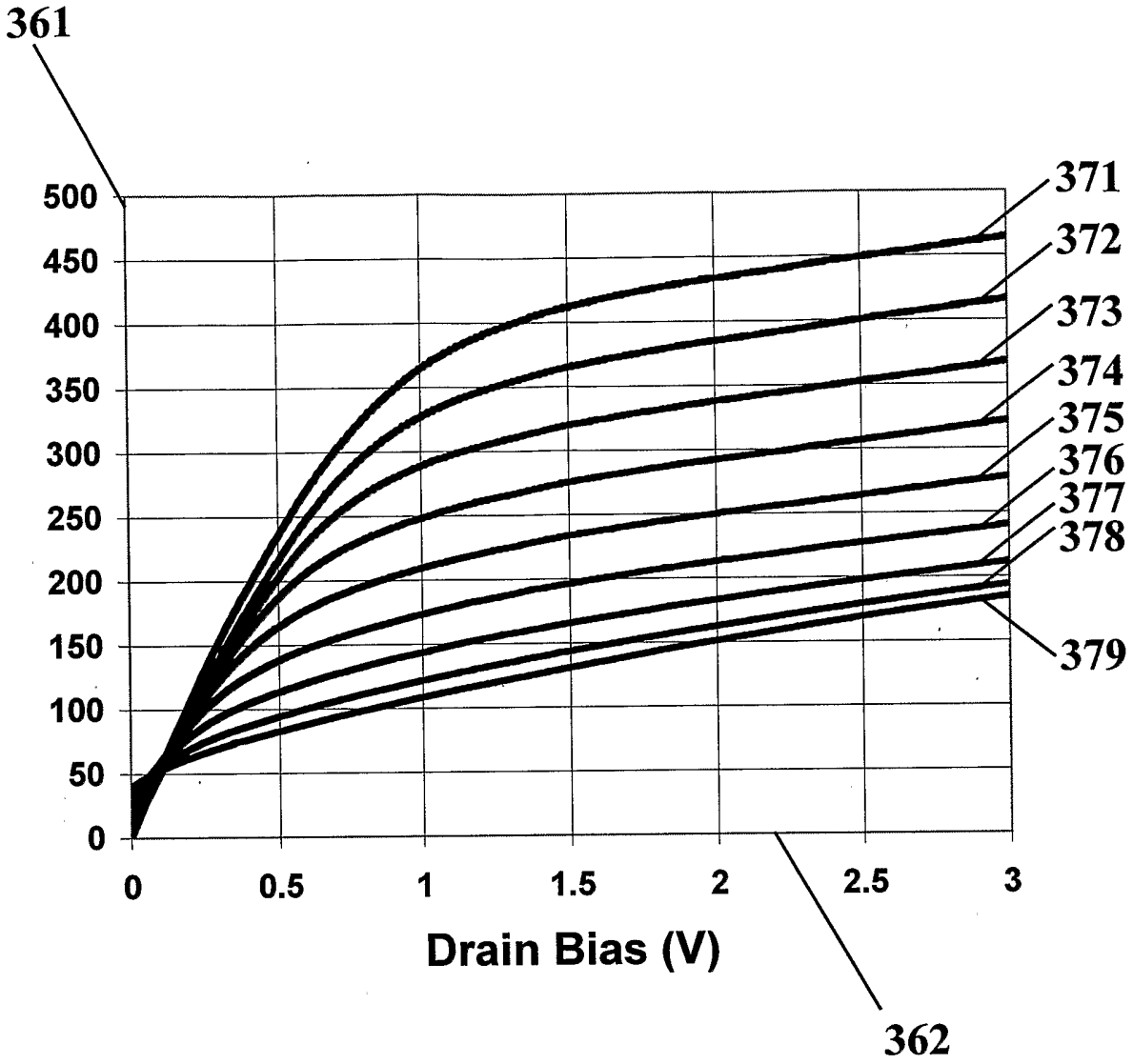

361
500
450
400
350
300
250
200
150
100
50
0
0
0.5
1
1.5
2
2.5
3
Drain Bias (V)
371
372
373
374
375
376
377
378
379
362

Figure 3E

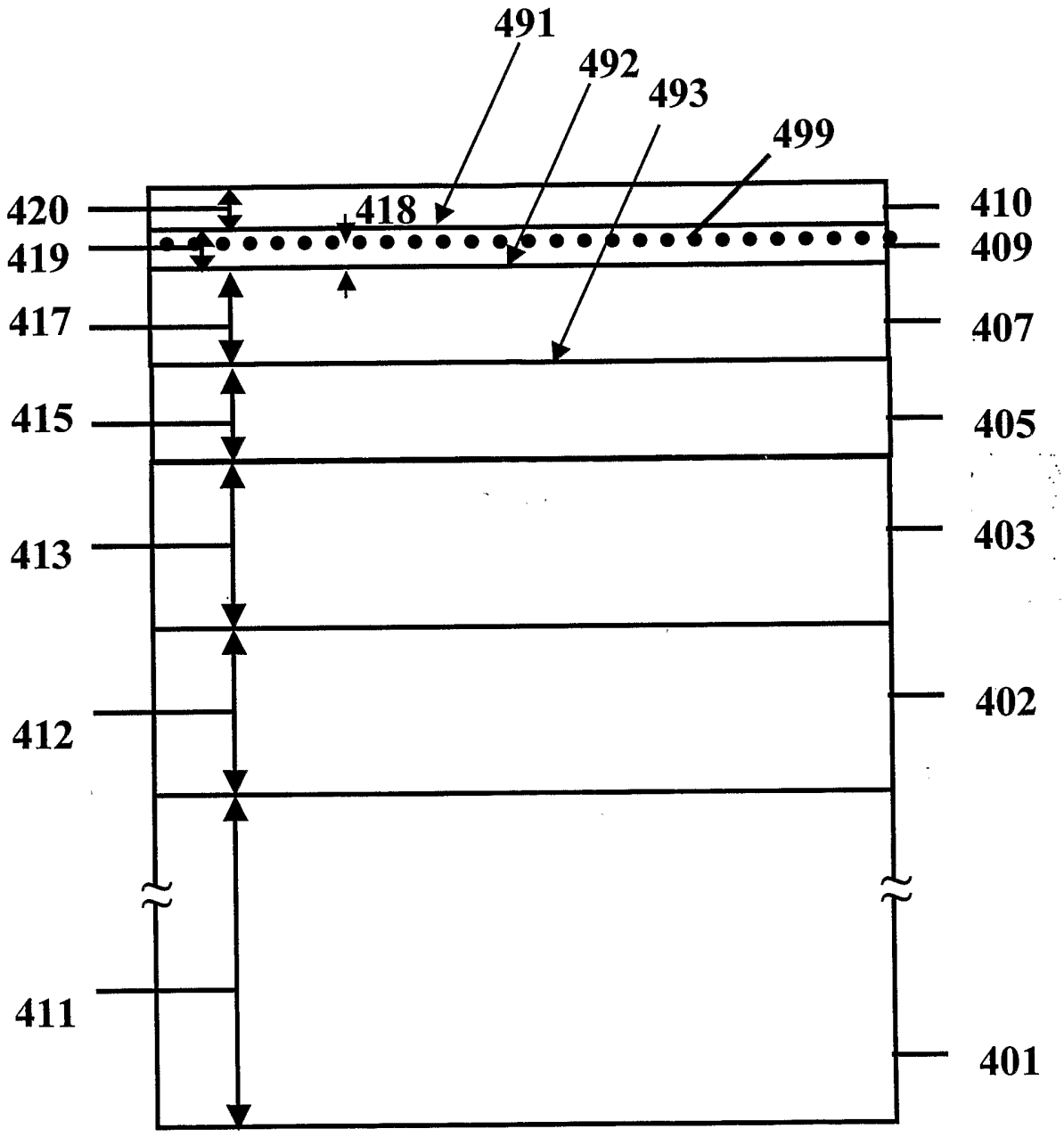

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Figure 4A

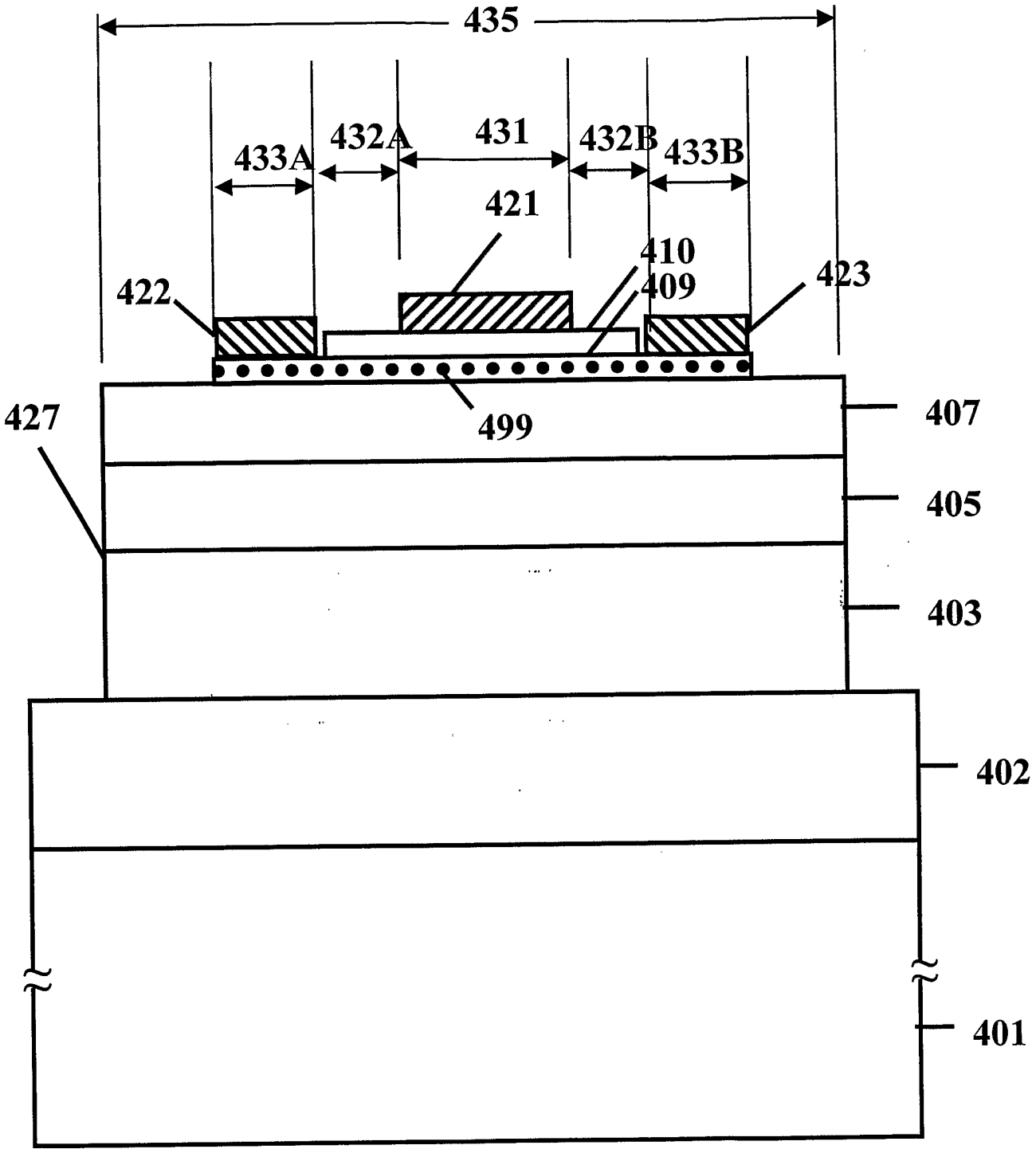

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433A
432A
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432B
433B
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Figure 4B

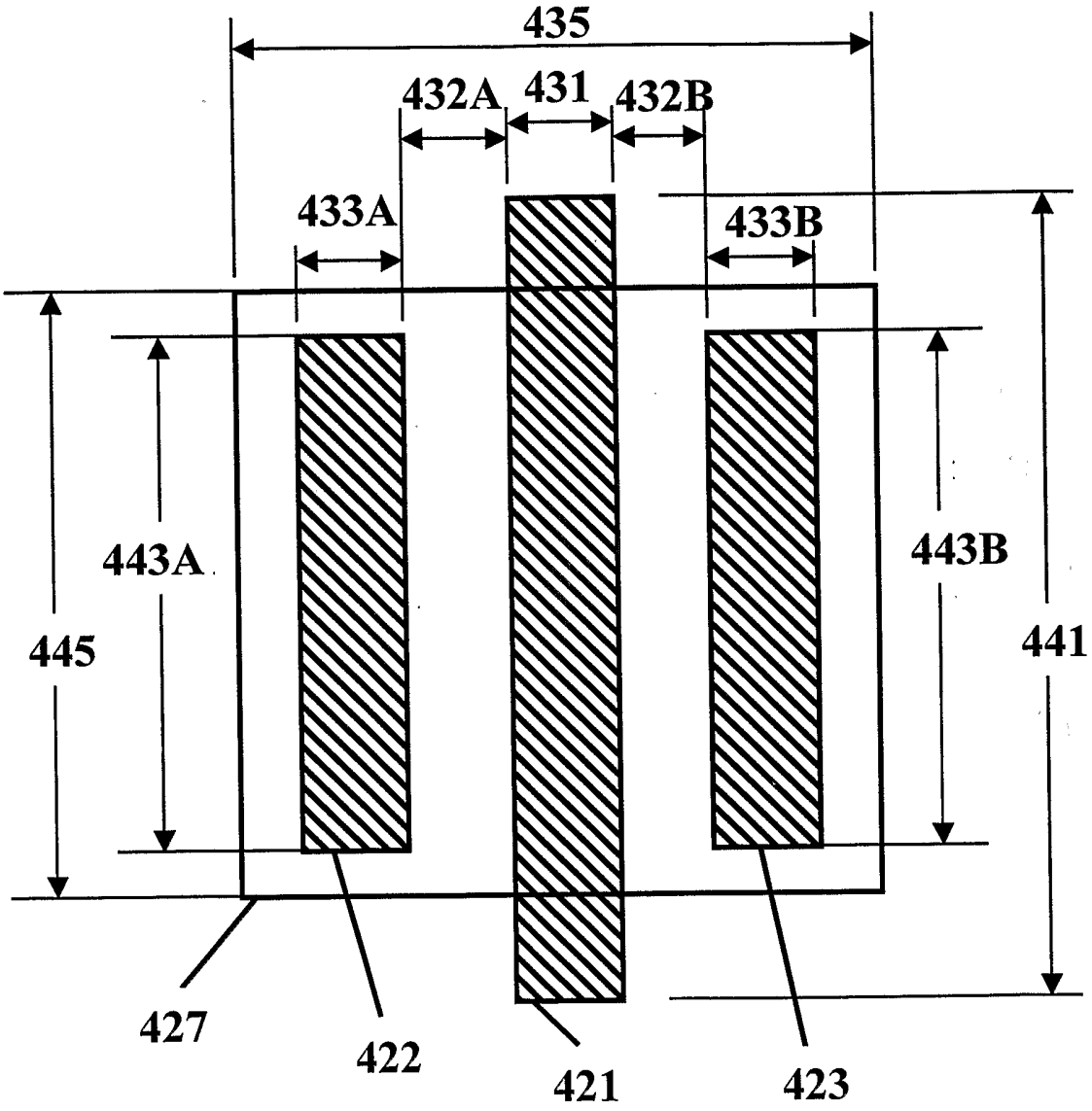


Figure 4C

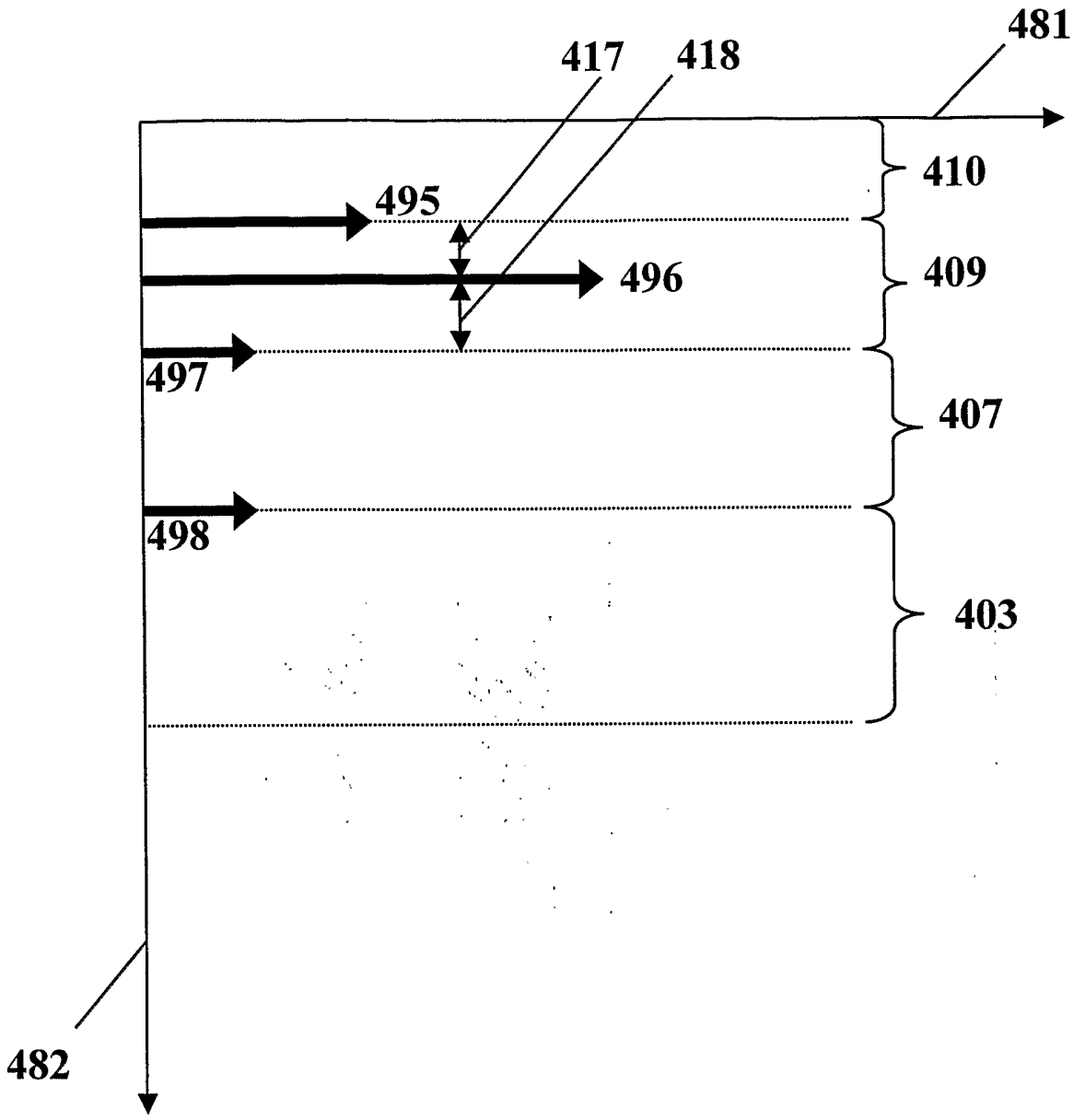


Figure 4D

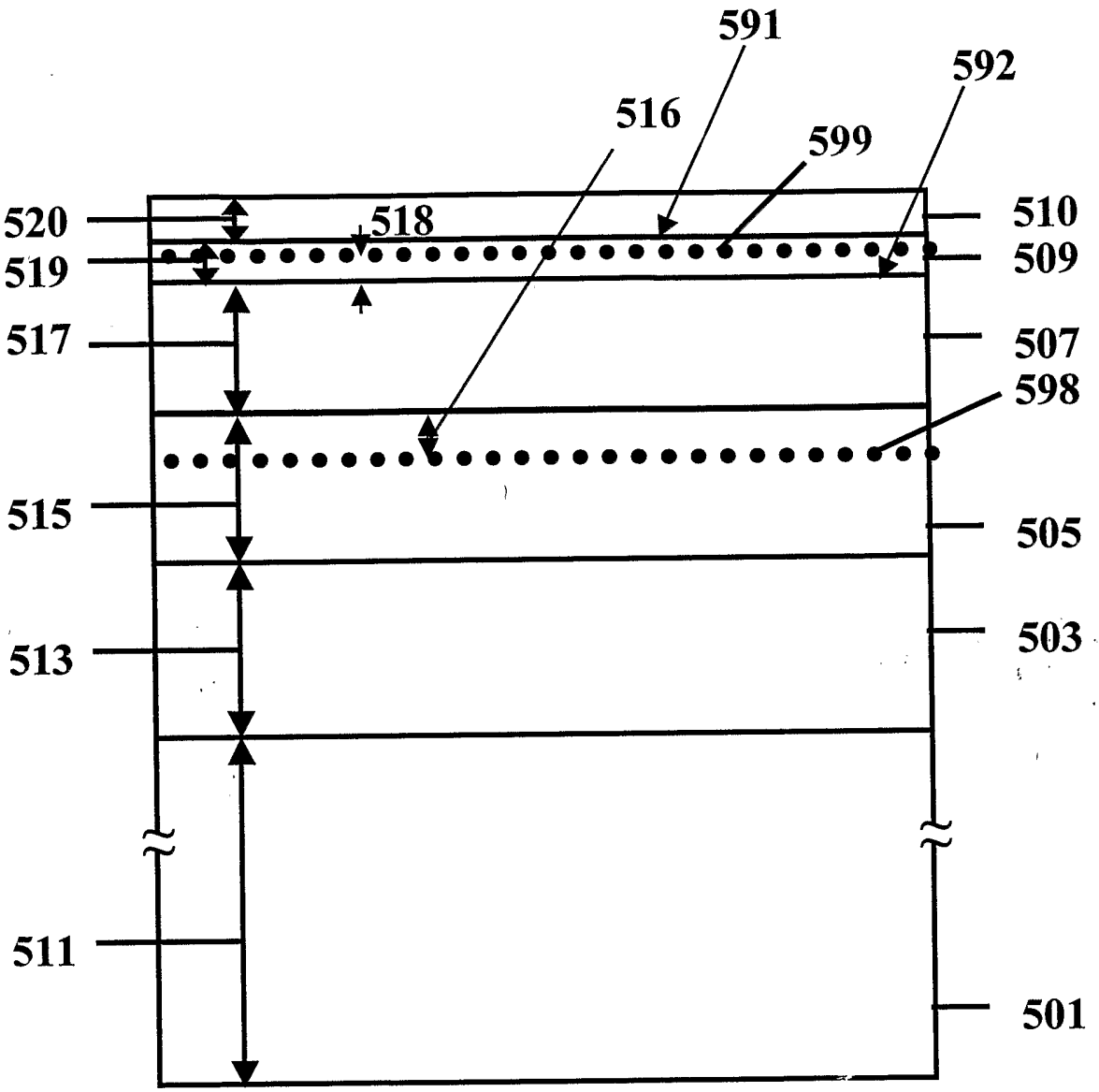

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501

Figure 5A

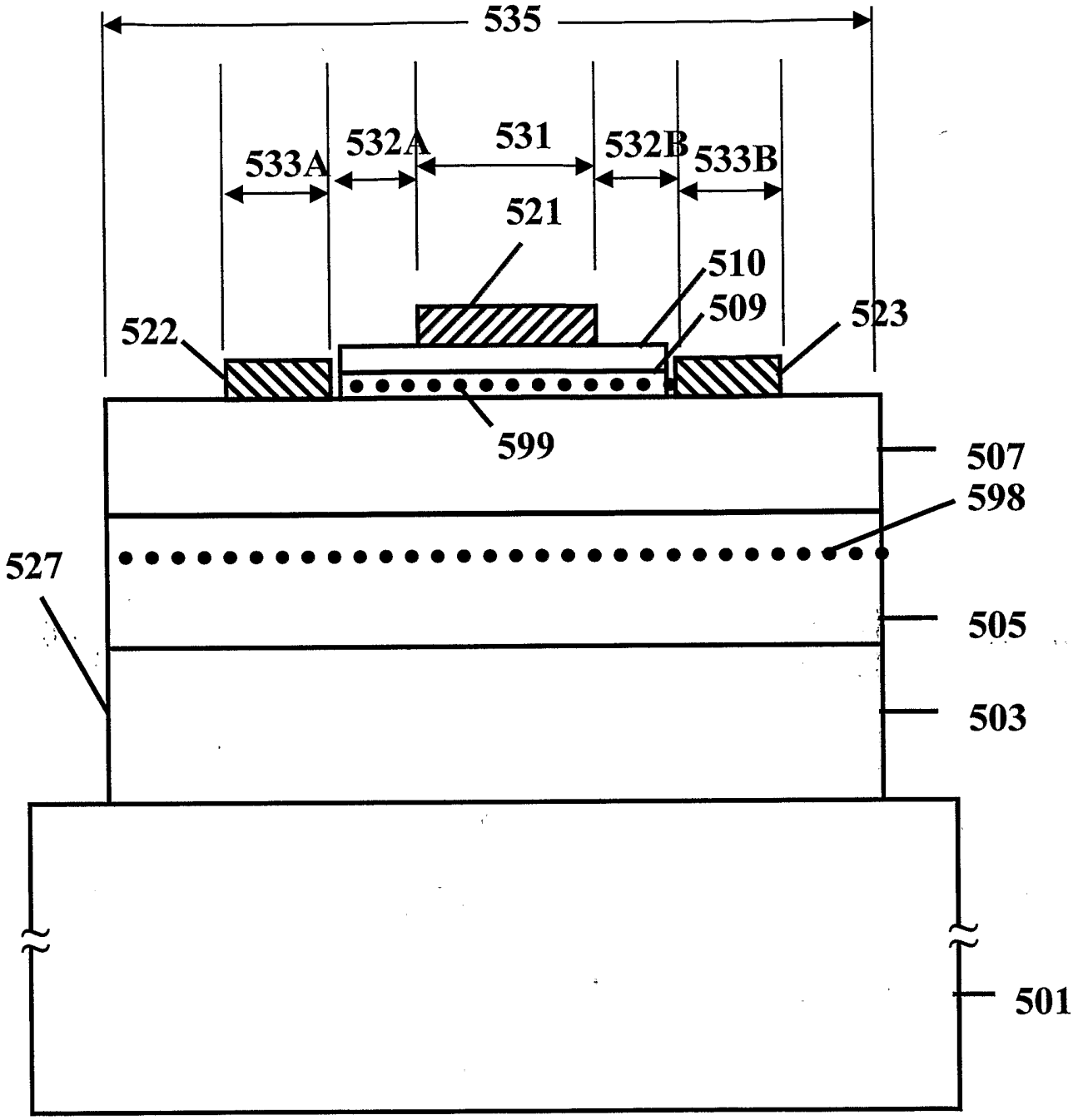

535
533A
532A
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532B
533B
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523
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Figure 5B

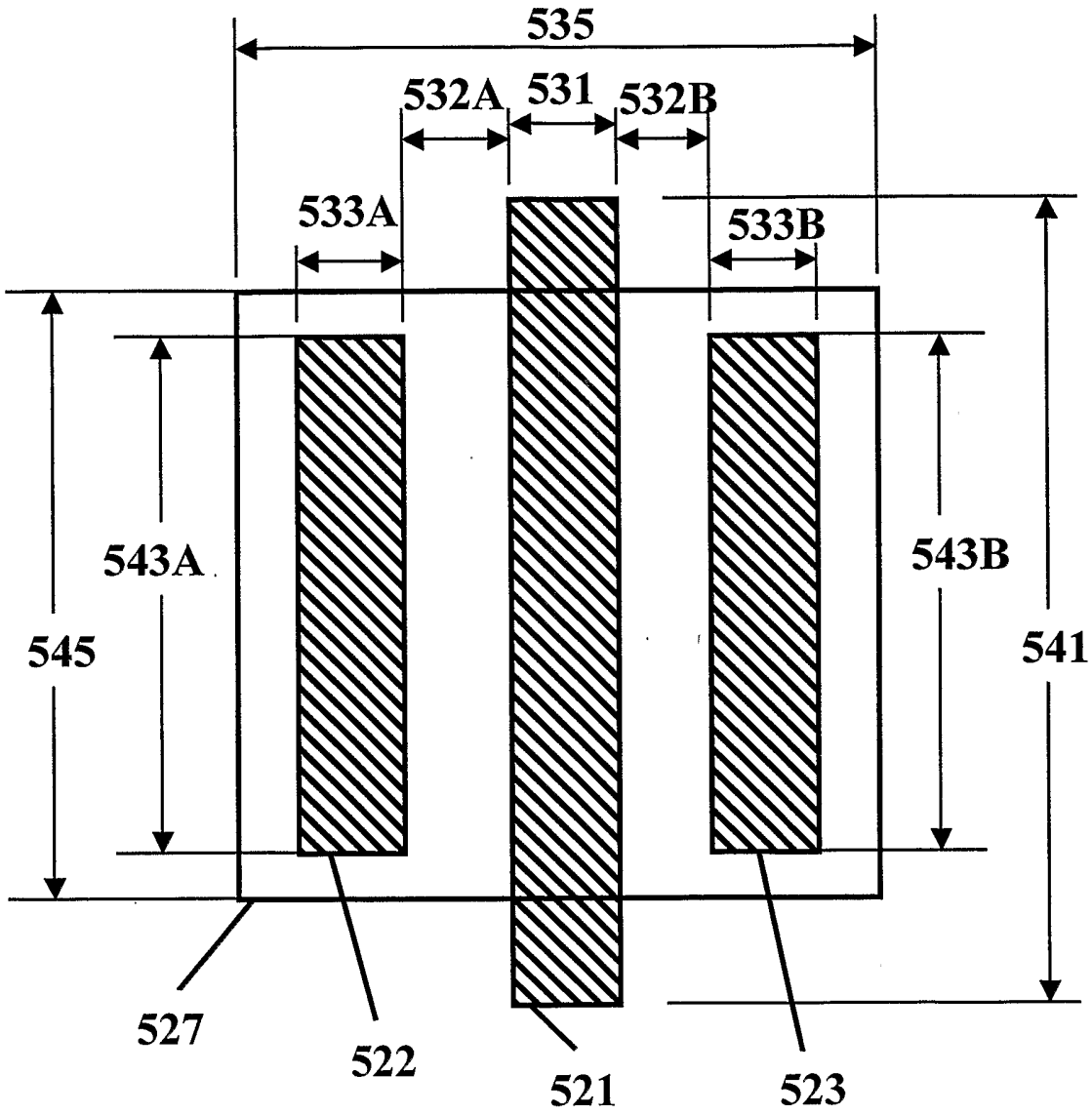


Figure 5C