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CONSTANT CURRENT CONSTANT VOLTAGE REGULATOR

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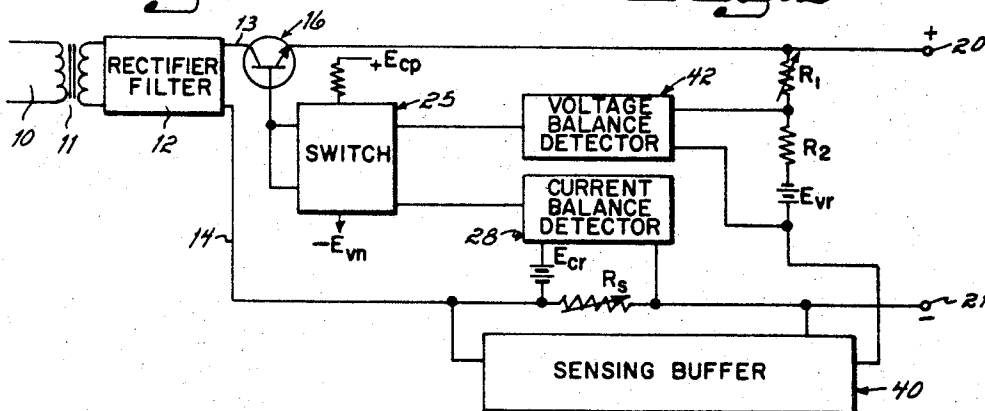
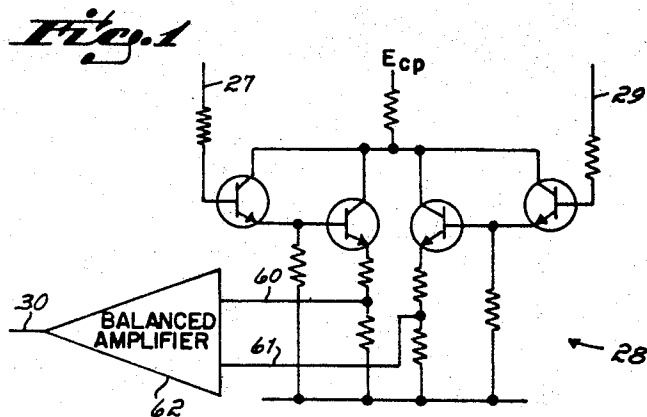
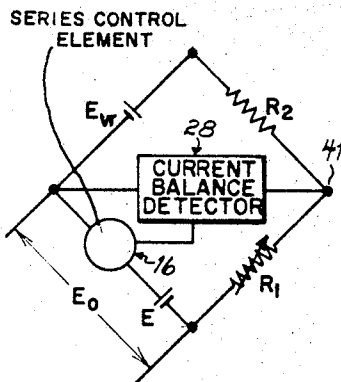
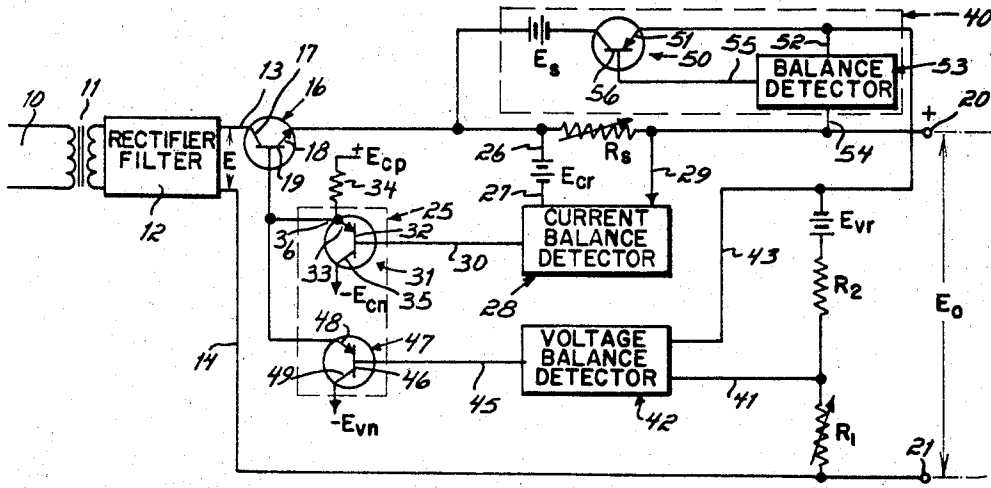


Fig. 4

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CONSTANT CURRENT CONSTANT VOLTAGE REGULATOR

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ABSTRACT OF THE DISCLOSURE

A regulator having a series control transistor and a current sensing resistor to provide constant voltage or current. A constant current mode of operation is provided utilizing the current sensing resistor when the output voltage is below a preselected value. A bridge circuit provides a constant voltage mode of operation when the output voltage attains the preselected value. A pair of transistors switch the regulator from one mode to the other. A buffer circuit, connected across the sensing resistor, eliminates the error produced by current required for constant voltage regulation while operating in the constant current mode.

This invention relates to a power supply and more particularly the invention relates to a power supply which is capable of delivering to output terminals a constant current of selected magnitude or alternatively a constant voltage of selected magnitude, the regulator including means for automatically switching from one operating mode to the other.

In constant current regulators, it is common to use a sensing resistor which is variable to select the current to be delivered to the load. The voltage drop across the sensing resistor is detected and utilized to control or hold the current in the load constant. In a constant voltage regulator, the voltage at the output terminals is detected and is utilized to hold the voltage at the output terminals constant. An objective of the present invention has been to provide a power supply having an unregulated voltage source, control means and distinct current and voltage regulating systems for actuating the control means so as to deliver to a single output constant current or constant voltage depending on the mode of operation.

When operating in the constant current mode, the voltage regulator is held inoperative by the switching means referred to above but nevertheless there is a finite current which flows into its sensing point. If its sensing point is between sensing resistor and the output terminals, then the regulator, in the constant current mode, would be inaccurate by the amount of current which does not flow to the output terminals, but rather circulates into the voltage regulator. Where the constant current supplied to the output terminals is large, that is, several amperes, the error produced by the circulating current is insignificant, for the operation of the voltage regulator requires but a few milliamps. However, where the power supply is required to supply currents of the order of a few microamps, then a circulating current in the voltage regulator of several microamps would produce an intolerable error.

If the sensing point for the voltage regulator is between the unregulated power supply and the current sensing resistor, no error would be introduced in the current regulator, but the voltage regulator would be inaccurate by the amount of the voltage drop across the sensing resistor.

In accordance with the present invention, the voltage regulator is connected to the circuit at a point between the unregulated power supply and the sensing resistor

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and a buffer circuit is connected between the sensing point and the input to the voltage regulator, the buffer circuit simulating the voltage drop across the sensing resistor. Thus, while the point of connection is on the power supply side of the sensing resistor, the effective potential applied to the voltage regulator is at the potential of the output terminal.

It has been another objective of the invention to provide a current regulator for supplying current of the order of microamps to the output terminals. Such a lower order constant current regulator of itself presents problems for some current must flow in the current regulating network across the sensing resistor. In order to keep this as low as possible, the invention provides a balanced detector having a high enough input impedance that the current input to it is in the low nano amp (10^{-9}) range, the detector provides a current gain sufficient to drive the amplifiers necessary to operate the system.

It has been another objective of the invention to provide a special switching network at the output of the current regulator network and voltage regulator network for selectively determining the mode of operation of the power supply. Through the use of the switch of the present invention and associated power supply circuitry, it is possible to set the power supply for a specific current and a specific voltage and operate the first on the constant current mode until the load resistance is increased to the extent that the preselected voltage at the output terminals is attained whereupon the operation automatically and instantaneously shifts to a constant voltage mode.

These and other objectives of the invention will become more readily apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. 1 is a circuit diagram of a power supply in accordance with the present invention,

FIG. 2 is a bridge circuit illustrating the operation of the DeBlasio voltage regulator utilized in the power supply,

FIG. 3 is a circuit diagram of the balanced current detector utilized in the power supply, and

FIG. 4 is a circuit diagram of an alternative manner of connecting the voltage regulator.

Referring to FIG. 1, the voltage regulator includes an alternating current source 10 coupled through a transformer 11 to a rectifier and filter system 12 to provide an unregulated direct current voltage E across a positive line 13 and a negative line 14.

The positive line includes, in series, a series control element 16 which is an NPN transistor having a collector 17 connected to the unregulated output E and emitter 18 connected to the output side of the regulator and a base 19 to which control signals are applied. It should be understood that the control element 16 could be a PNP transistor inserted in the negative line 14 and the additional circuit elements would be in a mirror image relation to the circuit, as described below.

The regulator has a positive output terminal 20 and a negative output terminal 21 across which an output voltage E_o is produced. The regulator may be provided with voltage sensing terminals as is common in this art.

The series control element 16 regulates the output voltage or current through the load attached to the output terminals by varying the conductance or inversely the resistive effect of the series control element. When the positive voltage on the base 19 is high, the resistive effect is low and, conversely, when the voltage on the base is low, the resistive effect is high.

The signal applied to the base 19 is derived either from a current regulator system or from a voltage regulator system, the system in control being determined by a switch 25.

The current regulator includes a sensing resistor R_s which is connected in series with the positive line 13. The sensing resistor is variable and preferably is constituted by decade resistors having suitable switches to control the net resistance of the sensing resistor and may be of the type described in copending application Ser. No. 532,633, filed Mar. 8, 1966.

A current reference voltage E_{cr} is connected at its positive terminal 26 to the high side of sensing resistor R_s and at its negative terminal 27 to one side of a current balanced detector 28. The low side of the sensing resistor R_s is connected through line 29 to the other side of the current balanced detector 28. The terms "high" and "low" refer to the high potential and low potential sides of the sensing resistor, assuming the conventional flow of current from plus to minus.

The current balanced detector which detects a difference in potential between lines 27 and 29, amplifies it, and feeds an output signal to the output 30 of the detector. The preferred circuit for the detector will be described below and is shown in FIG. 3.

The output 30 is amplified by an amplifier and is connected to a PNP transistor 31 at its base 32. The transistor 31 has an emitter 33 connected in series with a resistor 34 which is connected to the positive side E_{cp} of a power supply. The transistor 31 has a collector 35 connected to the negative side E_{cn} of the power supply. The power supply E_{cp} - E_{cn} supplies both a positive and negative potential with return to the positive line 13 at the low side of the series control element 16 so that the power supply "floats" with variations in potential of the positive line 13.

Current regulator operation

When the regulator is in the current regulator mode of operation, the balanced detector 28 compares the voltage drop across the sensing resistor R_s to the reference voltage E_{cr} . While a current change might be due to any of a number of causes, let it be assumed that the current has dropped by adding resistance across the output E_0 . The potential difference across sensing resistor R_s is reduced and the line 29 becomes positive with respect to the line 27. This potential difference is detected by the current balanced detector 28 and the output of the balanced detector is such as to raise the potential on the base 32 of transistor 31, thereby permitting less current to flow through the transistor 31. The reduction of current through the transistor 32 raises the potential of the junction point 36 and hence raises the potential on the base 19 of the control element to permit greater current to flow through the control element. This condition continues until a balance is achieved between the potentials across lines 27 and 29.

Voltage regulator system

The voltage regulator employs the basic circuitry described in DeBlasio Patents Nos. Re. 24,800 and 3,138,752. The circuit includes a decade variable resistance R_1 in series with a resistance R_2 and forming a voltage divider therewith and a reference voltage E_{vr} having its negative terminal connected to the positive line 13 through a positive sensing buffer 40. The junction between R_1 and R_2 is connected by line 41 to one input side of a voltage balanced detector 42, the other side being connected to a sensing point 43 which is common to the negative side of the reference voltage E_{vr} and the positive side of the output terminal. As will be explained below, the sensing buffer 40 holds the point 43 at the output potential of positive terminal 20.

The voltage balanced detector 42 has an output line 45 connected to a base 46 of a PNP transistor 47. The transistor 47 has its emitter 48 tied to the emitter 33 of transistor 31. The transistor 47 has a collector 49 connected to the negative side E_{vn} of a power supply.

The voltage regulator of the invention uses the DeBlasio bridge circuit configuration. As more clearly illustrated in FIG. 2, one side of the bridge is constituted by the voltage

divider R_2R_1 with the junction point 41 of the voltage divider being connected to the balanced detector. The other side of the bridge is formed by the reference voltage E_{vr} in one leg and in the other leg, the unregulated source E and the series control element 16.

In accordance with this DeBlasio regulator circuit of FIG. 2, the output voltage E_0 is equal to the drop across variable resistor R_1 and, as a consequence, the output voltage can be determined by the selection of the value of the resistance R_1 . While the DeBlasio bridge is preferred, the present invention is not restricted to its use.

Positive sensing buffer

As has been indicated above, the connection of the voltage sensing point 43 to the line of the regulator is of critical importance. If the connection is made at the output terminal, then, during operation of the invention on the current mode, current flows into the voltage balanced detector through the sensing point 43 as well as into the load across the output terminal E_0 . Since the sensing resistor R_s is detecting the total current flowing to the output terminals, the balance attained by the balanced detector is in error by the amount of current flowing into the voltage balanced detector 42. Where the desired output current is small, that is, of the order of microamps, the percentage of error introduced by current circulating into the voltage balanced detector is large.

On the other hand, if the sensing point 43 is connected to the high side of the sensing resistor R_s in order to avoid error in the current regulator, a similar error is introduced in the voltage regulator system. The sensing point 43 detects not the output voltage but rather the output voltage minus the drop across the resistor R_s .

These errors are substantially eliminated through the use of the buffer 40 which connects the sensing point 43 to the high side of the sensing resistor R_s while maintaining its level of potential the same as that of output terminals 20. Thus, by connecting the point to the high side of the sensing resistor, the accuracy of the current regulator is not impaired and by using the buffer to maintain the potential of the sensing point 43 at the level of the output terminal 20, the accuracy of the voltage regulator network is not impaired.

The buffer network includes a source voltage E_s and a transistor control element 50 connected in series with the input to detector 42. These elements are to produce a voltage drop equal to the drop across resistor R_s . The control element 50 has an emitter 51 connected to one input 52 of a balanced detector 53. The other input 54 to the balanced detector is connected to the output terminal 20. The output 55 of the balanced detector is connected to the base 56 of the transistor 50. The balanced detector regulates the voltage on the base 56 so that the potential at the point 52 which is common to the sensing point 43 is the same as the potential of the output terminal 20. Thus, the buffer system 40 causes the sensing point 43 to reproduce the potential at the output terminal 20 without being connected directly to it.

Operation of the regulator

In describing the operation of the regulator, it will be assumed that the regulating variables, principally R_s and R_1 , are preset to provide a current regulating function while the output voltage remains below 100 volts. However, R_1 is set to provide constant voltage regulation at 100 volts. Thus, when the resistance of the load connected across the output terminals 20 and 21 becomes so great that the output voltage rises to the level of 100 volts, the regulator will change from a current regulating mode to a voltage regulating mode. It will be understood that voltage regulation can be achieved at lower voltages simply by proper selection of the value of the R_1 .

In the steady state condition, the switching transistor 31 in the current regulator circuit is functioning and the switching transistor 47 in the voltage regulator is biased

to cut off, that is, its base is at such a high voltage level that its emitter-base junction is reverse biased.

As resistance is inserted in the output, the current tends to drop and the current regulator calls for a correction, that is, to raise the current to the original level. It does so by increasing the potential on the base 32 of transistor 31. This causes less current to flow to the emitter 33 and raises the potential of the junction point 36. This raises the potential on the base 19 of the control element 16, driving it into further conduction so that increased current flows to the load, thereby maintaining the current constant.

As the resistance increases with a constant current through the load, the voltage across the load must necessarily increase. When it reaches the 100 volts, the system is providing the current for which the regulator is programmed and the voltage for which the regulator is programmed.

As additional resistance is placed in the circuit, the current again tends to decrease at the crossover point. The current regulator calls for more current and the voltage balanced detector comes into equilibrium and starts to maintain constant voltage. In the current regulator, the bias potential on base 32 of transistor 31 becomes more positive, moving toward cutoff. In the voltage regulator, the base 46 of transistor 47 becomes more negative, moving toward saturation. Effectively, the resistance of transistor 31 is increasing and the resistance of transistor 47 is decreasing.

Consequently, more current is drawn through resistor 34, dropping the potential at point 36. As the potential of point 36 drops, the potential on the base 19 of transistor 16 drops, thereby permitting less current to flow to the output and hence the output voltage remains constant at 100 volts.

Current balanced detector

The current balanced detector 28 is diagrammatically illustrated in greater detail in FIG. 3. The input connections 27 and 29 are applied to the bases of transistors having very high input impedance. The transistor must also have a very low ICBO characteristic, that is, the collector to base current (leakage current) must be very low. The specific transistors employed are 2N930A transistors although any transistors having comparable or even superior characteristics may be employed. The transistors are connected as a balanced Darlington amplifier, the input stage drawing at its base about 4 nano amps.

The balanced detector is preferably connected to provide two output stages at 60 and 61 and the output from each of these stages is fed into two inputs of a balanced amplifier 62. Through the use of this system, it is possible to double the voltage gain in the whole system.

Alternative forms of the invention

While the sensing buffer of the present invention has been shown and described in the specific circuit of FIG. 1, it should be understood that modifications can be made to provide circuits which utilize the sensing buffer concept but which do not depart from the scope of the present invention. For example, the control of both the current and voltage is effected by a transistor control element 16 connected in series with one of the output lines of the power supply. In practice, more than one such transistor are utilized and connected in parallel in order to handle the power requirements of the system. Further, the regulator system, particularly including the sensing buffer, can be used with control means other than a series connected transistor. For example, the control means employed can be an SCR circuit as is known in the regulator art.

The preferred circuit does not necessarily require the control element and sensing buffer to be in the positive line of the power supply. A mirror image of the illustrated circuit will work equally as well with the principal elements being in the negative line of the power supply

and with corresponding changes made in the polarity and orientation of the reference voltage, the transistors, and the like.

The circuit will work equally as well when the series control element 16 and the sensing resistor R_s are in opposite output lines as shown, for example, in FIG. 4.

The circuit of FIG. 4 is substantially identical to the circuit of FIG. 1 except that the sensing resistor R_s has been placed in series with the negative line and the sensing buffer for the voltage regulator has been connected to the negative side of the power supply. The functioning of the circuit is otherwise identical to that described in connection with the circuit of FIG. 1.

We claim:

1. A combined current and voltage regulator comprising,
 - an unregulated power supply having positive and negative output lines terminating in output terminals,
 - output control means associated with said power supply for varying the current and voltage at said output terminals,
 - a resistance in one of said lines,
 - current regulating means connected across said resistance and including a reference voltage, said current regulating means comparing the voltage drop across said resistance to said reference voltage, said current regulating means having an output connected to said output control means for varying the current to bring the reference voltage and voltage drop into balance,
 - voltage regulating means having input leads connected across said output lines and including a reference voltage source, said voltage regulating means comparing the output voltage to said reference voltage and having an output connected to said output control means for varying its resistance to bring the output voltage and reference voltage into balance,
 - one input lead to said voltage regulating means including a buffer circuit, said buffer circuit being connected to a detecting point between said resistance and output control means,
 - said buffer circuit including means for detecting the voltage drop across said resistance and applying an equivalent voltage drop in said input lead.
2. A regulator according to claim 1 in which said buffer circuit comprises a sensing voltage source and a variable resistance control element connected in series with said input lead,
 - a balanced detector connected across the output terminal and the input to said voltage regulator means, said balanced detector having an output connected to said control element.
3. A regulator according to claim 1 in which said buffer circuit comprises,
 - a series control circuit including a voltage source and a transistor having a base and having a collector and an emitter connected in series with said voltage source,
 - said control circuit being connected between said detecting point and the input to said voltage regulating means,
 - a balanced detector connected across the input to said voltage regulating means and the side of said resistance opposite said detecting point, said balanced detector having an output connected to the base of said transistor.
4. A regulator according to claim 1, further comprising,
 - switch means connected between said output control means and said current and voltage regulating means,
 - said switch means rendering said voltage regulator inoperative until the output voltage reaches a preselected level, and renders said current regulator inoperative when said output voltage reaches said preselected level.

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5. A regulator according to claim 4 in which said switch means comprises a pair of transistors each having a base, and emitter and a collector,

said transistors having one of their remaining like terminals connected together at a junction point and the other of their like terminals connected to reference voltages, the outputs of said current and voltage regulators being connected to respective bases of said transistors,

said junction point being connected through a resistance to a voltage source of opposite polarity to said reference voltage,

said junction point being connected to said output control means.

6. A combined current and voltage regulator comprising,

an unregulated power supply having positive and negative output lines terminating in output terminals, a variable resistance control element in one of said lines,

a resistance in one of said lines,

current regulating means connected across said resistance and including a reference voltage, said current regulating means comparing the voltage drop across said resistance to said reference voltage, said current regulating means having an output connected to said control element for varying its resistance to bring

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the reference voltage and voltage drop into balance, voltage regulating means having input leads connected across said output lines and including a reference voltage source, said voltage regulating means comparing the output voltage to said reference voltage and having an output connected to said control element for varying its resistance to bring the output voltage and reference voltage into balance,

one input lead to said voltage regulating means including a buffer circuit, said buffer circuit being connected to a detecting point between said resistance and said control element,

said buffer circuit including means for detecting the voltage drop across said resistance and applying an equivalent voltage drop in said input lead.

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