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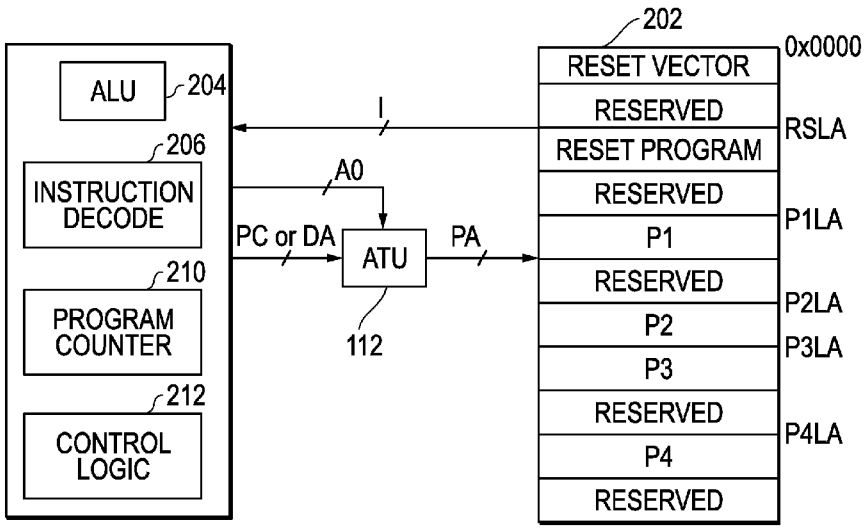

FIG. 2

(57) Abstract: A method and apparatus for microcontroller (MCU) memory relocation. The MCU includes a central processing unit (CPU) and memory, but lacks a memory management unit (MMU). In one embodiment of the method, a first program is selected for execution by the CPU. The first program is one of a plurality of programs stored in the memory of the MCU. Each of the programs includes position dependent instructions. The programs are compiled from source code written in position dependent code.

MICROCONTROLLER SIMPLE MEMORY RELOCATION FUNCTION

Jon Matthew Brabender

BACKGROUND OF THE INVENTION

[0001] A Microcontroller unit (MCU) is small computer formed on an integrated circuit. MCUs provide embedded control of a wide range of devices, such as electric motors, voltage regulators, office machines, appliances, implantable medical devices, etc.

[0001] An MCU includes a central processing unit (CPU), memory, and other components. Program memory stores a main program and a reset program (sometimes referred to as "boot code"). Program are typically stored in non-volatile flash memory.

[0002] A program includes a sequence of instructions that is derived by compiling a program written in human readable source code. On request, the CPU executes a program, instruction by instruction, until termination.

[0003] MCU program memory is organized into an array of addressable units. Instructions and data of a program are stored in addressable units of program memory. Each instruction or unit of data can be fetched from program memory at an address thereof.

SUMMARY OF THE INVENTION

[0004] A method and apparatus for microcontroller unit (MCU) memory relocation is disclosed. The MCU includes a central processing unit (CPU) and memory, but lacks a memory management unit (MMU). In one embodiment of the method, a first program is selected for execution by the CPU. The first program is one of a plurality of programs stored in the memory of the MCU. Each of the programs includes position dependent instructions or data. The programs are compiled from source code written in position dependent code.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention may be better understood in its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0006] Figure 1 is a block diagram illustrating an example MCU employing one embodiment of the present invention.

[0007] Figure 2 is a block diagram illustrating an example CPU coupled to memory via an address translation unit employing one embodiment of the present invention.

[0008] Figure 3 is block diagrams illustrating one embodiment of the address translation unit of Figure 2.

[0009] Figure 4 is a flow chart illustrating operational aspects of the CPU and address translation unit of Figures 2 and 3.

[0010] Figure 5 is a graphical representation of a table stored in memory of the example MCU.

[0011] The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION

[0012] As noted above, an MCU includes a CPU, memory, and other components. The CPU includes a program counter with a program count (PC), which is a direct or indirect address for the next instruction of the program being executed. As soon as that instruction's execution starts, the PC is advanced, and it points to the next instruction to be executed. The PC need not advance in sequential order. The PC can jump forward or backwards in varying increments in accordance with the program being run.

[0013] A fair amount of initialization and housekeeping must done before the CPU runs a main program. Some very critical hardware may need to be initialized. Then some software initialization may need to happen, such as setting up a stack pointer and perhaps copying data from nonvolatile memory to volatile memory where it can be accessed and perhaps modified by the CPU. Initialization and housekeeping is performed in accordance with the reset program embedded in program memory. The CPU runs the reset program in response to activation of a reset signal. When the reset signal is activated, the CPU immediately sets its PC to a predetermined value such as 0x0000 (hexadecimal), which is the direct memory address of a "reset vector." The reset vector tells the CPU where the reset program can be found in memory. The CPU sets the PC to an address fetched from the reset vector. This fetched address is the address of the reset program.

[0014] At the end of the reset process, the PC is set to another predetermined address, which points to a memory location where the main program can be found. This address is fixed (doesn't change after the reset program is loaded into memory) and is known as the main program link address (hereinafter the link address or LKA). At the end of the reset process, the CPU begins executing whatever program is at the main program link address. To emphasize this point, two identical MCUs are loaded with distinct main programs that implement different functions. Both programs are stored in their respective MCUs at the same main program link address, e.g., 0xFFFE. After the reset process, the PC in each MCU is set to 0xFFFE, and the CPU in each MCU begins running its respective program located at 0xFFFE.

[0015] In general, programs are written in position independent code or position dependent code. Position independent code (PIC) uses relative addressing, while positon

dependent code (PDC) uses absolute addressing. To illustrate, an instruction in a PIC program might look like: "jump 585 bytes from the current position" or "jump 5745 bytes from the address where the program is stored in memory." In contrast, a similar instruction in a PDC program might look like "jump to address 0xF6F5."

[0016] Because PIC programs employ relative addressing, PIC programs can be loaded anywhere in memory and properly executed therefrom. In contrast a PDC program must be stored or loaded at a predetermined address (e.g., the main program link address) in order to run properly. PDC programs could be stored anywhere in memory if the absolute addresses of instructions or data are translated by a memory management unit (MMU). An MMU, sometimes called paged memory management unit (PMMU), is a hardware unit through which all memory addresses are passed, primarily performing the translation of virtual memory addresses to physical addresses. MMUs typically divide a virtual address space into pages, each having a size which is a power of 2, usually a few kilobytes, but they may be much larger. The bottom bits of the address (the offset within a page) are left unchanged. The upper address bits are the virtual page numbers. MMUs use an in-memory table of items called a "page table," containing one "page table entry" (PTE) per page, to map virtual page numbers to physical page numbers in memory.

[0017] Software developers prefer to write programs for MCUs using PDC for various reasons. Few if any MCUs, however, employ MMUs and virtualized addressing. At the end of the reset program, the PC is set to the link address, and the CPU begins executing whatever program is found there. As a result, the main program for MCU must be loaded into memory at the link address in order to run properly. Because memories in MCU have only single physical addresses (and no virtualized addressing), two main programs cannot be loaded at the same link address. This situation would prevent two versions of the same "main program" to be loaded into an MCU at a time.

[0018] The present invention relates to an apparatus and method that enables a main program written in PDC to be loaded into any program memory location and later executed from this memory location in proper fashion. As a result of employing the present invention, MCU memory can store multiple main programs written in PDC. This advantage and others will be more fully described below.

[0019] MCUs have distinct architectures. In general, however, an MCU contains a CPU and program memory for storing a reset program and at least one main program. The present invention will be described with respect to an MCU that lacks an MMU. Figure 1 illustrates several components of an example MCU 100 that employs one embodiment of the present invention.

[0020] MCU 100 includes a CPU 102 that executes instructions of a reset program or a main program. Flash memory 104 stores several main programs written in PDC. The reset program can also be stored in flash memory 104. A computer system (not shown) can transmit main programs via a communications link to MCU 100 for subsequent storage in flash memory 104. MCU 100 also includes a small amount of RAM 110 that can be used by CPU 102 for storing temporary data. CPU 102 can access flash memory 104 to read program instructions or program data. RAM 110 includes general purpose registers, at least one of which can be used to store an address for data contained in a program.

[0021] MCU 100 includes an address translation unit (ATU) 112 that can translate a program count (PC) for program instructions as will be more fully described below. ATU 112 can also translate address for program data as will be more fully describe below. ATU 112 enables multiple main programs to be run from different locations in memory 104, even though each of the main programs are designed to operate from the same link address LKA.

[0022] MCU 100 includes one or more comparators 114, each of which is configured by CPU 102 to compare two input digital values. CPU 102 and comparators 114 are built to interpret or process digital data, and accordingly they are not able to do anything with analog signals received from, for example, devices external to MCU 100. ADCs 116 can convert analog signals into a form that CPU 102 or digital comparators 114 can recognize. MCU 100 also includes digital to analog converters (DACs 120), which allow MCU 100 to output analog signals for controlling devices external to the MCU.

[0023] A Universal Asynchronous Receiver/Transmitter (UART) block 122 makes it possible for MCU 100 to receive a new main program via a communication link with very little load on CPU 102. The new main program can be stored in flash memory 104. The UART or another component of MCU 100 is capable of asserting a reset signal after the

UART receives a new maim program. The reset signal, when asserted, prompts the CPU 102 to initiate its reset program. As noted, one of several main programs stored in flash memory 104, including the new main program, is selected during the reset process for subsequent execution.

[0024] MCU 100 includes timer channels 124. Timer channels are circuits that include one or more functional units such as compare/capture units, pulse-width modulation (PWM) units, etc. Not all timer channels of an MCU are identical. Some timer channels of an MCU may include only compare/capture units, while other timer channels of the MCU include only PWM units. Still other timer channels of the MCU may contain both compare/capture units and PWM units and other functional units. Timer channels usually contain at least one n-bit counter register (hereinafter counter register), which stores an n-bit counter value (hereinafter counter value). Counter registers count pulses of a clock signal or pulses of an event signal. In other words, a counter register may increment or decrement its counter value with each pulse of a clock signal or each pulse of an event signal. For most counter registers, the counter value overflows to zero after it reaches its maximum value. Clock pulses are typically produced by a clock generator that is internal or external to the MCU. Scalar units in timer channels may adjust the frequency of the clock signal. Event pulses are generated by devices that are internal or external to the MCU. Event pulses are generated with corresponding events. For example, a comparator internal to an MCU may generate an event pulse when the comparator detects equality between two input values. Or, an MCU may receive an event pulse generated by a magnetic sensor of an external device when the sensor detects a magnetic field of certain strength.

[0025] Watchdog timer channel 126 is a special timer channel that is used to detect and recover from MCU malfunctions. Watchdog timer channel 126 includes at least one counter register, which counts pulses of a clock signal. During normal operation, the CPU 102 regularly restarts the watchdog counter value to prevent it from reaching its maximum value. If, due to a hardware fault or program error, CPU 102 fails to restart the watchdog counter value, the watchdog timer channel 126 will assert the reset signal, which prompts the CPU 102 to initiate its reset program.

[0026] With continuing reference to Figure 1, MCU 100 includes an event link controller (ELC) 128. ELC 128 receives internally generated event signals IE1 – IEM from

components such as comparators 114, ADCs 116, timer channels 124, etc., via a communication system. ELC 128 can be configured by CPU 102 to select a subset E1 - EN of the internally generated event signals IE1 – IEM for transmission to one or more components via the communication system.

[0027] I/O system 128 contains I/O pins 130, some of which can be configured by CPU 102 to an input state or an output state. When I/O pins are in the input state, they are often used to read signals generated by devices external to the MCU 100. An I/O pin 130 configured in the input state will be referred to herein as an input pin 130. I/O pin 130-1 is configured as an input pin, and configured to receive an externally generated reset signal. When a device external to MCU 100 asserts the reset signal at pin 130-1, the CPU 102 initiates its reset program. In the output state, I/O pins 130 can drive devices external to the MCU 100.

[0028] An I/O pin 130 configured in the output state will be referred to herein as an output pin 130. Components 102 – 130 are in data communication with each other via a communication system 132. Although not shown, the communication system may 132 take form in one or more buses, signal lines and other devices that are configured to transmit control values, data, signals, addresses, instructions, etc.

[0029] With continuing reference to Figure 1, Figure 2 illustrates one embodiment of CPU 102 in data communication with program memory 202 and ATU 112. In the embodiment shown, program memory 202 is a logical presentation of flash memory 104. Program memory 202 is organized into an array of addressable units. Data and instructions of a program are stored in addressable units of memory. Accordingly, each data unit instruction can be fetched from a corresponding address in memory 202.

[0030] Figure 2 shows organization of memory 202. In particular, a reset vector is stored at address 0x0000. The reset vector points to the reset program loaded at address RSLA. Individual main programs P1 - P4 are loaded at addresses P1LA - P4LA, respectively. In one embodiment load address P1LA and link address LKA are identical. In another embodiment, LKA is outside the memory space of program memory 202. It is also noted that each of the programs P1 - P4 are written in PDC with the assumption that each will be loaded in memory

at link address LKA. In other words, when P1 - P4 were developed there was no special consideration to not being run from link address LKA.

[0031] CPU 102 includes an arithmetic logic unit (ALU) 204 coupled to an instruction decoder 206, program counter 210 and control logic 212. Instruction decoder 206 and control logic 212 decodes and carries out instructions fetched from memory 202. ALU 204 performs arithmetic and logic operations on the data contained in registers (not shown). ALU 204 is the heart of the CPU 102. Program counter 210 maintains the PC, which is the direct or indirect address of the next instruction to be fetched and executed. Once the instruction is executed, the PC is advanced. CPU 102 can write data addresses (DAs) in a general purpose register of RAM 110. These addresses point to data contained in a program. Although the figures show CPU 102 and ATU 112 as separate units, in an alternative embodiment, ATU 112 may be a subunit of CPU 102.

[0032] The PC is a direct or indirect address for the next instruction to be executed. DA is a direct or indirect address for data of a program in flash memory 104. In one embodiment, PC or DA is deemed indirect if it is contained in a specific range of addresses. For example, the PC or DA is an indirect address if certain bits (e.g., the 9 most significant bits) equate to a predetermined binary value (e.g., 000000100 binary). If indirect, ATU 112 translates the PC or DA into a direct address. After the instruction corresponding to the PC is fetched and executed, the PC advances in accordance with the program (e.g., reset program or main program) being executed. After data corresponding to DA is fetched and processed, CPU 102 can change the value of DA in the GPR.

[0033] Regardless of whether the PC or DA is translated, ATU 112 outputs a direct or physical address PA for the next instruction or program data. If the PC is determined to be a direct address, PA = PC. If PC is determined to be indirect, PA = f(PC). Stated differently, if PC is determined to be indirect, PA is generated as a function of PC. Similarly, If the DA is determined to be a direct address, PA = DA. If DA is determined to be indirect, PA = f(DA). In one embodiment, PA can be generated by adding an address offset AO of m bits to PC or DA. The m bits of AO can be added to the least significant m bits of PC or DA, or the middle m bits of PC or DA. In another embodiment, PA can be generated by adding the address offset AO to PC or DA, and then replacing the upper y bits (e.g., 9 bits) of the result with a predetermined binary value (e.g., 000000000 binary). This later embodiment can be

used when the link address LKA is outside the range of address space for memory 202. Regardless of whether PC or DA is a direct or indirect address, the instruction corresponding to the PC or the data corresponding to the DA is fetched from memory 202. As will be more fully described below, CPU 102 selects AO from a candidate list of AOs during the reset process. CPU 102 selects the AO after the CPU 102 selects one of the main programs P1 – P4 for subsequent execution.

[0034] Figure 3 illustrates relevant components of an example ATU 112 in block diagram form. ATU 112 includes an AO register 302 that receives and stores an m bit AO selected by CPU 102 during the reset process, as will be more fully described below. ATU 112 also includes a range register that receives and stores a y bit range value R. A compare circuit 310 uses R to determine if the PC or DA is a direct or indirect address. In one embodiment, if the most significant y bits of the PC or DA equates with R, the PC or DA is an indirect address that should be translated. For example, with R = 000000100 (binary) all PCs or DAs that begin with 000000100 (binary) are indirect addresses.

[0035] Adder 306 receives the offset AO and PC or DA, which has n bits. AO has m bits, which is less than n. Adder 306 generates a translated PC (TPC) or translated DA (TDA) having n bits. Adder 306 generates TPC or TDA by adding the m bits of AO to the least significant m bits of the PC or DA in the illustrated embodiment. For example, with AO = 4422380 (hexadecimal) and PC = 2001000 (hexadecimal), AO + PC = TPC = 2423380 (hexadecimal). In another embodiment, the m bits of AO are added to the middle m bits of the PC or DA. In still another embodiment in which the link address LKA for the program being executed is outside the address space for memory 202, an additional circuit is interposed between adder 306 and the input of selector 312. This added circuit sets the most significant z bits of TPC or TDA to a predetermined value (e.g., 000000000 binary). However, for the purposes of explanation only, the present invention will be described with no added circuit, so that the output TPC or TDA of adder 306 provided directly to selector 312 as one input. The PC or DA is provided to selector circuit 312 as the other input. Selector 312 selects either PC or TPC as the PA for the next instruction to be executed by CPU 102, or selector 312 selects either DA or TDA as the next PA for data from memory 202. The selection is based on the comparison performed by compare circuit 304. If compare circuit 310 detects equality between R and the most significant y bits of PC or DA,

PC or DA is an indirect address, and selector 312 selects TPC or TDA as the PA for the next instruction or data. If compare circuit 310 does not detect equality between R and the y bits of PC or DA, PC or DA is a direct address, and selector 312 selects PC or DA as the PA for the next instruction or data.

[0036] CPU 102 can receive an activated reset signal from any one of many different sources such as watchdog timer 126 or input 130-1. In response to receiving this activated reset signal, CPU 102 executes its reset program. During the reset process, CPU 102 selects one of the main programs P1 – P4 for subsequent execution. Figure 4 is a flow chart illustrating relevant aspects of a process implemented by CPU 102 in response to activation of the reset signal.

[0037] The process shown in Figure 4 begins with activation of the reset signal. In step 404, CPU 102 sets its PC to a predetermined address associated with the reset vector. For the purposes of explanation, the predetermined address is 0x0000 (hexadecimal). Presuming R in register 304 is set to 000000100 (binary), PC = 0x0000 is determined by compare circuit 310 to be a direct address. As a result, selector 312 selects PC = 0x0000 as the PA for the reset vector, regardless of the TPC that is generated by adder 306. The reset vector, which contains the load address of the reset program, is fetched from memory 202. In response to CPU 102 receiving the reset vector, CPU 102 sets its PC to RSLA, the load address of the reset vector, in step 406. In step 408, execution of the reset program is started. RSLA and all addresses for instructions or data of the reset program are direct addresses (i.e., the 9 most significant bits are not set to 000000100 binary). As a result selector 312 selects PC or DA as the PA for all instructions or data of the reset program.

[0038] During the reset process, CPU 102 selects one of the main programs P1 – P4 for subsequent execution as shown in step 410. The selection can be based on any one of a number of factors. For example, if the reset program was activated because a new program Pnew was loaded into memory 202, CPU 202 will select Pnew. In another embodiment, CPU 102 may maintain historical performance data (not shown) about each of the programs P1 – P4. For example, CPU 102 may count and store the number of times the execution of a program results in malfunction. From this information, CPU 102 may select the program that malfunctioned the least. In another embodiment, CPU 102 may select one of the programs

P1 – P4 based on the time of day, day of the week, or day of the year. In an alternative embodiment, CPU 102 may receive an instruction from an external device prior to the reset process. This instruction may identify the program to be executed on the next reset process. Additional or alternative program selection criteria can be written into the reset program.

[0039] Although not shown in the figures, a header for each main program P1 – P4 is created in memory 202 upon download. Each header can include an identification Px of its corresponding main program, where x is an integer. Additional information may be included in the header. For example, the header may include the length of the main program Px, version number of main program, load address PxLA in memory 202 of Px, and an address offset AOx calculated as a function of the load address PxLA and the link address LKA, etc. In one embodiment, AOx may be calculated by subtracting the link address LKA from the load address PxLA. In the embodiment shown, AO1 should be P1LA – LKA = 0x0000 (hexadecimal), AO2 should be P1LA – LKA, etc. During the reset process, CPU 102 may scan memory 202 for program headers and extract relevant information therefrom. For example, CPU 102 may scan the program headers for program identifications and corresponding address offsets. Once identified, these values can be mapped in a table (not shown) in memory 202. Figure 5 illustrates an example table that links or maps address offsets AOs to program identifications. During the reset process, CPU 102 may access this table and select a program for execution at step 410 in accordance with a selection criteria described above.

[0040] Once a main program is selected, CPU 102 accesses the table shown in Figure 6 and maps the selected program to its corresponding address offset AO. CPU 102 stores this address offset AO in the offset register 302 as shown in step 414. For the ease of illustration, program P3 is selected for execution, and as a result CPU 102 stores AO3 in register 302. The reset program continues initializing CPU 102 in accordance with instructions of the reset program. At the end of the reset process, CPU 102 sets its PC to link address LKA.

[0041] Link address LKA is within the range of addresses defined by R. As such LKA is an indirect address. ATU 112 will translate LKA. Specifically, selector 312 will not select PC = LKA as the PA for the first instruction of P3. Rather selector 312 will select TPC = LKA + P3AO as the PA, and CPU 102 will begin executing instructions in memory 202

beginning at LKA + P3AO. Thereafter PC will advance its PC after the instruction is executed. For example, CPU 102 may set PC=PC + 2. This new PC, and all subsequent PC values, should fall within the range of addresses defined by R. Accordingly, PC is continuously translated during execution of P3. In other words, selector 312 will select TPC as the PA for all instructions of P3. CPU 102 will continue to run P3, the selected program in the illustrated example, until the reset signal is activated in step 424.

[0042] Although the present invention has been described in connection with several embodiments, the invention is not intended to be limited to the specific forms set forth herein. On the contrary, it is intended to cover such alternatives, modifications, and equivalents as can be reasonably included within the scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method implemented in a microcontroller unit (MCU) that comprises a central processing unit (CPU), the method comprising:

selecting a first program for execution by the CPU;

wherein the first program is one of a plurality of programs concurrently stored in memory of the MCU;

wherein each of the programs comprises position dependent instructions.

2. The method of clam 1 further comprising:

setting a program counter to a predetermined value;

generating a first address in response to setting the program counter to the predetermined value.

3. The method of claim 3 wherein the programs are stored in the memory at respective load addresses, wherein the programs are mapped to respective address offsets, and wherein the address offsets correspond to the load addresses, respectively.

4. The method of claim 3 further comprising an act of mapping the first program to a first address offset.

5. The method of claim 4 further comprising:

comparing the X most significant bits of the first address with a predetermined set of X bits, where X is an integer equal to or greater than 1;

in response to determining a mismatch between the X most significant bits of the first address and the predetermined set of X bits, accessing a CPU executable instruction stored in the memory at the first address.

6. The method of claim 4 further comprising:

comparing the X most significant bits of the first address with a predetermined set of X bits, where X is an integer equal to or greater than 1;

in response to determining a match between the X most significant bits of the first address and the predetermined set of X bits, generating a modified first address as a function of the first address offset and the first address;

accessing a CPU executable instruction stored in the memory at the modified first address.

7. The method of claim 4 further comprising:

generating a modified first address as a function of the first address offset and the first address;

accessing a CPU executable instruction stored in the memory at the modified first address.

8. The method of claim 7 further comprising:

advancing the program counter;

the CPU generating a second address in response to advancing the program counter;

generating a modified second address as a function of the first address offset and the second address;

accessing a CPU executable instruction stored at the modified second address.

9. The method of claim 8 further comprising:

asserting a reset signal;

selecting a second of the plurality of programs in response to assertion of the reset signal;

mapping the second program to a second address offset;

the CPU regenerating the first address;

generating another modified first address as a function of the second address offset and the regenerated first address;

accessing a CPU executable instruction stored at the other modified first address.

10. The method of claim 4 further comprising:

receiving a new program from a device external to the MCU;

storing the new program into the memory at a new load address, wherein the new program is stored concurrently with the plurality of programs in the memory;

updating a data structure to map the new program to a new address offset, wherein the new address offset corresponds to the new load address.

11. The method of claim 1 wherein one of the programs is a later developed version of another of the programs.

12. An apparatus comprising:

a microcontroller unit (MCU) wherein the MCU comprises:

a central processing unit (CPU);

a memory for storing a plurality of programs that are executable by the CPU;

an address translation unit for selectively translating addresses generated by the CPU;

wherein each of the programs comprises position dependent instructions.

13. The apparatus of claim 12 wherein the MCU further comprises a reset program stored in the memory, wherein the reset program is executable by the CPU in response to assertion of a reset signal, wherein the CPU selects a first of the programs for execution by the CPU in response to executing the reset program.

14. The apparatus of claim 13 wherein the address translation unit comprises an adder and memory for storing an address offset and an enable bit, wherein the adder selectively adds the address offset to addresses generated by the CPU when the enable bit is set to a first state, and wherein the adder does not add the address offset to addresses generated by the CPU at any time the enable bit is set to a second state.

15. The apparatus of claim 14 wherein the address translation unit comprises a comparator for comparing the X most significant bits of addresses generated by the CPU with X predetermined bits, wherein the adder adds the address offset to an address generated by the CPU when the enable bit is set to the first state and when the X most significant bits of the address generated by the CPU compares equally with the X predetermined bits, and wherein the adder does not add the address offset to the address generated by the CPU when the enable bit is set to the second state and when the X most significant bits of the address generated by the CPU does not compare equally with the X predetermined bits.

16. The apparatus of claim 15 wherein the CPU is configured to select the address offset from among a plurality of address offsets that correspond to the programs, respectively.

17. The apparatus of claim 16 wherein the CPU is configured to calculate the address offsets as a function of respective load addresses of the programs, respectively, in the memory, and a link address.

18. An apparatus comprising:

a microcontroller unit (MCU) wherein the MCU comprises:

a central processing unit (CPU);

a memory for storing a plurality of programs that are executable by the CPU;

a reset program executable by the CPU, wherein the CPU is configured to select one of the programs for execution in response to executing the reset program;

wherein each of the programs comprises position dependent instructions.

19. The apparatus of claim 18 further comprising:

an address translation unit;

a program counter;

wherein the CPU is configured to set the program counter to a predetermined value in response to executing the reset program;

wherein the CPU is configured to generate a first address in response to setting the program counter to the predetermined value;

wherein the address translation unit is configured to translate the first address into a first translated address;

wherein the CPU is configured to receive a first instruction stored at the first translated address;

wherein the CPU is configured to execute the first instruction;

wherein the CPU is configure to advance the program counter in response to executing the first instruction;

wherein the CPU is configured to generate a second address in response to advancing the program counter;

wherein the address translation unit is configured to translate the second address into a second translated address;

wherein the CPU is configured to receive a second instruction stored at the second translated address;

wherein the CPU is configured to execute the second instruction.

20. The apparatus of claim 19 wherein the address translation unit is configured to add an address offset to the first and second addresses to generate the first translated addresses, respectively.

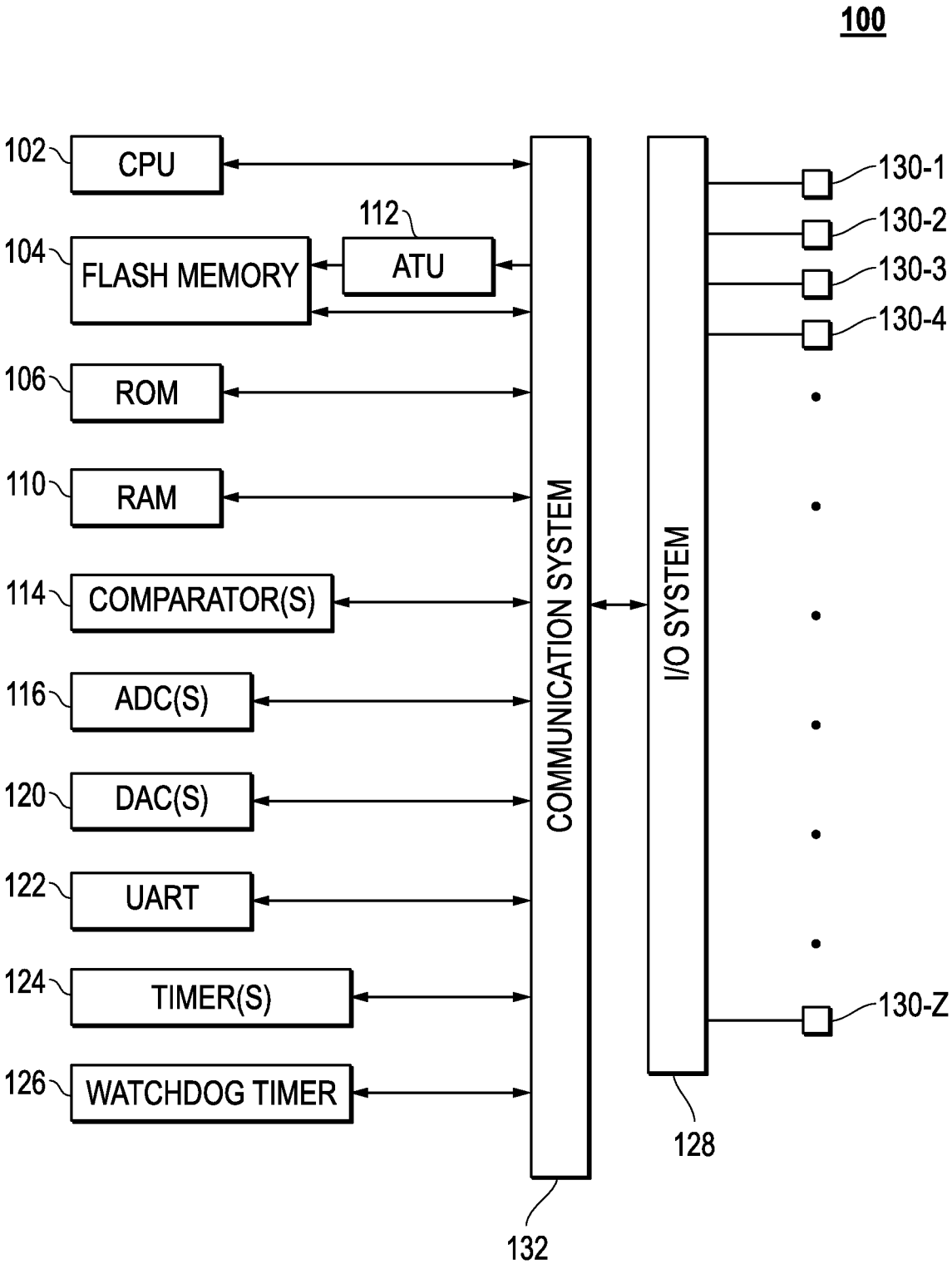
100
102
CPU
112
104
FLASH MEMORY
ATU
106
ROM
110
RAM
114
COMPARATOR(S)
116
ADC(S)
120
DAC(S)
122
UART
124
TIMER(S)
126
WATCHDOG TIMER
COMMUNICATION SYSTEM
I/O SYSTEM
130-1
130-2
130-3
130-4
130-Z
128
132

FIG. 1

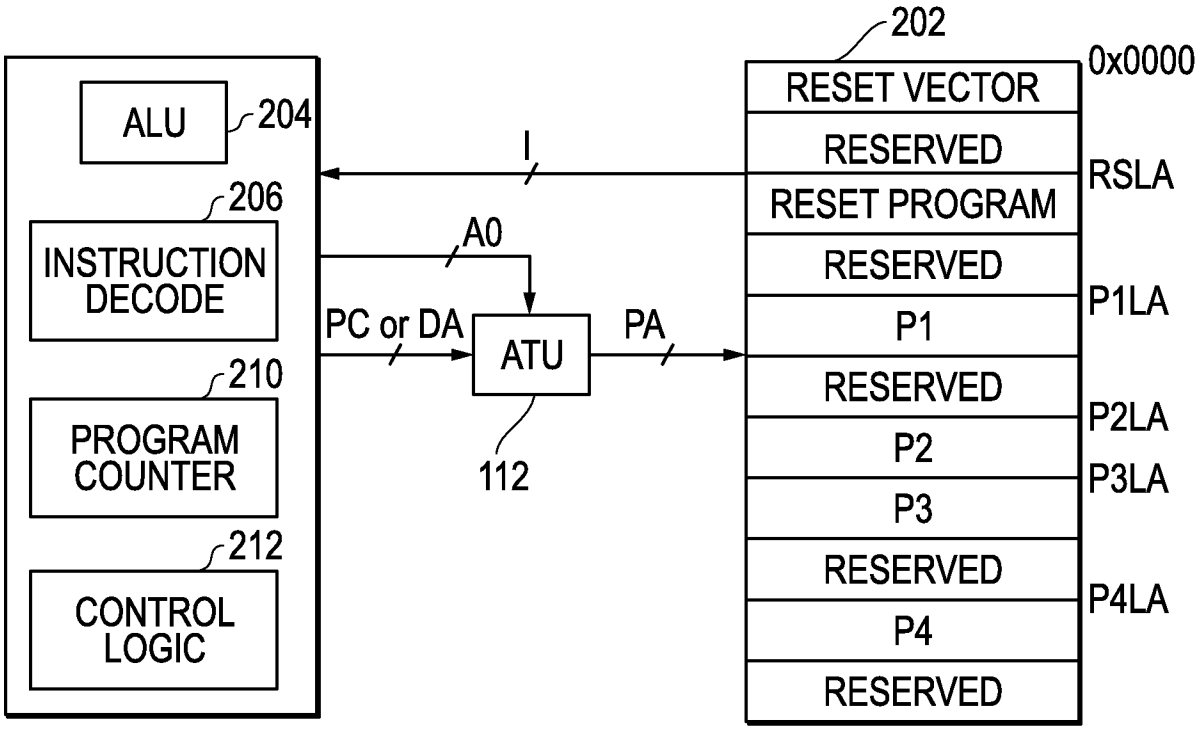

FIG. 2

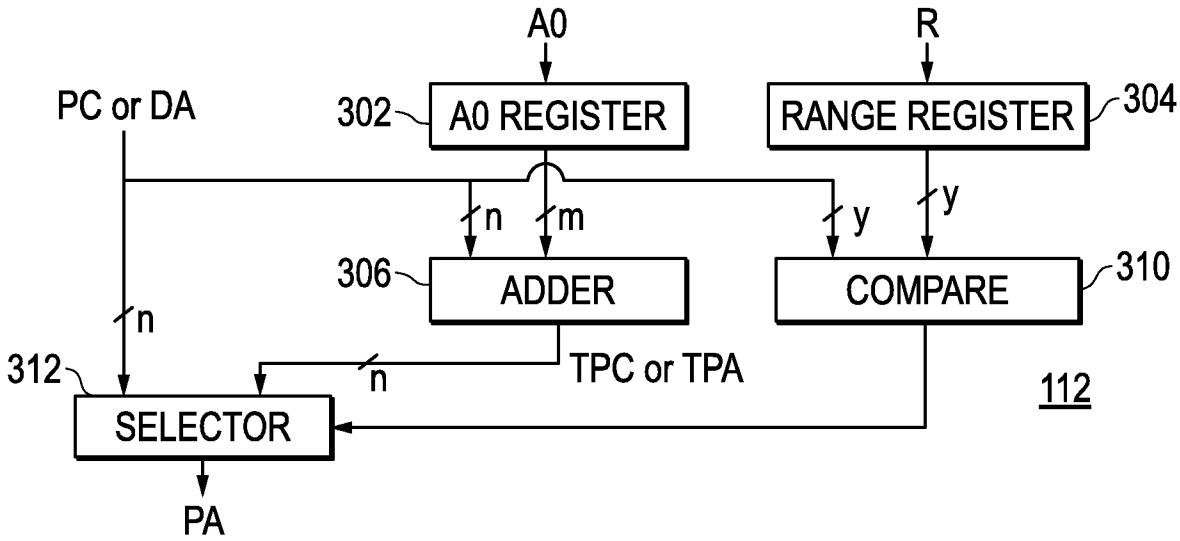

FIG. 3

PROGRAM	A0
P1	A01
P2	A02
P3	A03
P4	A04

FIG. 5

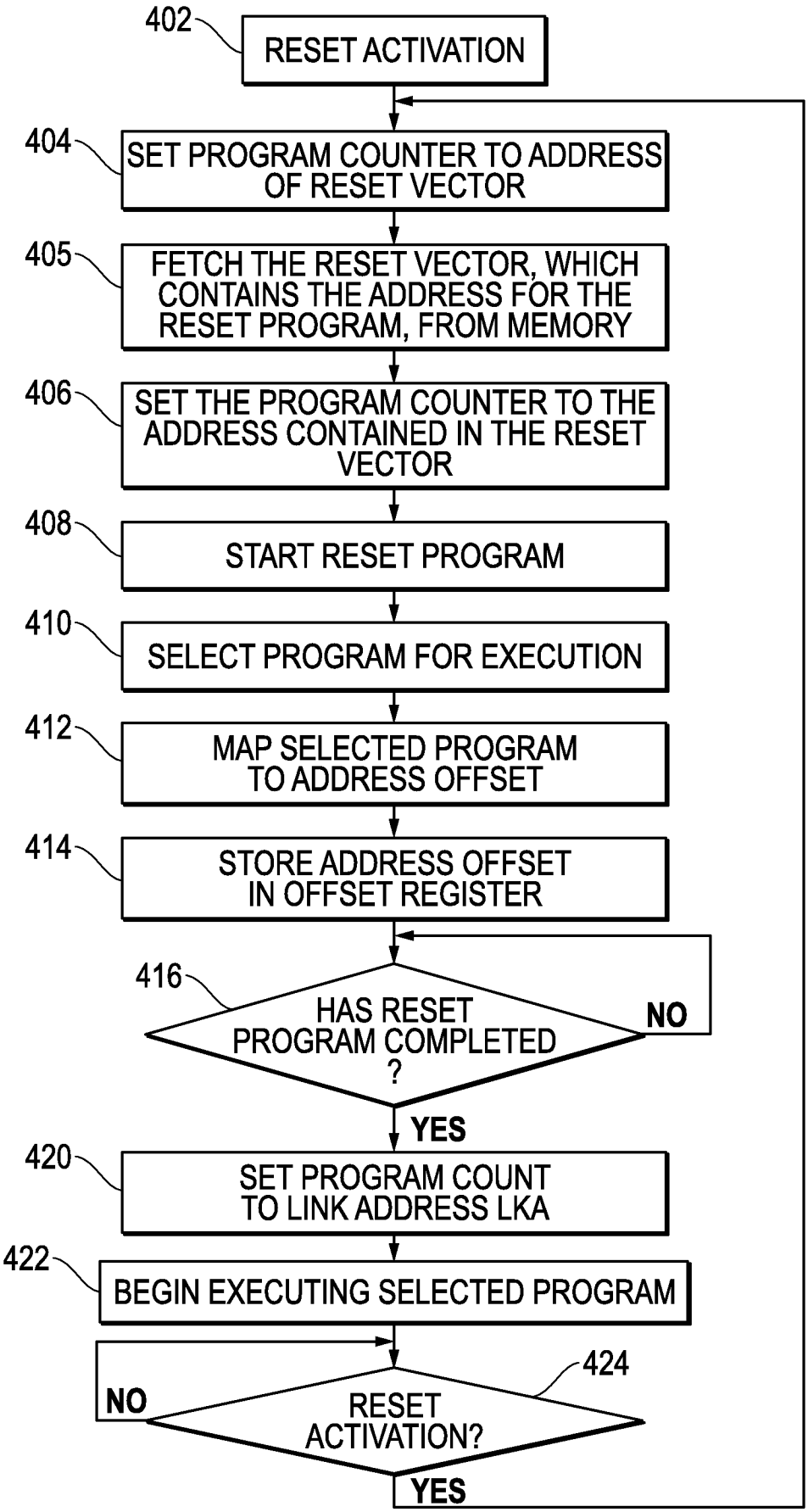
402
RESET ACTIVATION
404
SET PROGRAM COUNTER TO ADDRESS OF RESET VECTOR
405
FETCH THE RESET VECTOR, WHICH CONTAINS THE ADDRESS FOR THE RESET PROGRAM, FROM MEMORY
406
SET THE PROGRAM COUNTER TO THE ADDRESS CONTAINED IN THE RESET VECTOR
408
START RESET PROGRAM
410
SELECT PROGRAM FOR EXECUTION
412
MAP SELECTED PROGRAM TO ADDRESS OFFSET
414
STORE ADDRESS OFFSET IN OFFSET REGISTER
416
HAS RESET PROGRAM COMPLETED ?
NO
YES
420
SET PROGRAM COUNT TO LINK ADDRESS LKA
422
BEGIN EXECUTING SELECTED PROGRAM
424
RESET ACTIVATION?
NO
YES

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 16/35420

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 13/00 (2016.01)
CPC - G06F3/0647
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
CPC: G06F3/0647; IPC(8): G06F 13/00 (2016.01); USPC: 711/165

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC: G06F3/0647, G06F3/067, G06F3/0605, G06F3/061, G06F3/0689; USPC: 711/103, 711/165 (keyword limited; terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase; Google Scholar
Search Terms: microcontroller CPU program execution concurrently memory position dependent instruction

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/0062479 A1 (TAKATA) 23 May 2002 (23.05.2002), entire document, especially abstract and para [0010], [0035], [0038], [0061], [0084], Fig. 2, Fig. 3, Fig. 10.	1-11
A	US 2012/0131309 A1 (JOHNSON et al.) 24 May 2012 (24.05.2012), entire document.	1-11
A	US 2015/0032996 A1 (KOEBERL et al.) 29 January 2015 (29.01.2015), entire document.	1-11

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 July 2016 (28.07.2016)	07 OCT 2016
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 16/35420

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

– see extra sheet –

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-11

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 16/35420

In continuation of:
Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

Group I: Claims 1-11, directed to a method implemented in a microcontroller unit (MCU) that comprises a central processing unit (CPU), and further comprising selecting a first program for execution by the CPU, wherein the first program is one of a plurality of programs concurrently stored in memory of the MCU.

Group II: Claims 12-20, directed to an apparatus comprising a microcontroller unit (MCU) wherein the MCU comprising a central processing unit (CPU), and further comprising an address translation unit for selectively translating addresses generated by the CPU.

The groups of inventions listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical feature of the Group I invention is wherein the first program is one of a plurality of programs concurrently stored in memory of the MCU, not required by Group II. (See Fig. 5 for example).

The special technical feature of the Group II invention is an address translation unit for selectively translating addresses generated by the CPU, not required by Group I. (See Fig. 3 for example).

Groups I-II share the technical features of, in various combination, a microcontroller unit (MCU) that comprises a central processing unit (CPU), a plurality of programs, memory, and wherein each of the programs comprises position dependent instructions.

However, these shared technical features fail to represent a contribution over the prior art of US 2015/0032996 A1 to Koeberl, et al. (hereinafter 'Koeberl'), which discloses a microcontroller unit (MCU) (para [0025], [0069] - "microcontrollers") that comprises a central processing unit (CPU) (para [0064], [0111], Fig. 5C - "CPU"), a plurality of programs (para [0116] - "an instruction fetch unit to fetch a plurality of instructions for a plurality of applications executing in a multitasking environment"), memory (para [0077], [0110] - "main memory"), and wherein each of the programs comprises position dependent instructions (para [0078], [0116], [0124] - "transferring data stored in one memory location (e.g., position)"; "define an instruction region (I-space) in an I-space register"; "receive an instruction address for a first instruction of the plurality of instructions").

Thus, the inventions listed as Groups I-II lack unity of invention because they do not share a same or corresponding special technical feature providing a contribution over the prior art.