(12) UK Patent (19) GB (11) 2092826 B

(54) Title of invention

Semiconductor memory device and fabrication process thereof

(51) INT CL³; H01L 27/04

(21) Application No
8203074

(22) Date of filing
3 Feb 1982

(30) Priority data

(31) 56/015733

(32) 6 Feb 1981

(33) Japan (JP)

(43) Application published
18 Aug 1982

(45) Patent published
9 Jan 1985

(73) Proprietor
Hitachi Ltd.,
5—1 Marunouchi 1-chome
Chiyoda-ku
Tokyo
Japan

(72) Inventors
Nobuyoshi Tanimura
Tokumasa Yasui

(74) Agent and/or
Address for Service
Mewburn Ellis & Co.,
2/3 Cursitor Street
London EC4A 1BQ

(52) Domestic classification
H1K 11A3 11B3 11C1A 11C1B 11C4 11D1 11D3 11D 1BC 1CA 1FJ 4C11 4C14 4C1M 9B1 9B1A 9C1 9D1 9N2 9R2 GAX

(56) Documents cited
GB 1597725

(58) Field of search
H1K

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FIG. 1

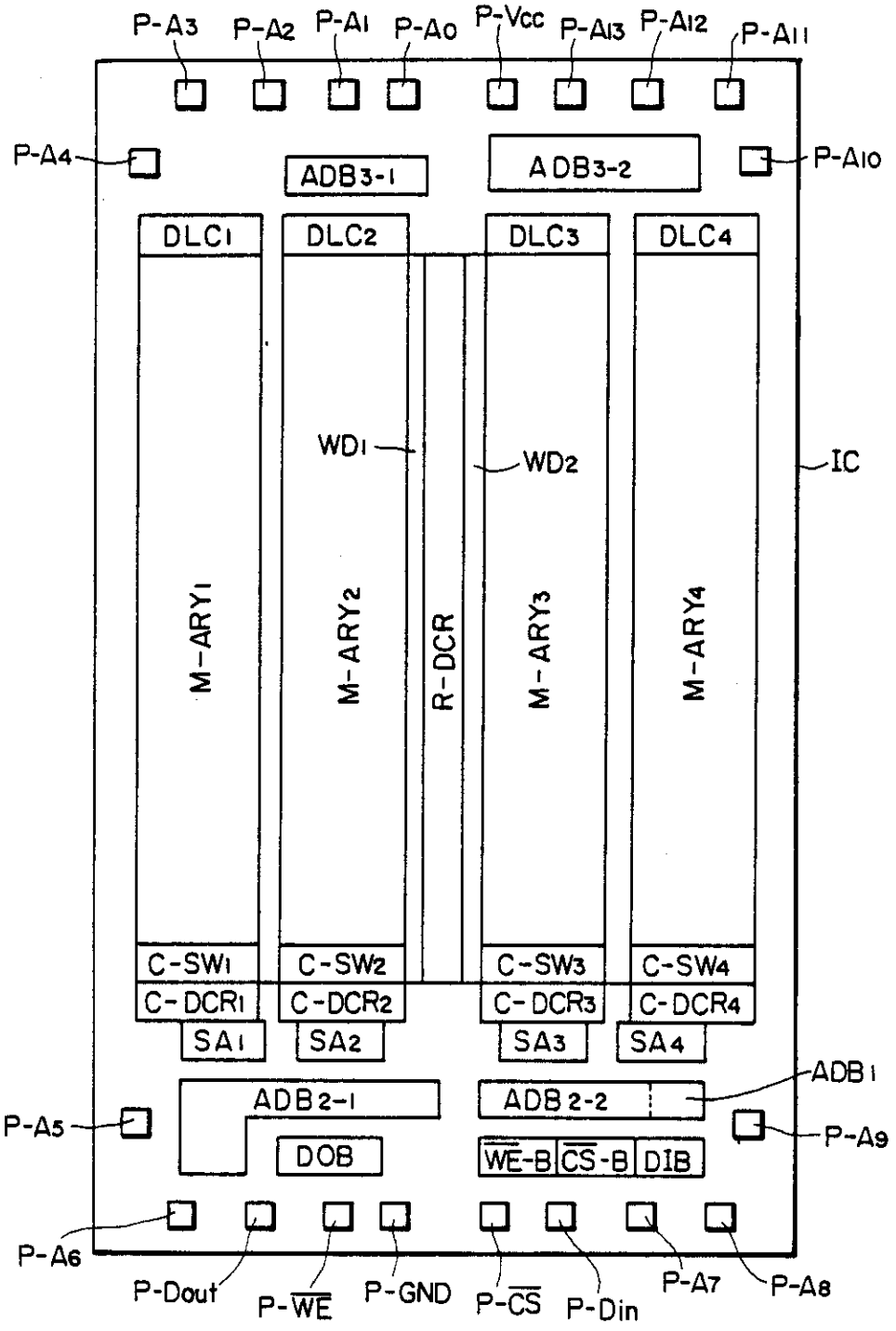
P-A3
P-A2
P-A1
P-A0
P-Vcc
P-A13
P-A12
P-A11
P-A4
P-A10
ADB3-1
ADB3-2
DLC1
DLC2
DLC3
DLC4
WD1
WD2
IC
M-ARY1
M-ARY2
R-DCR
M-ARY3
M-ARY4
C-SW1
C-SW2
C-SW3
C-SW4
C-DCR1
C-DCR2
C-DCR3
C-DCR4
SA1
SA2
SA3
SA4
ADB1
ADB2-1
ADB2-2
P-A5
P-A9
DOB
WE-B
CS-B
DIB
P-A6
P-Dout
P-WE
P-GND
P-CS
P-Din
P-A7
P-A8

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FIG. 2

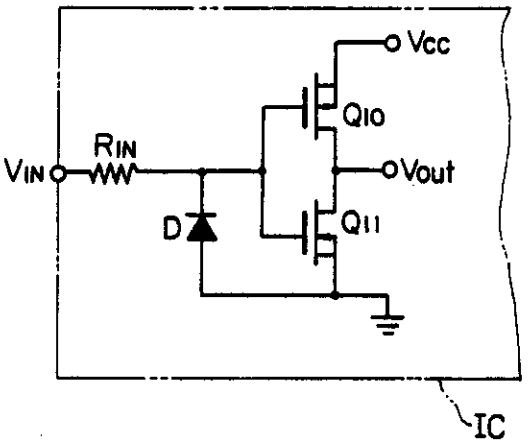


FIG. 4

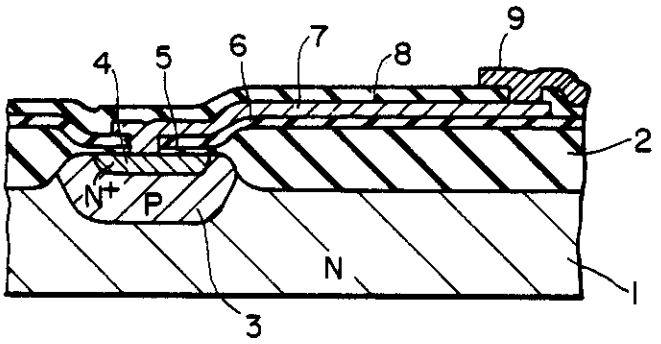


FIG. 3

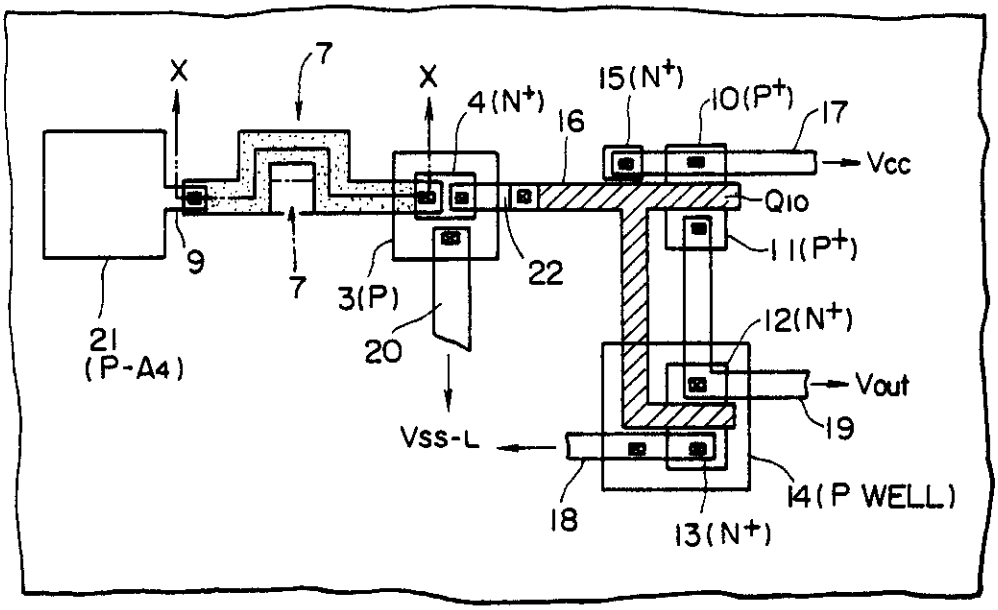
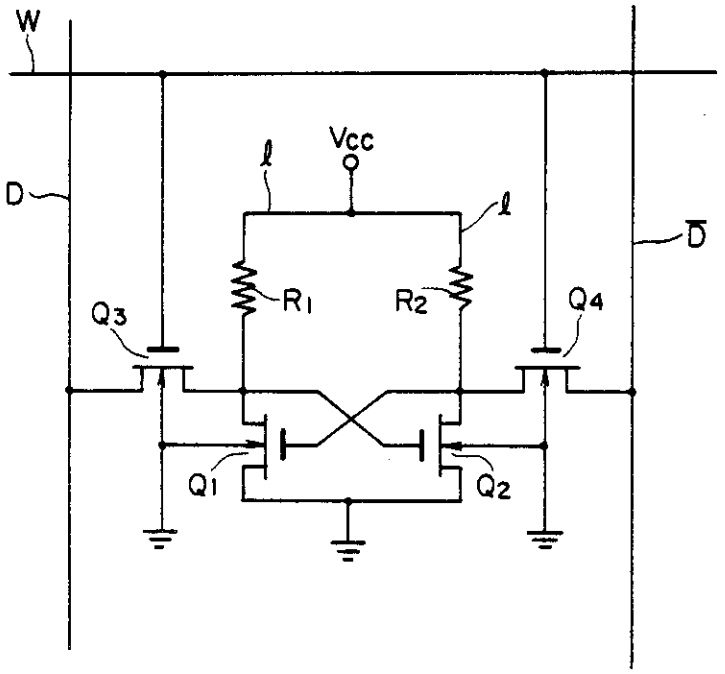

X
7
X
4(N+)
15(N+)
10(P+)
17
16
Vcc
Q10
11(P+)
9
7
3(P)
22
21
(P-A4)
20
12(N+)
Vout
19
Vss-L
18
13(N+)
14(P WELL)

FIG. 5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D
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R2
Q3
Q4
Q1
Q2

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FIG. 6

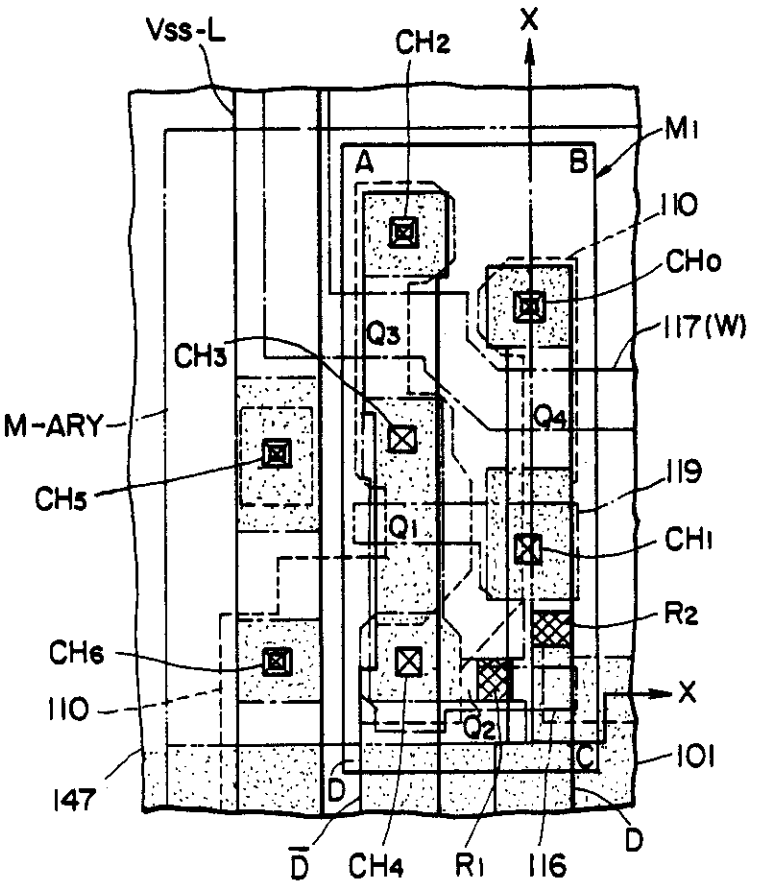
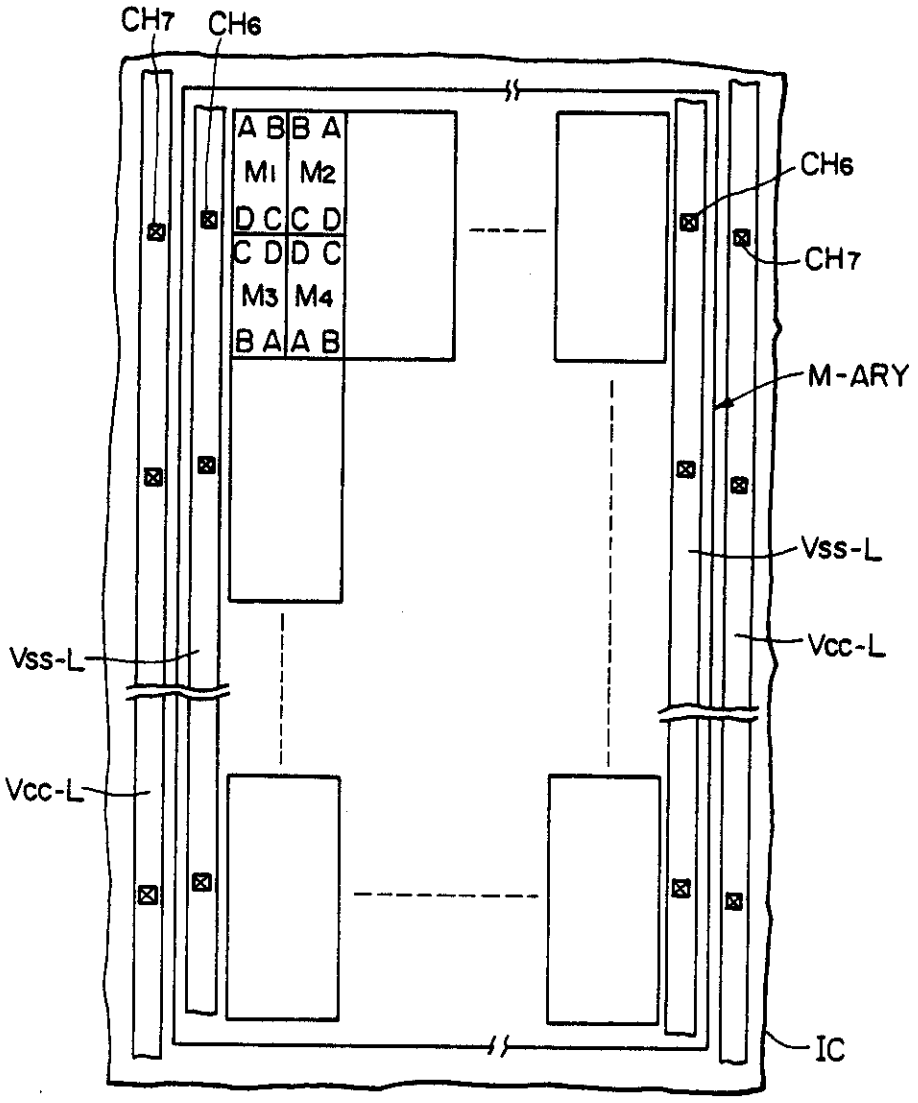


FIG. 7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CH6
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M1 M2
D C C D
C D D C
M3 M4
B A A B
CH6
CH7
M-ARY
Vss-L
Vcc-L
Vss-L
Vcc-L
IC

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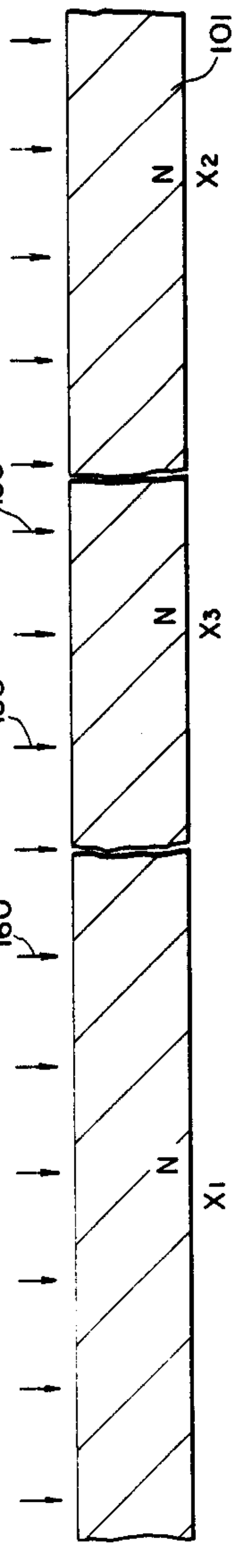


FIG. 8A

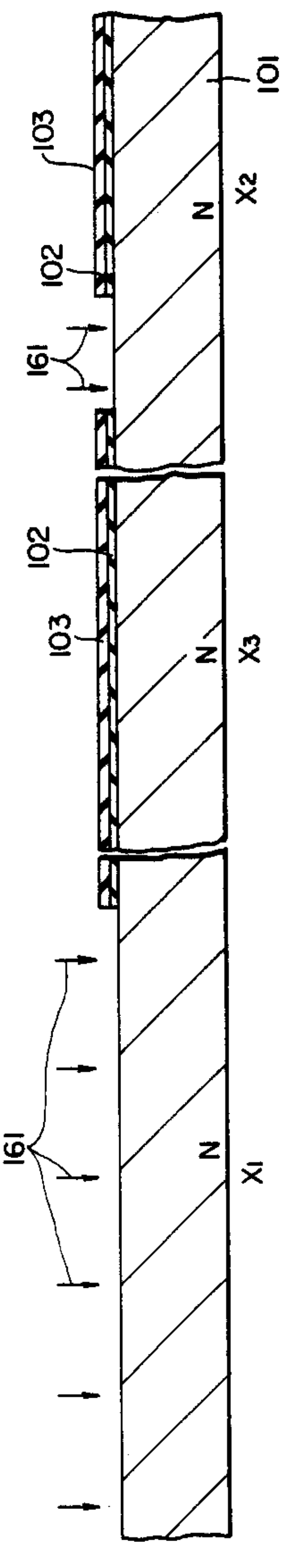


FIG. 8B

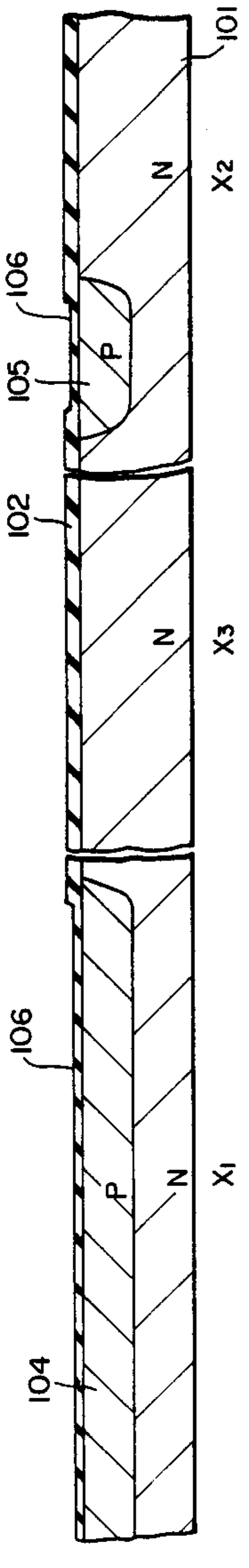


FIG. 8C

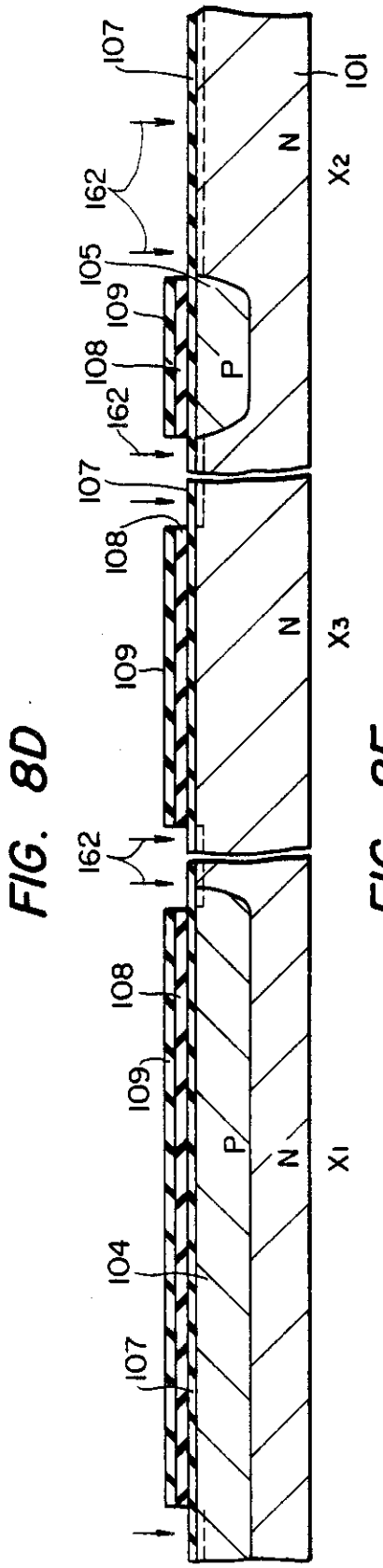


FIG. 8D

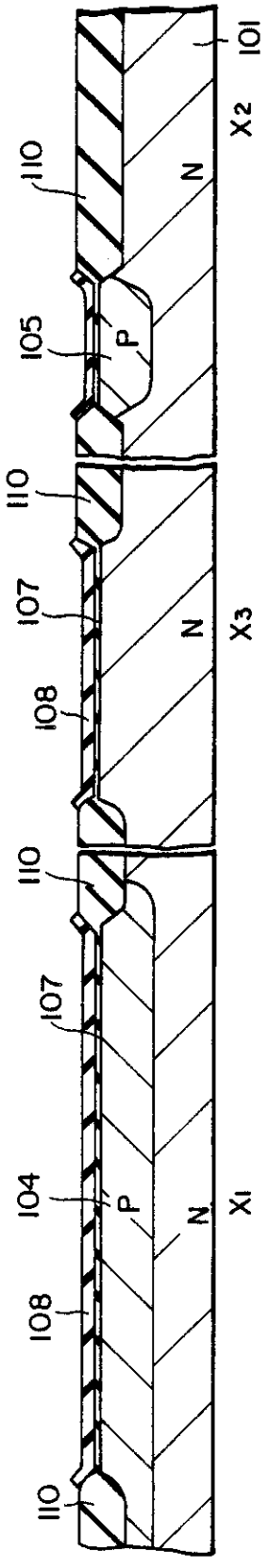


FIG. 8E

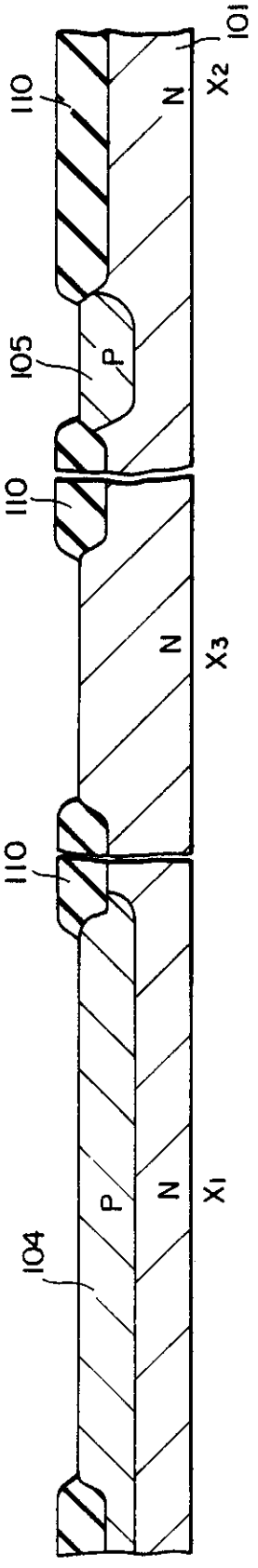


FIG. 8F

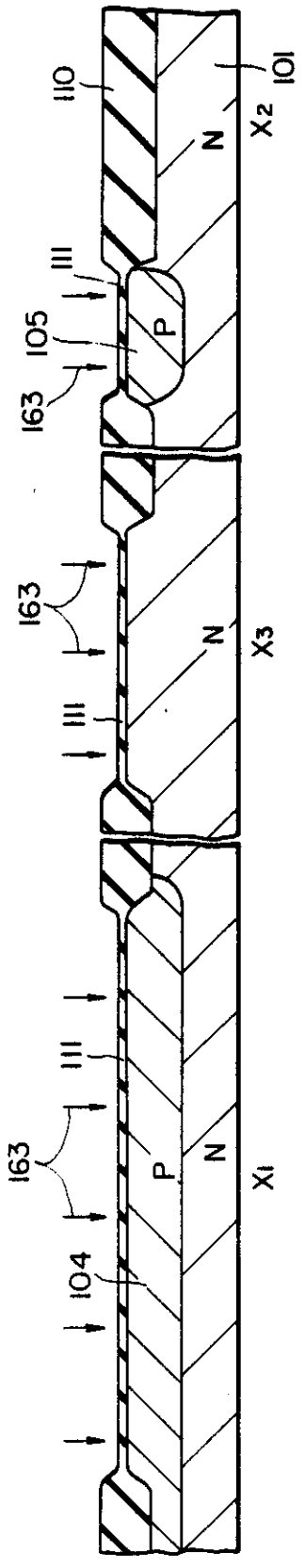


FIG. 8G

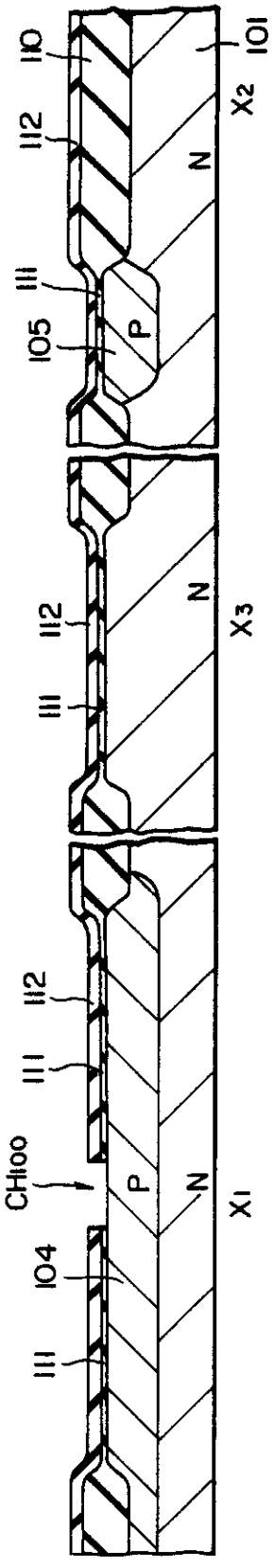


FIG. 8H

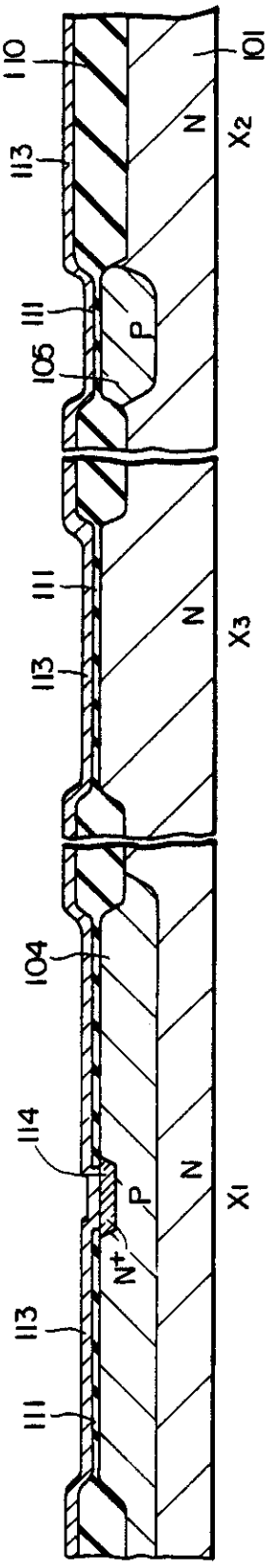


FIG. 8I

FIG. 8J

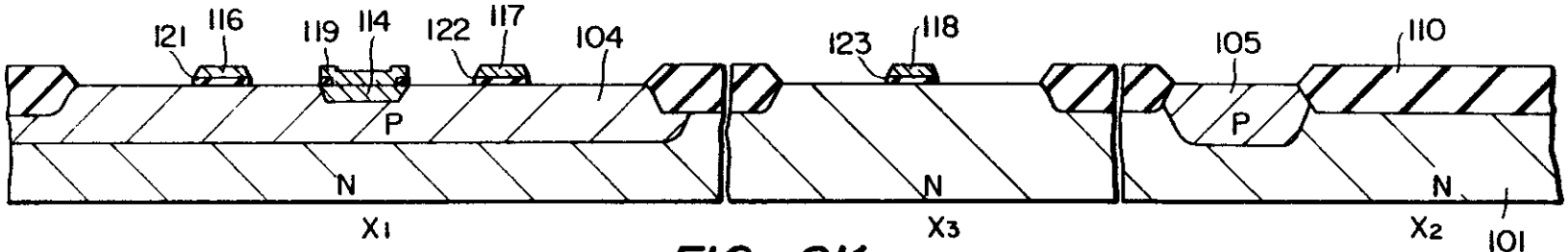


FIG. 8K

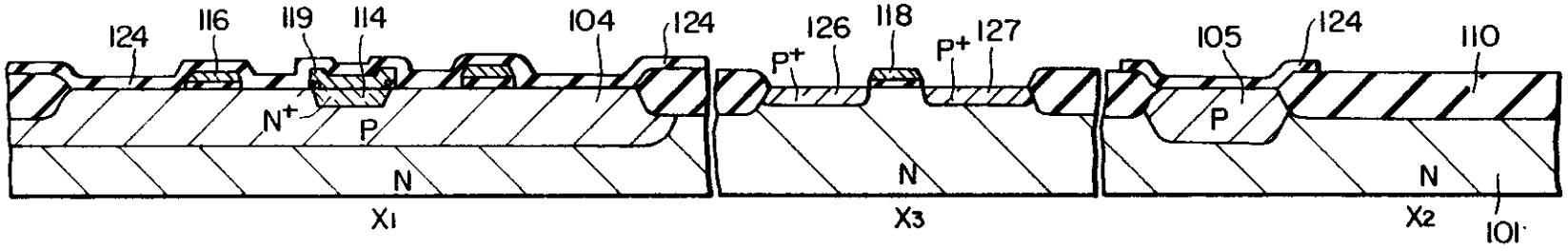


FIG. 8L

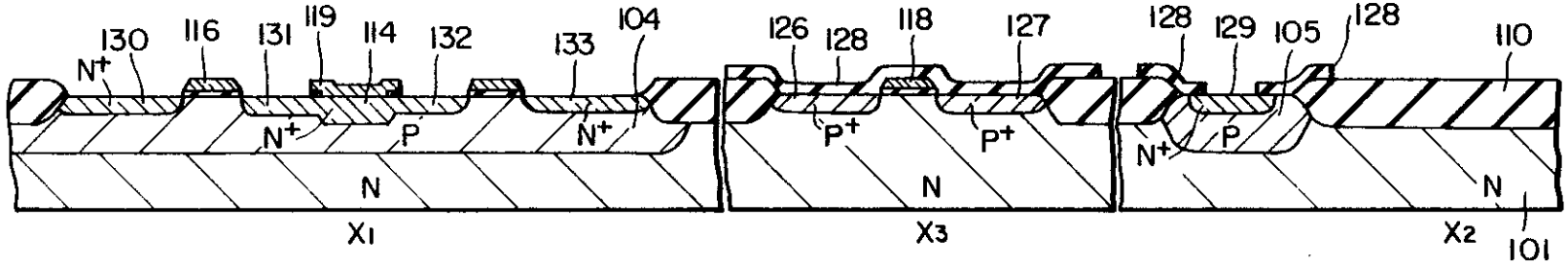


FIG. 8M

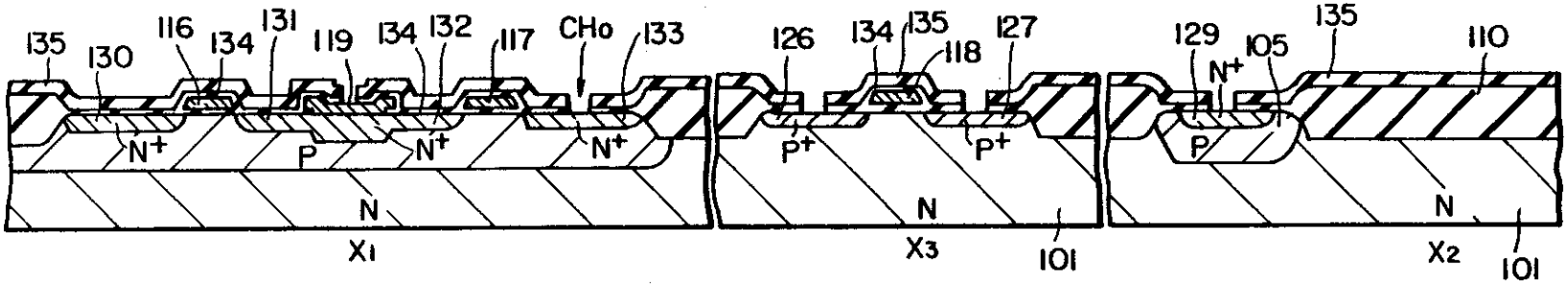


FIG. 8N

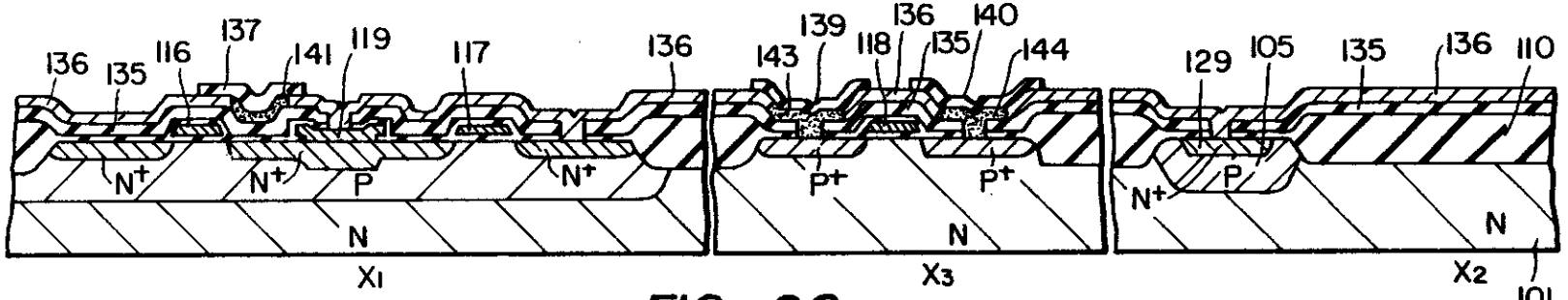
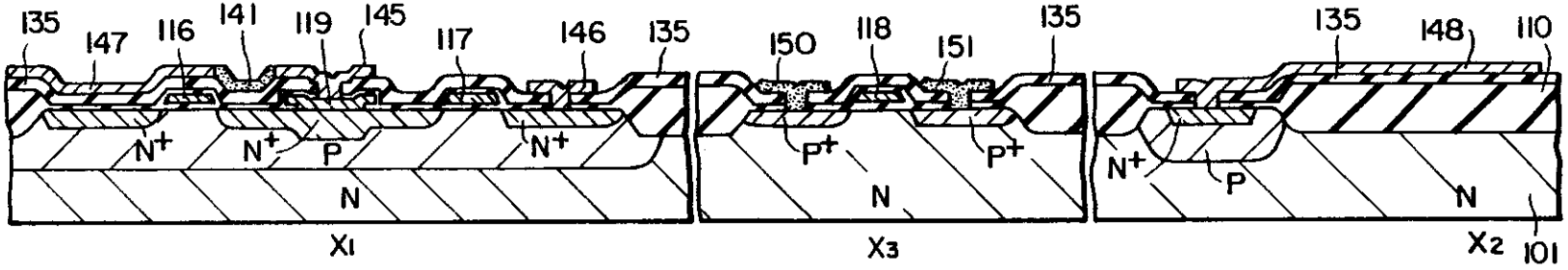
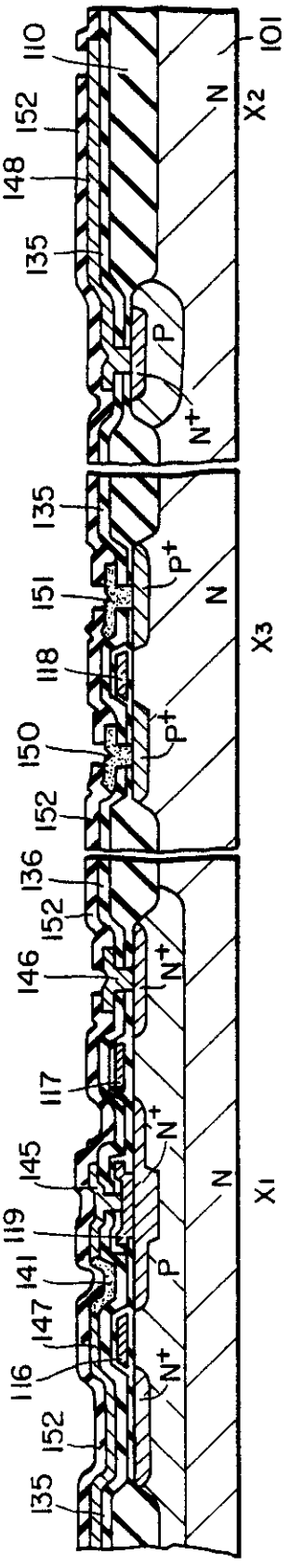


FIG. 8O




110
101
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X2
148
135
P
N+
135
P+
151
N
X3
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P+
150
152
136
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146
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N+
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N
X1
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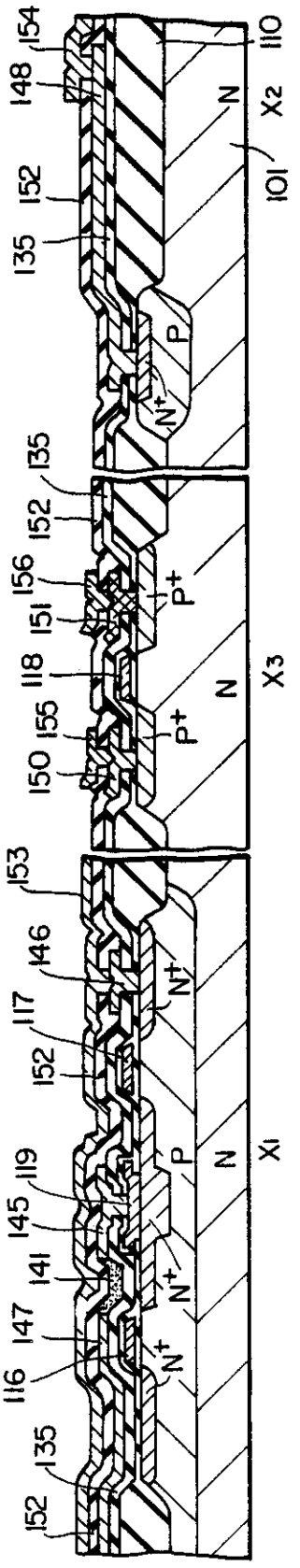
N+
116
152
135

FIG. 8P


154
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150
153
146
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N+
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152

FIG. 8Q

FIG. 9A

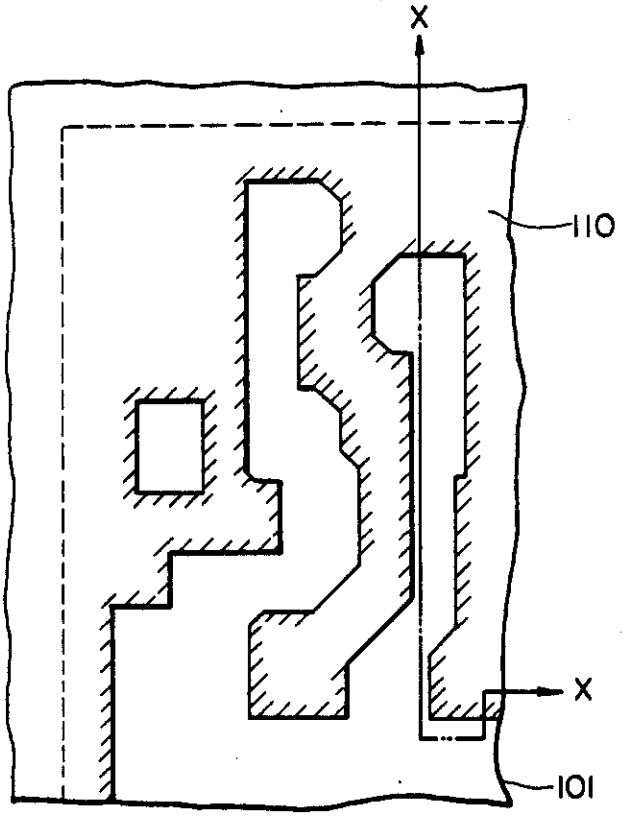


FIG. 9B

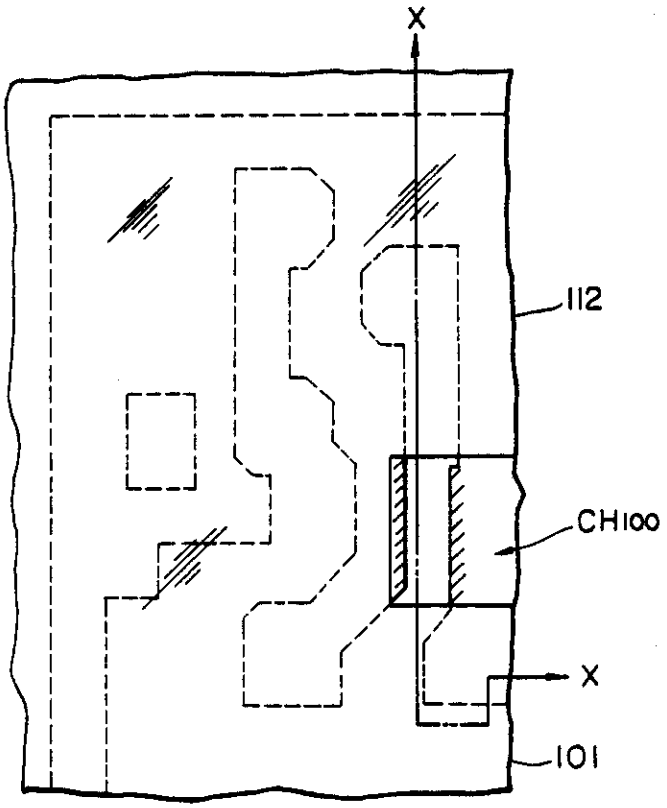


FIG. 9C

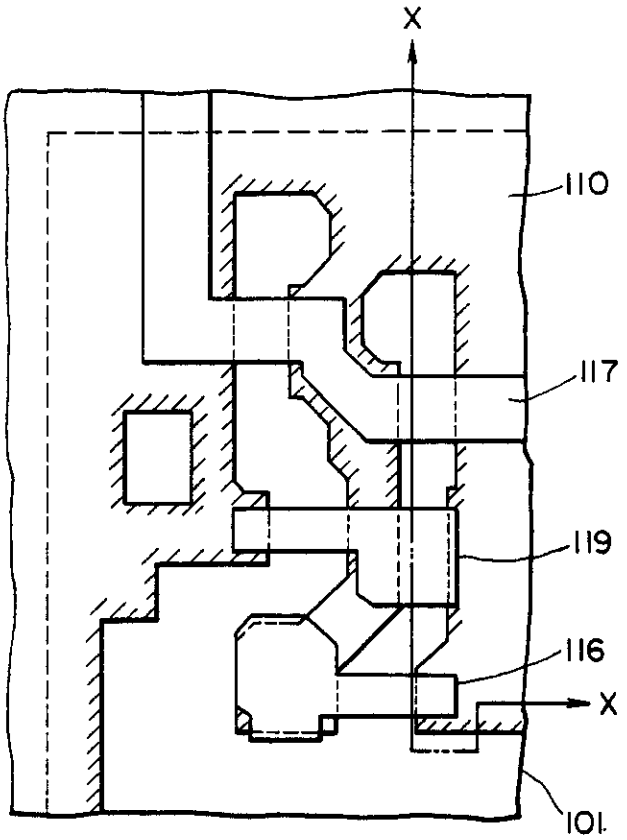


FIG. 9D

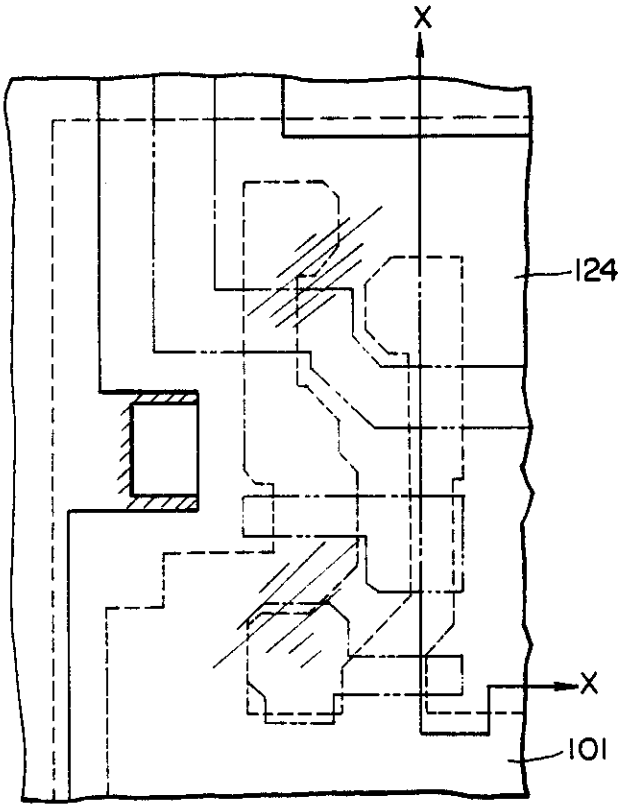


FIG. 9E

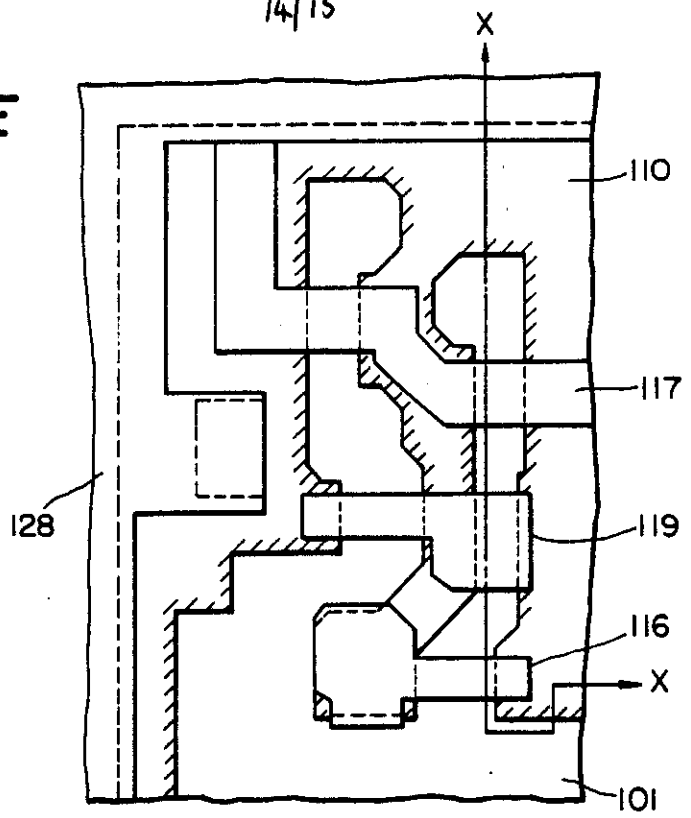


FIG. 9F

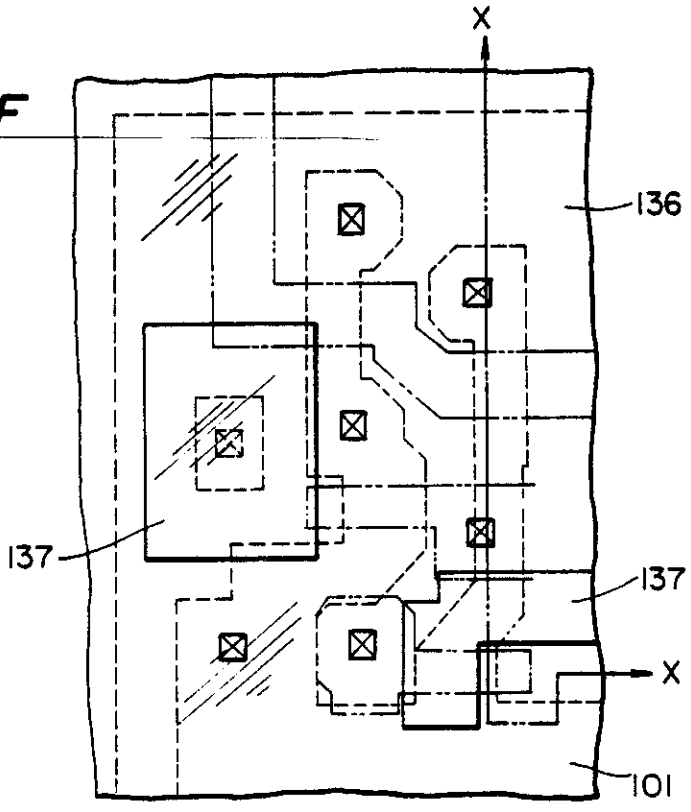


FIG. 9G

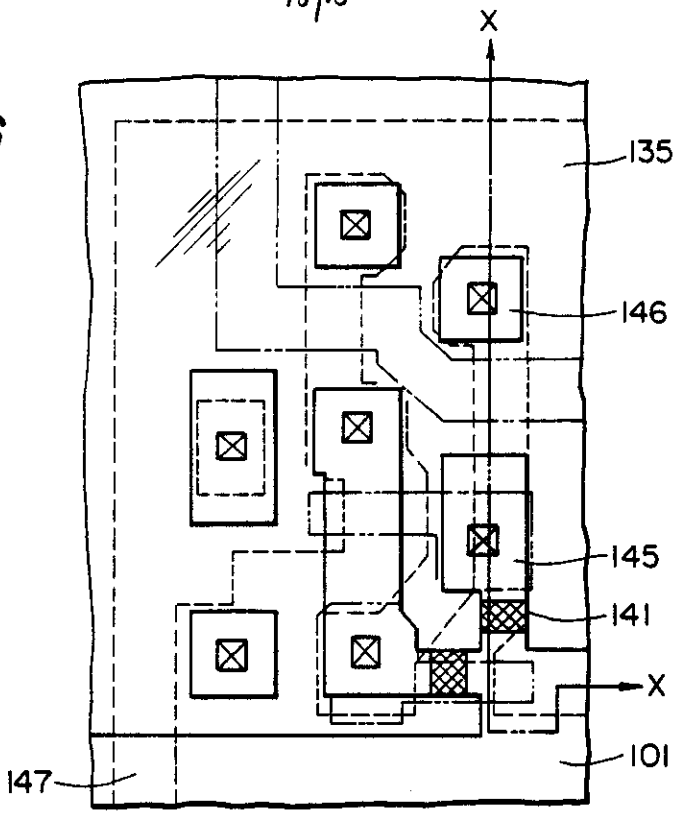
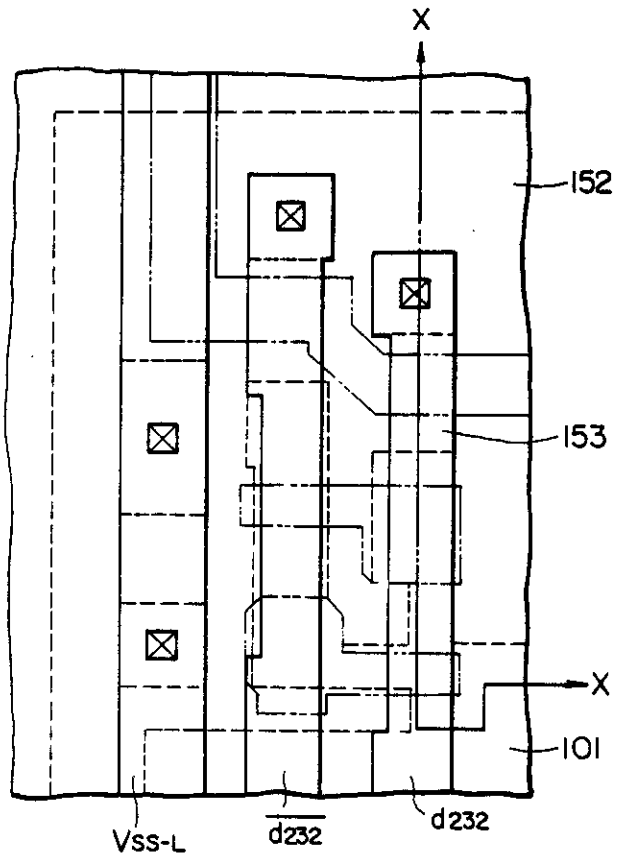


FIG. 9H



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Semiconductor Memory Device and Fabrication Process Thereof

The present invention relates to a semiconductor memory device and, more particularly, to a static RAM (i.e., Random Access Memory), which is composed of MIS (i.e., Metal Insulator Semiconductor) type field effect transistors (which will be referred to as "MISFETs") and a fabrication process thereof.

In a MIS type semiconductor integrated circuit device (which will be referred to as an "IC"), an input protection circuit composed of a resistor and a diode may be connected between an input terminal and a gate so as to protect the gate of a MISFET which is to be fed with a signal coming from the outside of the IC. It is conceivable to use a diffusion resistor, which is prepared in a semiconductor wafer by the diffusion technique, as that input protection resistor. According to out investigations, however, it has been found that, where a C-MOS is used in the peripheral circuit unit other than the memory cells of the aforementioned

static RAM, such a diffusion resistor is always formed with a PN junction so that the latch-up phenomenon takes place. In order to prevent this phenomenon, we have conceived to use a polycrystalline silicon film (which will be referred to as a "poly Si film"), which is formed over the field oxide film of the semiconductor wafer, as the input protection resistor. As a forming method of this input protection resistor, we have also conceived to use a poly-Si film formed simultaneously with the poly-Si gate electrodes of the MISFETs of the peripheral circuit unit, the poly-Si gate electrodes of the MISFETs in the memory cells and the poly-Si word lines in the memory cells. In this case, however, in order to shorten the propagation delay time of the signals at the gates and the word lines, the aforementioned poly-Si film has to be doped with phosphorus to have its specific resistance lowered (to 30 Ω/□, for example). In order to have the desired resistivity (about 2 KΩ) required of the input protection resistor, therefore, it is necessary to enlarge the wiring length of the poly-Si film. As a result, it has also been found that the area occupied by the protection resistor is enlarged, increasing the chip size, which is undesirable for the improvement of integration.

According to the present invention there is provided a memory device comprising a semiconductor integrated circuit device which comprises: (a) a multiplicity of memory

cells, each including a pair of driver MIS transistors series connected to respective load devices, and first conductive means for connecting each load device to a power supply; and (b) a multiplicity of peripheral circuits associated with the memory cells, said circuits including MIS transistors at least one of which has a gate connected with a protection resistor; and wherein said load devices and first conductive means are formed in a first strip which is formed from a single polycrystalline silicon layer, the portions constituting the load devices being of greater resistivity than the portions constituting the conductive means; and the or at least one said protection resistor is formed in a second strip which is formed from the single polycrystalline silicon layer whose resistivity is substantially equal to that of said conductive means portions.

In a second aspect the invention provides a fabrication process for such a memory device.

Preferred embodiments of the present invention enable one: to provide a static RAM of such a high integration that the area occupied by an input protection resistor is reduced; and to provide a fabrication process which can fabricate the aforementioned static RAM without any difficulty, preferably without any change in the existing fabrication process.

An embodiment of the present invention will now be described in greater detail with reference to the accompanying drawings, in which:

Fig. 1 is a schematic layout showing a static RAMIC embodying the present invention;

Fig. 2 is an equivalent circuit diagram showing the peripheral circuit unit of the static RAMIC shown in Fig. 1;

Fig. 3 is an enlarged top plan view showing a portion of the peripheral circuit unit shown in Fig. 2;

Fig. 4 is a section taken along line X - X of Fig. 3;

Fig. 5 is an equivalent circuit diagram showing a memory cell of the static RAMIC shown in Fig. 1;

Fig. 6 is an enlarged top plan view showing the memory cell shown in Fig. 5;

Fig. 7 is a schematic layout showing the overall memory array of the static RAMIC shown in Fig. 1;

Figs. 8A to 8Q are sectional views showing sequentially the steps of a fabrication process of fabricating the static RAMIC embodying the present invention; and

Figs 9A to 9H are top plan views showing the memory cell in accordance with the fabrication process shown in Figs. 8A to 8Q.

First of all, the top plan layout pattern of a static RAMIC according to an embodiment of the present invention will be described with reference to Fig. 1.

This RAMIC is made to have the so-called "four mat type layout pattern", in which four memory arrays are arranged in a single IC chip such that there are separately arranged in the IC chip four memory arrays $M\text{-}ARY_1$, $M\text{-}ARY_2$, $M\text{-}ARY_3$ and $M\text{-}ARY_4$ which are composed of a plurality of memory cells (M-CELs). The memory arrays $M\text{-}ARY_1$ and $M\text{-}ARY_2$ are arranged at one side of the IC chip whereas the memory arrays $M\text{-}ARY_3$ and $M\text{-}ARY_4$ are arranged at the other side, and a row decoder R-DCR for the memory arrays $M\text{-}ARY_1$ to $M\text{-}ARY_4$ is arranged at the center portion of the IC chip, which is sandwiched between the side portions. Between the memory array $M\text{-}ARY_2$ and the row decoder R-DCR and between the memory array $M\text{-}ARY_3$ and the row decoder R-DCR, moreover, there are arranged word drivers WD_1 and WD_2 for the memory arrays $M\text{-}ARY_1$ to $M\text{-}ARY_4$. In contact with one-side terminals of the memory arrays $M\text{-}ARY_1$

to M-ARY$_4$, there are arranged column switches C-SW$_1$, C-SW$_2$, C-SW$_3$ and C-SW$_4$ for those memory arrays M-ARY$_1$ to M-ARY$_4$, respectively. In contact with the column switches C-SW$_1$ to C-SW$_4$, moreover, there are arranged column decoders C-DCR$_1$, C-DCR$_2$, C-DCR$_3$ and C-DCR$_4$ for the memory arrays M-ARY$_1$ to M-ARY$_4$, respectively. In contact with those decoders, on the other hand, there are arranged sense amplifiers SA$_1$, SA$_2$, SA$_3$ and SA$_4$ for the memory arrays M-ARY$_1$ to M-ARY$_4$, respectively. Adjacent to the sense amplifiers SA$_1$ to SA$_4$, there are arranged address buffers ADB$_{2-1}$ and ADB$_{2-2}$ for address signals A_4 to A_{10}. A data output buffer DOB is arranged adjacent to the address buffer ADB$_{2-1}$, and a $\overline{WE}$ signal input buffer $\overline{WE}$-B, a $\overline{CS}$ signal input buffer $\overline{CS}$-B and a data input buffer DIB are arranged adjacent to the address buffer ADB$_{2-2}$. Along one end portion of the IC chip, there are arranged address signal impression pads P-A_5 and P-A_6, a data signal take-out pad P-D_{out}, a $\overline{WE}$ signal impression pad P-$\overline{WE}$, an earth potential connection pad P-GND, a $\overline{CS}$ signal impression pad P-$\overline{CS}$, a data signal input pad P-D_{in}, and address signal impression pads P-A_7, P-A_8 and P-A_9. In contact with the other terminal side of the memory arrays M-ARY$_1$ to M-ARY$_4$, on the other hand, there are arranged load circuits DLC$_1$, DLC$_2$, DLC$_3$ and DLC$_4$ for the data lines, respectively. Adjacent to the left and right sides of those MISFETs, there are arranged address buffers ADB$_{3-1}$ and ADB$_{3-2}$ for address signals A_0 to A_3,

A_{12} and A_{13}. Adjacent to those address buffers ADB_3, moreover, there are arranged along the periphery of the IC chip address signal impression pads $P\text{-}A_4$, $P\text{-}A_3$, $P\text{-}A_2$, $P\text{-}A_1$ and $P\text{-}A_0$, a V_{CC} voltage supply pad $P\text{-}V_{CC}$, and address signal impression pads $P\text{-}A_{13}$, $P\text{-}A_{12}$, $P\text{-}A_{11}$ and $P\text{-}A_{10}$.

In the RAMIC thus constructed, the input protection circuit and the peripheral circuit are constructed as shown in Figs. 2 to 4.

In Fig. 2, An external input terminal V_{IN} to be fed with a signal from the outside of the RAMIC corresponds to one of the address signal impression pads $P\text{-}A_0$ to $P\text{-}A_{13}$ and the other input signal impression pads $P\text{-}\overline{WE}$, $P\text{-}\overline{CS}$ and $P\text{-}D_{in}$. That input terminal V_{IN} is connected with each gate of the C-MOS inverter of the peripheral circuit through a polycrystalline silicon input protection resistor R_{IN} which has the same resistivity as that of a later-described second (or overlying) poly-Si film. That C-MOS inverter is composed of a P-channel MISFET Q_{10} and an N-channel MISFET Q_{11} and forms a part of the address buffer ADB, for example, of Fig. 1. An output V_{out} is commonly taken out of the drains of those two MISFETs and is fed (e.g.) to a subsequent inverter. The MISFET Q_{10} has its source fed with a power source voltage V_{CC} from a power source, which is connected with the voltage supply pad $P\text{-}V_{CC}$ of Fig. 1, whereas the other MISFET Q_{11} has its

source fixed at the earth potential or a reference potential (V_{SS}). Reference letter D indicates an input protection diode for clamping an abnormal excessive voltage, which is provided to prevent the gate oxide films of the MISFETs Q_{10} and Q_{11} from being broken by the excessive voltage. The input protection resistor R_{IN} forms part of a time constant circuit together with the wiring capacity. This is provided to delay the rising characteristics of the abnormally excessive voltage, which has a smaller rising equivalent time constant than the equivalent time constant of the diode D and which is to be impressed upon the protection diode, when that excessive voltage is impressed. In other words, the input protection resistor R_{IN} is provided to make gentler the rising waveform of the abnormally excessive voltage which is impressed upon the input terminal V_{IN}.

The circuit thus constructed at the input side is formed to have such a layout as is schematically shown in Fig. 3, and especially the input protection circuit is shown in section in Fig. 4. Over an N-type silicon substrate 1, there is formed a thick field oxide film 2 for element separation, which is used as a mask to form a P-type semiconductor region 3 by the diffusion technique. Moreover, that region 3 is provided with an N-type semiconductor region 4 by the diffusion technique using a thin oxide film 5 as a mask. Those two regions 3 and 4 construct together

the protection diode D shown in Fig. 2. Reference numeral 6 indicates a SiO_2 film which is prepared by the chemical vapor deposition (i.e. CVD). A poly-Si film 7 providing the aforementioned input protection resistor R_{IN} is formed over to extend from the N^+-type region 4 to the SiO_2 region 6 through contact holes which are formed in the SiO_2 films 5 and 6. That poly-Si film 7 is made to grow at the same step as that of the later-described second (i.e., overlying) poly-Si layer and is doped with an impurity so as to have a specific resistance of 150Ω/□, so that it may have a higher resistivity than a first poly-Si film 16 which forms the gate electrodes of the MISFETs Q_{10} and Q_{11}. Numeral 8 indicates a phosphorous silicate glass film, and numeral 9 indicates an aluminum wiring which is connected with the external input terminal V_{IN} of Fig. 2. The P-type region 3 is grounded to the earth through an earth potential connection line 20, whereas the N^+-type region 4 is connected with the respective gates of the MISFETs Q_{10} and Q_{11}, which construct the aforementioned C-MOS inverter, by aluminum wiring 21; and to the later-described C-MOS inverter (as indicated here at 16). In this C-MOS inverter, numerals 10 and 11 indicate the P^+-type source and drain regions of the MISFET Q_{10}, respectively, and numerals 12 and 13 indicate the N^+-type drain and source regions of the MISFET Q_{11}, respectively. Moreover: numeral 14 indicates a P-type well region at the

N-channel side; numeral 15 a contact N^+-type region for biasing the substrate; numeral 17 a V_{CC} voltage supply line of aluminum; numeral 18 an output line of aluminum; numeral 19 an earth potential connection line of aluminum; and numeral 21 a bonding pad which corresponds to the external input terminal V_{IN} of Fig. 2.

In the input protection circuit and the peripheral circuit thus far described, it is desirable that especially the input protection resistor R_{IN} (or 7) is made of the second (or overlying) poly-Si film and set at such a desired value (about 2 KΩ, for example) as to effect the aforementioned operations. For that reason, the poly-Si film 7 has phosphorus diffused therein so that it may have a sheet resistance such as 150 Ω/□ similarly to the wiring portion of the second poly-Si film of the later-described memory cell, so as to have a lower resistivity than that in the memory cell. As a result, the poly-Si film 7 exhibits a relatively high sheet resistivity suitable for attaining the desired resistance of 2KΩ while occupying a relatively small area, as shown in Fig. 3. Incidentally, that input protection resistor can be formed in a straight line, as is indicated by a chain-dotted line in Fig. 3. From the standpoint of the area reduction, the input protection resistor 7 is required to have a suitably high specific resistance, and a low enough resistance for it not to block the input

signal. For this requirement, it is advantageous that the overall resistance of the input protection resistor 7 can be set at 1 to 2 KΩ while having its sheet resistivity of the aforementioned value of about 150 Ω/□. In the peripheral C-MOS circuit, on the other hand, the polycrystalline silicon wiring 16 to be used as the gate is required to have such a low resistance as to shorten the signal transmission time and, accordingly, the access time, for example, a sheet resistance of 30 Ω/□. Nevertheless, that poly-Si film can be formed simultaneously with the first poly-Si film which serves as the gate electrode of the MISFET of the later-described memory cell.

Fig. 5 shows the circuit of the memory cell in one bit of the static RAM shown in Fig. 1.

This memory cell is composed of: a flip-flop, which comprises the inputs and outputs of a pair of inverter circuits each composed of a load resistor and a driver transistor connected in series; and a pair of transmission gate MISFETs Q_3 and Q_4. The paired inverter circuits are composed of a first inverter, which has a load resistor R_1 and a driver MISFET Q_1 connected in series, and a second inverter which has a load resistor R_2 and a driver MISFET Q_2 connected in series. The load resistors R_1 and R_2 have their one-side terminals fed with the voltage V_{CC} through a wiring ℓ, whereas the driver MISFETs Q_1 and Q_2 have their

source terminals grounded to earth. Moreover, the output of the first inverter is fed to the gate terminal of the MISFET Q_2 of the second inverter, whereas the output of the second inverter is fed to the gate terminal of the MISFET Q_1 of the first inverter. The flip-flop having the construction thus far described is used as information memory means. Moreover, the output of the first inverter is connected through the MISFET Q_3 with a data line D, whereas the output of the second inverter is connected through the MISFET Q_4 with a data line $\overline{D}$. In other words, the transmission gate is used as address means for controlling the information transmission between the flip-flop and the complementary data line couple D and $\overline{D}$ and has its operations controlled by the address signal which is to be impressed upon a word line W.

Next, the layout pattern of the memory cell M-CEL of one bit will be described with reference to Fig. 6.

In Fig. 6, the section within the rectangle ABCD is a region which is occupied by the memory cell M-CEL of one bit. Broken lines indicate a thick field insulation film 110 made of SiO_2 and having the form shown in Fig. 9A. Single-dotted lines indicate a polycrystalline silicon layer (i.e., a poly-Si layer). Especially, the regions, which are enclosed by the single-dotted lines but not shaded, indicate first poly-Si layers 117,

119 and 116 and have the patterns shown in Fig. 9C. The shaded regions indicate a second poly-Si layer 147 and a second poly-Si layer over contact holes CH_0, CH_2, CH_5 and CH_6 and have the patterns shown in Fig. 9G. Double-dotted lines indicate a memory array M-ARY which is composed of a plurality of memory cells. This memory array M-ARY is a P-type well region which is formed in the N-type semiconductor substrate. Letters D, $\overline{D}$ and V_{SS}-L indicate wiring layers made of aluminum. Among these, more specifically, the letters D and $\overline{D}$ indicate the complementary data line couple shown in Fig. 5, and letters V_{SS}-L indicate the earth potential supply line.

Contact holes CH_0, CH_2 and CH_6 are provided to connect the wiring layers D, $\overline{D}$ and V_{SS}-L with the N^+-type drain region of the MISFET Q_4, the N^+-type drain region of the MISFET Q_3 and the N^+-type source region shared between the MISFETs Q_1 and Q_2, respectively. The second poly-Si layer is sandwiched between those aluminum wiring layers and the N^+-type semiconductor regions. The contact hole CH_5 is provided to connect the P-type well regions of the wiring layer V_{SS}-L and the memory array M-ARY while sandwiching the second poly-Si layer inbetween. The contact holes CH_1, CH_3 and CH_4 are provided to connect the second poly-Si layer 147 with the first poly-Si layer 119, the N^+-type region, which is shared between the drain region of the MISFET Q_1 and the source region

of the MISFET Q_3, and the first poly-Si layer 116, respectively.

Next, the relationships among the aforementioned respective regions will be described with reference to Fig. 6.

First of all, the second poly-Si layer 147 extends at the lower lefthand side of the drawing and is connected with the power source voltage supply line V_{CC}-L outside of the memory array M-ARY, as shown in Fig. 7. The power source voltage V_{CC} impressed upon the second poly-Si layer 147 by the aforementioned means is impressed through the higher resistor, which is made of polycrystalline silicon having a higher resistivity, upon the source of the MISFET Q_4, the drain of the MISFET Q_2 and the gate electrode of the MISFET Q_1. In other words, the second poly-Si layer 147 is connected through the contact hole CH_1 with the first poly-Si layer 119, which contacts in the so-called "direct" manner with the N^+-type semiconductor region shared between the source of the MISFET Q_4 and the drain of the MISFET Q_2. On the other hand, the aforementioned first poly-Si layer 119 serves as the gate electrode of the MISFET Q_1, too, as is apparent from Figs. 5 and 6. The drain of the MISFET Q_4 is connected through the contact hole CH_0 with the data line D. Moreover, the aforementioned second poly-Si layer 147 is connected through the other higher resistor R_1, which is made of polycrystalline silicon having a higher resistivity, with the drain of the MISFET Q_1, the source of the MISFET Q_3 and the

gate electrode of the MISFET Q_2, all of which are shown in Fig. 6. In other words, the second poly-Si layer 147 is connected through the contact hole CH_4 with the first poly-Si layer 116 acting as the gate electrode of the MISFET Q_2 and further through the contact hole CH_3 with the N^+-type semiconductor region which is shared between the drain of the MISFET Q_1 and the source of the MISFET Q_3. Moreover, the drain of the MISFET Q_3 is connected through the contact hole CH_2 with the data line $\overline{D}$. The gate electrodes of the MISFETs Q_3 and Q_4 are made of the first poly-Si layer 117, which acts as the word line W shown in Fig. 1, too. This word line W is arranged to intersect the data lines at a right angle. The source regions of the MISFETs Q_1 and Q_2 merge into each other below the rectangle ABCD which contains the memory cell of one bit, and share their N^+-type region inbetween. Moreover, this N^+-region further extends to the right of and below the outside of the rectangle ABCD, and merges into the N^+-type region which provides the sources of the MISFETs Q_1 and Q_2 of the adjoining memory cells. On the other hand, the wiring line V_{SS}-L is disposed at the left hand side of the memory cell, along one side of the memory array M-ARY and in parallel with the data lines. That wiring line V_{SS}-L is connected through the contact hole CH_5 with the P-type well. As a result, this P-type well is grounded to the earth. The

second poly-Si layer exists between the wiring layer V_{SS}-L and the P-type well. On the other hand, that wiring layer V_{SS}-L is connected through the contact hole CH_6 with the aforementioned N^+-type region which extends to the lefthand side of the memory cell. As a result, this N^+-region is grounded to the earth. The second poly-Si layer exists between the wiring layer V_{SS}-L and the N^+-type region. This N^+-type region merges into the N^+-type region which provides the sources of the MISFETs Q_1 and Q_2 of the adjoining memory cells, as has been described hereinbefore. As a result, if that N^+-type region is connected with the wiring region V_{SS}-L in at least one position so that it is grounded to the earth, it becomes necessary to form the wiring layer for supplying the earth potential to those respective memory cells sharing that N^+-type region inbetween. In other words, by grounding that N^+-type region to the earth, the source regions of the MISFETs Q_1 and Q_2 of the respective memory cells sharing that N^+-type region are grounded to the earth so that the earth potential supply lines for the respective memory cells can be dispensed with.

The overall layout of the memory array will be schematically described in the following with reference to Fig. 7.

Each memory array is arranged with a line (in the direction of the word line) of thirty two sections (i.e., the memory cells of one bit), which are enclosed by the

rectangle ABCD shown in Fig. 6, and with a row (in the direction of the data lines) of one hundred and twenty eight sections. First of all, the layout pattern providing a basis for the memory array construction is formed in accordance with the layout pattern of the memory cell of one bit shown in Fig. 6. This basic layout pattern is composed of four memory cells M_1 to M_4 of one bit, which are arranged as is shown in Fig. 7. The reference M_1 indicates a memory cell having the same layout pattern as that of the memory cell of one bit shown in Fig. 6. M_2 indicates a memory cell having such a layout pattern as is axisymmetric to the memory cell M_1 with respect to the side BC. M_3 indicates the memory cell having such a layout pattern as is centrally symmetric to the memory cell M_2 with respect to the point C (or D). M_4 indicates a memory cell having such a layout pattern as is axisymmetric to the memory cell M_3 with respect to the side DA. The basic layout pattern is so constructed that those memory cells M_1 to M_4 are arranged continuously without any spacing, as shown in Fig. 7. Moreover, a memory array is constructed by arranging those basic layout patterns continuously without any spacing. More specifically, the memory array is constructed with sixteen basic layout patterns in a line and sixty four basic layout patterns in a row, as shown in Fig. 7. From the description thus far made, it is understood that the N^+-type

semiconductor region, which provides the source regions of the MISFETs Q_1 and Q_2 shown in Fig. 6, and the first poly-Si layer are shared among the four memory cells M_1 to M_4 and among the sixteen basic layout patterns which are arranged in the line.

Other than the regular layout thus far described, two wiring layers V_{SS}-L are arranged at respective sides of the memory array. Below those two wiring layers V_{SS}-L, there extend from the adjoining memory cells, as shown in Fig. 6, the N^+-type regions which provide the source regions of the MISFETs Q_1 and Q_2 and which are connected with each other through the contact hole CH_6. As a result, those N^+-type regions are grounded to the earth. Thus this N^+-region is common to the sixteen basic layout patterns which are arranged in the common line, as has been described hereinbefore, so that the source regions of the MISFETs Q_1 and Q_2 of the memory cells of sixty four bits in the sixteen basic layout patterns are grounded to the earth. As a result, it becomes unnecessary to form special wiring layers for supplying the ground potential to the memory cells of sixty four bits.

Outside of the memory array, two wiring layers V_{CC}-L are arranged in parallel with the wiring layers V_{SS}-L. Below those two wiring layers V_{CC}-L, there extend from the adjoining memory cells, respectively, the second poly-Si layers 147 which merge into each other through the wiring layers V_{CC}-L

and the contact hole CH_7, as shown in Fig. 6. As a result, that second poly-Si layer 147 thus merging is fed with the voltage V_{CC}. This second poly-Si layer 147 is shared among the sixteen basic layout patterns, which are arranged in the common line, as has been described hereinbefore, so that the memory cells of sixty four bits therein are fed with the voltage V_{CC}.

As has been described hereinbefore, the static RAMIC according to the present embodiment is characterized in that the input protection resistor R_{IN} (or 7) of the peripheral portion is made of the poly-Si film which has the same resistivity (suitably a sheet resistance of 150 Ω/□) as that of the poly-Si wiring ℓ (i.e., the second poly-Si layer 147) merging into the load resistors of the memory cell. We have found that the load resistors R_1 and R_2 of the memory cell can have a remarkably high resistance (e.g., 10^7 to 10^{10}Ω) and have found that there arises no problem in the operation of the memory cell even if the resistance of the wiring ℓ between the load resistors and the power source voltage V_{CC} is enlarged somewhat. Therefore, the requirement that the input protection resistor R_{IN} be made to have the desired resistance can be ingeniously met by using the wiring ℓ of the aforementioned load resistors. More specifically, the first poly-Si film of the memory cell is doped with an impurity at high concentration, until

it has such a low resistivity as, e.g. to have a sheet resistance of 30 Ω/□, so that it may be used as the gate and the word line. Therefore, the aforementioned increase in the occupied area cannot be avoided if that poly-Si film is used as the input protection resistor. In the present embodiment, however, the second poly-Si film of the memory cell, which is left undoped with phosphorus has a sheet resistance of 10^8 to 10^{11} Ω/□, which is sufficient that the poly-Si film can be used as it is as the load resistor in the memory cell. On the other hand, that wiring ℓ (i.e., the second poly-Si film doped with phosphorus has a relatively low resistance of 150 Ω/□ but exhibits such a suitable sheet resistivity that it is used as the input protection resistor. As a result, if the second poly-Si film 147 of that wiring portion is used as the input protection resistor R_{IN}, the specific resistance is about five times as high as use of the first poly-Si film would give, and the input signal is not blocked. As a result, the area occupied by the input protection resistor can be reduced to about one fifth so that the chip size can be reduced to enhance the integration density.

The input protection resistor according to the present embodiment is prepared simultaneously with the second poly-Si layer of the memory cell. The fabrication process of the aforementioned static RAM will be described with reference to Figs. 8A to 8Q. In each of these Figures:

region X_1 is a sectional view at the respective stage of the process, taken along line X - X of the memory cell M-CEL shown in Fig. 6; region X_2 is a sectional view at the respective stage, taken along line X - X of the input protection resistor shown in Fig. 3; and region X_3 is a sectional view at the respective stage, showing the P-channel MISFETs of the peripheral circuit of the memory cell.

First of all, a semiconductor substrate 101 is prepared, as shown in Fig. 8A. For example, an N-type single crystalline silicon substrate made of a (100) crystal is used as that semiconductor substrate. That substrate has a specific resistance of 8 to 12 Ωcm. An N-type impurity 160 is introduced into all the main face of that silicon substrate by ion implantation, for example. Phosphorus is preferred as that N-type impurity, and the implanting energy and the dose in that case are sufficient at 125 KeV and at 3×10^{12} atoms/cm^2, respectively. The implantation of the phosphorus into all the face is performed for following reason. That is to say, an N^+-type region is formed by implanting the N-type impurity in advance thereby to form a channel stopper for preventing any parasitic MISFET.

Next, as shown in Fig. 8B, an oxide film (i.e., a SiO_2 film) 102 having a thickness of about 500 Å is formed over the face of the silicon substrate 101 by the thermal oxidization.

Next, in order to remove the SiO_2 film 102 existing over the region where a well is to be formed, a photo resist film 103 is selectively formed over the SiO_2 film. This photo resist film 103 is used as a mask to etch the SiO_2 film. Next, under condition leaving the photo resist film 103, an impurity 161 is introduced to form the well. The impurity used was of P-type. Ion implantation is preferred as the introducing method. For example, boron (B) is preferred as that P-type impurity. In this case, the implantation energy of 75 KeV and the dose of 8×10^{12} atoms/cm^2 are sufficient. At this time, the boron fails to reach the silicon substrate 101 where the photo resist film 103 is left. On the other hand, the boron introduced into the silicon substrate 101 is sufficient to override the concentration of the phosphorus which has been implanted before into the whole face, thereby to form a P-type well.

Next, after the photo resist film 103 is removed, as shown in Fig. 8C, the P-type impurity, which has been selectively introduced into the silicon substrate 101, is thermally diffused at a temperature of about 1200 ^{o}C to form a well region 104 and a P-type region 105 which is to become the input protection diode shown in Fig. 4. At this time, a thin oxide film 106 is formed over the face of the silicon substrate 101. In the well region 104, there is formed the memory cell which is shown in Fig. 6.

Next, all the oxide film extending over the silicon substrate 101 shown in Fig. 8C is removed to expose the clean face of the silicon substrate 101 to the outside. As shown in Fig. 8D, an oxide film (e.g. a SiO_2 film) 107 having a thickness of about 500 Å is formed over the face of the silicon substrate 101. Over this oxide film 107, moreover, an insulation film (i.e., an oxidization resisting film), which is impermeable to oxygen, e.g., a Si_3N_4 film 108 is formed to have a thickness of about 1400 Å by chemical vapor deposition (i.e. CVD). The Si_3N_4 film 108 is used as a mask for selectively forming a later-described field insulation film. Incidentally, the aforementioned SiO_2 film 107 is formed for the following reason. That is to say, if the Si_3N_4 film 108 is formed directly over the silicon substrate 101, a crystal defect is established on the face of the silicon substrate 101 due to the thermal strain which is caused as a result of the difference in the coefficients of thermal expansion inbetween. The SiO_2 film 107 is formed in order to prevent that crystal defect. Next, in order to complete the maks for forming the later-described field insulation film, a photo resist film 109 is selectively formed over the Si_3N_4 film. More specifically, the photo resist film 109 is formed in the region other than that where the field insulation film is to be formed. Moreover, that photo resist film 109 is used as a mask to etch the Si_3N_4 film 108

by the plasma etching process of high precision thereby to form the mask for forming the field insulation film. Under conditions leaving the photo resist film 109, a P-type impurity 162 is introduced into the silicon substrate 101 so as to form a channel stopper. For example, ion implantation is used as the introducing process. In this case, the P-type impurity fails to reach the SiO_2 film 107 and the silicon substrate 101 at the region, where the photo resist film 109 is left, but goes into the silicon substrate 101 through the SiO_2 film 107 at the region where the face of the SiO_2 film 107 is exposed to the outside. Boron fluoride BF_2 is preferred as the aforementioned P-type impurity. The implantation energy of 30 KeV and the dose of 5×10^{13} atoms/cm^2 are sufficient. The boron ions implanted into the P-type well form a P^+-type region to provide the channel stopper. On the contrary, the boron ions implanted into the N-type silicon substrate 101 are overridden by the phosphorus, which has been implanted by the phosphorus implantation shown in Fig. 8A, i.e., by the N-type impurity. As a result, that region remains N-type, thereby to provide the N-type channel stopper.

Next, after the photo resist film 109 has been removed, as shown in Fig. 8E, the face of the silicon substrate 101 is selectively thermally oxidized in an oxidizing atmosphere at about 1000 ^{o}C to form the field insulation film 110 having a thickness of about 9500 Å. Since, at this time, the Si_3N_4

film 108 or the oxidization resisting film is impermeable to oxygen, the silicon underlying the Si_3N_4 film is left unoxidized. During this heat treatment, the aforementioned channel stopper is extended and diffused just below the field insulation film to form the channel stopper having a desired depth (although not shown).

Next, after the Si_3N_4 film 108 has been removed by the use of hot phosphoric acid (H_3PO_4), for example, the SiO_2 film 107 is removed from the face of the silicon substrate 101, as shown in Fig. 8F, so as to form a clean gate oxide film. For example, the whole face is thinly etched with the use of hydrofluoric acid (HF) to remove the SiO_2 film 107 thereby to expose the face of the silicon substrate 101 at a portion where the field insulation film 110 is not formed. The top plan view of the memory cell M-CEL under this condition is shown in Fig. 9A. In other words, the sectional view taken along line X - X of Fig. 9A is shown in the section X_1 of Fig. 8F.

Next, in an oxidizing atmosphere at about 1000 °C, the face of the silicon substrate shown in Fig. 8F is provided by thermal oxidization with a gate insulation film 111 having a thickness of about 400 Å, as shown in Fig. 8G. The gate insulation film 111 thus formed becomes the gate insulation film of all the MISFETs which are formed over the silicon substrate 101. Next, under this condition, the ion implantation

of a P-type impurity 163 is performed so as to regulate the threshold voltage V_{th} of all the MISFETs. Boron (B) is preferred as the aforementioned P-type impurity. The implantation energy of 30 KeV and the dose of 5.5×10^{11} atoms/cm^2 are sufficient. The dose affects the level of the threshold voltage V_{th}. The ion implantation is performed without the use of any mask but all over the face. As a result, all the N-channel MISFETs have an equal threshold voltage V_{tN} whereas all the P-channel MISFETs have an equal threshold voltage V_{tP}. Furthermore, the boron ions are implanted into the portion of the region X_3 in which the input protection diode is to be formed.

Next, as has been described with reference to Fig. 6, a photo resist film 112 is selectively formed over the SiO_2 film so as to form the contact holes, which are use to provide direct connection between the later-described first poly-Si layer and the silicon substrate 101, i.e., the so-called "direct contact holes". As shown in Fig. 8H, moreover, the SiO_2 film 111 to provide the gate insulation film is etched by using that photo resist film 112 as the mask to expose the face of the silicon substrate 101 to the outside, thereby to form a direct contact hole CH_{100}. This contact hole CH_{100} provides the connections between the MISFETs Q_1 and Q_2 and the poly-Si resistor R_2 having a high resistivity, all of which are shown in Fig. 5. The top plan view of the memory

cell M-CEL under this condition is shown in Fig. 9B. In other words, the sectional view taken along line X - X of Fig. 9B is shown in the region X_1 of Fig. 8H.

Next, after the photo resist film 112 has been removed, a first conductive layer 113 is formed all over the face, as shown in Fig. 8I. A poly-Si layer doped with an impurity is used as the first conductive layer. First of all, the first poly-Si layer 113 having a thickness of about 3500 Å is formed all over the face by the CVD method. Next, in order to lower the specific resistance of that first poly-Si layer 113, an N-type impurity such as phosphorus is introduced by the diffusion method. As a result, the resistance of the first poly-Si layer 113 is reduced to about 30 Ω/□. At this time, the phosphous is diffused from the first poly-Si layer 113 through the direct contact hole CH_{100} into the silicon substrate 101 thereby to form an N^+-type region 114. This N^+-type region is caused by a subsequent heat treatment to have a desired depth. The region 114 provides connection between the MISFETs Q_2 and Q_4 shown in Fig. 5.

Next, the first poly-Si layer 113, which has been doped with the phosphorus as has been described hereinbefore, is etched, as shown in Fig. 8J, to have a desired shape by the plasma etching process of high precision thereby to form the gate electrodes 116, 117 and 118 of the MISFETs and the first poly-Si layer 119 (which is in so-called "direct contact"

with the silicon substrate 101). Subsequently, the SiO_2 film 111 is etched in the same shape to form gate insulation films 121, 122 and 123. At this time, the face of the silicon substrate 101 is selectively exposed to the outside, as shown in Fig. 8J. The top plan view of the memory cell M-CEL under this condition is shown in Fig. 9C. In other words, the sectional view taken along line X - X of Fig. 9C is shown in the region X_1 of Fig. 8J.

Next, as shown in Fig. 8K, a mask is formed so as to form P^+-type source and drain regions. As this mask, for example, there is used a SiO_2 film 124 which is selectively formed to have a thickness of about 1500 Å by the CVD method. In other words, the regions, in which the N-channel MISFETs including the memory cell are to be formed, are covered with the SiO_2 film 124. Under this condition, moreover, a P-type impurity is introduced by the diffusion method, for example. Boron (B) is preferred as that P-type impurity. As shown in Fig. 8K, the boron is diffused to form the source and drain regions 126 and 127 of all the P-channel MISFETs. Incidentally, a thin oxide film (although not shown) is formed over the face of the silicon substrate 101 in accordance with the heat treatment during that diffusion. The top plan view of the memory cell M-CEL under that condition is shown in Fig. 9D. In other words the sectional view taken along line X - X of Fig. 9D is shown in the region X_1 of Fig. 8K. At this time,

a P^+-type region is formed for providing connection between the P-type well and the earth potential line V_{SS}-L, which are shown in Fig. 6.

Next, after the aforementioned SiO_2 film 124 and the thin oxide film have been removed, a mask 128 is newly formed, as shown in Fig. 8L, so as to form N^+-type source drain regions and emitter regions. An SiO_2 film 128, which is selectively formed to have a thickness of about 1500 Å by the CVD method, for example, is used as that mask. In other words, the regions formed with all the P-channel MISFETs are covered with the SiO_2 film 128. Moreover, an N-type impurity is introduced in the manner shown in Fig. 8L by the diffusion method, for example. Phosphorus is preferred as that N-type impurity. The phosphorus is diffused into the silicon substrate 101 to form both an N^+-type region 129 for forming the input protection diode shown in Fig. 4 and the source and drain regions of all the N-channel MISFETs. Incidentally, a thin oxide film (although not shown) is formed over the face of the silicon substrate 101 in accordance with the heat treatment during that diffusion. The top plan view of the memory cell M-CEL under that condition is shown in Fig. 9E. In other words, the sectional view taken along line X - X of Fig. 9E is shown in the region X_1 of Fig. 8L.

Next, after the aforementioned SiO_2 film 128 and the thin oxide film have been removed, as shown in Fig. 8M, all of

the face of the silicon substrate 101 that is exposed to the outside is thermally oxidized to form an oxide film 134. Since, at this time, the silicon substrate 101 and the poly-Si layers 116 to 119 have different oxidation rates, a SiO_2 film having a thickness of about 100 Å is formed over the silicon substrate whereas a SiO_2 film having a thickness of about 300 Å is formed over the poly-Si layers 116 to 120. Next, a SiO_2 film 135 having a thickness of about 1500 Å is newly formed all over the face by the CVD method. The SiO_2 film 135 thus formed is provided to ensure insulation between the silicon substrate and the later-described second conductive layer. Next, over the SiO_2 film 135, there is selectively formed a photo resist film (although not shown), which is used as a mask to continuously etch the SiO_2 film 135 and the SiO_2 film 134 thereby to form contact holes. These contact holes are provided to provide connection between the later-described second conductive layer and the first poly-Si layer 119 or the semiconductor region formed in the silicon substrate 101. Incidentally, the thickness of the SiO_2 film 134 is different at positions, i.e., about 300 Å over the poly-Si layers 116 to 119 but about 100 Å over the silicon substrate 101. It is, therefore, necessary to continue the etching operation until the SiO_2 film extending over the poly-Si layers 116 to 119 is completely etched. At this time, a mixture solution of HF + NH_4F is preferred as the etching liquid. This etching liquid

does not act upon silicon so that the silicon substrate 101 is never etched.

Next, as shown in Fig. 8N, a second conductive layer 136 is formed all over the face. A poly-Si layer doped with an impurity is used as the second conductive layer. First of all, the second poly-Si layer 136 is formed all over the face with a thickness of about 2000 Å by the CVD method. The second poly-Si layer 136 thus formed is used to provide connection between a third conductive layer and the semiconductor region in the silicon substrate 101 or the first poly-Si layer 119, as will be described hereinafter. Moreover, the second poly-Si layer 136 is also used to provide the power source voltage supply wiring and the high resistors R_1 and R_2, which are shown in Fig. 5.

Next, as shown in Fig. 8N, SiO_2 films 137, 139 and 140 having a thickness of about 1500 Å are selectively formed by the CVD method to partially cover the second poly-Si layer 136. Under this condition, for example, phosphorus is introduced by the diffusion method so as to reduce the specific resistivity of the second poly-Si layer 136. As a result, the resistance of the second poly-Si layer 136 is reduced to about 150 Ω/□. However, the phosphorus is not introduced into those portions of the second poly-Si layer, which are covered by the aforementioned SiO_2 films 137, 139 and 140. As a result, the polycrystalline silicon having a

high specific resistance (e.g., 10^{10} to 10^{11} Ω/□) is partially left. Incidentally, the phosphorus which has been diffused into the second poly-Si layer 136, is more or less diffused in the horizontal direction, but the SiO_2 films 137, 139 and 140 providing the mask are designed to take that horizontal diffusion into consideration. A second poly-Si layer 141 having a high resistivity, which is covered with the SiO_2 film 137, is used as the high resistor R_2 shown in Fig. 5. Moreover, second poly-Si layers 143 and 144, which are covered with the SiO_2 films 139 and 140, are turned into P-type poly-Si layers having a low specific resistance when the P-type metal for forming a later-described third conductive layer is diffused when said third conductive layer is to be connected. The top plan view of the memory cell M-CEL under this condition is shown in Fig. 9F. In other words, the sectional view taken along line X - X of Fig. 9F is shown in the region X_1 of Fig. 8N.

Next, after the SiO_2 films 137, 139 and 140 have been removed, the second poly-Si layer 136 is etched to a desired shape to form electrodes 145, 146, 150 and 151 and the wiring layer 147 and an input protection resistor 148, as shown in Fig. 8O. The electrodes 150 and 151 are used for providing connections with the source and drain regions of all the P-channel MISFETs. The input protection resistor 148 is used as the resistor R_{IN} shown in Fig. 2. The electrode 146 is

used as the electrode of the MISFET Q_4 shown in Fig. 5. The wiring layer 147 is supplied with the power source voltage V_{CC}, as shown in Fig. 5, and is connected through the highly resistive poly-Si layer 141 (or R_2) with the first poly-Si layer 119 which is in so-called "direct contact" with the source and drain regions of the MISFETs Q_1 and Q_4. The top plan view of the memory cell M-CEL under this condition is shown in Fig. 9G. In other words, the sectional view taken along line X - X of Fig. 9G is shown in the region X_1 of Fig. 8O.

Next, as shown in Fig. 8P, an interlayer insulating film 152 is formed all over the face. A phosphorus silicate glass film is preferred as that interlay insulation film. This glass film 152 is formed to have a thickness of about 6500 Å by the CVD method. The glass film 152 thus formed is required as the interlayer insulation film between the later-described conductive layer and the second poly-Si layer. Next, a photo resist film (although not shown) is selectively formed and is used as a mask to etch the glass film 152 thereby to form contact holes.

Next, as shown in Fig. 8Q, third conductive layers 153 to 156 are selectively formed. For example, aluminum (Al), which is a P-type impurity to the silicon, is preferred those third conductive layers. The aluminum layers 153 to 156 are formed to have a thickness of about 8000 Å by vacuum evaporation. At this time, the aluminum is diffused

into the electrodes 150 and 151, which are made of the second poly-Si layer having a high resistivity, so that P-type conductive layers having a low specific resistance are formed. The electrode 153 is used as the data line shown in Fig. 5. The top plan view of the memory cell M-CEL under this condition is shown in Fig. 9H. In other words, the sectional view taken along line X - X of Fig. 9H is shown in the region X_1 of Fig. 8Q. Incidentally, Fig. 9H is essentially identical to Fig. 6.

As is now apparent from the steps thus far described, according to the present embodiment, the first poly-Si layer is doped with an impurity in high concentration to have a low resistivity thereby to provide the gate electrodes of the MISFETs and the word line. The second poly-Si layer is made to grow over the memory cell and simultaneously to form the input protection resistor film. It is doped with impurity to give such a resistive film as is suitable as the wirings or input resistors in the memory cell, whereas the portions undoped with the impurity are left as the load resistors of the memory cell. As a result, the poly-Si films having suitable resistivities as the input resistors can be easily prepared without any change in the existing RAM fabrication process.

According to the present embodiment, moreover, the first and second poly-Si films and the poly-Si film (which is made to have three kinds of resistivities as a result of

the occurrence and extent of the doping steps for the first and second poly-Si films with the impurity) can be advantageously used in different modes including the aforementioned one and a variety of others. Moreover, since the input protection resistor is formed of the second poly-Si film, another pattern such as the MISFET using the resistor or the first poly-Si film as its gate electrode may be placed to underlie the second poly-Si film.

Although the present invention has been exemplified hereinbefore, the embodiment thus far described may be further modified in accordance with the technical concept of the present invention. For example, the resistivities of the input protection resistor and the wirings of the load resistors of the memory cell can be changed in various manners in accordance with the doping extent and kind of the impurity, and the pattern itself may also be changed in various manners. On the other hand, the gates and word lines of the MISFET unit need not be made of the aforementioned first poly-Si film but may be made instead of metal having a high melting point (such as Mo, W or Ta) or its silicide. Moreover, the conduction types of the aforementioned respective semiconductor regions and the materials of the respective layers used may be changed.

As has been described hereinbefore, according to the present invention, since the protection resistor of the peripheral

circuit unit is made of the poly-Si film which has substantially the same resistivity as that of the overlying poly-Si film (which merges into the load resistor of the memory cell unit), it can have such a relatively high resistivity as does not block the input signal. Thus it can have a sufficient resistance even if it has its occupied area reduced, whereby the chip size can be accordingly remarkably reduced. Moreover, since that protection resistor can be formed at the same step as that of the overlying poly-Si film, it can be fabricated easily with a high yield without any change in the existing steps.

CLAIMS:

1. A memory device comprising a semiconductor integrated circuit device which comprises: (a) a multiplicity of memory cells, each including a pair of driver MIS transistors series connected to respective load devices, and first conductive means for connecting each load device to a power supply; and (b) a multiplicity of peripheral circuits associated with the memory cells, said circuits including MIS transistors at least one of which has a gate connected with a protection resistor; and wherein said load devices and first conductive means are formed in a first strip which is formed from a single polycrystalline silicon layer, the portions constituting the load devices being of greater resistivity than the portions constituting the conductive means; and the or at least one said protection resistor is formed in a second strip which is formed from the single polycrystalline silicon layer whose resistivity is substantially equal to that of said conductive means portions.

2. A memory device according to claim 1 wherein each said memory cell includes second conductive means for cross-coupling the gate of one of said driver MIS transistors to the drain of the other driver MIS transistor.

3. A memory device according to claim 1 or claim 2 wherein said driver MIS transistors of the memory cells are formed at a preselected portion of a face of a semiconductor substrate; said first strip of poly-

crystalline silicon is formed over an insulation film over the face of said semiconductor substrate, and said peripheral circuits are formed at another preselected portion of the face of said semiconductor substrate, said second strip of polycrystalline silicon being formed over said insulation film.

4. A memory device according to claim 3, further comprising: lower strips of polycrystalline silicon; and upper strips of polycrystalline silicon formed over the insulation film extending over said lower strips, said protection resistor and said load devices being formed into said upper strips.

5. A memory device according to claim 4, wherein the resistivity of said lower strips is lower than that of said upper strips, and wherein said lower strips forms word lines connecting between each of said memory cells.

6. A memory device according to any one of the preceding claims wherein each of said multiplicity of peripheral circuits includes complementary MIS transistors, and wherein said protection resistor is commonly connected with the gates of said complementary MIS transistors.

7. A memory device substantially as described herein with reference to and as claimed in the accompanying drawings.

8. A fabrication process comprising:

(a) forming a first film of polycrystalline silicon, which serves as the gate of each of a mulitplicity of MIS transistors of memory cells, over a semiconductor substrate, said first film having a first resistivity;

(b) forming an insulation film to cover the semiconductor

substrate whjch is formed with each of the MIS transistors of said memory cells; and

(c) forming over said insulation film covering said semiconductor substrate second polycrystalline silicon films, which respectively serve as load resistors of each of said memory cells, as a wiring for connecting said load resistors with power supply means and as one or more protection resistors connected with the gate of at least one MIS transistor of a peripheral circuit; the resistivity of the second films serving as said protection resistor(s) and as said wiring being lower than that of the second film serving as said load resistor and higher than that of said first film.

9. A fabrication process for a memory cell substantially as described herein with reference to the accompanying drawings.

2092826

Dated:	Application No.:	Published:
2092826 3 February 1982	8203074	18 August 1982

Priority: 6 February 1981 Japan 15733/1981

HITACHI, LTD., 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo, Japan, a Japanese Company,

NOBUYOSHI TANIMURA, 1-22-7-402, Naka-machi, Musashino-shi, Tokyo, Japan.

TOKUMASA YASUI, 1586-1-301, Josuihon-cho, Kodaira-shi, Tokyo, Japan.

Semiconductor memory device and fabrication process thereof:

Address for Service:

Mewburn Ellis & Co, 2/3 Cursitor Street, London EC4A 1BQ.

Request for examination:	1 FEB 1983
Application refused or withdrawn:	
Patent granted:	WITH EFFECT FROM SECTION 9 JAN 1985
Renewal Fee paid in respect of	
5th Year	
6th Year	
7th Year	
8th Year	
9th Year	
10th Year	
11th Year	
12th Year	
13th Year	
14th Year	
15th Year	
16th Year	
17th Year	
18th Year	
19th Year	
20th Year	
Patent ceased or expired:	