Dec. 15, 1970 A. G. BLACKWELL 3,548,407

KEYING APPARATUS FOR USE WITH BEACON MARKERS OR THE LIKE

Filed May 22, 1967 2 Sheets-Sheet 1

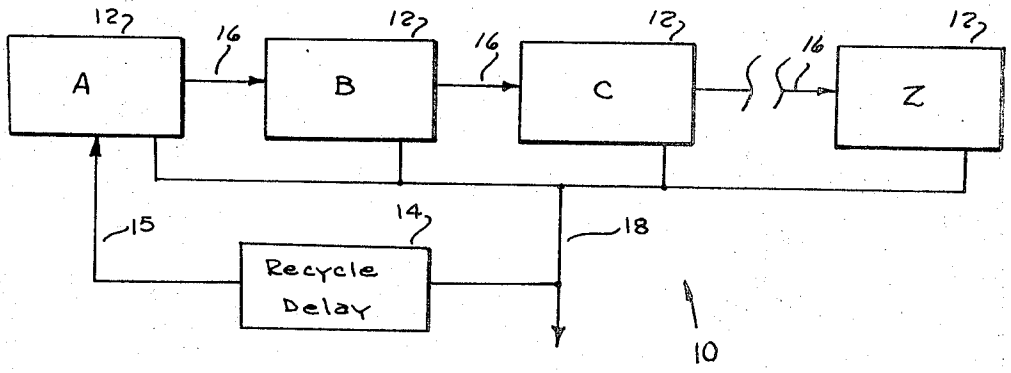


Fig 1

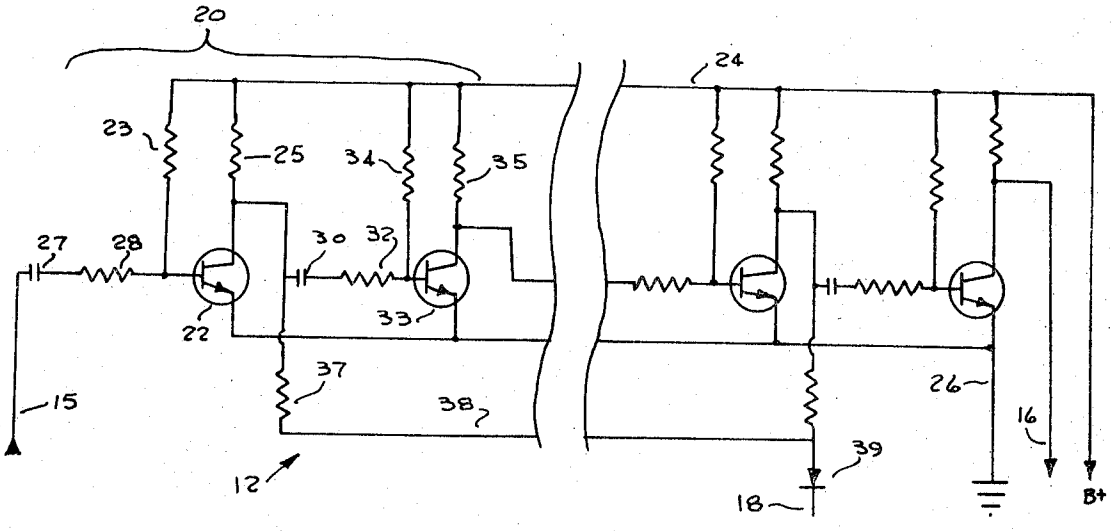


Fig 2

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KEYING APPARATUS FOR USE WITH BEACON MARKERS OR THE LIKE

Filed May 22, 1967 2 Sheets-Sheet 2

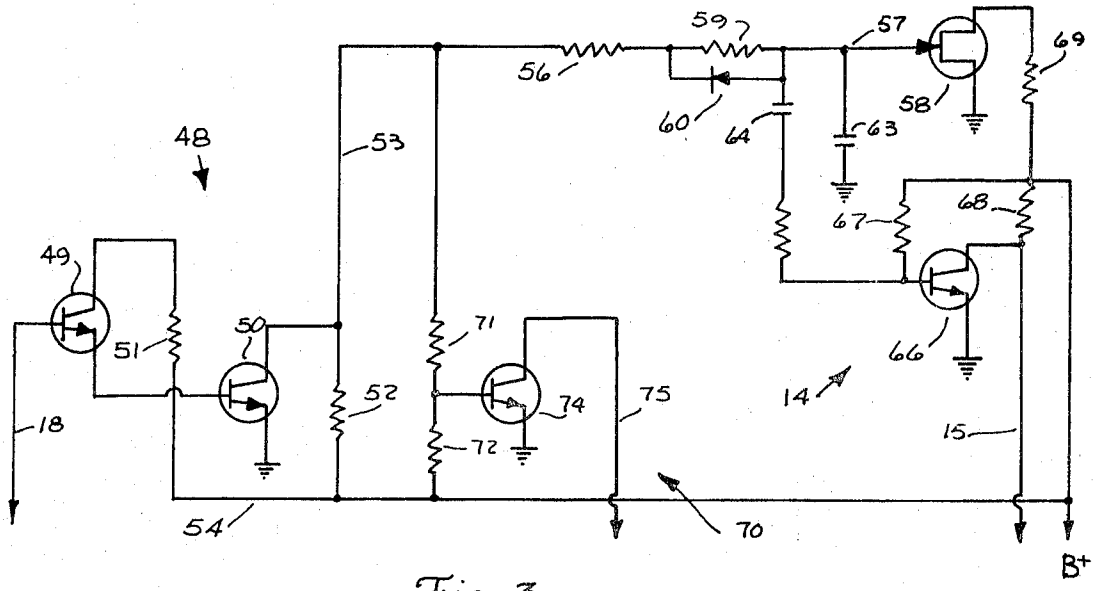


Fig 3

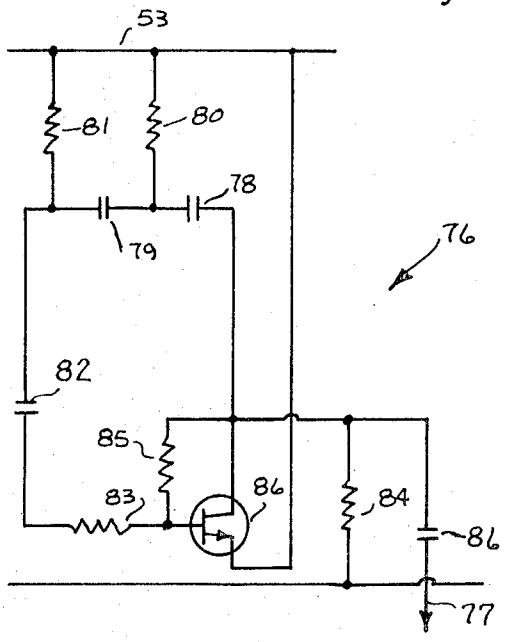


Fig 3-A

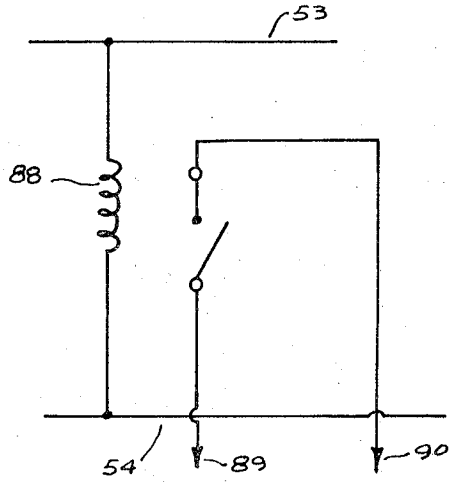


Fig 3-B

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3,548,407

KEYING APPARATUS FOR USE WITH BEACON MARKERS OR THE LIKE

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Int. Cl. G06k 9/06
U.S. Cl. 340—353 11 Claims

ABSTRACT OF THE DISCLOSURE

For the identification of transmitting facilities and the like, a solid state keyer, preferably having a symbol board of plug-in construction for each symbol, including up to eight time determining circuits sequentially connected for forming dots, dashes and spaces as needed, said symbol forming units being adapted to be connected in sequence with recycling means for restarting the first after a time interval.

SUMMARY OF PROBLEM AND INVENTION

Transmitters used as navigational facilities and having other functions usually transmit in a repetitive manner a code group indicating the identity of the beacon marker, facility, radio beacon, VOR, ILS, VORTAC, and so on. Reference is made to transmitters maintained by the Federal Aviation Agency for identifying the facility to aircraft, and the Coast Guard likewise aids water borne vessels with light blinkers, horns, and other warning devices. The code group is recognized within the aircraft and response is made thereto in accordance with the needs of the navigator. By and large, beacon markers are intended to be left in operation for indefinite periods of time without maintenance or inspection. The requirements of keying devices have been recognized by the present invention within the apparatus summarized as preferably including a code symbol plug-in unit adapted to form appropriate dots and dashes for the Morse code representation of the symbol, means for sequentially operating a predetermined number of code symbol forming units as a code group and means for recycling operation whereby the code group is formed in a repetitive manner.

One object of the present invention is to provide a new and improved solid state keying unit for use with beacon markers and the like which has no relay contacts, breaker mechanisms or other mechanical apparatus which is prone to failure, requires extensive maintenance and is usually inflexible.

Another object of the present invention is to provide a new and improved means electronically forming an indefinitely expandable code group in order which is recycled from the last symbol to the first without regard to the length of the code group.

A further object of the present invention is to provide a new and improved keyer unit having a symbol forming plug-in unit with four identical portions thereof for forming appropriate dots or dashes, wherein the only differences needed are change of values in RC timing circuit means to form both dots and dashes.

Yet another object of the present invention is to provide a new and improved keyer apparatus gated at a consistent rate determined in all stages of the apparatus.

A noteworthy object of the present invention is to provide a relatively inexpensive and reliable keying means which adds or deletes code symbols to a code group in an easily facilitated manner.

Other objects and advantages of the present invention will become readily apparent from a consideration of the specification and drawings, wherein:

FIG. 1 is an overall schematic block diagram of the present invention showing sequential arrangement of an indefinite number of code symbols;

FIG. 2 is a detailed wiring schematic of the circuitry for forming a code symbol;

FIG. 3 is a detailed wiring schematic of means for recycling operation of the keying apparatus of the present invention; and

FIGS. 3A and 3B illustrate alternative interface means for use with the present invention.

In the drawings, attention is first directed to FIG. 1 which illustrates the keying means **10** of the present invention. The means **10** incorporates a plurality of code symbol generating means **12** such as those labeled at A, B, C and Z, it being appreciated that an indefinite number of code symbol units **12** can be sequentially connected. The code symbol forming units **12** are identical to one another with the exception that a minimal number of circuit elements are changed to form dots or dashes to comprise Morse code letters. As shown in FIG. 1, the circuit also includes a recycle delay means **14** communicated by way of a conductor **15** to the first of the code symbol forming units **12**. After means **12A** operates, it triggers operations of the second means **12B**, which then triggers operation of the third unit, and so on. On operation of the last unit in the sequential arrangement, a conductor **16** returns a signal to the recycle delay means, which re-starts operation after an appropriate time delay. An output is derived from all of the units **12** in the form of a signal on a conductor **18**. It will be appreciated that a sequentially operated, repetitive triggered means is provided by the present invention.

Considering the invention more in detail, it is appropriate to first detail construction of the symbol forming means **12** which is illustrated in FIG. 2. As will be noted in alphabetic telegraphic symbols, four units (dots or dashes) encode all alphabetic characters. Of course, those having fewer than four symbols are generated by the symbol forming means **12** of the present invention without utilizing the entirety of the circuits provided therefor. Alphabetic characters having four units also include four spaces to separate the various dots and dashes. Therefore, the symbol forming means **12** shown in FIG. 2 preferably includes eight similar or even identical timing circuits which cooperatively form the required dots and dashes with spaces therebetween for the entire alphabet, it being appreciated that shorter characters are derived from an abbreviated version of the repetitive circuit means **12** shown in FIG. 2. Since the circuit means **12** preferably includes eight identical stages in the complete embodiment, several (four) stages have been omitted from the drawings for clarity because they are identical to the circuitry shown in the drawings.

Considering the input to the circuit means **12**, a trigger input signal is provided from a source to be described on the conductor **15** which communicates with a series capacitor and resistor. A pulse is provided on the conductor **15** to initiate operation of the first portion of the circuit means **12**. The first portion of circuitry which is associated with the first symbolic unit, a dot or dash, is encompassed by the bracket **20** to indicate the entirety of means forming the first dot and dash and the delay interval preceding the next dot or dash. The NPN transistor **22** is biased on by a base resistor **23** communicated with the B+ supply **24** which is connected to a collector load resistor **25**. The collector load resistor **25** maintains adequate current flow in the transistor **22** with the emitter grounded to a bus **26**. An input pulse on the conductor **15** is communicated with a relatively large storage capacitor **27** and a series resistor **28**. In the quiescent condition, the transistor is normally turned on since the base is connected with a positive bias source. The continued cur-

rent flow through the transistor establishes a voltage potential on the plates of the capacitor **27** after an interval of time which maintains the quiescent condition. On occurrence of a negative going pulse to the capacitor **27**, the base potential is driven negative with respect to the emitter and the transistor is cut off. The change in base voltage is reflected at the collector where the voltage rises substantially to the supply voltage, and is maintained for an interval of time. The negative charge communicated to the plates of the capacitor **27** is slowly reduced because the bias resistor connected to the supply line **24** restores the capacitor voltage to a positive value which permits the transistor to reconduct. The interval during which the transistor is cut off is determined primarily by the RC time constant of the circuit which includes the capacitor **27** and the series resistors **23** and **28**. While the transistor is cut off for a controlled interval of time, a pulse from the collector is transferred in the manner noted below.

The transistor **22** co-operates with the collector load resistor **25** wherein the output signal derived from the collector is communicated to a coupling capacitor **30**. The capacitor **30** is not only a coupling capacitor to the next transistor **33**, but is similar to capacitor **27** in functioning as part of an RC timing circuit for operation of the transistor **33**. More will be noted concerning this stage hereinafter.

The output from the collector of transistor **22** is also serially communicated through a resistor **37** and then to a conductor **38**. As was previously noted, the symbol forming unit **12** preferably forms up to four dots and dashes as needed. The conductor **38** is connected to each of the four stages which forms the dots and dashes for the code symbol. A maximum of four resistors is connected to the conductor **38** for conveying up to four dots or dashes, and of course, fewer resistors **38** are used with symbols having less than four dots and dashes. However, further attention will be devoted to details concerning the circuit arrangement hereinafter.

Returning again to the output signal from the transistor **22**, it was noted above that the capacitor **30** couples signals to the transistor **33**. The circuitry associated with the transistor **33** is similar to that of the transistor **22** More particularly, an input series resistor **32** communicates the signals to the base of the transistor which is biased on by a resistor **34**. A collector resistor **35** communicates with the supply conductor **24**. The emitter of the transistor is grounded. In the quiescent state, the transistor **33** is normally biased on and continues to conduct for an indefinite period of time. When the circuitry associated with the transistor **22** forms a positive going pulse at its collector, the positive going pulse is communicated to the base of the transistor **33**. Since the transistor is already on, the positive going pulse has no effect on operation of the transistor **33** except to increase the degree of saturation. The change in bias is essentially ineffective on output voltage. At the trailing edge of the positive pulse formed at the collector of transistor **22**, the signal is negative going which change is coupled through capacitor **30** to the base to drive the transistor **33** to cutoff to thereby form the leading edge of the positive pulse its collector. The pulse from the transistor **33** is similar to the pulse formed by the transistor **22**, but is delayed by an interval of time.

It will be appreciated that the connection of eight similar or even identical transistor circuits in sequence in the manner above noted will provide eight sequential pulses with the leading edge of each pulse coinciding with the trailing edge of the pulse formed by the preceding stage. The chain reaction progresses through the circuitry to the last transistor as will be described in detail hereinafter.

In the foregoing, it was noted that the eight consecutive stages form time pulses between dots and dashes. An output (dot or dash) is derived from alternative

stages including the first, third, fifth and seventh transistors. These alternating stages in the chain form pulses coupled through the resistors **37** to the bus **38**. Also, the second, fourth, sixth and eighth transistor circuits form the spaces for intervals between dots and dashes, and, of course, have no output save the serial connection with other stages shown in FIG. 2.

As was previously noted, the symbol forming means **12** forms up to four dots and dashes. As a generalization, dashes are preferably three times as long as dots. In the present embodiment, a dot is preferably on the order of 0.13 second long, while a dash is approximately 0.39 second long. The timed interval between dots and dashes is determined by the time constant of the RC circuit including the capacitor **30** and series resistors **32** and **34**. This interval is preferably about 50% longer than the interval of one dot, and is therefore approximately .20 second long. This is preferably consistent for the time constant of all space determining circuits connected between means for forming the dots and dashes of each code symbol, and in the example of FIG. 2, describes the second, fourth, sixth and eighth transistors.

As previously noted, the dots and dashes formed in each of the unit means **12** are output through resistors such as the resistor **37** shown in FIG. 2. Since all the circuitry of FIG. 2 is preferably placed on one circuit board, the bus wire **38** then communicates with an output diode **39** as the output of the circuit board. The diode **39** communicates with the conductor **18** forming a keyed output in co-operation with other circuit means as will be described in greater detail. The dots and dashes are, so to speak, delivered in sequence as a result of their parallel connection to the conductor **38**. The conductor **38** is normally maintained at a relatively low potential since it is connected at a number of parallel collectors of transistors which are conducting and which therefore have low voltage. However, the formation of a positive pulse at any of the collectors is communicated to the conductor **38** and through the diode **39** to the conductor means **18**. The passage of several pulses to the conductor **18** forms the sequential units comprising the various symbols formed by the present invention.

Attention is directed to the conductor **16** at the right hand portion of FIG. 2 which carries a trigger output from the circuit means **12A** which forms the first symbol in code group. The trigger starts formation of the second symbol in the means **12B**. Referring again to FIG. 1 by way of illustration, means **12A** and **12B** are serially connected. As will be recalled by those familiar with code, the symbol for "A" is comprised of a dot and dash, while "B" is a dash and three dots. To relate the circuit means shown in FIG. 2 and its symbol "A" and the formation of "B," the conductor **16** communicates with the input of the circuit means **12B** comprising the second means in sequence. Because of the need for the timed interval between adjacent letters in a code representation, the conductor **16** is connected to the fourth transistor in the means **12A** while the third transistor stage forms the dash of the letter "A." It will be appreciated that a timed interval is needed between letters; the timed interval is provided by the fourth stage to which the conductor **16** is connected. Of course, the circuit means **12B** likewise needs a trigger output to the means **12C** forming the symbol "C." The connective arrangement is repeated throughout the apparatus to form the code group repeated by the means of the present invention.

Attention is next directed to the circuitry shown in FIG. 3 which illustrates the circuit details of the recycle delay means **14**. More particularly, the circuit means shown in FIG. 3 incorporates a circuit which forms a trigger pulse for application over the conductor **15** to initiate operation of the symbol forming means **12A**. Operation of the circuit means **14** shown in FIG. 3 is withheld by the circuit means indicated generally at **48** in FIG. 3 so long as the various means **12A**, **12B**, and so on are

operative to form the dots and dashes comprising the code group. For instance, if the five symbol forming means **12** are connected in sequence, when the operation of the last of the five units is completed, an interval of time is permitted to pass. During this interval of time, the absence of dots or dashes input to the circuit means **48** terminates its withholding action to permit the recycle delay means **14** to form the pulse on the conductor **15** which restarts the sequential operation of the means **12**. As was noted, a positive pulse is formed on the conductor **18** shown in FIG. 2. The positive pulse withholds action of the recycle delay means **14** for the predetermined interval of time between code groups.

For consideration of details of the circuitry shown in FIG. 3, attention is first directed to the input conductor **18** which is connected with an emitter follower transistor **49**. Transistor **49** is input to the base of transistor **50** with both the transistors provided with B+ potential through collector resistors **51** and **52**, respectively. The emitter follower arrangement shown in FIG. 3 provides current amplification to avoid heavy loading on the signals on the conductor **18**. The pulse input is communicated to the transistor **50** and the amplified output is derived from the collector over the conductor **53**. An adequate positive potential is provided to transistors **49** and **50** through a supply conductor **54**.

When a positive potential (dot or dash) is applied to the base of the transistor **50**, the collector voltage of the transistor **50** drops substantially and is communicated over the conductor **53**. This drop is communicated through a series resistor **56** to lower the potential at a nodal point **57** connected to the input terminal of a unijunction transistor **58**. Low potential at the input of the unijunction transistor **58** withholds its trigger action which is dependent on input potential exceeding a predetermined level. An additional series resistor **59** and parallel diode **60** permit dropping of the input potential at node **57** rapidly in response to reduced voltage caused by each pulse formed in the conductor **18**.

Circuit means connected to the unijunction transistor **58** normally accumulate a charge level whereby the transistor **58** forms a pulse. This is provided by a storage capacitor **63** which accumulate the charge. A charging path is provided for the capacitor **63** through series resistors **52**, **56** and **59**. This presupposes that the transistor **50** is essentially cut off with the collector maintained at a relatively high voltage as is the case when no input pulses are applied to the transistor **50**.

A voltage drop on the conductor **53** is communicated through a capacitor **64** and series resistor **65** to cut off a transistor **66**. The transistor **66** is normally biased on by a base resistor **67** which communicates with the B+ voltage. The transistor has a conventional collector resistor **68** communicated with the B+ supply, and a current source for the unijunction transistor **58** includes a resistor **69** connected with the supply.

In operation, the recycle delay means of the present invention forms a pulse of the unijunction transistor **58** when the voltage at the node **57** rises to a predetermined level. When the level is reached, a pulse is communicated to the transistor **66**. Since the transistor **66** is normally biased on, and the pulse from the unijunction transistor is negative going, the transistor is cut off. Since the conductor **15** is connected to the collector of the transistor **66**, the collector pulse is on, the conductor **15** is applied to the means **12** comprising the code group forming means. Thereafter, the additional means **12** are operated to form pulses returned to the means **48** which withholds operation of the recycle delay means **14** for the duration of the code group formed by the means **12**.

The time delay of the recycle delay means **14** is subject to variation, but is preferably similar to the delay between words of telegraphic operators transmitting at a speed of perhaps eight to ten words per minute. The delay, of course, is subject to some variation, but is determined primarily by the value of the capacitor **63** and the resistance of the serial resistors **52**, **56** and **59**.

FIG. 3 incorporates an interface means indicated generally at **70** for supplying the output of the present invention to cooperative circuitry (not shown) selected by those needing application of the present invention. A voltage divider including resistors **71** and **72** is supplied with the pulsed signals on the conductor **53**. It should be recalled that the conductor **53** communicates from the circuit means **48**. The mid-point of the voltage divider is connected with a base of a transistor **74** whereupon the occurrence of a pulse on conductor **53** provides a synchronized signal to the transistor **74** turning it off and on as the case may be. An output conductor **75** is connected with the collector of the transistor **74** to communicate the output signal to connective apparatus for use with the present invention. It will be appreciated that the operation characteristics of the transistor **74** are subject to a wide range of variation dependent on the transistor selection.

Attention is next directed to FIG. 3A of the drawings of the present invention which illustrates an oscillator circuit means indicated generally by the numeral **76**. The means **76** is keyed off and on by the signal on the conductor **53**, and is adapted to form an output in a conductor **77** which is an audio tone synchronized with the pulses from the means **12A**, **12B** and so on. In the main, the means **76** includes an RC phase shift network connected between the base and the collector. The circuitry includes phase shift capacitors and resistors indicated by the numerals **78**, **79**, **80**, and **81**. The base signal is provided through a coupling capacitor **82** to series resistor **83**. The transistor is biased on by the connection of a base resistor **85** to the collector. The collector load resistor **84** is connected to supply line **54**. The pulse output tone is derived from the collector by a coupling capacitor **86**.

On provision of a low voltage signal on the conductor **53** (coincident with a pulse) adequate phase shift is provided between the collector signal through the RC phase shifting network to the base to cause positive feedback and oscillations into the circuit. The oscillations are supplied to the conductor **77** for application to a selected output device responsive to the tone formed by the audio oscillator means **76**. During the absence of a pulse indicative of information. The conductor **53** becomes a high voltage conductor, and is approximately equal to the voltage found on the conductor **54**. This inhibits operation of the RC phase shifting network and prevents positive feedback to terminate oscillations in the oscillator means **76**.

Attention is last directed to FIG. 3B of the drawings which also shows means connected with the conductors **53** and **54** as an output means. A reed relay **88** is connected between conductors **53** and **54**. On low voltage on the conductor **53**, adequate current flows through the reed relay **88** to cause closure of the contacts coincident with the pulses. On the other hand, high voltage in the conductor **53** provides a minimal current flow through the reed relay **88** inadequate to close the relay contacts which are then opened.

While the foregoing has described the details of the present invention specifically, it should be noted that the present invention is subject to a range of variation understood by those skilled in the art. More particular, the device described has been constructed with the view of maintaining a relatively inexpensive circuit which is particularly adapted for use in unmanned beacons and markers for continued operation for an extended period of time. The timing means of the present invention is RC circuitry used to bias off sequentially arranged transistor stages. However, more elaborate means may be adapted such as multivibrators. If the apparatus of the present invention is to be subjected to wide temperature extremes, it may be wise to provide

a heater or other temperature stabilizing apparatus to maintain the RC timing circuits at generally constant temperatures whereby operation of the apparatus is neither speeded up or impeded. Of course, thermistors and temperature stabilizing circuit elements may be used.

While the foregoing describes the preferred embodiment of the present invention, it will be appreciated that variations in application may be adopted. For instance, the foregoing illustrates in FIG. 1 the application of four code symbol forming means **12**. The sequential arrangement wherein completion of operation of the first unit triggers operation of the second is useful without practical limitation on the number of sequentially connected units. As noted above, this arrangement permits the invention to sequentially and repetitively transmit a code group of any predetermined length. For ease and convenience, each of the means **12** is preferably formed on a separate printed circuit board co-operative with plug-in apparatus to permit the code group to be changed in a relatively easy manner. In a typical installation, sockets may be sequentially wired for perhaps eight or ten symbols in a code group. The ground and voltage connections are provided to all of the sockets as needed, and of course, appropriate wires in the harness are included to accommodate the conductors **16** shown in FIG. 1. The first aliphatic representation is selected for the first socket, and an appropriate printed circuit board is placed therein. The additional printed circuit boards are selected for the additional sockets in order and all are connected in sequence to form the code group. The above arrangement requires no special means to terminate the code group other than to place the printed board representing the last alphabetic symbol in the apparatus and to rely on operation of the recycle delay means to restart the code group. A degree of flexibility heretofore never achieved is provided by the present invention, and by these means, a solid state device is provided which operates over an extended period of time. As was previously noted, each of the plug-in boards in the above example are preferably identical, save for alteration of the resistance of the resistor **23** to provide dots or dashes as needed, and further to omit unneeded stages of the means shown in FIG. 2.

What is claimed is:

1. Code forming apparatus providing a repetitive code group of selected symbols, comprising:

(a) first electronic circuit means for forming the first of the selected symbols;

(b) additional electronic circuit means for forming additional selected symbols;

(c) connective means extending from said first circuit means to the next of said circuit means for providing thereto a signal starting formation of the symbol from said circuit means;

(d) additional connective means between the several circuit means operative to sequentially start operation of said several units;

(e) there being a common output conductor means provided with signals from said several circuits means; and,

(f) re-cycle circuit means connected to said several circuit means and provided with signals therefrom which suppress operation of said re-cycle circuit means, said re-cycle circuit means forming a re-cycle signal applied to said first circuit means after passage of an interval of time indicative of completion of one cycle of operation of said several circuit means, said re-cycle signal beginning operation of said first circuit means.

2. The invention of claim **1** wherein said first circuit means includes up to four unit forming means connected for sequentially forming the symbol thereof.

3. The invention of claim **2** wherein said sequentially connected unit forming means form code symbols having less than four units thereto.

4. The invention of claim **1** wherein the code symbols are formed of code units of two time lengths determined by RC timing circuit means which are similar configurations providing the different time lengths on change of component values.

5. The invention of claim **1** wherein said first circuit means is adapted to form dots and dashes associated with Morse code and said first means forms dots having a duration of approximately 0.13 second as determined by RC timing circuit means.

6. The invention of claim **5** wherein the dashes are approximately three times the time duration of the dots.

7. The invention of claim **1** wherein the code symbols are formed of dots and dashes and wherein the time between symbols is approximately the time of one dash.

8. The invention of claim **1** wherein said last named means provides a predetermined interval approximately equal to three times the interval of one dash.

9. The invention of claim **1** wherein said last named means incorporates a unijunction transistor triggered at a rate determined at least partially by an RC circuit means.

10. The invention of claim **9** wherein said unijunction transistor is triggered in relation to the last code unit of the last selected symbols.

11. The invention of claim **1** wherein said first circuit means incorporates:

(a) a normally conducting transistor;

(b) a bias resistor connected to the base of said conducting transistor; and

(c) a capacitor for driving said transistor to cut-off on receiving a pulse from said last named means of claim **1**.

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U.S. Cl. X.R.

178—26