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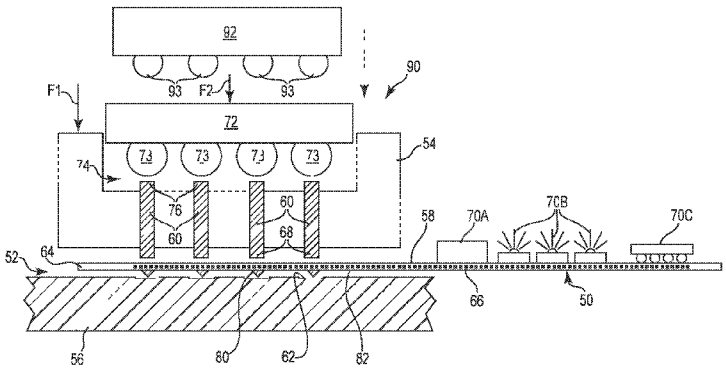

Fig. 2

(57) Abstract: Diagnostic tools for testing integrated circuit (IC) devices, and a method of making the same. The first diagnostic tool includes a first compliant printed circuit with a plurality of contact pads configured to form an electrical interconnect at a first interface between proximal ends of contact members in the socket and contact pads on a printed circuit board (PCB). A plurality of printed conductive traces electrically couple to a plurality of the contact pads on the first compliant printed circuit. A plurality of electrical devices are printed on the first compliant printed circuit at a location external to the first interface. The electrical devices are electrically coupled to the conductive traces and programmed to provide one or more of continuity testing at the first interface or functionality of the IC devices. A second diagnostic tool includes a second compliant printed circuit electrically coupled to a surrogate IC device.

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COMPLIANT PRINTED CIRCUIT SOCKET DIAGNOSTIC TOOL

Field of the Invention

[0001] The present application relates to a compliant printed circuit that provides an electrical interconnect with integrated circuit devices, sockets and printed circuits, and in particular, to a diagnostic tool for testing IC devices, sockets, and printed circuit boards.

Background of the Invention

[0002] There are many applications where a socket is used to connect an integrated circuit (IC) device to a printed circuit board (PCB) so that the electrical connection is made in a separable manner. As illustrated in Figure 1, a socket 20 in a test system 21 may receive a packaged integrated circuit 22 (IC package) and connect each terminal 24 on the IC package 22 to the corresponding terminal 26 on the PCB 28. The terminals 24 on the IC package 22 are held against contact members 32 by applying a load 30 that maintains intimate contact and reliable connection during testing. No permanent connection is required, such that the IC package 22 can be removed or replaced without the need for reflowing solder connections.

[0003] In general, sockets such as the socket 20 contain a series of contact members 32 that form the electrical interface between the IC package 22 and the PCB 28. At least one contact member 32 corresponds to each terminal 24. The contact members 32 have at least two interface points, a first interface 34 with a terminal 24 of the IC package 22 and a second interface 36 with a terminal 26 of the PCB 28. When a user utilizes the socket 20 to connect the IC package 22, the assumption is that the connection points at the first and second interfaces for each terminal 24 are reliable. In the event the system is powered and the function of the IC package 22 is not as expected, there are many connection points at the interfaces 34, 36 that may be the cause of the error. Trouble shooting or otherwise resolving these errors can be challenging.

[0004] If the IC package 22 is removed and replaced and the issue is resolved, then a conclusion can be drawn that all of the other components in the test system 21 are connected and functioning properly. In the event the error is not resolved or another issue is introduced, a user must systematically sort through the various components and connections within the test system 21 to resolve the issue. In many

cases, the socket 20 may be a source of error due to the number of connections at the interfaces 34, 36 and the potential for at least one of those connections to be improperly positioned. The typical method is to replace the socket 20 with another socket, or place the socket 20 on an interface known to function properly to attempt to determine if the socket 20 is the source of the error. If the new socket functions properly, then the original socket 20 is deemed the problem. If the new socket does not work, then the issue is not resolved since the issue may be common or related to how the socket 20 interfaces to the IC package 22 or to the PCB 28. This systematic process can be extremely time consuming and can cause major delays, and can impact continued testing of IC packages.

[0005] There are several limitations to traditional methods of trouble shooting and resolving connection problems. The common method of replacing the socket 20 with another is typically the first avenue, and requires that additional sockets 20 are available. A successful result depends on whether the issue is isolated to the initial socket 20. This method can identify whether there is an anomaly with the initial socket 20 such as a damaged contact or poor connection. In the event the new socket does not produce desired results, further investigation is required. There may be a problem that is common to the sockets generally, and the user does not know if they need to look elsewhere or if the issue remains with the socket 20.

[0006] Another method may involve creating an external validation vehicle, such as a PCB that mimics the system board. This method can be more determinant than an "in the system" approach such as replacing the socket 20. The socket interfaces can be isolated and, if there is an issue with the group of contacts or specific contacts, the issue can be readily identified. One limitation with this method can be the requirement that these external tools be created ahead of time so they are available if and when they are needed. The result can be additional effort and expense that may not be needed if the socket 20 performs as expected.

[0007] Establishing these tools ahead of time can provide confidence that the socket is functioning properly and in the end reduce effort since the user can trust the socket is working. However, there is some risk that the external tools may not match the actual system circuit board precisely in form or function, and that issues that are not present on the external tools may be present on the system PCB. Another limitation with this method may be the adverse consequences of failing to produce these external tools ahead of time, since the lead time to design and

produce these external tools can be long. Still another limitation is that an external circuit board or test system may not precisely match the make-up of the actual system and/or utilize an exact IC device. Typically, a surrogate IC device is used to simulate the actual IC device and a surrogate PCB is used to simulate the system PCB. The surrogate IC device and surrogate PCB may manifest issues different from or not present in the actual IC device and PCB. Similarly, the surrogates may not manifest issues present in the actual IC device and PCB. Accordingly, problems may go undetected.

[0008] In the event the foregoing methods do not identify the problem, the actual IC device may be soldered to the site intended for the socket to eliminate the socket from the equation. This method defeats the advantages of using a socket, including eliminating the desired separability.

Brief Summary of the Invention

[0009] The present disclosure relates to a compliant printed circuit that provides an electrical interconnect with IC devices, sockets and printed circuits. The compliant printed circuit may form the basis for a diagnostic tool for testing IC devices, sockets, and PCBs. A variety of passive and active electrical devices are incorporated into the present diagnostic tool to provided testing capabilities independent of, or supplementary to, conventional testing stations.

[0010] The present disclosure aims to leverage the capabilities of printed electronics to provide a diagnostic tool to validate socket function either external to the system or while the socket is installed in the system. The present disclosure provides an electrical interconnect that can enable next generation electrical performance. Some of the embodiments include a high performance interconnect architecture on the interconnect.

[001 1] Printing processes permit compliant printed circuits and electrical devices of diagnostic tools to be produced by a direct writing method based upon images, without the need for artwork, lengthy lead-times for circuit design and production, and subtractive circuit techniques. The present diagnostic tools can be simple or complex, and can be produced in minutes. The diagnostic tools can also be adapted as needed to accommodate additional diagnostic functions or tests. The additive nature of many printing processes, such as for example the inkjet printing process, can also provide an excellent avenue to directly print electrical devices as part of printing the diagnostic tools. The electrical devices that may be printed may include,

but are not limited to, passive components, transistors, display function or adaptive intelligence. Revisions to the diagnostic tools can be accomplished in moments by altering the image files and reprinting the diagnostic tools. Traditional methods, by contrast, may take weeks to generate a revision.

[0012] A diagnostic tool can be as simple as a daisy chain to verify continuity, or as complex as functional testing directly on the diagnostic tool. Positioning functional testing on the present diagnostic tool dramatically increases the value to the user by eliminating a need to connect to external systems or testing analyzers. The diagnostic tools can be printed with simple low-cost or low-speed circuitry, or the circuitry can be printed with high frequency capability in the event an external measurement tool is connected.

[0013] The cost to produce a diagnostic tool in accordance with the present disclosure is a fraction the of cost of a conventional tool. A tool produced with conventional methods might cost $10,000 to $20,000 to design and produce, typically with a 4-6 week lead-time. A diagnostic tool according to the present disclosure can be produced in minutes for a fraction of the cost. The ability to modify the design or correct errors which would cause the $20,000 investment to be wasted, and reprint and reprint the tool easily at little additional cost, offers tremendous improvements over conventional methods. Image libraries and design rules can be created to semi-automate the design process and dramatically reduce engineering time, with tremendous flexibility to make changes substantially on the fly during the testing process.

[0014] The use of additive printing processes can permit the material set in a given layer to vary. Traditional PCB and circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0015] The compliant printed circuit can also be processed to add functions and electrical enhancements not found in traditional printed circuits. The diagnostic tool

according to the present disclosure can be configured with conductive traces that reduce or redistribute the terminal pitch, without the addition of an interposer or daughter substrate. Grounding schemes, shielding, electrical devices, and power planes can be added to the present diagnostic tools, reducing the number of connections to the PCB and relieving routing constraints while increasing performance.

[0016] The resulting circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to recesses in a previously deposited layer. The use of additive printing processes permit conductive material, non-conductive material, and semi-conductive material to be deposited and positioned on a single layer.

[0017] In one embodiment, pre-formed conductive trace materials are located in the recesses. The recesses can be plated to form conductive traces with substantially rectangular cross-sectional shapes. In another embodiment, a conductive foil is pressed into at least a portion of the recesses. The conductive foil is sheared along edges of the recesses. The excess conductive foil not located in the recesses is removed and the recesses are plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0018] One embodiment can be directed to a diagnostic tool for testing IC devices coupled to a PCB by a socket. A first diagnostic tool can include a first compliant printed circuit with a plurality of contact pads configured to form an electrical interconnect at a first interface between proximal ends of contact members in the socket and contact pads on the PCB. A plurality of printed conductive traces electrically couple to a plurality of the contact pads on the first compliant printed circuit. A plurality of electrical devices can be printed on the first compliant printed circuit at a location external to the first interface. The electrical devices can be electrically coupled to the conductive traces and programmed to provide one or more of continuity testing at the first interface or functionality testing of the IC devices.

[0019] The electrical devices printed on the first compliant printed circuit can include any of a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae. The first compliant printed circuit can optionally include one or more printed layers, including for example a dielectric layer, a ground plane, or a power plane.

[0020] A second diagnostic tool including a surrogate IC device with a plurality of contact pads can be configured to form an electrical interconnect with distal ends of the contact members in the socket at a second interface. The surrogate IC device can be preferably programmed to provide one or more of continuity testing at the second interface or testing of the first diagnostic tool. In one embodiment, a second compliant printed circuit can be electrically coupled to the surrogate IC device. A plurality of printed conductive traces can be coupled to the plurality of the contact pads on the second compliant printed circuit. A plurality of electrical devices can be printed on the second compliant printed circuit at a location external to the second interface. The electrical devices are electrically coupled to the conductive traces on the second compliant printed circuit and programmed to provide one or more of continuity testing at the second interface or functionality testing of the first diagnostic tool.

[0021] The first and second diagnostic tools can be used separately or together as a diagnostic system for testing IC devices.

[0022] The present disclosure is also directed to a method of making a diagnostic tool for testing IC devices coupled to a PCB by a socket. The method can include printing a plurality of contact pads on a first compliant printed circuit. The contact pads can be configured to form an electrical interconnect at a first interface between proximal ends of contact members in the socket and contact pads on the PCB. A plurality of conductive traces electrically coupled to a plurality of the contact pads can be printed on the first compliant printed circuit. A plurality of electrical devices can be printed on the first compliant printed circuit at a location external to the first interface such that the electrical devices are electrically coupled to the conductive traces. The first compliant printed circuit can be positioned to form an electrical interconnect at the first interface. The first diagnostic tool can be used to evaluate one or more of continuity at the first interface or functionality of one or more IC devices located in the socket.

[0023] The conductive traces, the electrical devices, and optional planes can be printed on the first compliant printed circuit.

[0024] The present disclosure is also directed to a method of making and using a second diagnostic tool. An electrical interconnect can be formed with distal ends of the contact members and contact pads on a surrogate IC device in the socket at a second interface. The surrogate IC device can be electrically coupled with a second

compliant printed circuit. Conductive traces and electrical devices can be printed on the second compliant printed circuit. One or more of continuity at the second interface or functionality of the first diagnostic tool can be evaluated by the second diagnostic tool.

Brief Description of the Several Views of the Drawing

[0025] Figure 1 is a cross-sectional view of a prior art socket used to test IC devices.

[0026] Figure 2 is a schematic illustration of a test system with a diagnostic tool electrically coupling a socket to a PCB in accordance with an embodiment of the present disclosure.

[0027] Figure 3 is a schematic illustration of test system with an alternate diagnostic tool mated with a surrogate IC package in accordance with an embodiment of the present disclosure.

[0028] Figure 4 is a schematic illustration of a test system with an alternate diagnostic tool merged with a surrogate IC package in accordance with an embodiment of the present disclosure.

[0029] Figure 5 is a schematic illustration of a test system with a diagnostic tool substituted for the PCB in accordance with an embodiment of the present disclosure.

[0030] Figure 6 is a schematic illustration of a test system with first and second diagnostic tools in accordance with an embodiment of the present disclosure.

[0031] Figure 7 is a schematic illustration of a test system with first and second diagnostic tools adapted to engage with LGA devices in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0032] Figure 2 is a schematic illustration of a diagnostic tool 50 electrically coupled at an interface 52 of a socket 54 and a printed circuit board (PCB) 56 in accordance with an embodiment of the present disclosure. A compliant printed circuit 58 of the diagnostic tool 50 is positioned to act as an electrical interconnect between contact members 60 on the socket 54 and contact pads 62 on the PCB 56.

[0033] The present compliant printed circuit 58 can operate with fine contact-to-contact spacing (pitch) on the order of less than 1.0 millimeter, and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. The socket 54 permits IC packages 72, 92 to be installed and uninstalled without the need to reflow solder.

[0034] The compliant printed circuit 58 is a flexible polymeric sheet 64 with a plurality of conductive traces 66 arranged in an array to electrically couple with proximal ends 68 of the contact members 60 and contact pads 62 on the PCB 56. A force F1 is preferably provided to the socket 54 to compressively couple the proximal ends 68 with the contact pads 62 through the compliant printed circuit 58. The conductive traces 66 can electrically couple the contact members 60 and the contact pads 62 with one or more electrical devices 7OA, 7OB, 7OC (collectively "70") located at a distal end of the diagnostic tool 50. The electrical devices 70 can be positioned on the compliant printed circuit 58 external to the first interface 52. The electrical devices 70 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like.

[0035] In the configuration of Figure 2, the diagnostic tool 50 can evaluate the operation of the PCB 56, the interface 52, the socket 54, an interface 74 between the IC package 72 and the distal ends 76 of the contact members 60, and/or the IC package 72. For example, an LCD 7OA can display a pin-map of the contact members 60, LED's 7OB can indicate open/short, and an integrated circuit 7OC can provide specific diagnostic functionality to make the diagnostic tool 50 more than a basic open or short testing tool. In one embodiment, the IC package 72 can be a surrogate electrical device designed to validate operation of a test system 90. Once operation of the test system 90 is verified, the socket 54 is ready to test production IC devices 92.

[0036] The flexible polymeric sheet 64 can optionally include contact members 80 arranged in an array along a surface 82 of the compliant printed circuit 58. The contact members 80 can correspond with the contact pads 62 on the PCB 56. The contact members 80 can optionally have a pitch that is different than the pitch of the proximal ends 68 of the contact members 60. In an alternate embodiment, a variety of other circuit members can be substituted for the PCB 56, such as for example another flexible circuit, a packaged or unpackaged bare die silicon device, an integrated circuit device, an organic or inorganic substrate, or a rigid circuit.

[0037] The flexible polymeric sheet 64 can be optionally singulated around the contact members 80. Singulation refers to a complete or partial separation of the terminal 80 from the sheet 64 that does not disrupt the electrical integrity of the

conductive trace 66. The singulation may be a slit surrounding a portion of the contact member 80. The slit may be located adjacent to the perimeter of the contact member 80 or offset therefrom. Singulation of the compliant printed circuit 58 can control the amount of force and the range of motion, and can assist with creating a more evenly distributed force vs. deflection profile across the array.

[0038] The singulations can be formed at the time of manufacture of the polymeric sheet 64 or can be subsequently patterned by mechanical methods such as stamping or cutting, chemical methods such as photolithography, electrical methods such as excess current to break a connection, a laser, or a variety of other techniques. In one embodiment, a laser system, such as an Excimer laser, a CO_2 laser, or a YAG laser, can create the singulation. A singulated structure is advantageous in several ways, because the force of movement is greatly reduced where the compliant printed circuit 58 is no longer a continuous membrane, but a series of flaps or bond sites with a living hinge and bonded contact.

[0039] The IC package 72 is illustrated as a ball grid array (BGA) device with a series of contact members in the form of solder balls 73. A force F2 preferably compressively couples solder balls 73 with distal ends 76 of the contact members 60. The force F2 can be provided by a cover assembly, such as disclosed in U.S. Pat. Nos. 7,101,210 (Lin et al.); 6,971,902 (Taylor et al.); 6,758,691 (McHugh et al.); 6,461,183 (Ohkita et al.); and 5,161,983 (Ohno et al.), which are incorporated herein by reference. The distal ends 76 of the contact members 60 can be configured to test any type of IC package, such as for example a land grid array (LGA), a plastic leaded chip carrier (PLCC), a pin grid array (PGA), a small outline integrated circuit (SOIC), a dual in-line package (DIP), a quad flat package (QFP), a leadless chip carrier (LCC), a chip scale package (CSP), or packaged or unpackaged integrated circuits.

[0040] The compliant printed circuit 58 and the electrical devices 70 are preferably manufactured using printing technology, such as for example, inkjet printing, screen printing, printing through a stencil, flexo-gravure printing, and offset printing, rather than traditional PCB fabrication techniques. Various methods of printing the compliant printed circuit and the electrical devices are disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.);

6,521 ,489 (Duthaler et al.); 6,459,41 8 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,31 2,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,1 77,921 (Comiskey et al.); 6,1 20,588 (Jacobson); 6,1 18,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are incorporated herein by reference. For example, conductive inks containing metal particles are printed onto the compliant printed circuit 58 and subsequently sintered.

[0041] A printing process can preferably be used to fabricate various functional structures, such as conductive paths and electrical devices without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0042] Recesses may be formed in layers of the compliant printed circuit 58 to permit control of the location, cross section, material content, and aspect ratio of the contact members 80 and the conductive traces 66 in the compliant printed circuit 66. Maintaining the conductive traces with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the recesses to control the aspect ratio of the conductive traces 66 results in a more rectangular or square cross-section of the conductive traces, with the corresponding improvement in signal integrity.

[0043] U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated herein by reference, teach using inkjet printing to make various electrical devices, such as resistors, capacitors, diodes, inductors (or elements which can be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistors (including, light emitting, light sensing or solar cell elements, field effect transistors, top gate structures), and the like.

[0044] U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference, teach using aerosol printing to create various electrical devices and features.

[0045] Printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semiconductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[0046] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or teflon.

[0047] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[0048] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from Dupont located in Wilminton, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[0049] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite

or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[0050] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic/organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[0051] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomehc semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181 (Bhdenbaugh et al.), which is incorporated herein by reference.

[0052] A protective layer can optionally be printed onto the electrical devices and features. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[0053] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present invention.

[0054] An inkjet print head, or other print head, preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[0055] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061 089 (King et al.), which are hereby incorporated by reference.

[0056] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetosthctive, electromechanical, electropneumatic, electrostatic, rapid ink heating, magnetohydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[0057] While inkjet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: premetered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; aerosol printing processes; and other similar techniques.

[0058] The additive nature of inkjet printing of electrical devices and features provides an excellent means to print electrical devices to perform the desired functions directly on the compliant printed circuit 58, rather than mounting the electrical devices discretely. For example, the electrical devices 70 can be a capacitor, a resistor, a battery, a filter, a signal or power altering and enhancing device, a memory device, an embedded integrated circuit, and a RF antennae. The electrical devices 70 can be printed on either surface of the polymeric sheet 64. InkJet printing can also be used to form additional layers on the flexible polymeric

sheet 64, such as for example dielectric layers covering the conductive traces 66, power planes, ground planes, and the like.

[0059] Positioning such electrical devices 70 on the compliant printed circuit 58 in close proximity to the IC package 72 can improve performance of the diagnostic tool 50. The present diagnostic tool 50 permits IC manufacturers to reduce the pitch of the contact members 73, 93 on the IC packages 72, 92, and perform any required signal routing in the compliant printed circuit 58, rather than in the printed circuit board 56 or by adding daughter boards to the system. IC manufacturers also are limited by current sockets when designing a configuration of contacts 73, 93 on the IC packages 72, 92. Performing the routing in the present compliant printed circuit 58 permits quick and inexpensive changes.

[0060] In another embodiment, the conductive traces 66 of the compliant printed circuit 50 are formed by transferring pre-patterned or pre-etched thin conductive foil circuit traces to recesses in a layer of the compliant printed circuit 50. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses not occupied by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses.

[0061] In another embodiment, a thin conductive foil is pressed into the recesses, and the edges of the recesses act to cut or shear the conductive foil. The process positions a portion of the conductive foil in the recesses, but leaves the negative pattern of the conductive foil not wanted outside and above the recesses for easy removal. Again, the foil in the recesses is preferably post plated to add material to increase the thickness of the conductive traces and to fill any voids left between the conductive foil and the recesses.

[0062] Figure 3 is a schematic illustration of an alternate diagnostic tool 100 mated with a surrogate IC package 102 in accordance with an embodiment of the present disclosure. Conductive traces 104 on a compliant printed circuit 106 can be electrically coupled with solder balls 108 on the surrogate IC package 102, either by soldering or in a solderless manner. The surrogate IC package 102 can be a BGA device as illustrated, but any other IC package configuration can be used with the diagnostic tool 100 of Figure 3.

[0063] The compliant printed circuit 106 can be configured to simulate the IC package to be tested in the socket 110, with desired functions, such as for example open/close shorting, daisy chain, or a diagnostic IC built into the electrical devices 112A, 112B, 112C (collectively "112") of the diagnostic tool 100. An electrical connection 134 can be optionally provided between the diagnostic tool 100 and a PCB 120.

[0064] In the configuration of Figure 3, a test system 132 can evaluate operation of the PCB 120, the interface 122, the socket 110, an interface 124 between the surrogate IC device 102 and the distal ends 126 of contact members 128, and/or production IC devices 130. Again, the compliant printed circuit 106 and the electrical devices 112 are preferably manufactured using inkjet printing technology, aerosol printing technology, or other maskless deposition techniques, as described above, rather than traditional PCB fabrication techniques. The electrical devices 112 may be printed on the compliant printed circuit 106 at a position external to the interface 124.

[0065] Figure 4 is a schematic illustration of an alternate diagnostic tool 150 with a compliant printed circuit 156 merged with a surrogate IC package 152 in accordance with an embodiment of the present disclosure. The conductive traces 154 on the compliant printed circuit 156 can be electrically coupled with solder balls 158 or directly to the IC device 160, such as for example by wire bonding 162. The compliant printed circuit 156 can be preferably attached or bonded to the IC package 152. As used herein, "bond" or "bonding" refers to, for example, adhesive bonding, solvent bonding, ultrasonic welding, thermal bonding, or any other techniques suitable for attaching adjacent layers.

[0066] Figure 5 is a schematic illustration of a diagnostic (test) system 200 with a diagnostic tool 202 substituted for the PCB in accordance with an embodiment of the present disclosure. Conductive traces 204 on the compliant printed circuit 206 can electrically couple contact members 208 on the socket 210 with the electrical devices 212A, 212B, 212C (collectively "212").

[0067] Either a surrogate IC package 214 or production IC packages 216 can be tested in the socket 210. In the configuration of Figure 5, the diagnostic tool 202 can evaluate an interface 218 between the socket 210 and the diagnostic tool 202, the socket 210, an interface 220 between IC device 214 and distal ends 222 of contact members 208, and/or IC devices 214, 216. The compliant printed circuit 206 and the

electrical devices 212 are preferably manufactured using printing technology, as described above, rather than traditional PCB fabrication techniques.

[0068] Figure 6 is a schematic illustration of a diagnostic (test) system 250 with a first diagnostic tool 252 merged with a surrogate IC package 254 used in conjunction with a second diagnostic tool 256 that acts as an interconnect between a socket 258 and a PCB 260, in accordance with an embodiment of the present disclosure. In another embodiment, the second diagnostic tool 256 can substitute for the PCB 260.

[0069] In the diagnostic system 250 of Figure 6, the first diagnostic tool 252 can evaluate an interface 262 between the surrogate IC device 254 and the distal ends 264 of contact members 266 in the socket 258, while the second diagnostic tool 256 can evaluate the socket 258, an interface 268 between the PCB 260 and the socket 258, and the PCB 260. An electrical connection 270 can permit the electrical devices 272A, 272B, 272C (collectively "272") on the first diagnostic tool 252 to interact with the electrical devices 274A, 274B, 274C (collectively "274") on the second diagnostic tool 256 to provide additional functionality and cross-checking of, for example, the various diagnostic tests. The electrical devices 272, 274 can be a variety of passive and active devices, such as for example, a power plane, a ground plane, a capacitor, a resistor, a battery, a filter, a signal or power altering and enhancing device, a memory device, an embedded integrated circuit, or a RF antennae. The electrical devices 272, 274 can be printed on either surface of the polymeric sheets 276, 278. The test system 250 of Figure 6 can eliminate the need for a separate test station 280 or can supplement the functionality of the test station 280.

[0070] Figure 7 is a schematic illustration of a diagnostic (test) system 300 including a first diagnostic tool 302 with an array of terminals 304 on the compliant printed circuit 306 configured to couple with contact pads 308 on an IC package 310. In the illustrated embodiment, the IC package 310 is a LGA device. A second diagnostic tool 312 acts as an interconnect between a socket 314 and a PCB 316. The compliant printed circuit 318 can include printed contact members 320 configured to electrically couple with contact pads 322 on the PCB 316.

[0071] In the configuration of Figure 7, the first diagnostic tool 302 can evaluate the interfaces 330, 332, as well as test the IC device 311 located in the IC package 310. The second diagnostic tool 312 can evaluate the interface 334 between the contact members 336 of the socket 314 and the PCB 316. An electrical connection

340 can permit the electrical devices 342A, 342B, 342C (collectively "342") on the first diagnostic tool 302 to interact with the electrical devices 344A, 344B, 344C (collectively "344") on the second diagnostic tool 312 to provide additional functionality and cross-checking of various diagnostic tests.

[0072] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the invention. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the invention.

[0073] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[0074] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the embodiments of the present invention are not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[0075] Other embodiments of the invention are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the invention, but as merely providing illustrations of some of the presently preferred embodiments of this invention. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the

embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the invention. Thus, it is intended that the scope of at least some of the present invention herein disclosed should not be limited by the particular disclosed embodiments described above.

[0076] Thus the scope of this invention should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A diagnostic system for testing integrated circuit (IC) devices coupled to a printed circuit board (PCB) by a socket, the diagnostic system comprising a first diagnostic tool comprising:

a first compliant printed circuit comprising a plurality of contact pads configured to form an electrical interconnect at a first interface between proximal ends of contact members in the socket and contact pads on the PCB;

a plurality of printed conductive traces electrically coupled to a plurality of the contact pads on the first compliant printed circuit; and

a plurality of electrical devices printed on the first compliant printed circuit at a position external to the first interface, the electrical devices electrically coupled to the conductive traces and programmed to provide one or more of continuity testing at the first interface or functionality testing of the IC devices.

2. The diagnostic system of claim 1, wherein the conductive traces comprise substantially rectangular cross-sectional shapes.

3. The diagnostic system of claim 1, wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer of the compliant printed circuit.

4. The diagnostic system of claim 1, further comprising raised contact members printed on the compliant printed circuit in an array configured to electrically couple with the contact pads on the PCB.

5. The diagnostic system of claim 1, wherein the electrical devices comprise one of a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae.

6. The diagnostic system of claim 1, wherein the first compliant printed circuit comprises one or more printed layers comprising one or more of a dielectric layer, a ground plane, or a power plane.

7. The diagnostic system of claim 1, further comprising a second diagnostic tool including a surrogate IC device having a plurality of contact pads configured to form an electrical interconnect with distal ends of the contact members in the socket at a second interface.

8. The diagnostic system of claim 7, wherein the surrogate IC device is programmed to provide one or more of continuity testing at the second interface or testing of the first diagnostic tool.

9. The diagnostic system of claim 1, further comprising:

a surrogate IC device including a plurality of contact pads configured to form an electrical interconnect with distal ends of the contact members in the socket at a second interface;

a second compliant printed circuit electrically coupled to the surrogate IC device, and a plurality of printed conductive traces coupled to the plurality of the contact pads on the second compliant printed circuit; and

a plurality of electrical devices printed on the second compliant printed circuit at a location external to the second interface, the electrical devices electrically coupled to the conductive traces on the second compliant printed circuit and programmed to provide one or more of continuity testing at the second interface or functionality testing of the first diagnostic tool.

10. The diagnostic system of claim 9, wherein the second compliant printed circuit is electrically coupled with contact pads on the surrogate IC device using one or more of solder, wire bonding, and a compressive connection.

11. The diagnostic system of claim 9, further comprising an electrical connection between the first diagnostic tool and the second diagnostic tool.

12. A diagnostic system for testing integrated circuit (IC) devices coupled to a printed circuit board (PCB) by a socket, the diagnostic system comprising a first diagnostic tool comprising:

a surrogate IC device including a plurality of contact pads configured to form an electrical interconnect with distal ends of the contact members in the socket at a first interface;

a first compliant printed circuit having a plurality of contact pads electrically coupled to the contact pads on the surrogate IC device, and a plurality of printed conductive traces coupled to the plurality of the contact pads on the first compliant printed circuit; and

a plurality of electrical devices printed on the first compliant printed circuit at a position external to the first interface, the electrical devices electrically coupled to the conductive traces and programmed to provide one or more of continuity testing at

the first interface or continuity testing at a second interface between the PCB and proximal ends of the contact members in the socket.

13. The diagnostic system of claim 12, wherein the plurality of electrical devices comprise one of a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae.

14. The diagnostic system of claim 12, wherein the first compliant printed circuit comprises one or more printed layers comprising one or more of a dielectric layer, a ground plane, or a power plane.

15. The diagnostic system of claim 12, further comprising:

a second compliant printed circuit comprising a plurality of contact pads configured to form an electrical interconnect with proximal ends of contact members in the socket and contact pads on the PCB at a second interface;

a plurality of printed conductive traces electrically coupled to the plurality of the contact pads on the second compliant printed circuit; and

a plurality of electrical devices printed on the second compliant printed circuit at a position external to the second interface, the electrical devices electrically coupled to the conductive traces on the second compliant printed circuit and programmed to provide one or more of continuity testing at the second interface or functionality testing of IC devices located in the socket.

16. The diagnostic tool of claim 15, further comprising an electrical connection between the first diagnostic tool and the second diagnostic tool.

17. A method of making a first diagnostic tool for testing integrated circuit (IC) devices coupled to a printed circuit board (PCB) by a socket, the method comprising the steps of:

printing a plurality of contact pads on a first compliant printed circuit, the contact pads configured to form an electrical interconnect at a first interface between proximal ends of contact members in the socket and contact pads on the PCB;

printing a plurality of printed conductive traces electrically coupled to a plurality of the contact pads on the first compliant printed circuit; and

printing a plurality of electrical devices on the first compliant printed circuit at a location external to the first interface so that the electrical devices are electrically coupled to the conductive traces;

positioning the first compliant printed circuit to form an electrical interconnect at the first interface; and

evaluating one or more of continuity at the first interface or functionality of one or more IC devices located in the socket.

18. The method of claim 17, wherein the conductive traces comprise substantially rectangular cross-sectional shapes.

19. The method of claim 17, further comprising printing a conductive material, a non-conductive material, and a semi-conductive material on a single layer of the compliant printed circuit.

20. The method of claim 17, further comprising printing one or more of a capacitor, a resistor, a filter, a signal or power altering and enhancing device, a capacitive coupling feature, a memory device, an embedded integrated circuit, and a RF antennae on the first compliant printed circuit.

21. The method of claim 17, further comprising printing one or more of a dielectric layer, a ground plane, or a power plane on the first compliant printed circuit.

22. The method of claim 17, further comprising a method of making a second diagnostic tool comprising the steps of:

forming an electrical interconnect with distal ends of the contact members and contact pads on a surrogate IC device in the socket at a second interface;

electrically coupling the surrogate IC device with a second compliant printed circuit;

printing a plurality of printed conductive traces electrically coupled to the surrogate IC device;

printing a plurality of electrical devices on the second compliant printed circuit at a location external to the second interface so that the electrical devices are electrically coupled to the conductive traces on the second compliant printed circuit; and

evaluating one or more of continuity at the second interface or functionality of the first diagnostic tool.

23. The method of claim 22, further comprising merging the surrogate IC device with the second compliant printed circuit.

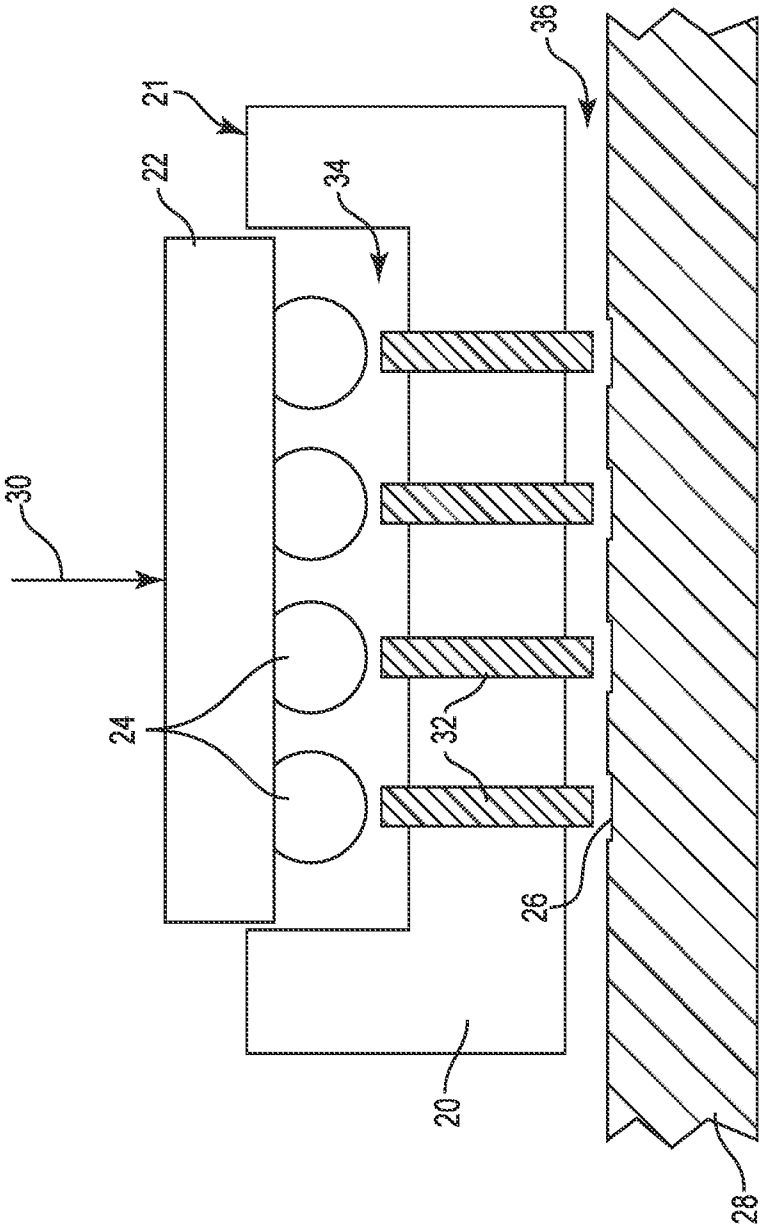

Fig. 1
PRIOR ART

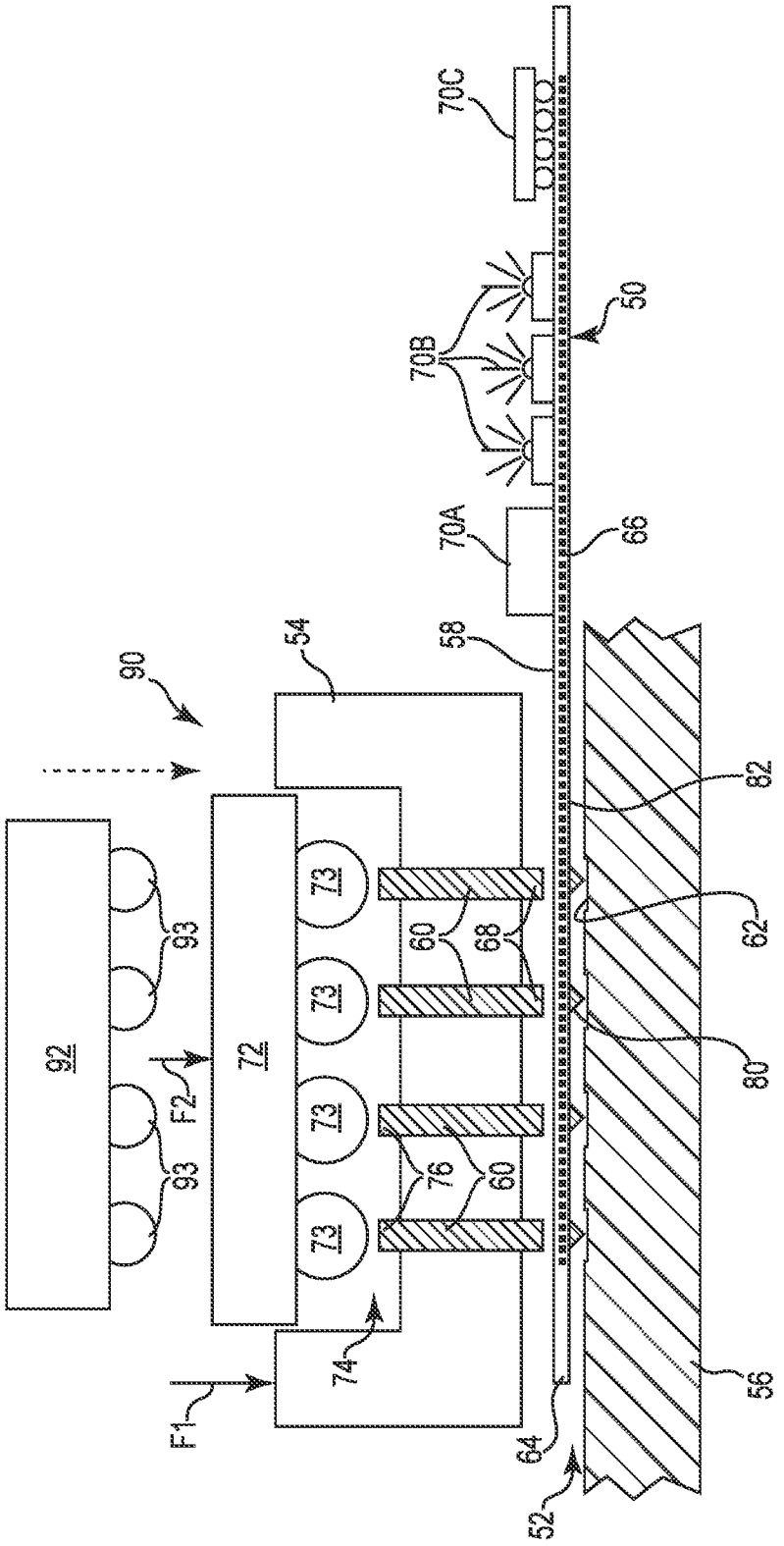
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Fig. 2

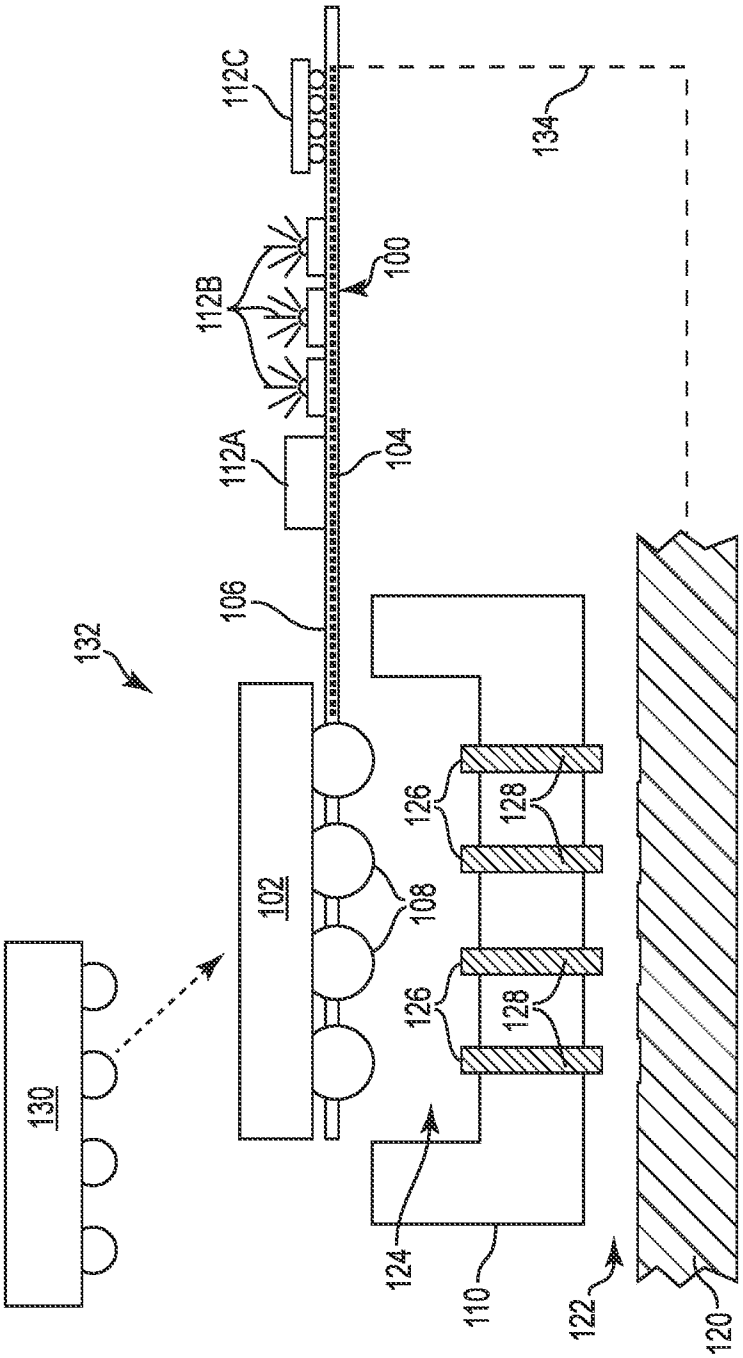
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Fig. 3

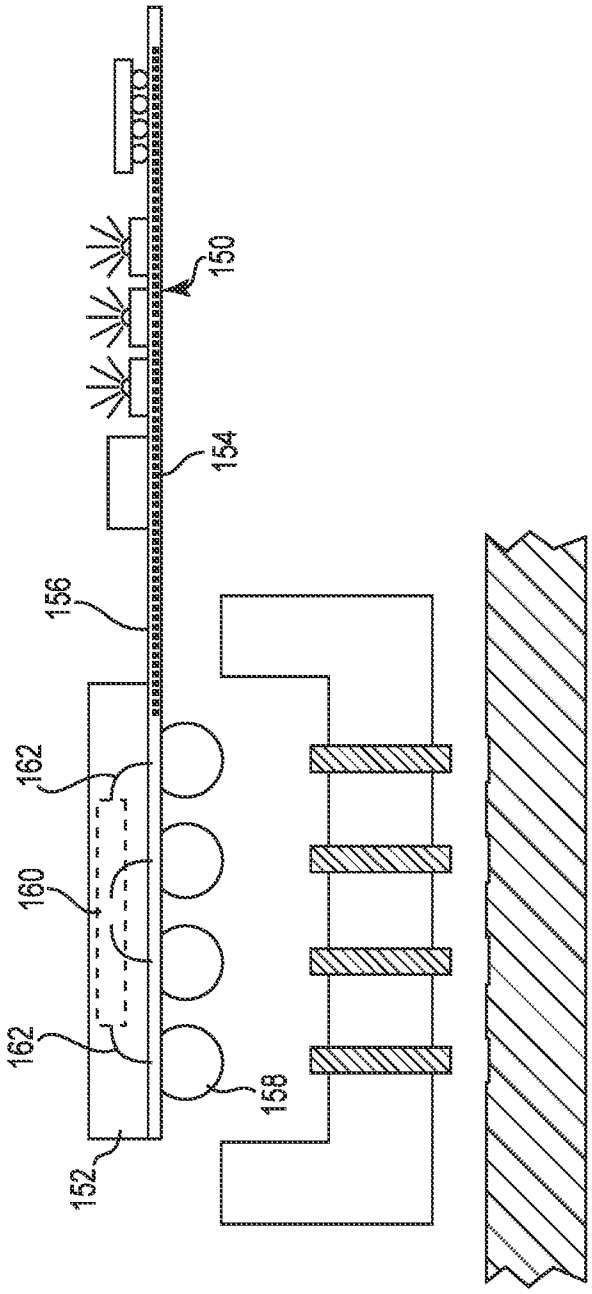

Fig. 4

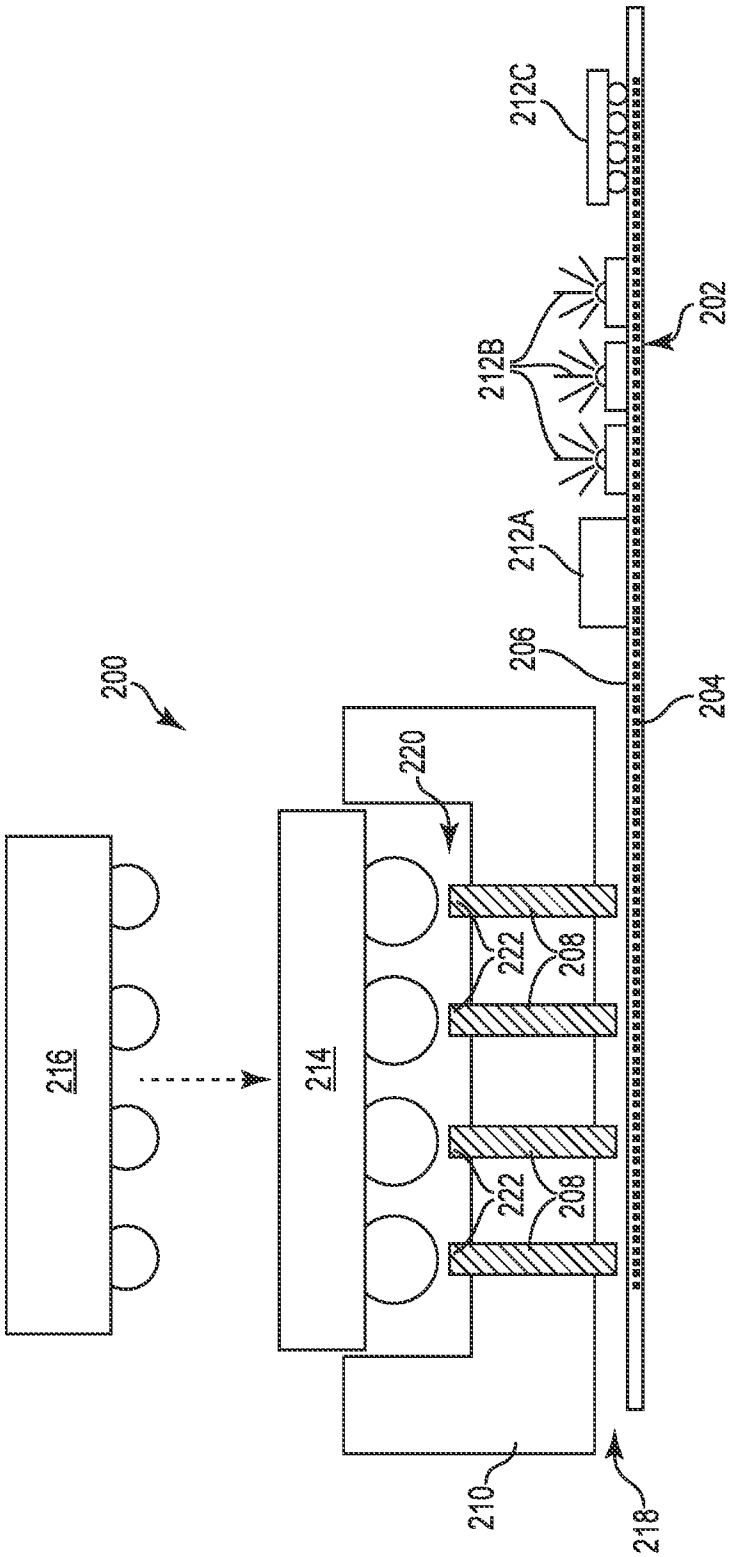

Fig. 5

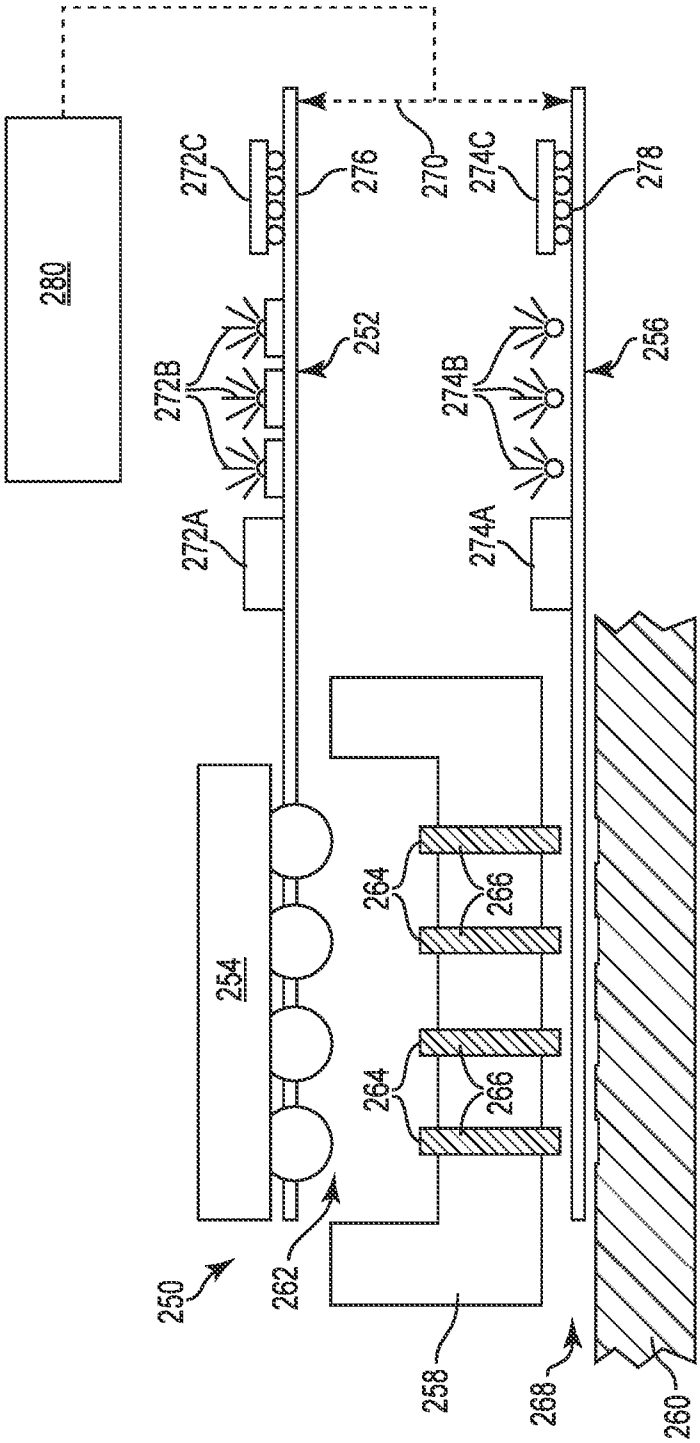
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Fig. 6

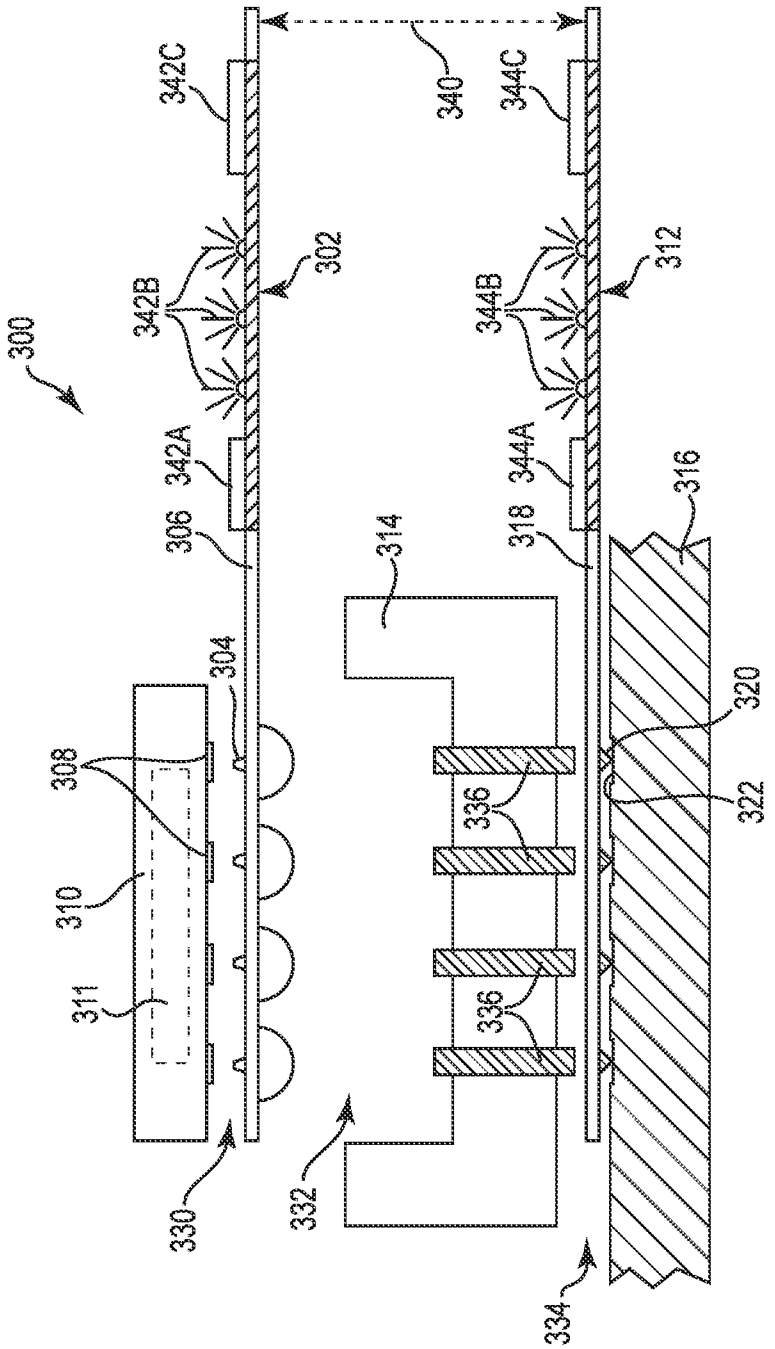
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Fig. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/036377

A CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G01R 31/02 (2010.01)
USPC - 324/765
According to International Patent Classification (IPC) or to both national classification and IPC

B FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - G01R 31/02 (2010 01)
USPC - 324/754, 755, 756, 759, 763, 765

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO EAST System

C DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
Y	US 2002/0062200 A1 (MORI et al) 23 May 2002 (23 05 2002) entire document	1-23
Y	US 2004/0174180 A1 (FUKUSHIMA et al) 09 September 2004 (09 09 2004) entire document	1-23
Y	US 5,509,019 A (YAMAMURA) 16 April 1996 (16 04 1996) entire document	1-23
Y	US 2007/0273394 A1 (TANNER et al) 29 November 2007 (29 11 2007) entire document	1-23
Y	US 2002/0105080 A1 (SPEAKMAN) 08 August 2002 (08 08 2002) entire document	1-23
Y	US 2003/01 17161 A1 (BURNS) 26 June 2003 (26 06 2003) entire document	7-1 1, 15, 16, 22, 23

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- **"P" document published prior to the international filing date but later than the priority date claimed**
- **"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention**
- **"X" document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone**
- **"Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art**
- **"&" document member of the same patent family**

Date of the actual completion of the international search
23 July 2010

Date of mailing of the international search report
28 JUL 2010

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PCTOSP 571-272-7774

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