

- [54] **MULTIPLEXED ALARM TRANSMISSION  
SYSTEM HAVING ALARM STORAGE  
CIRCUITS**
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- [51] **Int. Cl. .... G08b 25/00, G08b 26/00**
- [58] **Field of Search .... 340/412, 409, 413**

[56] **References Cited**

## UNITED STATES PATENTS

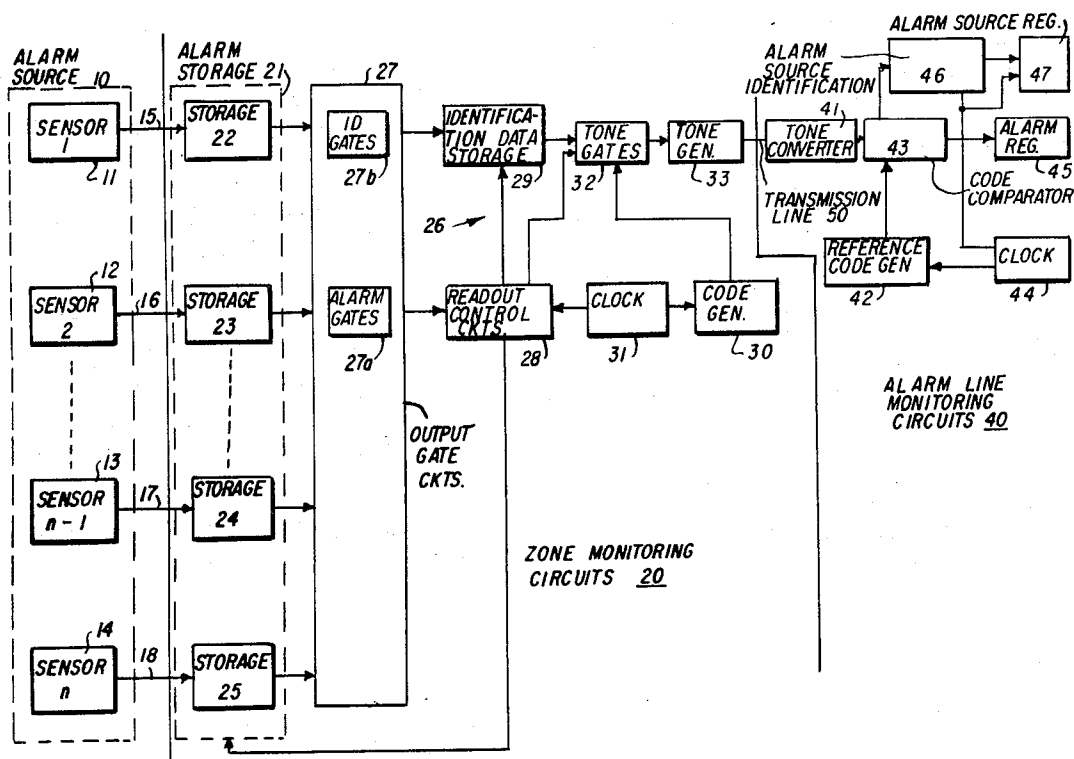
|           |         |                 |         |
|-----------|---------|-----------------|---------|
| 3,293,605 | 12/1966 | Moore .....     | 340/412 |
| 3,611,363 | 10/1971 | McCrea .....    | 340/412 |
| 3,636,546 | 1/1972  | Lomonaco .....  | 340/409 |
| 3,710,372 | 1/1973  | Andersson ..... | 340/409 |

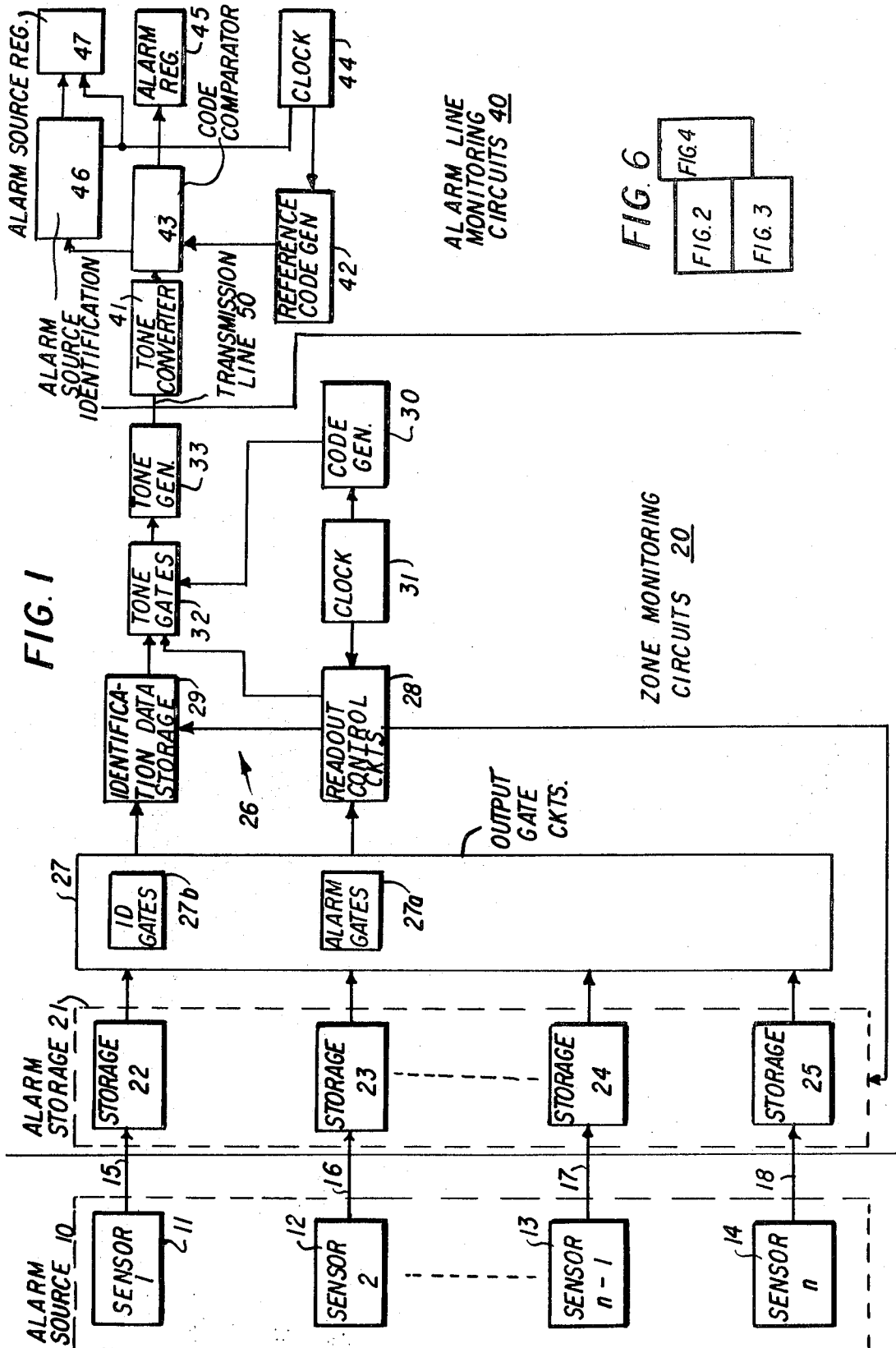
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Verbeck & Wager

**ABSTRACT**  
An alarm transmission system for transmitting alarm

information provided by a plurality of alarm sources to a central monitor over a common transmission line includes zone monitoring circuits having a code generator for generating a line monitoring code comprised of a continuous sequence of bits, for transmission over the transmission line to the central monitor, alarm storage circuits which provide separate storage locations for storing alarm outputs provided by each alarm source, and alarm readout circuits operable in response to an alarm output provided by an alarm source to complement the next bit of the line monitoring code generated to indicate that an alarm has been provided and to thereafter selectively complement successive bits of the line monitoring code generated to represent the source of the alarm. Alarm line monitoring circuits at the central monitor include a code comparator which compares each bit of the line monitoring code with bits of a reference code comprised of a sequence of code bits in which each bit is normally identical with a corresponding bit of the line monitoring code at any given time. Whenever a bit of the line monitoring code differs with the corresponding bit of the reference code, an alarm indication is provided at the central monitor, and alarm source identification circuits are enabled to scan subsequent bits of the line monitoring code to determine the source of the alarm.

### 15 Claims, 6 Drawing Figures





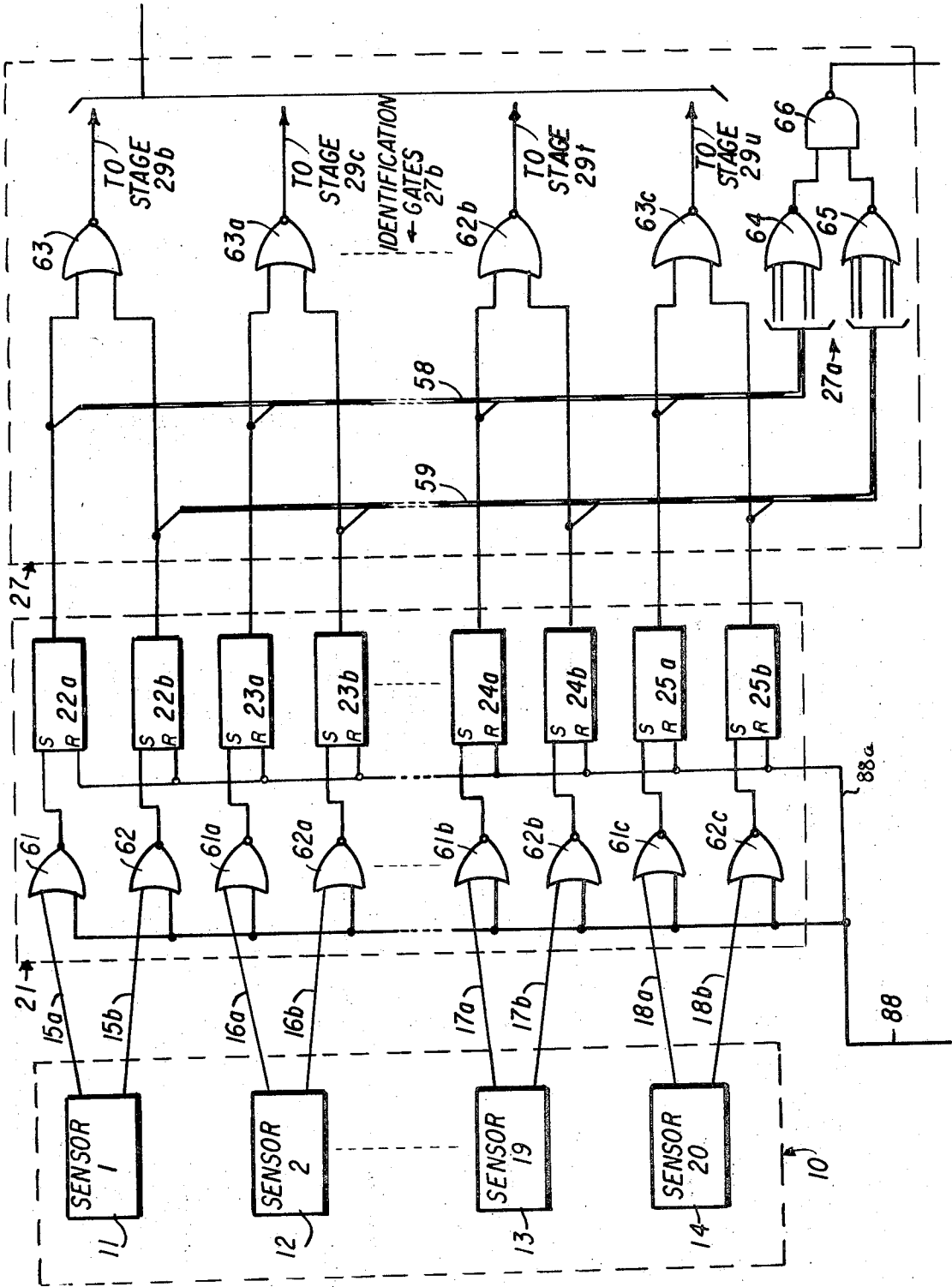


FIG 2

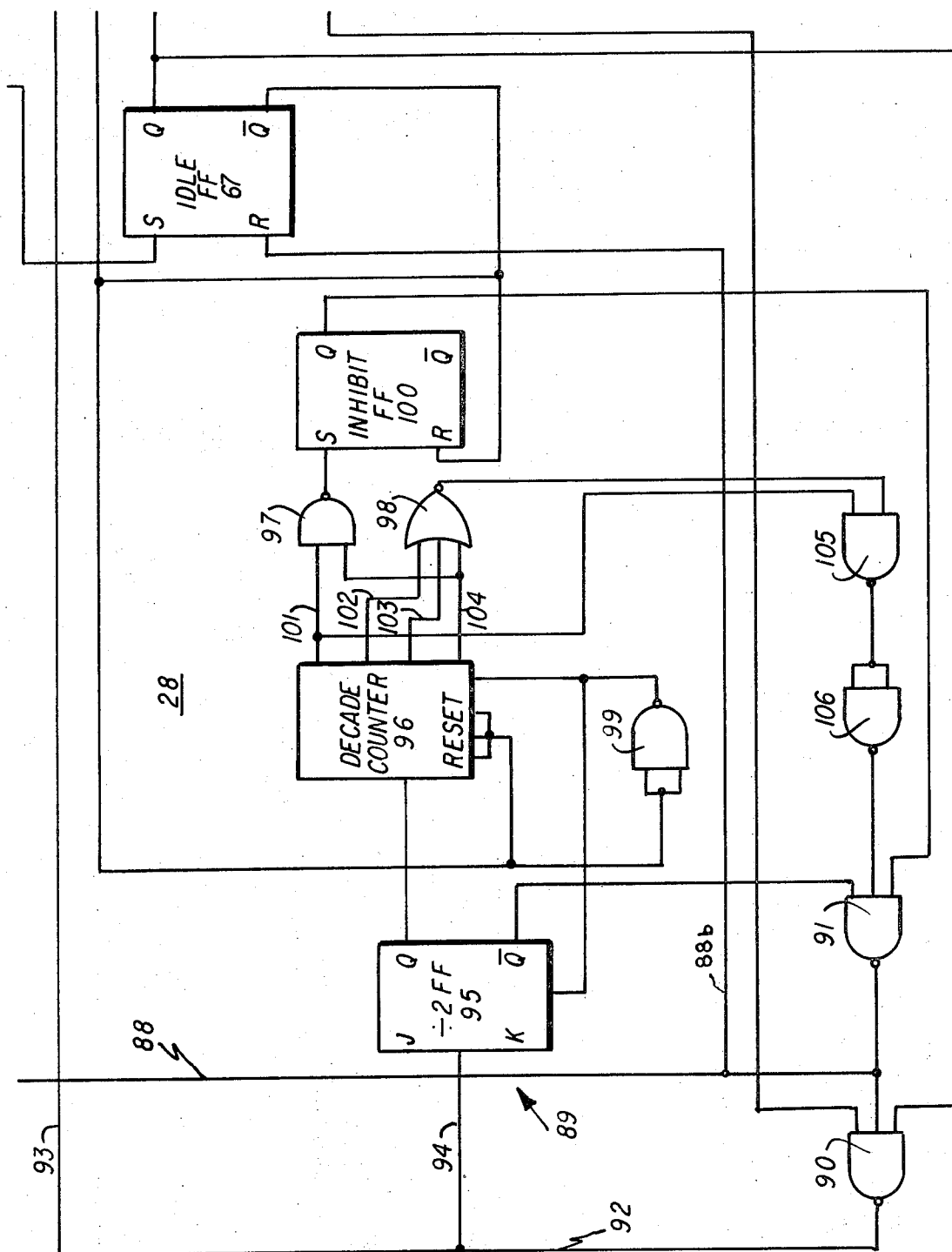
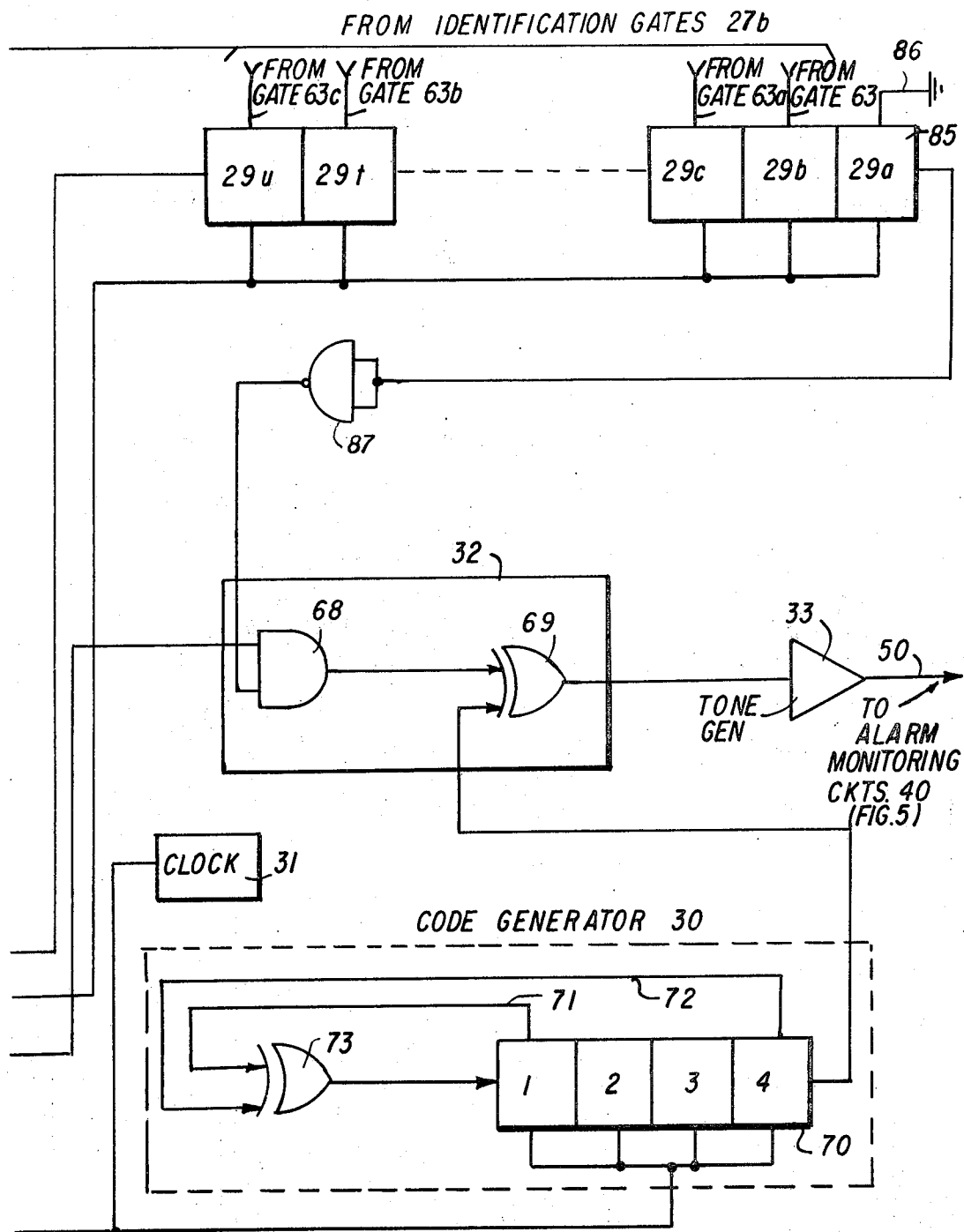
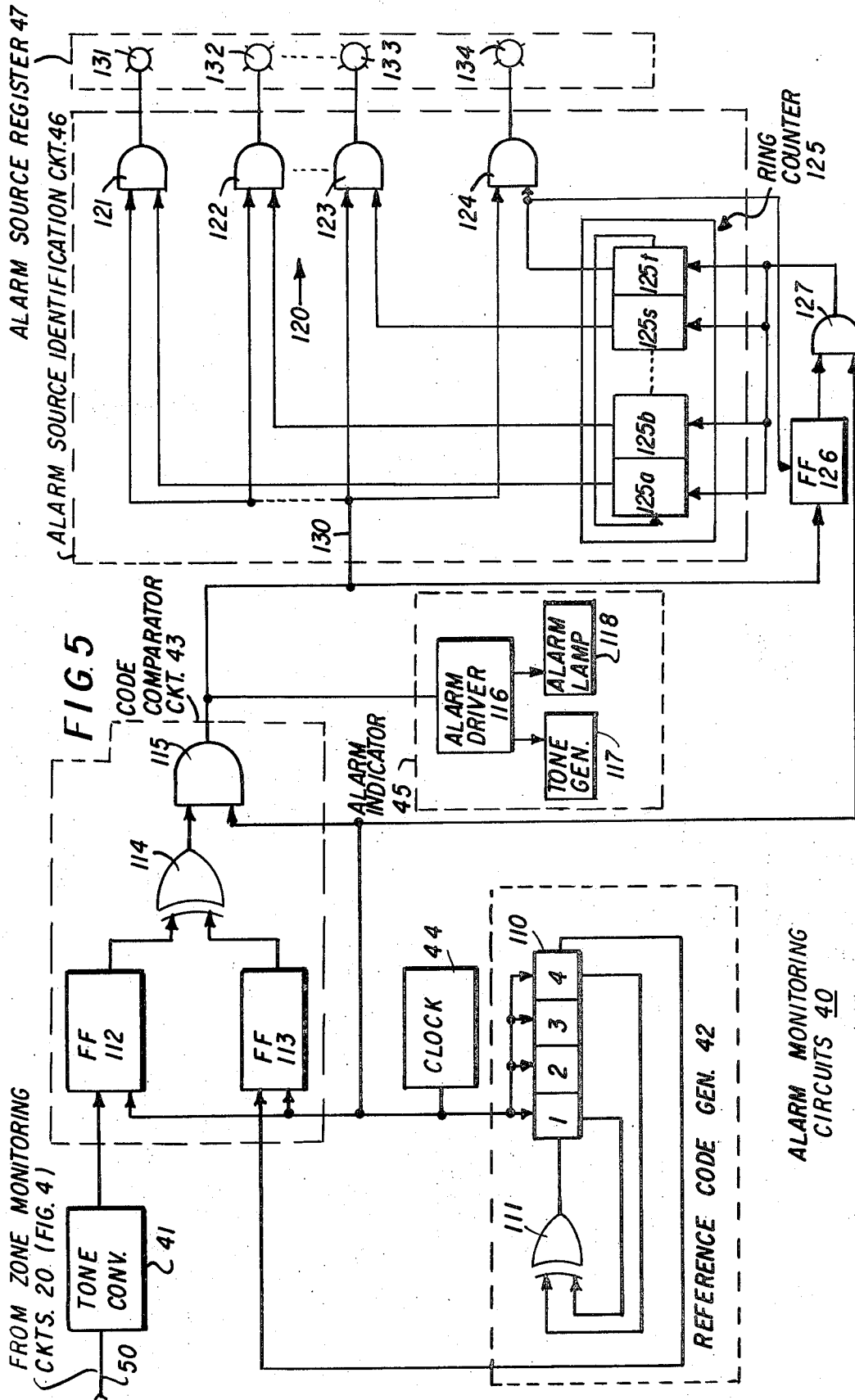


**FIG. 3**

FIG. 4





# MULTIPLEXED ALARM TRANSMISSION SYSTEM HAVING ALARM STORAGE CIRCUITS

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention relates to remote alarm monitoring systems, and, more particularly to a multiplexed alarm transmission system wherein alarm information from a plurality of alarm sensors is transmitted to a central monitor over a single transmission line.

### 2. Description of the Prior Art

In security systems, it is frequently necessary to interconnect a multiplicity of sensors to one central monitor. Typically, the sensors are separated by relatively short distances as, for example, when employed for detecting unauthorized entry of classrooms in a school, while the central monitor could be a relatively large distance away from any of the sensors as, for example, when located in the school administration building.

When the distance over which alarm information must be transmitted is great, the transmission lines which carry such alarm data must be protected as, for example, through the use of a line monitoring code. To minimize alarm data transmission costs and to enhance the security of the alarm transmission system when alarm data must be transmitted over long distances, it is desirable to employ a single transmission line connected between the central monitor and a monitoring location near the alarm sensors. Therefore, there exists a need for a multiplexed alarm data transmission system which permits multiple sensors to be connected to a central monitor over a single secured transmission line while transmission line complexity and costs of associated multiplexing circuits are minimized.

In general, there are two types of multiplexing arrangements, namely frequency division multiplexing and time division multiplexing, which can be used to transmit data from a plurality of sources to a central location.

Frequency division multiplexing systems require a plurality of tone generators including an individual tone generator for each data source. The information from different sources is coded by tones of different frequencies, and coded tones representing the data from all of the sources is transmitted over the transmission line simultaneously. Filter circuits are required at the central monitor to separate the coded tones and a plurality of tone detectors are needed to detect the tones transmitted from each source.

In time division multiplexing systems, information from a plurality of data sources is transmitted over the line on a shared time basis. Accordingly, only one tone generator and tone detector are required, and thus, the cost of the data transmission circuits is less than those required in systems employing frequency division multiplexing. However, the use of time division multiplexing has not found much acceptance in the security area. There is a prevailing feeling that a necessary condition for maximum security requires continuous monitoring of all protected areas. Thus, any time division multiplexing system which inherently results in a brief interruption between a sensor and the central monitor to provide a time interval for interleaving of the signals from a plurality of sensors has not been well accepted. Part of this disfavor results from the fear that a momentary alarm indication provided by a given sensor may

occur between the two instants at which the output of such sensor is sampled and that such alarm indication may not be detected.

## SUMMARY OF THE INVENTION

The present invention provides a secure line alarm transmission system which employs a time division multiplexing arrangement for transmitting alarm information provided by a plurality of alarm sensors to a central monitor over a single communication line and which includes alarm storage means for storing alarm indications provided by the alarm sensors. Accordingly, alarm indications will not be missed even though a time division multiplexing arrangement is used for monitoring the status of a plurality of alarm sensors.

In accordance with one embodiment of the invention, the multiplexed alarm transmission system includes zone monitoring means for monitoring the status of a plurality of alarm sensors, each located in a different area to be protected, and for effecting the transmission of alarm information provided by the sensors to a central monitor over a transmission line. The zone monitoring means includes alarm storage means which provides separate locations for storing alarm outputs provided by each sensor and readout means responsive to alarm outputs provided by one or more of the sensors to effect readout of the alarm storage means to enable transmission of alarm information to the central monitor.

The zone monitoring means further includes code generator means for generating a line monitoring code comprised of a known sequence of code bits for transmission via the transmission line to the central monitor to normally indicate that the transmission line is secure.

Whenever an alarm indication is provided by one or more of the sensors, the readout means is operable to provide an alarm code comprising an alarm bit which indicates the detection of an unauthorized entry of one of the protected areas and a plurality of identification bits which represent the status of all of the alarm sensors, a separate identification bit being provided for each sensor. The bits of the alarm code sequence which represent the condition of a sensor (or sensors) providing an alarm are different from corresponding bits of the monitor code which would normally be provided by the code generator means whereas the bits of the alarm code sequence which represent the conditions of sensors in secure areas are the same as corresponding bits of the monitoring code.

The central monitor includes reference code generator means which generates a sequence of code bits which is identical to the bit sequence normally provided by the code generator means associated with the zone monitoring means. The central monitor also includes comparator means which accepts the coded bits transmitted to the central monitor over the transmission line from each alarm source and compares such bits with the reference code bits generated by the reference code generator means. Under normal conditions (i.e., when the transmission line and all protected areas are secure), the sequence of bits received from the zone monitoring means will be identical with the sequence of bits provided by the reference code generator means.

However, whenever an alarm indication is provided by one or more of the alarm sources, the alarm code transmitted from the zone monitoring means will indi-

cate the alarm condition and the identification of the source of the alarm. Accordingly, whenever a bit of the code sequence transmitted from the zone monitoring means fails to compare with the corresponding bit of the reference code sequence, an alarm indication is provided at the central monitor. Thereafter, identification bit decoding means of the central monitor is enabled to be responsive to the bits of the received code sequence which represent the conditions of the alarm sensors to determine the source of the alarm.

Thus, the alarm transmission system of the present invention provides an alarm indication at the central monitor whenever an alarm is provided by one or more of the sensors. Thereafter, the origin of the alarm is determined through readout of the alarm storage means to effect the generation of an identification word comprised of a plurality of bits, each bit of which represents the status of a different alarm sensor.

Both the alarm bit and the bit representing the condition of the sensor indicating an alarm may effect registration of an alarm indication at the central monitor. Thus, if for some reason one of the bits was not detected at the central monitor, the other bit could initiate the indication of the alarm condition at the central monitor.

In a described embodiment of the invention, the code generator means and the reference code generator means each are operable to provide code bits in a known yet pseudo-random sequence. Since the random line monitoring code thus provided cannot easily be anticipated, the system provides protection from tampering with the communication line. Severing of the line or the injection of signals onto the line will cause the system to indicate an alarm.

Moreover, in accordance with a feature of the invention, alarm information is transmitted to the central monitor by selectively modifying bits of the random line monitoring code. For example, whenever an alarm indication is provided by one of the sensors, the readout means is effective to complement the next sequential bit of the line monitoring code generated after the alarm indication is provided. Thereafter, the readout means provides a sequential scan of the conditions of all of the alarm sensors.

If the condition of a sensor scanned indicates the associated protected area is secure, the random bit generated by the code generator means will be passed unaltered to the transmission line. If, on the other hand, the scanned sensor is indicating an alarm condition, the random bit generated will be complemented as the bit is passed to the line. Thus, in response to an alarm, the first bit of the line monitoring code will be complemented indicating an alarm condition in one or more of the protected areas and thereafter as the alarm sensors are sequentially scanned, successive bits of the line monitoring code will each be complemented or passed unaltered to the transmission line in accordance with the conditions of the sensors.

Other advantages and features of the invention will become apparent from the following detailed description of the invention which makes reference to the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a multiplexed alarm transmission line security system provided by the present invention;

FIGS. 2-4 when assembled as shown in FIG. 6 show a schematic representation of the alarm storage and readout circuits of the system shown in FIG. 1;

FIG. 5 is a schematic representation of the alarm line monitoring circuits of the system shown in FIG. 1; and FIG. 6 shows how FIGS. 2-3 are to be assembled.

#### DESCRIPTION OF A PREFERRED EMBODIMENT

##### General Description

Referring to the block diagram of an exemplary illustration of the alarm transmission system shown in FIG. 1, the system comprises zone monitoring circuits 20 for effecting the transmission via a transmission line 50 of alarm information provided by a plurality of alarm sources 10 to alarm line monitoring circuits 40 at a central location which is remote from the location of the alarm sources 10.

The alarm sources 10 include a plurality of alarm sensors, such as sensors 11-14 shown in FIG. 1, each located in a different area to be protected. Each of the alarm sensors 11-14 may, for example, be an intrusion detector which provides an alarm output in response to the detection of an unauthorized entry of an area protected by such intrusion detector.

The zone monitoring circuits 20 include alarm data storage circuits 21 and alarm storage readout circuits 26 including output gating circuits 27, readout control circuits 28 and identification data storage circuits 29. The alarm storage circuits 21 include separate alarm storage circuits, such as storage circuits 22-25 for storing the alarm outputs provided by each of the alarm sensors 11-14, respectively.

The alarm sensors 11-14 are connected to the associated alarm storage circuits 22-25 via DC supervised lines 15-18, respectively. Such supervision provides for an alarm upon a change of more than 5 percent in a DC current which continuously flows in the lines 15-18. Thus, opening or shorting of any one of the lines 15-18 will immediately result in an alarm. Alarm information may be provided in the form of contact closures, as is customary in security systems.

The zone monitoring circuits 20 further include a code generator 30 which is driven by a clock 31 at a predetermined rate to generate a line monitoring or supervision code which is comprised of logic 1 and logic 0 bits in a known sequence. The bit sequence provided at the output of the code generator 30 is passed via a tone gate 32 to a tone generator 33 which converts the logic level bits of the line monitoring code into tone signals coded in frequency to represent the monitoring code. The tone generator 33 includes a dual frequency oscillator which is responsive to each logic 1 level bit to provide an output tone of a first frequency and responsive to each logic 0 level bit to provide a tone output of a second frequency. The sequence of coded tones thus provided is transmitted over the transmission line 50 to the alarm line monitoring circuits 40.

Under normal conditions, that is when none of the alarm sources 10 are providing an alarm, the line monitoring code being conducted over the transmission line 50 provides security for the transmission line 50 which interconnects the zone monitoring circuits 20 and the alarm line monitoring circuits 40.

The alarm line monitoring circuits 40 include a tone converter circuit 41, a reference code generator 42 and a comparator circuit 43. The tone sequence transmit-

ted from the zone monitoring circuits 20 is received by the tone converter circuit 41 and converted into logic 1 and logic 0 level bits representing the line monitoring code.

The reference code generator 42 is driven by a clock 44 to generate a reference code comprising a known sequence of bits in which each bit is normally identical with corresponding bits of the line monitoring code at any given time. The bits of the line monitoring code received from the zone monitoring circuits 20 are compared with corresponding bits of the reference code by the comparator circuit 43, and under normal conditions, the bits of the monitor and reference codes which are compared will be the same, indicating that the transmission line 50 is secure and that all protected areas are secure.

Whenever an unauthorized intrusion is detected in one or more of the protected areas, the alarm sensor, such as alarm sensor 11, in such area provides an alarm output which is extended via D.C. line 15 to alarm data storage circuits 21 and stored in the storage circuit 22 associated with alarm sensor 11. In response to the storing of an alarm output in one or more of the storage circuits, such as storage circuit 22, the readout circuits 26 will be enabled to effect the transmission of an alarm indication to the alarm line monitoring circuits 40 and to thereafter effect sequential readout of the status of the alarm sensors for all of the protected areas (as indicated by the alarm data stored in the alarm storage circuits 21) to enable the source of the alarm to be determined at the central monitor.

The outputs of all of the alarm data storage circuits 22-25 are combined by alarm gates 27a of the output gates circuits 27 to provide a control signal for the readout control circuits 28. The output gating circuits 27 also include identification gates 27b which extend each of the outputs of the alarm storage circuits, including storage circuits 22-25, over a separate path to inputs of the identification data storage circuits 29. The identification data storage circuits 29 may comprise a multistage serial shift register having a separate stage for each alarm storage circuit, such as circuits 22-25, and a further stage which normally stores an alarm bit. The output stage of the identification data storage circuits 29 stores the alarm bit, and the remaining stages store bits representative of the data stored in the alarm storage circuits 21, and thus the conditions of all of the alarm sensors 10.

Accordingly, when the alarm output provided by alarm sensor 11 is stored in the alarm storage circuit 22, such alarm output will be gated over the identification gates 27b to a predetermined stage of the multistage shift register of the identification data storage circuits 29. The alarm output is also gated over the alarm gates 27a to enable the readout control circuits 28 to gate clock pulses from the clock pulse generator 31 to the identification data storage circuits 29 in synchronism with the generation of code bits by the code generator 30 which is driven by the clock 31. Each clock pulse gated to the identification data storage circuits 29 will cause a different stored bit to be read out.

The readout control circuits 28 also provide a signal for enabling the tone gates 32 to follow the bits read out of the identification data storage circuits 29. Thus, the bits read out of the identification storage circuits 29 are effective to selectively modify bits of the monitor code generated by the code generator 30 in accordance

with the alarm information stored in the identification data storage circuits 29.

The alarm bit, which is the first bit read out of the identification data storage circuits 29, controls the tone gates 32 to complement the next bit of the monitor code which is provided after the alarm indication has been received by the zone monitoring circuits 20. Thereafter, as the identification data bits, representing the conditions of the alarm sensors, are read out in sequence, each bit which identifies an alarm sensor which is in the normal condition (indicating that the associated protected area is secure) will allow a code bit generated by the code generator 30 to pass unaltered to the tone generator 33. On the other hand, each bit which identifies an alarm sensor, such as sensor 11, which is providing an alarm output will control the tone gates 32 to complement a code bit generated by the code generator 30.

Thus, the modified line monitoring code or alarm code provided at the output of the tone gates 32 will include an alarm bit followed by a sequence of identification bits which indicate the status of each alarm sensor. The logic 1 and logic 0 level bits of the alarm code are converted into tone signals by the tone generator 33 and transmitted over the transmission line 50 to the alarm monitoring circuits 40.

The coded tone signals representing the alarm code are converted to logic level bits by the tone converter 41 and the bits of the resulting bit sequence are compared by the comparator circuit 43 with the bits of the reference code generated by the reference code generator 42. Since the first bit of the alarm code received is the alarm bit, which has been complemented, the compared bits will be different and the comparator circuit 43 will provide an output for enabling an alarm circuit 45 to indicate that an alarm has been provided by one or more of the alarm sources 10. In addition, the comparator circuit 43 will enable an alarm source identification circuit 46 to receive subsequent bits of the alarm code to enable determination of the source of the alarm. Consequently, when the identification bit representing the status of sensor 11 is received by the alarm line monitoring circuits 40, the alarm source identification circuits 46 will provide an output for enabling an alarm registration circuit 47 to provide an indication of the detection of an alarm provided by alarm sensor 11.

After all of the identification data bits have been read out of the identification data storage circuits 29, the readout control circuits are operable to clear the alarm storage circuits 21 and reset the identification data storage circuits 29 thereby returning the zone monitoring circuits 20 to the normal condition.

#### Detailed Description

A schematic representation of the zone monitoring circuits 20 is shown in FIGS. 2-4 when arranged in a side-by-side relationship as shown in FIG. 6. For purposes of illustration of the operation of the zone monitoring circuits 20, it is assumed that the zone monitoring circuits 20 monitor twenty alarm sensors, such as sensors 11-14 shown in FIG. 2.

The nature of many commercially available alarm sensors is such that separate alarm indications (as represented, for example, by changes in relay contact states) are available for intruder detection and for supervisory indication of sensor component malfunctions. The alarm transmission system of the present in-

vention provides for separate storage of both types of sensor information.

Accordingly, the alarm storage circuits 21 provide a pair of storage flip flops for each alarm sensor. For example, flip flops 22a-25a store intrusion alarm outputs provided by sensors 11-14, respectively in response to the detection of an unauthorized entry of the areas protected by sensors 11-14. Flip flops 22b-25b store supervisory alarm outputs provided by sensors 11-14 as the result of component malfunctions of sensors 11-14.

The intrusion alarm output of sensor 11 is connected over a DC supervised line 15a and a NOR gate 61 to the set input of the alarm flip flop 22a associated with sensor 11. The supervisory output of the sensor 11 is connected over a DC supervised line 15b and a NOR gate 62 to the set input of the supervisory flip flop 22b associated with sensor 11.

Similarly, the alarm outputs of sensors 12-14 are connected over respective D.C. supervised lines 16a-18a and NOR gates 61a-61c to the set inputs of alarm flip flops 23a-25a, and the supervisory outputs of sensors 12-14 are connected over respective D.C. lines 16b-18b and NOR gates 62a-62c to the set inputs of supervisory flip flops 23b-25b, respectively.

A logic 1 level signal on lines 15a-18a and 15b-18b represents a normal condition, and a logic 0 level on one or more of the lines 15a-18a or 15b-18b indicates that an intrusion or supervisory alarm indication is being provided by the sensor connected to such line.

An enabling signal at logic 0 level is normally extended over conductor 88 from the readout circuits 26 to each of the NOR gates 61, 61a-61c and 62, 62a-62c. Accordingly, Whenever one or more of the alarm sensors, such as alarm sensor 11, provides an intrusion alarm output over conductor 15a or a supervisory alarm output over conductor 15b, such alarm outputs will enable the associated NOR gates 61 or 62. Whenever NOR gate 61 is enabled, the alarm flip flop 22a will be set and whenever NOR gate 62 is enabled, the supervisory flip flop 22b will be set. The alarm flip flop 22a and the supervisory flip flop 22b, when set in response to an alarm indication by the associated sensor 11, will remain set, storing such alarm indications until reset by the readout circuits 26. Thus, an alarm indication provided by any of the alarm sensors, such as sensor 11, will be stored in the alarm storage circuits 21 until the alarm indication has been transmitted to the central monitor.

Each of the alarm storage flip flops, such as flip flops 22a-25a, and each of the supervisory flip flops, such as flip flops 22b-25b, normally provide a logic 0 output when associated sensors 11-14 are not providing an alarm output.

The outputs provided by the alarm flip flops 22a-25a and the supervisory flip flops 22b-25b are combined by alarm gates 64-66 of the output gating circuits 27a and 27b. For example, the outputs of the alarm flip flops, such as flip flops 22a-25a, are extended via cable 58 to individual inputs of a NOR gate 64 of output gates 27a. The outputs of the supervisory flip flops, such as flip flops 22b-25b, are extended via cable 59 to individual inputs of a NOR gate 65. The outputs of NOR gates 64 and 65 are connected to inputs of a NAND gate 66.

Whenever all of the alarm flip flops, such as flip flops 22a-25a, and all of the supervisory flip flops, such as flip flops 22b-25b are in a reset condition, NOR gates 64 and 65 will be enabled, thereby enabling alarm gate

66. NOR gate 64 will be disabled whenever an alarm output is stored in one or more of the alarm flip flops, and NOR gate 65 will be disabled whenever an alarm output is stored in one or more of the supervisory flip flops. The alarm gate 66 will be disabled whenever either gate 64 or 65 is disabled, to thereby provide an output which enables the readout control circuits 26 to effect the readout of the alarm data stored in the alarm storage circuits 21.

The outputs of the alarm data storage circuits 21 are also extended over identification gates 27b, including gates 63, 63a, 63b and 63c, to the identification data storage circuits 29 shown in FIG. 4, to enable the conditions of the alarm sensors (as represented by the presence or absence of alarm outputs in the alarm data storage flip flops) to be read out sequentially. The identification data storage circuits 29 may comprise a multi-stage shift register 85 which, in the present example, has 21 stages 27a-27u, including separate stages 27b-27u for each of the twenty sensors which comprise the alarm sources 10 monitored by the zone monitoring circuits 20.

In accordance with the present example, the outputs of the alarm flip flop and the supervisory flip flop associated with a given sensor are extended over a common identification gate to a preassigned stage of the identification data register 85. Thus, for example, the outputs of alarm flip flop 22a and supervisory flip flop 22b associated with sensor 11 are extended over NOR gate 63 to stage 29b of the identification data register 85, and the outputs of flip flops 23a and 23b associated with sensor 12 are extended over gate 63a to stage 29c of register 85. The outputs provided by the other 18 sensors, including sensors 13 and 14, are extended over separate identification gates, such as gates 63b, and 63c, to stages 29d-29u of register 85.

The inputs provided over the identification gates 27b to the stages 29a-29u are read into the register stages when an enabling signal is provided by a NAND gate 90 of the data readout control circuits 28 as will be shown hereinafter.

Whenever the pair of alarm and storage flip flops associated with a given sensor, such as flip flops 22a, 22b associated with sensor 11, are in the reset condition, the identification gate 63 connected to the outputs of such flip flops will be enabled and a logic 1 level bit will be stored in the corresponding stage 29b of the identification data register 85. If either one of the flip flops 22a, 22b is set in response to an alarm or supervisory output provided by the associated sensor 11, the identification gate 63 will be disabled and a logic 0 level bit will be stored in stage 29b of the register 85.

In addition, the output stage 29a of the identification data register 85 stores a logic 0 level alarm bit provided by a wired input 86 which is connected to ground.

Thus, under normal conditions, when no alarm indications are being provided, the identification data register 85 stores a logic 0 level alarm bit in stage 29a and logic 1 level bits in sensor identification stages 29b-29u. When an alarm indication is provided by an alarm sensor, such as sensor 11, the identification data register will store logic 0 bits in stages 29a and 29b and logic 1 bits in stages 29c-29u.

The storage locations 29b-29u are preassigned to the twenty alarm sensors 10 to enable identification of the alarm source providing an alarm by the alarm line monitoring circuits 40 (FIG. 5).

It is pointed out that although the outputs of both the alarm flip flop and the supervisory flip flop for a given alarm sensor are shown to extend to a common stage of the identification data storage register 85, it is also possible to provide separate storage locations in the identification data storage register 85 for the two types of alarm information. In such case, the central monitor would receive alarm information indicating both the source of an alarm indication and the nature of the alarm indication, that is, whether there is an intrusion of the indicated area of a component malfunction in the indicated sensor.

### Alarm Data Transmission Circuits

The alarm gate 66 (FIG. 2) controls a system idle flip flop 67 shown in FIG. 3, which is set by a logic level output provided by the alarm gate 66 whenever gate 66 is disabled. When the idle flip flop is set, a logic 1 level signal at the Q output of the idle flip flop 67 controls the tone gates 32 shown in FIG. 4, and the readout control circuits 28 shown in FIG. 3, to effect the transmission of the alarm information present in the alarm storage circuits 21 to the central monitor.

The tone gates 32 include an AND gate 68 and an Exclusive OR gate 69. The AND gate 68 has a first input connected to the Q output of the idle flip flop 67 and a second input connected to the output of an inverter 87 which has an input connected to the output of the identification data storage circuits 29. The output of the AND gate 68 is connected to a first input of the Exclusive OR gate 69. A second input of the Exclusive OR gate is connected to the output of the code generator 30.

The code generator 30 generates a known sequence of random bits which form a line monitoring code for the transmission line 50 which carries alarm information from the zone monitoring circuits 20 to the alarm line monitoring circuits 40.

One code generator suitable for this purpose is described in the copending application U.S. Ser. No. 193,450 of John C. Donovan, Ramesh, Krishnaiyer and Frank J. Esser, which was filed on Oct. 28, 1971.

In an exemplary embodiment, the code generator 30 includes a four stage shift register 70 having feedback connections over conductors 71 and 72 from the first and fourth stages, respectively, connected through an Exclusive OR circuit 73 to the input of the first stage. The Exclusive OR circuit 73 provides a logic 0 output whenever the two inputs to the Exclusive OR circuit are the same logic level, and provides a logic 1 output whenever the inputs are different logic levels. Code generator 30 preferably includes at least a 16 stage register and may be as much as a 32 stage register capable of generating a pseudo-random sequence of bits, the length of the sequence being given by the relationship  $2^N - 1$ , where N is the number of stages which comprise the shift register of the code generator circuit 30. In the present example, for convenience only, a four stage register 70 is shown, and 15 bits are provided.

To illustrate the operation of the code generator 30, it is assumed that initially all stages of the register 70 state logic 1 level bits and that the register 70 is thereafter cycled under the control of clock pulses provided by a clock pulse generator 31. The sequence of words given in Table I will appear in the stages of the shift register 70 as successive clock pulses are provided.

TABLE I

| Register Stage<br>(Initial) |    | 1 | 2 | 3 | 4 |
|-----------------------------|----|---|---|---|---|
| Clock Pulse                 |    | 1 | 1 | 1 | 1 |
| 1                           | 5  | 0 | 1 | 1 | 1 |
| 2                           |    | 1 | 0 | 1 | 1 |
| 3                           |    | 0 | 1 | 0 | 1 |
| 4                           |    | 1 | 0 | 1 | 0 |
| 5                           |    | 1 | 1 | 0 | 1 |
| 6                           |    | 0 | 1 | 1 | 0 |
| 7                           |    | 0 | 0 | 1 | 1 |
| 8                           |    | 1 | 0 | 0 | 1 |
| 9                           | 10 | 0 | 1 | 0 | 0 |
| 10                          |    | 0 | 0 | 1 | 0 |
| 11                          |    | 0 | 0 | 0 | 1 |
| 12                          |    | 1 | 0 | 0 | 0 |
| 13                          |    | 1 | 1 | 0 | 0 |
| 14                          |    | 1 | 1 | 1 | 0 |
| 15                          |    | 1 | 1 | 1 | 1 |

Since initially, stages 1 and 4 both contain binary ones, the Exclusive OR circuit 73 provides a logic 0 output which is gated into the first stage of the shift register 70 with receipt of the first sync pulse as can be seen in step 1. The sync pulse also shifts the logic 1's from stages 1-3 to stages 2-4, respectively. When the second clock pulse is received, the outputs of stages 1 and 4 are different, and accordingly the Exclusive OR circuit 73 will provide a logic 1 output which will be gated into first stage of the shift register 70 as the bits in stages 1 through 3 are gated into stages 2-4, respectively. In a similar manner, for clock pulses 3-14, outputs fed back to the input of the first stage cause the sequence of words given in Table I to be generated.

The sequence given in Table I repeats after the 15 clock pulse. Thus, it is seen that 15 pseudo-random words are provided when the number of stages of the shift register is equal to four. The total number of combinations of n bits is  $2^n$ , so only one combination is missing. The missing multi-bit word is 0000 which can be seen to repeat itself or have a trivial cycle of one in the code generator circuit.

The random bit sequence generated by the code generator 30 is extended to the Exclusive OR gate 69. Under normal conditions, that is when no alarm indications are being provided by the alarm sources 10, the idle flip flop 67 is reset, and accordingly AND gate 68 is disabled by the logic 0 level at the Q output of the idle flip flop 67. In such case, the random bits provided by the code generator 30 are passed over the Exclusive OR gate 69 unaltered to the tone generator 38 which is connected to the output of the Exclusive OR gate 69.

The tone generator 33 comprises a dual frequency oscillator which is responsive to each logic 1 level bit of the random sequence to provide a tone signal of a first frequency and is responsive to each logic 0 level bit provided by the random code generator 30 to provide a tone signal of a second frequency. The tone sequence thus generated is transmitted to the central monitoring area via transmission line 50.

### Alarm Generation

Whenever an alarm output is provided by any of the alarm sensors 10, the idle flip flop 67 will be set, when the alarm gate 66 is disabled. When the system idle flip flop 67 is set, the output of the idle flip flop is extended to a NAND gate 90. A second input to the NAND gate 90, provided by NAND gate 91, is a logic 1 level. Accordingly, NAND gate 90 will be enabled to follow the output of the clock pulse generator 31 which is extended to a third input of the NAND gate 90. Each gated clock pulse thus provided is extended over con-

ductors 92 and 93 to the identification data shift register 85.

The first clock pulse gated to the shift register 85 will cause the signal outputs of the identification gates 27b to be read into the shift register 85 and will thereafter effect the readout of the alarm bit stored in the output stage 27a of the register 85. Thereafter, the 20 identification bits, representing the status of the twenty alarm sources 10, will be read out sequentially.

Each bit read out of the identification data storage register 85 is extended over inverter 87 to an input of AND gate 68 which is enabled by the system idle flip flop 67 to follow the bits read out of the register 85. Thus, gate 68 will be enabled by each logic 1 level bit read out of the register 85 and will be disabled by each logic 0 level bit read out of the register 85.

When the system is indicating an alarm condition as represented by the idle flip flop being set, the clock pulses provided by clock pulse generator 31 to effect the generation of random bits by the code generator 30 are also gated via gate 90 to the shift register 85 to effect readout of bits of the identification word stored in the register 85. Each logic 0 level bit read out of the register 85 will control the tone gates 32 to complement the random bit provided by the code generator 30, and each logic 1 level bit read out of the register 85 will control the tone gates 32 to pass the random bit unaltered to the tone generator 33.

Thus, since the alarm bit is a logic 0 level bit, the first random bit generated after the idle flip flop 67 is set will be complemented by the tone gate circuits 32. Thereafter, as each identification bit is read out of the register 85 by successive clock pulses, the random bits generated as the result of such clock pulses will be complemented or passed unaltered to the tone generator 33 in accordance with the identification data stored in the register 85. The tone generator 33 will thus be responsive to the outputs of the tone gate circuits 32 to generate a sequence of tone signals coded to represent the identification data word stored in the register 85.

#### System Reset

The gated clock pulses which effect readout of the identification data word stored in the register 85 are also extended via conductors 92 and 94 to a counting circuit 89 which includes a divide-by-two flip flop 95, a decade counter 96, associated gating circuits 97-99, and an inhibit flip flop 100. The counting circuit 89 is operable to count the number of pulses gated to the shift register 85 and to effect reset of the zone monitoring circuits 20 after a number of pulses sufficient to effect readout of the 21 bit word have been supplied to the register 85.

The clock input of the divide-by-two flip flops 95 is connected over conductors 94 and 92 to the output of gate 90. The Q output of flip flop 95 is connected to the clock input of the decade counter 96 and the Q output of the flip flop 95 is connected to an input of NAND gate 91.

The decade counter 96 has four outputs 101-104. Outputs 101 and 104 are connected over a NAND gate 97 to the set input of the inhibit flip flop 100. Outputs 102-104 are connected over a NOR gate 98 to an input of a NAND gate 105. Output 101 of the decade counter 96 is connected to a second input of gate 105. The output of gate 105 is connected over an inverter 106 to a second input of gate 91. The Q output of the

inhibit flip flop 100 is connected to a third input of gate 91.

In operation, the counting circuit 89 counts the clock pulses gated to the shift register 85, and at the twenty second clock pulse, the inhibit flip flop 100 is set by an output provided by gate 97 responsive to outputs of the decade counter 96. The logic 1 level provided at the Q output of the inhibit flip flop 100 is extended to an input of gate 91, enabling gate 91 which has second and third inputs at logic 1 levels.

When enabled, gate 91 provides an end of shift pulse which inhibits gate 90 to prevent the passage of further clock pulses. The end of shift pulse is also extended over conductors 88 and 88a to the reset inputs of all of the alarm and supervisory flip flops, including flip flops 22a-25a and 22b-25b, causing all of the alarm and supervisory data storage flip flops to be reset. The end of shift pulse is further conducted over conductors 88 and 88b to the reset input of the idle flip flop 67, resetting the idle flip flop 67.

When the idle flip flop 67 is reset, the logic 1 level provided at the Q output thereof resets the inhibit flip flop 100, the counting flip flop 95, the decade counter 96 and identification data register 85 whereby the zone monitoring circuits 20 are restored to their idle condition. If there are any further alarm indications being provided by any of the alarm sensors over associated NOR gates (such as gates 61 and 62 for sensor 11) the corresponding alarm and/or supervisory flip flops (22,23) associated with such area will be set when the end of shift pulse terminates, and the alarm read out sequence will be reinitiated.

#### Alarm Monitoring Circuits

The coded tone sequence provided by the zone monitoring circuits 20 is transmitted via cable 50 to the alarm monitoring circuits 40 (FIG. 5) at the central monitoring area. As has been indicated, the coded tone sequence provides for supervision of the interconnecting line 50 as well as for the transmission of alarm information and the identification of the source of an alarm.

The monitoring circuits 40 includes a tone detecting and converter circuit 41 which converts the dual frequency code tone signals generated by the zone monitoring circuits 20 into a logic level code. The output of the tone converter 41 is extended to a code comparator circuit 43 which compares the bits of the received sequence of code bits with corresponding bits of a reference code provided by a reference code generator 42. The reference code generator 42 is similar to the code generator 30 of the zone monitoring circuit 20 and operates in sequence with code generator 30 to provide a sequence of random bits in which each bit is normally identical with a corresponding bit of the random bit sequence at any given time. In an exemplary embodiment, the reference code generator 42 comprises a four-stage shift register 110 having outputs of stages 1 and 4 fed back over an Exclusive OR circuit 111 to the input of the first stage. The reference code generator 42 is driven by clock pulses provided by a clock pulse generator 44 to provide the sequence of random bits shown in Table I that is provided by the code generator 30.

The code comparator circuit 43 includes a pair of flip flops 112, 113, an Exclusive OR gate 114 and an AND gate 115. The set input of flip flop 112 is connected to the output of tone converter circuit 41. The set input

of flip flop 113 is connected to the output of the reference code generator 42. Clock inputs of the flip flops 112, 113 are connected to the output of the clock pulse generator 44.

The outputs of the flip flops 112, 113 are extended to separate inputs of the Exclusive OR gate 114. The output of the Exclusive OR gate 114 is extended to an input of AND gate 115 which has a second input connected to the output of the clock pulse generator 44.

The AND gate 115 of the code comparator circuit 43 is enabled whenever corresponding bits of the reference code and the code received from the zone monitoring circuits 20 are different. The AND gate 115 controls an alarm indication circuit 45 which, for example, may provide an audible and a visual alarm indication at the central monitor.

The AND gate 115 also enables an alarm source identification circuit 46 to be responsive to the identification bits of the alarm code extended to the alarm source identification circuit 46 from the output of the code comparator 43 to identify the source of the alarm. The alarm source identification circuit 46 controls an alarm source registration circuit 47 which, for example, may provide a visual registration of the source of the alarm.

Under normal conditions, as each bit of the received line monitoring code is extended over the tone converter 41 to the set input of the flip flop 112, the corresponding bit of reference code generated by the reference code generator 42 and extended to the set input of flip flop 113 will be identical with the bit extended to flip flop 112. The bits provided at the inputs of flip flops 112, 113 are clocked to the outputs of the flip flops 112, 113 by the clock pulse which effects the generation of the reference code bit.

Whenever the bits provided at the outputs of flip flops 112, 113 are the same, the Exclusive OR gate 114 connected to the outputs of flip flops 112, 113 will provide a logic 0 level output which maintains AND gate 115 disabled.

Whenever the zone monitoring circuits 20 are providing an alarm code, bits of the line monitoring code are selectively complemented to indicate that an alarm output has been provided by one or more of the alarm sources 10 and to identify the source of the alarm. Thus, when the alarm bit is received at the alarm monitoring circuits 40 and passed to the input of flip flop 112 of the code comparator circuits 43, the corresponding bit of reference code sequence provided at such time will be at a different level.

Accordingly, since the bits extended over flip flops 112, 113 to the inputs of the Exclusive OR gate 114 are different, the Exclusive OR gate 114 will provide a logic 1 level output. The logic 1 level output provided by the Exclusive OR gate 114 will enable AND gate 115, which has a second input at a logic 1 level provided by the clock pulse which clocked the alarm bit and the reference bit into the flip flops 112, 113, respectively.

When AND gate 115 is enabled in response to the receipt of the alarm bit at the alarm monitoring circuits 40, a logic 1 level output provided by AND gate 115 will enable an alarm driver 116 of the alarm indication circuit 45 to energize an alarm tone generator 117, which generates an audible alarm tone, and lights an alarm lamp 118 at the central monitor. In addition, the output of AND gate 115 also enables the alarm source

identification circuits 46 to scan the next twenty bits of the alarm code as the bits are received to determine the source of the alarm.

The alarm source identification circuit 46 may comprise a plurality of AND gates 120 and a multi-stage ring counter 125. In the present example, wherein the status of twenty alarm sources 10 is to be monitored, the alarm source identification circuit 46 includes 20 AND gates, including gates 121-124 shown in FIG. 4, a separate gate being provided for each alarm source, and the ring counter 125 has 20 stages 125a-125t, each having an output connected to a different one of the gates 120 for sequentially enabling the gates 120 to be responsive to the identification bits of the alarm code in a manner which will become apparent hereinafter.

Each of the AND gates 120, such as gate 121, is operable when enabled to effect the energization of an associated alarm lamp, such as alarm lamp 131, of the alarm source register 47. Each alarm lamp indicates the condition of a different one of the alarm sources 10. For example, alarm lamps 131-134 shown in FIG. 5 represent the conditions of alarm sensors 11-14 (FIG. 2), respectively.

The outputs of the stages 125a-125t of the ring counter 125 are individually connected to inputs of the AND gates 120. Thus, for example, stages 125a, 125b, 125s and 125t are connected to inputs of AND gates 121-124, respectively. A second input of each of the AND gates 120 is connected to the output of the code comparator circuit 43 at gate 115.

Whenever AND gate 115 of the code comparator circuit 43 is enabled, the logic 1 level signal provided at the output thereof sets a flip flop 126 of the alarm source identification circuits 46 which enables and AND gate 127 connected to the output of the flip flop 126 to pass further clock pulses provided by the clock pulse generator 44 to a clock pulse input of the ring counter 125.

One of the stages of the ring counter 125 normally contains a logic 1 level and the remaining stages normally contain logic 0 level bits. Successive clock pulses provided to the ring counter 125 will cause the logic 1 level stored in the ring counter register to be shifted sequentially from stage to stage, thereby providing an enabling signal for each of the twenty AND gates 120, including gates 121-124. The output of the last stage 125t of the ring counter 125 may be connected to the reset input of flip flop 126 to cause the flip flop 126 to be reset after 20 clock pulses have been extended to the ring counter 125.

Thus, assuming the logic 1 level bit is stored in stage 125t of the ring counter 125, when the flip flop 126 is set by the output provided by the code comparator circuit 43, the next clock pulse will be gated over AND gate 127 to the ring counter 125, causing the logic 1 level bit to be shifted to the first stage 125a of the ring counter 125. Accordingly, an enabling signal will be extended to one input of AND gate 121 which is connected to the output of stage 125a of the ring counter 125.

The same clock pulse will gate the next bit of the alarm code received and the next bit of the reference code generated into the flip flops 112, 113, respectively, of the code comparator circuit 43.

Assuming that alarm sensor 11 (FIG. 2) is providing an alarm output and the other 19 sensors which comprise the alarm sources 10 are indicating that asso-

ciated protected areas are secure, then the second bit of the alarm code sequence, which represents the condition of sensor 11, will be complemented, and the third through 21 bits of the alarm code will be identical with corresponding bits of the reference code.

Thus, the second bit of the alarm code will differ with the corresponding bit of the reference code, and when such bits are compared by the code comparator circuit 43, gate 115 will be enabled, providing a logic 1 level signal at the output thereof.

The logic 1 level output of the gate 115 is extended over conductor 130 to the inputs of all of the AND gates 120, including gate 121. At the time the second bit of the alarm code is received, the logic 1 level output provided by stage 125a of the ring counter 125 is extended to the other input of the AND gate 121. Accordingly, AND gate 121 will be enabled, providing an output for energizing lamp 131 of the alarm source register 47, to indicate that an alarm has been provided by alarm sensor 11.

Thereafter, as subsequent bits of the alarm code are received and passed to the code comparator circuit 43 for comparison with corresponding bits of the reference code, the logic 1 enabling output provided by the ring counter 125 will be extended in sequence to inputs of the other AND gates of the alarm source identification circuit 46, including gates 122-124. However, since it is assumed that only alarm sensor 11 is providing an alarm output, the identification bits representing the conditions of the other 19 alarm sensors, including sensor 12-14, will not be complemented. Accordingly, as each of the subsequent bits of the alarm code are received and compared with corresponding bits of the reference code, the code comparator circuit 43 will provide a logic 0 output signal which will maintain the AND gates of the alarm source identification circuits 46 associated with such sensors disabled.

We claim:

1. In a security system including a transmission line for carrying alarm information from a plurality of protected areas within a predetermined zone to a central monitor that is remote from the protected areas, zone monitoring means including alarm storage means having a separate flip flop for each protected area for storing a first data bit whenever the corresponding protected area is secure and a second data bit to indicate an alarm condition for the corresponding protected area, readout means enabled in response to the storage of said second data bit in one of said flip flops to effect the sequential readout of said alarm storage means to provide an alarm output code including a sequence of data bits coded to represent the conditions of the protected areas, and means for enabling said alarm code to be transmitted over said transmission line to said central monitor, and line monitoring means at said central monitor including first means responsive to at least one of the data bits of said alarm code to indicate that an alarm condition has been indicated for one or more of said protected areas and second means responsive to other data bits of said alarm code sequence to determine the protected area providing an alarm.

2. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an individual alarm sensor for each protected area, each of said alarm sensors being operable to provide an

alarm output signal in response to an alarm condition for an associated protected area, alarm sensor monitoring means including alarm data storage means including separate alarm output storage means for each of said alarm sensors for storing the alarm output signals provided by the alarm sensors, and alarm transmission means controlled by said alarm storage means in response to the receipt of an alarm output signal provided by at least one of said alarm sensors to effect the readout of said alarm storage means to provide an alarm code for transmission over said transmission line to said central monitor, said alarm code being comprised of a sequence of coded bits in which a first bit indicates that an alarm output has been provided by at least one of the alarm sensors and further bits of the sequence are coded to indicate which alarm sensor has provided the alarm output, and line monitoring means at said central monitor including means responsive to the first bit of said alarm code to provide an alarm indication at said central monitor and means responsive to said further bits of said alarm code to determine the source of the alarm.

3. A system as set forth in claim 2 wherein each of said alarm sensors are further operable to provide a supervisory alarm output signal in response to a component failure of the alarm sensor, and wherein said alarm storage means further includes separate supervisory storage means for each of said alarm sensors for storing supervisory alarm outputs provided by the alarm sensors, said alarm transmission means being responsive to either an alarm output signal or a supervisory output signal to provide an alarm code for transmission to said central monitor.

4. A system as set forth in claim 3 wherein each of said alarm output storage means comprises a first normally reset bistable data storage circuit and each of said supervisory storage means comprises a second normally reset bistable data storage circuit, a first data storage circuit being set whenever an alarm output signal is provided by an associated alarm sensor and a second data storage circuit being set whenever a supervisory alarm output signal is provided by an associated alarm sensor.

5. A system as set forth in claim 4 wherein said readout means includes means for resetting all of the bistable data storage circuits of said alarm storage means after said alarm code has been transmitted to said central monitor.

6. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an individual alarm sensor for each protected area, each of said alarm sensors being operable to provide an alarm output signal in response to an unauthorized intrusion of an associated area, alarm sensor monitoring means including alarm storage means having an individual bistable storage means for each alarm sensor settable to a first state in response to the receipt of an alarm output signal provided by an associated alarm sensor, code generating means for continuously generating a line monitoring code comprised of a known sequence of code bits for transmission over said transmission line to said central monitor, and readout means including means controlled by said alarm storage means in response to the receipt of an alarm output signal provided by one of said alarm sensors to selectively modify

bits of the line monitoring code sequence to provide a modified code sequence in which the first bit of the modified sequence represents an alarm indication and subsequent bits of the modified sequence of bits represent the conditions of the alarm sensors, and means for resetting said storage means after the modified code sequence has been provided.

7. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an individual alarm sensor for each protected area, each of said alarm sensors being operable to provide an alarm output signal in response to an unauthorized intrusion of an associated area, alarm sensor monitoring means including alarm storage means having an individual storage means for each alarm sensor for storing the alarm output signals provided by the corresponding alarm sensor, code generating means for continuously generating a line monitoring code comprised of a known sequence of coded bits, bit gating means for passing the bits of the line monitoring code to said transmission line for transmission to said central monitor, and readout means controlled by said alarm storage means in response to the receipt of an alarm output signal provided by an alarm sensor to effect readout of said alarm storage means thereby providing a sequence of alarm data bits and to enable said bit gating means to be responsive to said sequence of alarm data bits to modify a bit of the line monitoring code to indicate that an alarm output signal has been provided by at least one of said alarm sensors and to thereafter selectively modify further bits of the line monitoring code to identify the source of the alarm, and line monitoring means at said central monitor including reference code generating means for generating a reference code comprised of a sequence of coded bits, each bit of which is normally identical with corresponding bits of the line monitoring code at any given time, code comparator means for receiving the bits of the line monitoring code and comparing the monitor code bit sequence with the reference code bit sequence, first means controlled by said code comparator means for providing an alarm indication whenever corresponding bits of the sequence are different, and second means responsive to said further bits of said alarm code to determine the source of the alarm.

8. A system as set forth in claim 7 wherein each storage means comprises an alarm flip flop, each alarm flip flop being normally reset to provide an output bit at a first logic level and being set in response to an alarm output signal provided by an associated alarm sensor to provide an output bit at a second logic level.

9. A system as set forth in claim 8 in which said readout means includes multistage shift register means having an individual stage for each alarm flip flop of said alarm storage means, means for extending the output

bits provided by different alarm flip flops to a different stage of the shift register means, and means for extending a bit at said second logic level to a further stage of said shift register means whereby said shift register means stores alarm data including data representing the conditions of all of the alarm sensors.

10. A system as set forth in claim 9 wherein said readout means includes readout control means responsive to an output bit at said second logic level provided by at least one of said alarm flip flops to provide a plurality of gated clock pulses for said shift register means for effecting the serial readout of the data bits stored therein thereby providing said sequence of alarm data bits at the output of said shift register means.

11. A system as set forth in claim 10 wherein said bit gating means includes means responsive to each data bit at said second logic level read out of said shift register means to complement a bit of the line monitoring code.

12. A system as set forth in claim 10 wherein said readout control means includes means for generating clock pulses for controlling said code generating means to generate code bits at a predetermined rate, and clock pulse gating means operable when enabled to gate said clock pulses to said shift register means to effect the serial readout of the bits stored therein in synchronism with the generation of the code bits of the line monitoring code, and enabling means responsive to an alarm output signal provided by at least one of said alarm sensors to enable said clock pulse gating means.

13. A system as set forth in claim 12 wherein said bit gating means includes Exclusive OR gating means having a first input connected to receive the bits of the line monitoring code generated by said code generating means and a second input connected to receive the bits of the alarm code read out of said identification data storage register, and control gating means enabled by said enabling means to pass the bits of the alarm code to the second input of said Exclusive OR gating means, said Exclusive OR gating means being responsive to each bit of the alarm code read out of the shift register which is at the first logic level to pass a code bit of the line monitoring code unaltered to the transmission line and responsive to each bit of the alarm code read out of the shift register which is at the second logic level to complement a code bit of the line monitoring code as such code bit is passed to the transmission line.

14. A system as set forth in claim 12 in which said readout control means includes reset means for resetting the alarm flip flops after the alarm code has been transmitted to the central monitor.

15. A system as set forth in claim 14 wherein said reset means includes means for disabling said clock pulse gating means after a predetermined number of clock pulses have been extended to said shift register means.

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