



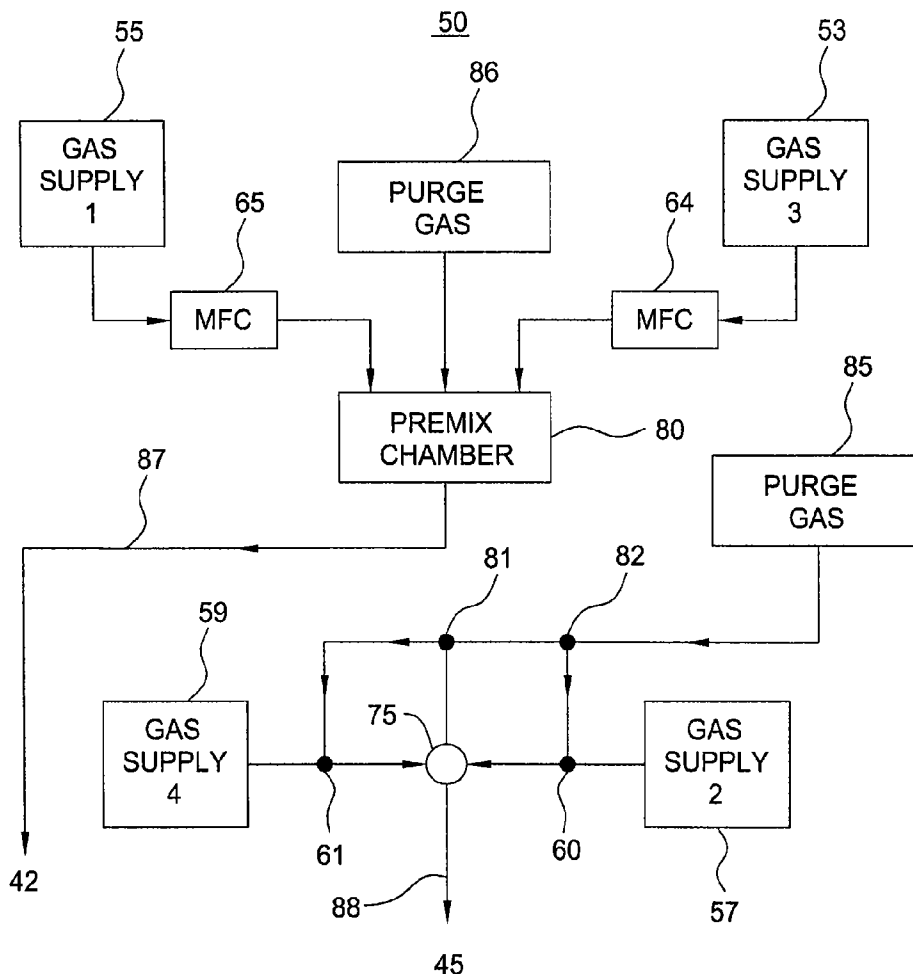
US 20110100295A1

(19) **United States**(12) **Patent Application Publication**  
**Xi et al.**(10) **Pub. No.: US 2011/0100295 A1**(43) **Pub. Date: May 5, 2011**(54) **SYSTEM AND METHOD FOR FORMING AN  
INTEGRATED BARRIER LAYER****Publication Classification**(51) **Int. Cl.**  
**C23C 16/52** (2006.01)  
**C23C 16/455** (2006.01)  
(52) **U.S. Cl.** ..... **118/706**  
(57) **ABSTRACT**(76) **Inventors:** **Ming Xi**, Palo Alto, CA (US);  
**Michael Yang**, Palo Alto, CA (US);  
**Hui Zhang**, Santa Clara, CA (US)(21) **Appl. No.: 12/987,962**(22) **Filed: Jan. 10, 2011****Related U.S. Application Data**

(60) Division of application No. 11/770,735, filed on Jun. 29, 2007, now Pat. No. 7,867,914, which is a continuation of application No. 10/414,271, filed on Apr. 15, 2003, now Pat. No. 7,279,432.

(60) Provisional application No. 60/386,221, filed on Apr. 16, 2002.

An apparatus for processing a substrate is provided. The apparatus includes a process chamber, and a dual-mode gas distribution plate disposed within the process chamber. The dual-mode gas distribution plate comprises a first gas distribution zone disposed in a center of the gas distribution plate, and a second gas distribution zone surrounding the first gas distribution zone, the second gas distribution zone being fluidly isolated from the first gas distribution zone, wherein the first gas distribution zone is coupled to a valve system to deliver sequential pulses of a first gas to the first gas distribution zone to perform a cyclical deposition process, and the second gas distribution zone is in communication with a flow controller to deliver a second gas to perform a chemical vapor deposition process.



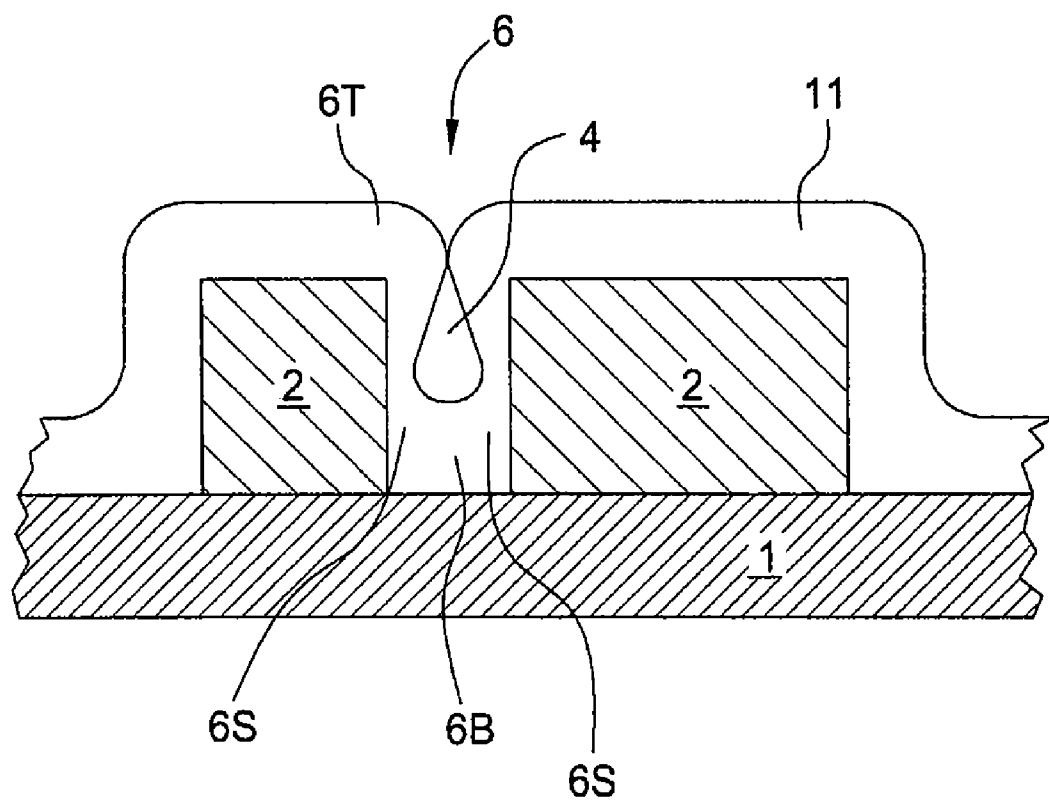
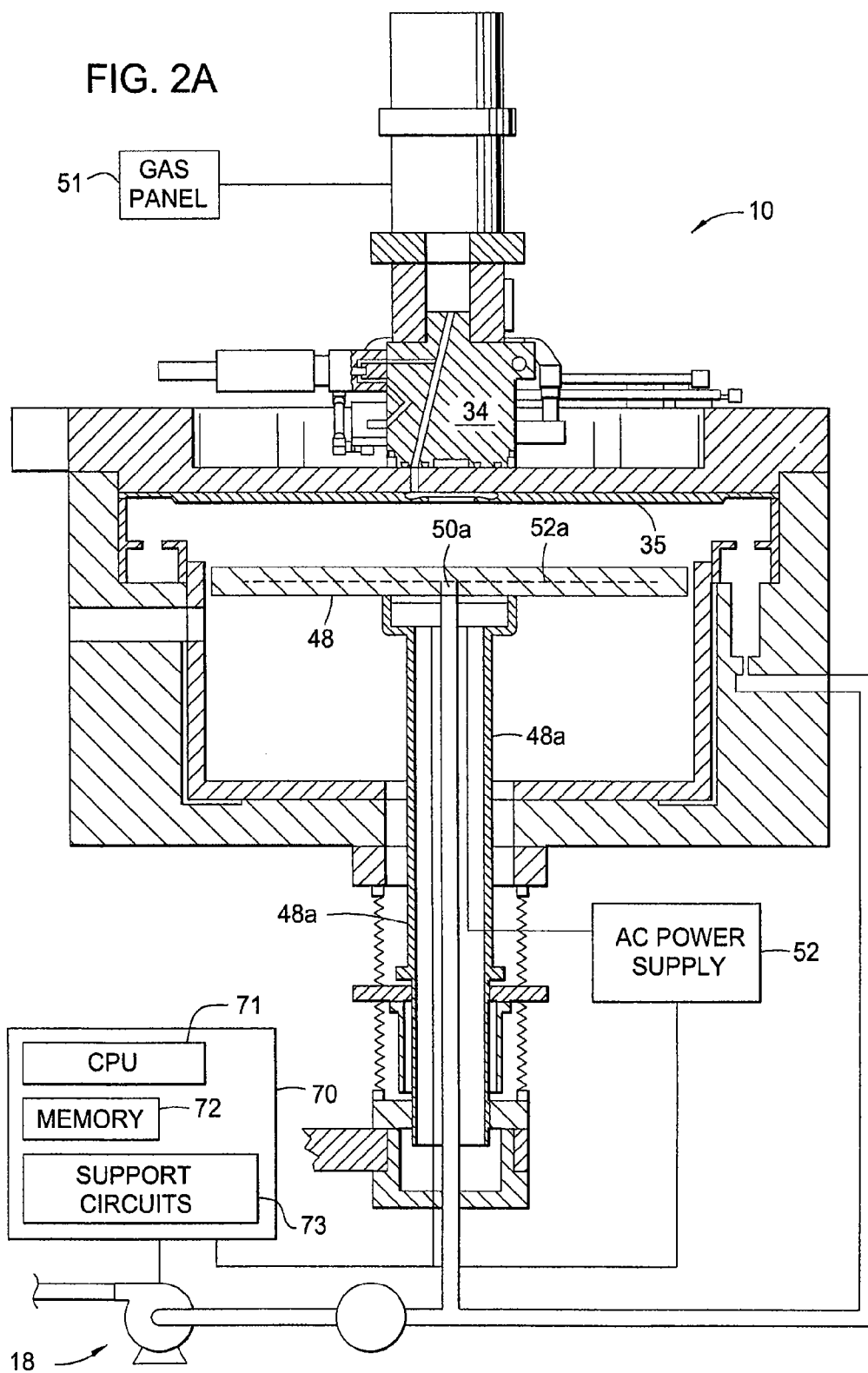


FIG. 1



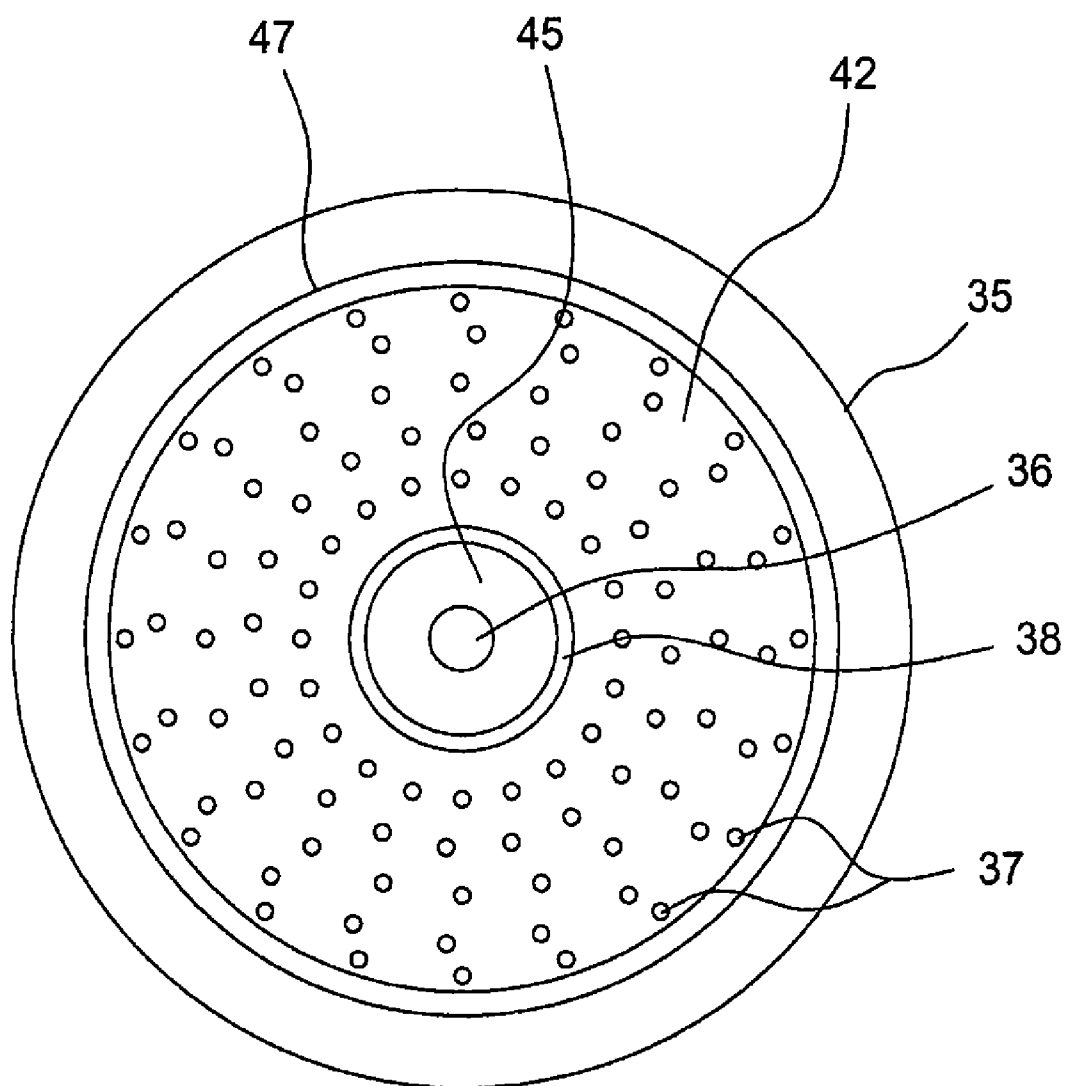


FIG. 2B

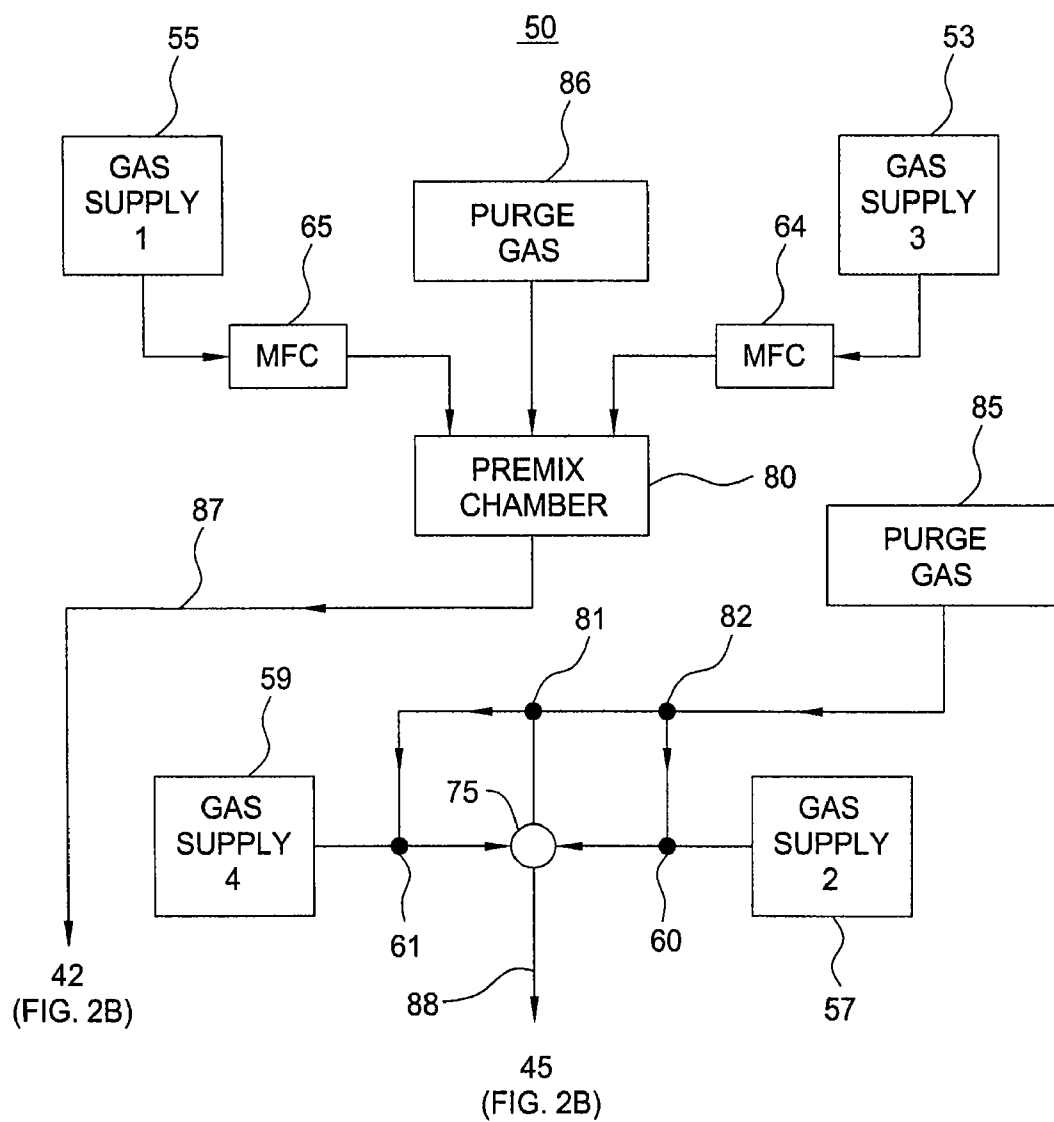


FIG. 3

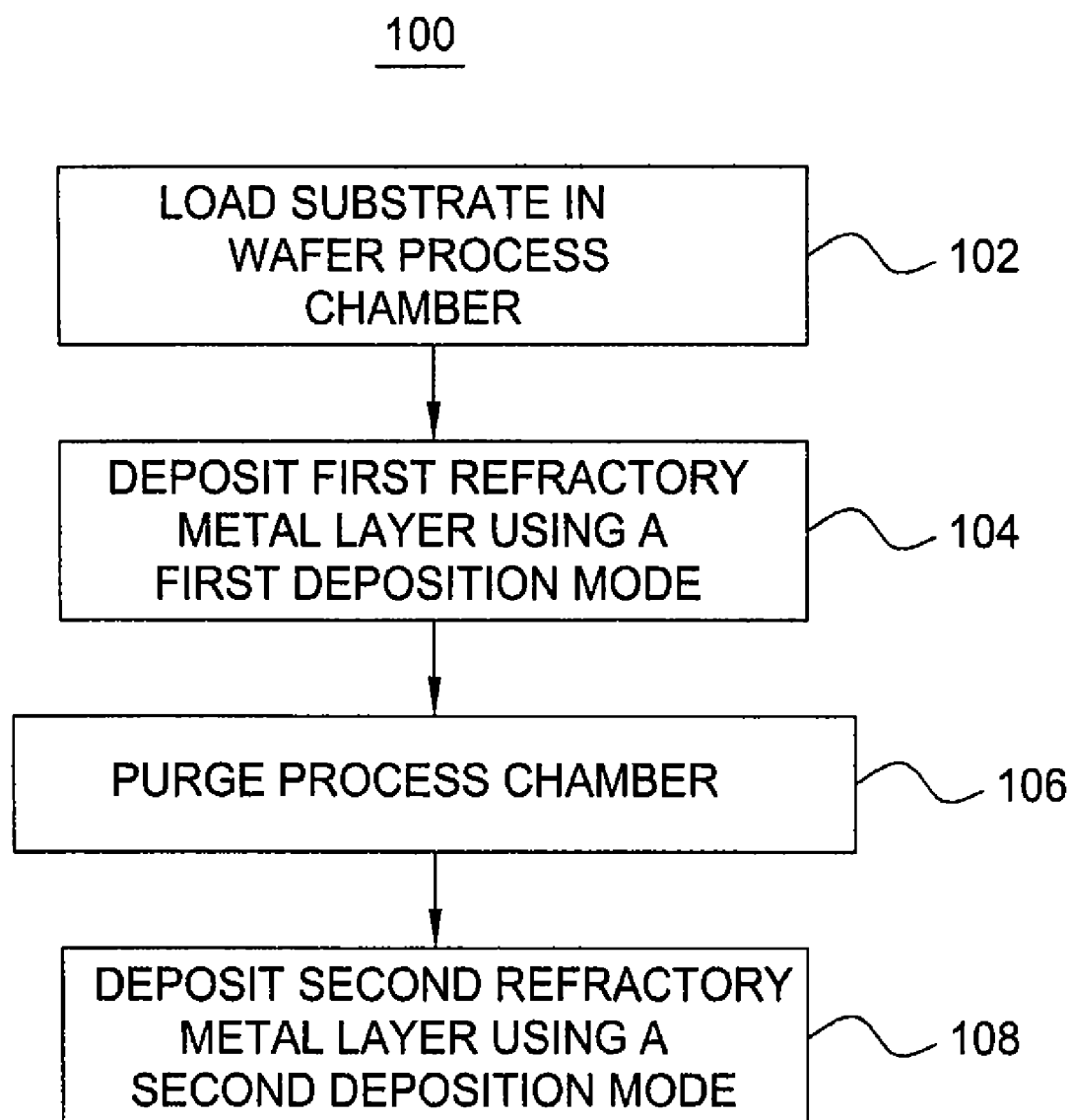


FIG. 4

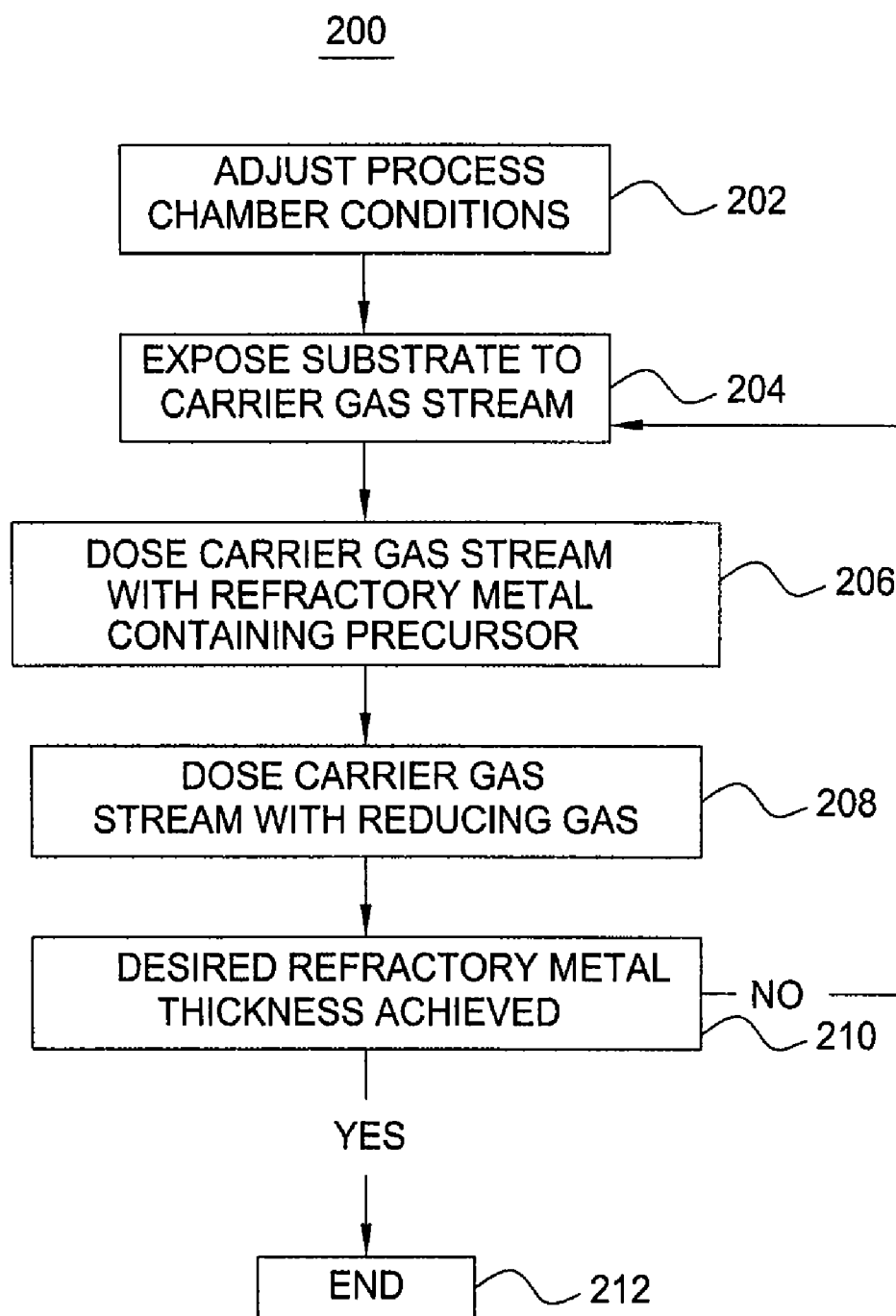


FIG. 5

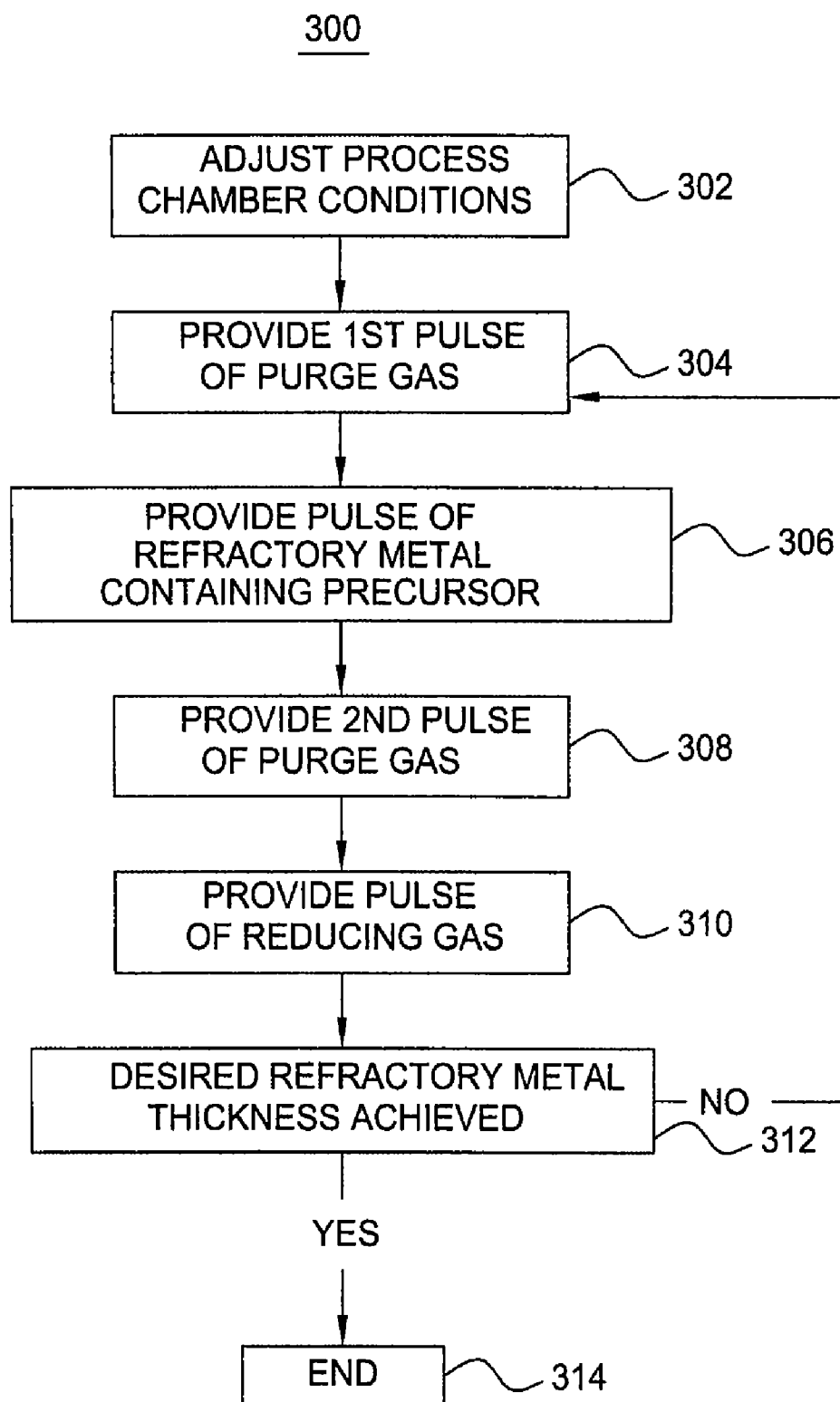


FIG. 6



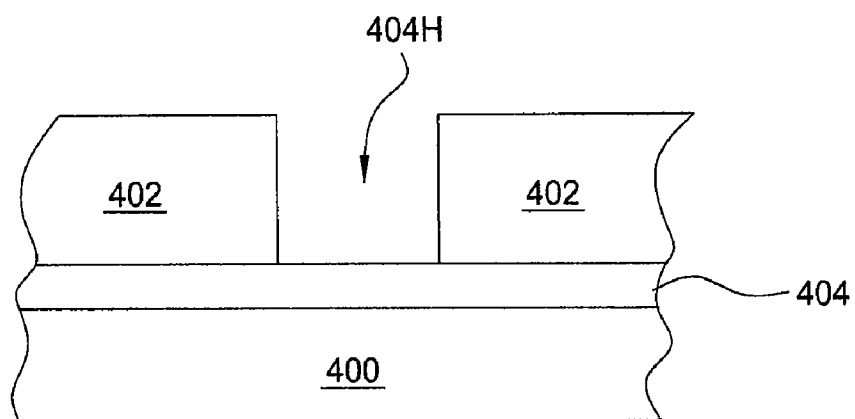


FIG. 7A

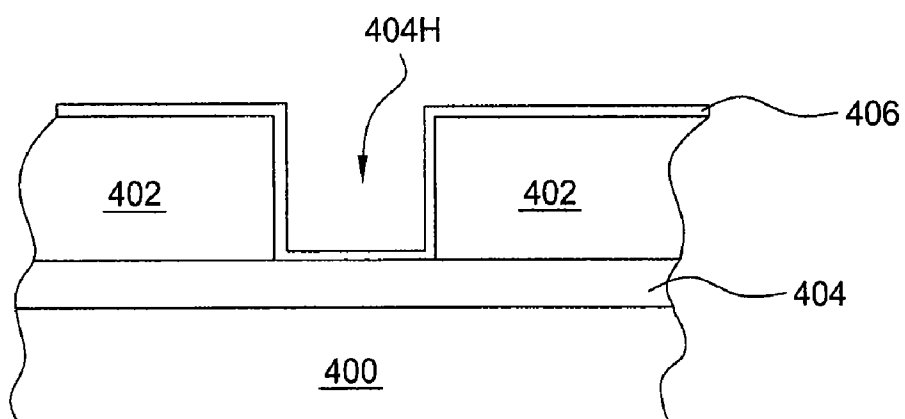


FIG. 7B

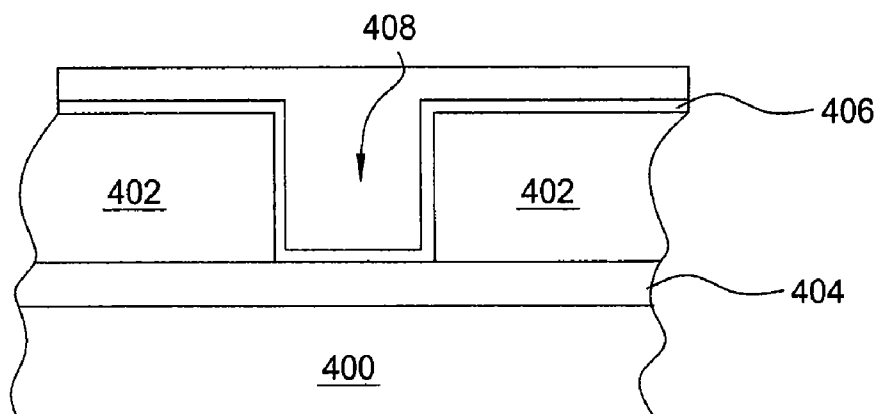


FIG. 7C

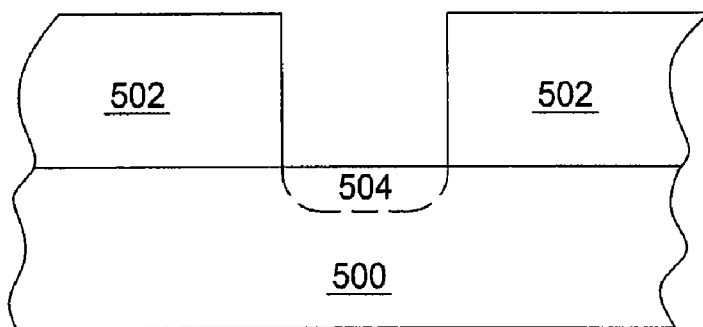


FIG. 8A

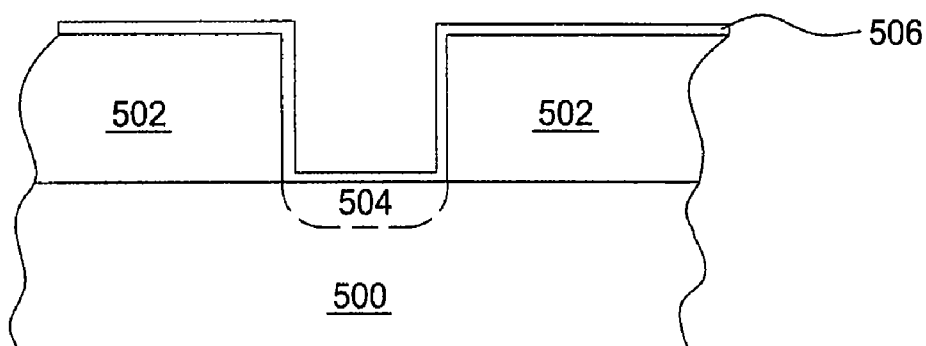


FIG. 8B

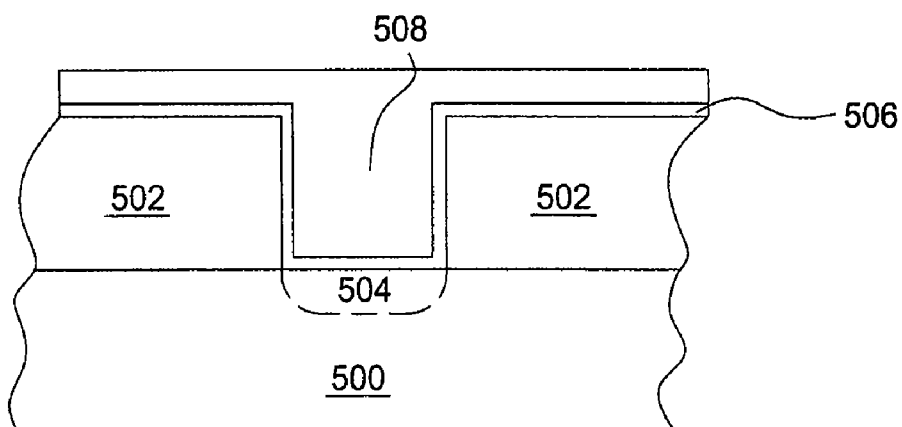


FIG. 8C

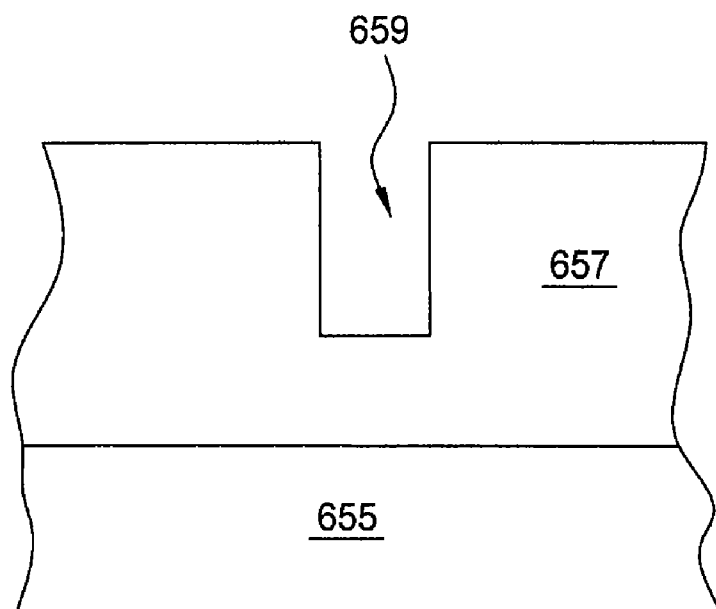


FIG. 9A

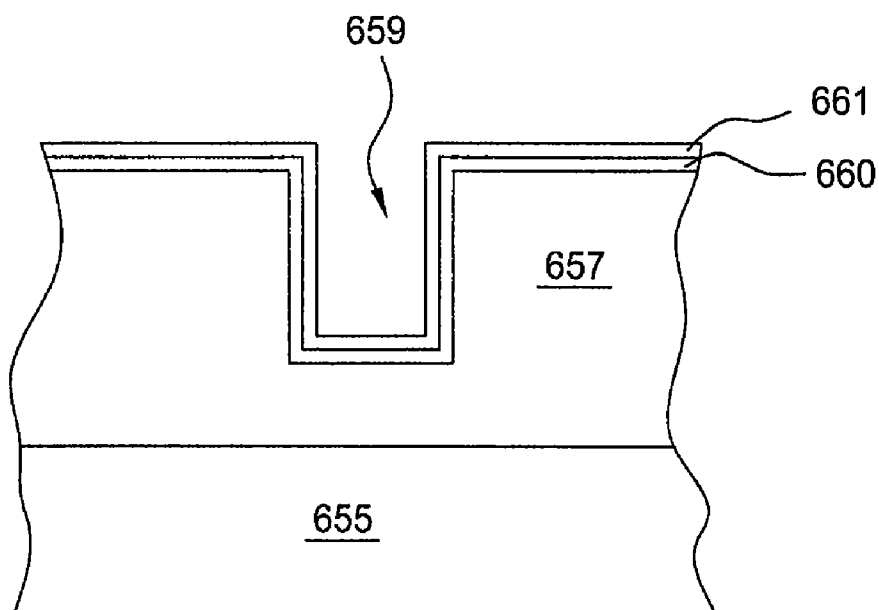


FIG. 9B

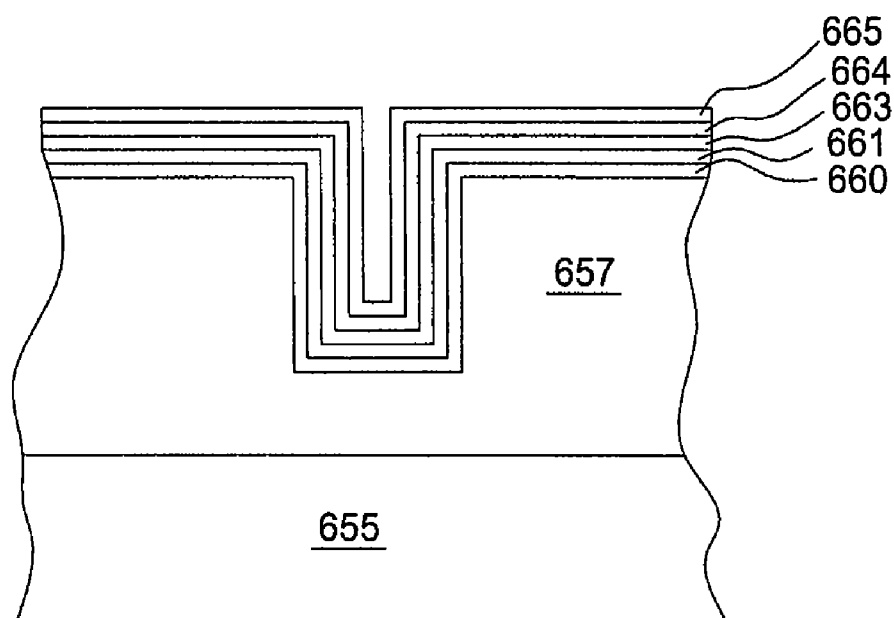


FIG. 9C

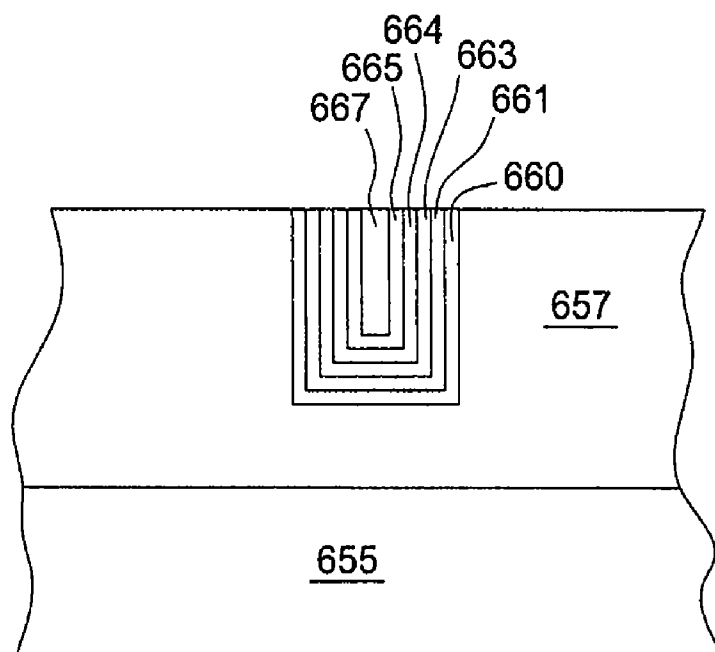


FIG. 9D

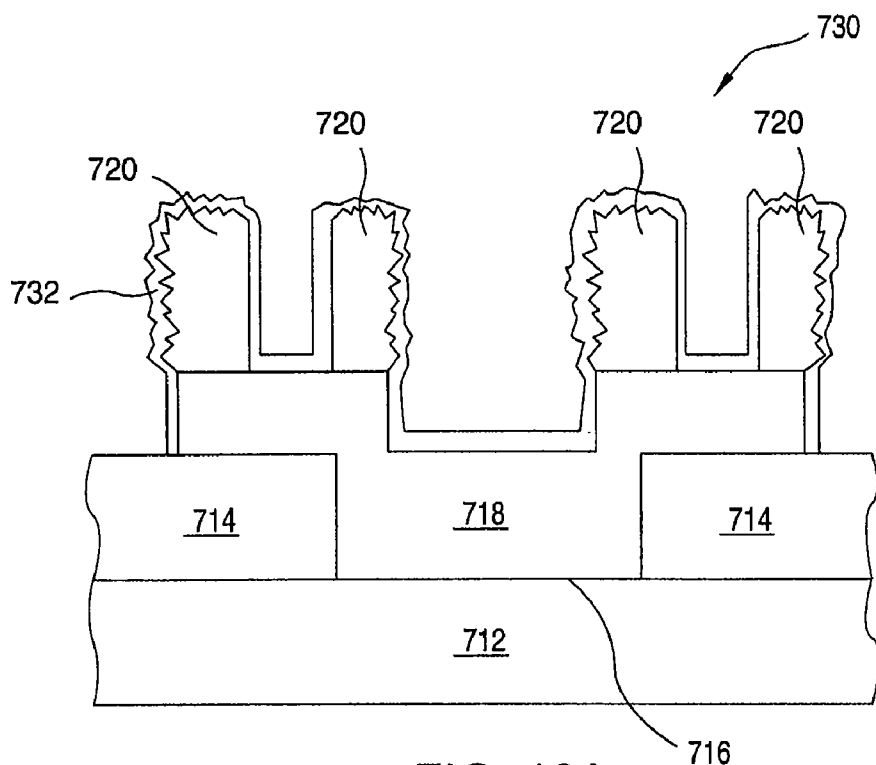


FIG. 10A

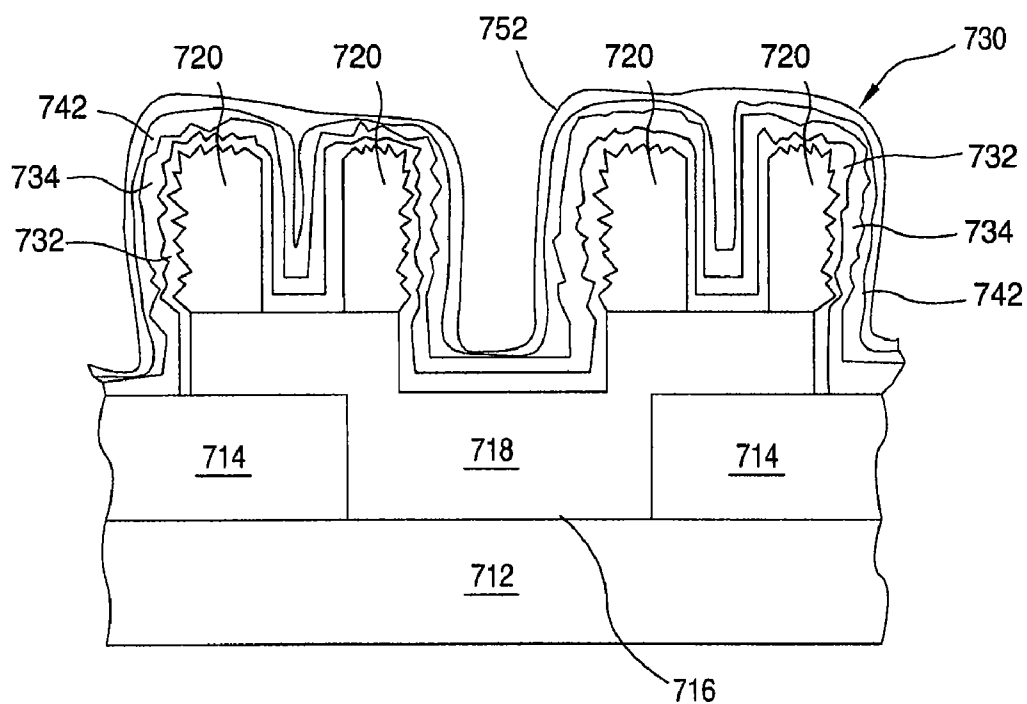


FIG. 10B

## SYSTEM AND METHOD FOR FORMING AN INTEGRATED BARRIER LAYER

### CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of U.S. patent application Ser. No. 11/770,735, filed Jun. 29, 2007, which is a continuation of U.S. patent application Ser. No. 10/414,271, filed Apr. 15, 2003 and issued as U.S. Pat. No. 7,279,432 on Oct. 9, 2007. U.S. patent application Ser. No. 10/414,271 claims the benefit of U.S. Provisional Patent Application No. 60/386,221, filed Apr. 16, 2002. All of the aforementioned patent applications are incorporated by reference herein.

### BACKGROUND OF THE DISCLOSURE

[0002] 1. Field of the Invention

[0003] Embodiments of the present invention generally relate to a method of barrier layer formation and, more particularly to a method of integrated barrier layer formation using both cyclical deposition techniques and chemical vapor deposition techniques.

[0004] 2. Description of the Background Art

[0005] In the manufacture of integrated circuits, contact level metallization schemes are often used to provide low resistance contacts to an underlying semiconductor material. Typically, contact level metallization schemes combine an integrated barrier layer with a contact level metal layer.

[0006] For example, when a gate electrode of a transistor is fabricated, an integrated barrier layer (e.g., titanium nitride/tungsten (TiN/W)) is formed between the gate material (e.g., polysilicon) and the contact level metal layer (e.g., aluminum (Al) or copper (Cu)) of the gate electrode. The integrated barrier layer inhibits the diffusion of the aluminum (Al) or copper (Cu) into the polysilicon gate material. Such aluminum (Al) or copper (Cu) diffusion is undesirable because it potentially changes the characteristics of the transistor, rendering the transistor inoperable.

[0007] The integrated barrier layer typically comprises two different material layers. Each of the material layers is typically formed using a separate process chamber. For example, separate deposition chambers may be used for depositing the titanium nitride (TiN) layer and the tungsten (W) layer comprising a titanium nitride/tungsten (TiN/W) integrated barrier layer. The separate deposition chambers may include, for example, physical vapor deposition (PVD) chambers and/or chemical vapor deposition (CVD) chambers. However, the use of separate deposition chambers to form each material layer comprising the integrated barrier layer is costly.

[0008] Additionally, as circuit densities increase, the widths of integrated circuit features such as, for example, gate electrodes, may decrease to sub-micron dimensions (e.g., less than 0.25 micrometers), whereas the thickness of material layers between such features typically remains substantially constant, increasing the aspect ratios therefor. The term aspect ratio as used herein refers to the ratio of the feature height divided by the feature width. Many traditional deposition processes have difficulty filling sub-micron features where the aspect ratio exceeds 8:1, and especially where the aspect ratio exceeds 10:1.

[0009] FIG. 1 illustrates the possible consequences of material layer deposition in a high aspect ratio feature 6 formed on a substrate 1. The high aspect ratio feature 6 may be any opening such as a space formed between adjacent

features 2, a contact, a via, or a trench defined in a material layer. As shown in FIG. 1, a material layer 11 that is formed using conventional deposition techniques (e.g., chemical vapor deposition (CVD) and/or physical vapor deposition (PVD)) tends to be deposited on the top edges 6T of the feature 6 at a higher rate than at the bottom 6B or sides 6S thereof creating an overhang. This overhang or excess deposition of material is sometimes referred to as crowning. Such excess material continues to build up on the top edges 6T of the feature 6, until the opening is closed off by the deposited material 11, forming a void 4 therein. The presence of voids may result in unreliable integrated circuit performance.

[0010] Therefore, a need exists for a system and method for forming integrated barrier layer structures.

### SUMMARY OF THE INVENTION

[0011] An apparatus for processing a substrate is provided. In one embodiment, the apparatus includes a process chamber, and a dual-mode gas distribution plate disposed within the process chamber. The dual-mode gas distribution plate comprises a first gas distribution zone disposed in a center of the gas distribution plate, and a second gas distribution zone surrounding the first gas distribution zone, the second gas distribution zone being fluidly isolated from the first gas distribution zone, wherein the first gas distribution zone is coupled to a valve system to deliver sequential pulses of a first gas to the first gas distribution zone to perform a cyclical deposition process, and the second gas distribution zone is in communication with a flow controller to deliver a second gas to perform a chemical vapor deposition process.

[0012] In another embodiment, an apparatus for processing a substrate is provided. The apparatus includes a process chamber, and a dual-mode gas distribution plate disposed within the process chamber. The dual-mode gas distribution plate comprises a first gas distribution zone having an opening in a center of the gas distribution plate and a second gas distribution zone having a plurality of openings surrounding the opening in the center of the gas distribution plate, the second gas distribution zone being fluidly isolated from the first gas distribution zone. The first gas distribution zone is coupled to an electronic valve to deliver sequential pulses of a first gas to the first gas distribution zone to perform a cyclical deposition process, and the second gas distribution zone is in communication with a flow controller to deliver a second gas to perform a chemical vapor deposition process.

[0013] In another embodiment, an apparatus for processing a substrate is described. The apparatus includes a process chamber, and a dual-mode gas distribution plate disposed within the process chamber. The dual-mode gas distribution plate comprises a first gas distribution zone having an opening in a center of the gas distribution plate, and a second gas distribution zone having a plurality of openings radially dispersed around the opening in the center of the gas distribution plate, the second gas distribution zone being fluidly isolated from the first gas distribution zone. The first gas distribution zone is coupled to an electronic valve to deliver sequential pulses of a tungsten containing gas and a reducing gas to the first gas distribution zone to perform a cyclical deposition process, and the second gas distribution zone is in communication with a flow controller to deliver a second gas comprising a titanium containing precursor gas to perform a chemical vapor deposition process.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above recited features of the present invention are attained and can readily be

understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0015] It is to be noted, however, that the appended drawings illustrate only typical embodiments of the invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0016] FIG. 1 is a cross-sectional view of one possible deposition result for high aspect ratio features filled using conventional prior art deposition techniques;

[0017] FIGS. 2A-2B depicts a schematic cross-sectional view of a process chamber and a top view of a gas distribution plate that can be used for the practice of embodiments described herein;

[0018] FIG. 3 is a block diagram of a gas delivery system for the gas distribution plate shown in FIG. 2B;

[0019] FIG. 4 illustrates a process sequence for integrated barrier layer formation;

[0020] FIG. 5 illustrates a process sequence for material layer formation using cyclical deposition techniques according to one embodiment described herein;

[0021] FIG. 6 illustrates a process sequence for material layer formation using cyclical deposition techniques according to an alternate embodiment described herein;

[0022] FIGS. 7A-7C illustrate schematic cross-sectional views of a substrate at different stages of an interconnect fabrication sequence;

[0023] FIGS. 8A-8C illustrate schematic cross-sectional views of a substrate at different stages of a gate electrode fabrication sequence;

[0024] FIGS. 9A-9D illustrate schematic cross-sectional views of a substrate at different stages of a trench capacitor fabrication sequence; and

[0025] FIGS. 10A-10B depict cross-sectional views of a substrate at different stages of a crown capacitor fabrication sequence.

## DETAILED DESCRIPTION

[0026] FIG. 2A depicts a schematic cross-sectional view of a process chamber 10 that can be used to perform deposition processes in accordance with embodiments described herein. The process chamber 10 generally houses a wafer support pedestal 48, which is used to support a substrate (not shown). The wafer support pedestal 48 is movable in a vertical direction inside the process chamber 10 using a displacement mechanism 48a.

[0027] Depending on the specific deposition process, the substrate can be heated to some desired temperature prior to or during deposition. For example, the wafer support pedestal 48 may be heated using an embedded heater element 52a. The wafer support pedestal 48 may be resistively heated by applying an electric current from an AC power supply 52 to the heater element 52a. The substrate (not shown) is, in turn, heated by the pedestal 48. Alternatively, the wafer support pedestal 48 may be heated using radiant heaters such as, for example, lamps (not shown).

[0028] A temperature sensor 50a, such as a thermocouple, is also embedded in the wafer support pedestal 48 to monitor the temperature of the pedestal 48 in a conventional manner. The measured temperature is used in a feedback loop to control the AC power supply 52 for the heating element 52a, such that the substrate temperature can be maintained or

controlled at a desired temperature which is suitable for the particular process application.

[0029] A vacuum pump 18 is used to evacuate the process chamber 10 and to maintain the pressure inside the process chamber 10. A gas manifold 34, through which process gases are introduced into the process chamber 10, is located above the wafer support pedestal 48. The gas manifold 34 is coupled to a gas panel 51, which controls and supplies various process gases to the process chamber 10.

[0030] Proper control and regulation of the gas flows to the gas manifold 34 are performed by mass flow controllers (not shown) and a microprocessor controller 70. Additionally, the gas manifold 34 may optionally be heated to prevent condensation of the reactive gases within the manifold.

[0031] The gas manifold 34 includes a gas distribution plate 35. Referring to FIG. 2B, the gas distribution plate 35 is configured to include two gas distribution zones 42, 45 for providing process gases to the process chamber for either a chemical vapor deposition (CVD) process or a cyclical deposition process. A first gas distribution zone 45 comprises a center opening 36 through which process gases for the cyclical deposition process are provided to the process chamber. A second gas distribution zone 42 comprises a plurality of openings 37 radially dispersed around the center opening 36.

[0032] The first gas distribution zone 45 and the second gas distribution zone 42 are isolated from one another using one or more seals 38, 47 which inhibit mixing of the process gases provided thereto. The one or more seals 38, 47 may comprise any suitable material that is non-reactive with the process gases provided to the process chamber, such as, for example, an o-ring.

[0033] FIG. 3 depicts a gas distribution system 50 that may be used to provide process gases to the gas distribution plate 35 (FIG. 2A). The gas distribution system 50 includes process gas supplies 53, 55, 57, 59, purge gas supplies 85, 86, electronic control valves 60, 61, mass flow controllers (MFC) 64, 65, gas splitters 81, 82, a three-position valve 75 and a premix chamber 80.

[0034] For the cyclical deposition mode, a process gas from supplies 57, 59 is provided to electronic control valves 60, 61, respectively. A purge gas from the purge gas supply 85 may be mixed with the process gases through gas splitters 81, 82. The electronic control valves 60, 61 as used herein refer to any control valve capable of providing rapid and precise gas flow to the process chamber 10 with valve open and close cycles of less than about 1-2 seconds, and more preferably less than about 0.1 second. The electronic control valves 60, 61 are coupled to the center opening 36 in the first gas distribution zone 45, via three-position valve 75 and gas line 88.

[0035] For the chemical vapor deposition (CVD) mode, process gases from gas supplies 53, 55 are coupled through mass flow controllers (MFC) 64, 65, respectively, to premix chamber 80. A purge gas from purge gas supply 86 may also be provided to the premix chamber 80. In the premix chamber 80, the process gases are caused to mix. Generally, these gases are reactants that will react when they are exposed to a heated substrate. The mixed gases are provided from the premix chamber 80 to the plurality of openings 37 in the second gas distribution zone 42 via gas line 87.

[0036] The microprocessor controller 70 may be one of any form of general purpose computer processor (CPU) 71 that can be used in an industrial setting for controlling various chambers and sub-processors. The computer may use any suitable memory 72, such as random access memory, read

only memory, floppy disk drive, hard disk, or any other form of digital storage, local or remote. Various support circuits 73 may be coupled to the CPU for supporting the processor in a conventional manner. Software routines as required may be stored in the memory or executed by a second CPU that is remotely located.

**[0037]** The software routines are executed to initiate process recipes or sequences. The software routines, when executed, transform the general purpose computer into a specific process computer that controls the chamber operation so that a chamber process is performed. For example, software routines may be used to precisely control the activation of the electronic control valves for the execution of process sequences according to embodiments described herein. Alternatively, the software routines may be performed in hardware, as an application specific integrated circuit or other type of hardware implementation, or a combination of software and hardware.

#### Integrated Barrier Layer Formation

**[0038]** A dual-mode deposition process for forming an integrated barrier layer structure on a substrate is described. The dual-mode deposition process is performed in a single deposition chamber and comprises a chemical vapor deposition (CVD) step as well as a cyclical deposition step.

**[0039]** FIG. 4 illustrates an embodiment of the dual-mode deposition process sequence 100 detailing the various steps used for the formation of the integrated barrier layer structure. The integrated barrier layer comprises at least a first refractory metal layer and a second refractory metal layer. The dual-mode deposition process may be performed in a process chamber similar to that described above with respect to FIGS. 2-3.

**[0040]** As indicated in step 102, a substrate is provided to the process chamber. The substrate may be for example, a silicon substrate having gate regions formed thereon. Referring to step 104, a first refractory metal layer is formed on the substrate using a first deposition mode. The first deposition mode may comprise, for example, a chemical vapor deposition process wherein a refractory metal-containing precursor is thermally decomposed.

**[0041]** The first refractory metal layer may comprise for example titanium (Ti), titanium nitride (TiN), tantalum (Ta), or tantalum nitride (TaN), among others. Suitable titanium-containing precursors for a CVD process may include, for example, titanium tetrachloride (TiCl<sub>4</sub>), tetrakis(dimethylamido)titanium (TDMAT) and tetrakis(diethylamido)titanium (TDEAT), among others. Suitable tantalum-containing precursors for a CVD process may include, for example, pentakis(dimethylamido)tantalum (PDMAT), pentakis(ethylmethylamido)tantalum (PEMAT), tertbutylimidotris(diethylamido)tantalum (TBTDET), and pentakis(diethylamido)tantalum (PDEAT), among others.

**[0042]** One exemplary process of depositing a titanium nitride (TiN) layer using a chemical vapor deposition (CVD) process comprises thermally decomposing a titanium-containing precursor such as, for example, tetrakis(dimethylamido)titanium (TDMAT). The tetrakis(dimethylamido)titanium (TDMAT) may be provided to radially dispersed openings 37 (FIG. 2B) of the distribution plate 35 (FIG. 2B) in the process chamber at a flow rate between about 20 sccm to about 200 sccm, preferably between about 50 sccm to about 100 sccm. A carrier gas comprising helium (He) may be provided along with the tetrakis(dimethylamido)titanium

(TDMAT) at a flow rate between about 500 sccm to about 2000 sccm, preferably between about 1000 sccm to about 1500 sccm. The substrate may be maintained at a temperature between about 200° C. to about 400° C., preferably between about 300° C. to about 350° C., at a chamber pressure between about 5 torr to about 15 torr, preferably about 10 torr.

**[0043]** Referring to step 106, after the first refractory metal layer is formed on the substrate using a first deposition mode, the process chamber is purged to remove any process gases remaining therein. Suitable purge gases may include argon (Ar), helium (He) and nitrogen (N<sub>2</sub>). Thereafter, a second refractory metal layer is formed on the first refractory metal layer using a second deposition mode, as indicated in step 108. The second refractory metal layer may be formed using a cyclical deposition process by alternately adsorbing a refractory metal-containing precursor and a reducing gas on the substrate.

**[0044]** FIG. 5 illustrates an embodiment of a cyclical deposition process sequence 200 according to the present invention detailing the various steps used for the deposition of the second refractory metal layer. As shown in step 202, the process chamber conditions such as, for example, the temperature and pressure are adjusted to enhance the adsorption of the process gases on the substrate.

**[0045]** In one embodiment where a constant carrier gas flow is desired, a carrier gas stream is established within the process chamber through the center opening 36 (FIG. 2B) in the gas distribution plate 35 (FIG. 2B), as indicated in step 204. Carrier gases may be selected so as to also act as a purge gas for removal of volatile reactants and/or by-products from the process chamber. Carrier gases such as, for example, helium (He), argon (Ar), nitrogen (N<sub>2</sub>) and hydrogen (H<sub>2</sub>), and combinations thereof, among others may be used.

**[0046]** Referring to step 206, after the carrier gas stream is established within the process chamber, a pulse of a refractory metal-containing precursor is added to the carrier gas stream. The term pulse as used herein refers to a dose of material injected into the process chamber or into the carrier gas stream. The pulse of the refractory metal-containing precursor lasts for a predetermined time interval.

**[0047]** The second refractory metal layer may comprise for example, tungsten (W), tungsten nitride (WN), or tungsten boride (WB), among others. Suitable tungsten-containing precursors may include, for example, tungsten hexafluoride (WF<sub>6</sub>) and tungsten carbonyl (W(CO)<sub>6</sub>), among others.

**[0048]** The time interval for the pulse of the refractory metal-containing precursor is variable depending on a number of factors such as, for example, the volume capacity of the process chamber employed, the vacuum system coupled thereto and the volatility/reactivity of the reactants used. For example, (1) a large-volume process chamber may lead to a longer time to stabilize the process conditions such as, for example, carrier purge gas flow and temperature, requiring a longer pulse time; and (2) a lower flow rate for the process gas may also lead to a longer time to stabilize the process conditions requiring a longer pulse time. In general, the process conditions are advantageously selected so that a pulse of the refractory metal-containing precursor provides a sufficient amount of precursor, such that at least a monolayer of the refractory metal-containing precursor is adsorbed on the substrate. Thereafter, excess refractory metal-containing precursor remaining in the chamber may be removed from the process chamber by the carrier gas stream in combination with the vacuum system.



**[0049]** In step 208, after the excess refractory metal-containing precursor has been sufficiently removed from the process chamber by the carrier gas stream to prevent co-reaction or particle formation with a subsequently provided process gas, a pulse of a reducing gas is added to the carrier gas stream. Suitable reducing gases may include for example, silane ( $\text{SiH}_4$ ), disilane ( $\text{Si}_2\text{H}_6$ ), dichlorosilane ( $\text{SiCl}_2\text{H}_2$ ), ammonia ( $\text{NH}_3$ ), hydrazine ( $\text{N}_2\text{H}_4$ ), monomethyl hydrazine ( $\text{CH}_3\text{N}_2\text{H}_3$ ), dimethyl hydrazine ( $\text{C}_2\text{H}_6\text{N}_2\text{H}_2$ ), t-butyl hydrazine ( $\text{C}_4\text{H}_9\text{N}_2\text{H}_3$ ), phenyl hydrazine ( $\text{C}_6\text{H}_5\text{N}_2\text{H}_3$ ), 2,2'-azoisobutane ( $((\text{CH}_3)_2\text{C}=\text{N}-\text{N}=\text{C}(\text{CH}_3)_2)$ ), ethylazide ( $\text{C}_2\text{H}_5\text{N}_3$ ), borane ( $\text{BH}_3$ ), diborane ( $\text{B}_2\text{H}_6$ ), triborane ( $\text{B}_3\text{H}_9$ ), tetraborane ( $\text{B}_4\text{H}_{10}$ ), pentaborane ( $\text{B}_5\text{H}_{11}$ ), hexaborane ( $\text{B}_6\text{H}_{12}$ ), heptaborane ( $\text{B}_7\text{H}_{13}$ ), octaborane ( $\text{B}_8\text{H}_{14}$ ), nanoborane ( $\text{B}_9\text{H}_{15}$ ) and decaborane ( $\text{B}_{10}\text{H}_{16}$ ), among others.

**[0050]** The pulse of the reducing gas also lasts for a predetermined time interval. In general, the time interval for the pulse of the reducing gas should be long enough to provide a sufficient amount of the reducing gas for reaction with the refractory metal-containing precursor that is already adsorbed on the substrate. Thereafter, excess reducing gas is flushed from the process chamber by the carrier gas stream in combination with the vacuum system.

**[0051]** Steps 204 through 208 comprise one embodiment of a deposition cycle for the second refractory metal-containing layer. For such an embodiment, a constant flow of the carrier gas is provided to the process chamber modulated by alternating periods of pulsing and non-pulsing where the periods of pulsing alternate between the refractory metal-containing precursor and the reducing gas along with the carrier gas stream, while the periods of non-pulsing include only the carrier gas stream.

**[0052]** The time interval for each of the pulses of the refractory metal-containing precursor and the reducing gas may have the same duration. That is the duration of the pulse of the refractory metal-containing precursor may be identical to the duration of the pulse of the reducing gas. For such an embodiment, a time interval ( $T_1$ ) for the pulse of the refractory metal-containing precursor equals a time interval ( $T_2$ ) for the pulse of the reducing gas.

**[0053]** Alternatively, the time interval for each of the pulses of the refractory metal-containing precursor and the reducing gas may have different durations. That is the duration of the pulse of the refractory metal-containing precursor may be shorter or longer than the duration of the pulse of the reducing gas. For such an embodiment, a time interval ( $T_1$ ) for the pulse of the refractory metal-containing precursor is different than a time interval ( $T_2$ ) for the pulse of the reducing gas.

**[0054]** In addition, the periods of non-pulsing between each of the pulses of the refractory metal-containing precursor and the reducing gas may have the same duration. That is, the duration of the period of non-pulsing between each pulse of the refractory metal-containing precursor and each pulse of the reducing gas is identical. For such an embodiment, a time interval ( $T_3$ ) of non-pulsing between the pulse of the refractory metal-containing precursor and the pulse of the reducing gas equals a time interval ( $T_4$ ) of non-pulsing between the pulse of the reducing gas and the pulse of the refractory metal-containing precursor. During the time periods of non-pulsing only the constant carrier gas stream is provided to the process chamber.

**[0055]** Alternatively, the periods of non-pulsing between each of the pulses of the refractory metal-containing precursor and the reducing gas may have different durations. That is,

the duration of the period of non-pulsing between each pulse of the refractory metal-containing precursor and each pulse of the reducing gas may be shorter or longer than the duration of the period of non-pulsing between each pulse of the reducing gas and the pulse of the refractory metal-containing precursor. For such an embodiment, a time interval ( $T_3$ ) of non-pulsing between the pulse of the refractory metal-containing precursor and the pulse of the reducing gas is different from a time interval ( $T_4$ ) of non-pulsing between the pulse of the reducing gas and the pulse of the refractory metal-containing precursor. During the time periods of non-pulsing only the constant carrier gas stream is provided to the process chamber.

**[0056]** Additionally, the time intervals for each pulse of the refractory metal-containing precursor, the reducing gas and the periods of non-pulsing therebetween for each deposition cycle may have the same duration. For such an embodiment, a time interval ( $T_1$ ) for the pulse of the refractory metal-containing precursor, a time interval ( $T_2$ ) for the pulse of the reducing gas, a time interval ( $T_3$ ) of non-pulsing between the pulse of the refractory metal-containing precursor and the pulse of the reducing gas and a time interval ( $T_4$ ) of non-pulsing between the pulse of the reducing gas and the pulse of the refractory metal-containing precursor, each have the same value for each subsequent deposition cycle. For example, in a first deposition cycle ( $C_1$ ), a time interval ( $T_1$ ) for the pulse of the refractory metal-containing precursor has the same duration as the time interval ( $T_1$ ) for the pulse of the refractory metal-containing precursor in subsequent deposition cycles ( $C_2 \dots C_N$ ). Similarly, the duration of each pulse of the reducing gas as well as the periods of non-pulsing between the pulse of the refractory metal-containing precursor and the reducing gas in the first deposition cycle ( $C_1$ ) is the same as the duration of each pulse of the reducing gas and the periods of non-pulsing between the pulse of the refractory metal-containing precursor and the reducing gas in subsequent deposition cycles ( $C_2 \dots C_N$ ), respectively.

**[0057]** Alternatively, the time intervals for at least one pulse of the refractory metal-containing precursor, the reducing gas and the periods of non-pulsing therebetween for one or more of the deposition cycles of the second refractory metal layer may have different durations. For such an embodiment, one or more of the time intervals ( $T_1$ ) for the refractory metal-containing precursor, the time intervals ( $T_2$ ) for the reducing gas, the time intervals ( $T_3$ ) of non-pulsing between the pulse of the refractory metal-containing precursor and the pulse of the reducing gas and the time interval ( $T_4$ ) of non-pulsing between the pulse of the reducing gas and the pulse of the refractory metal-containing precursor may have different values for one or more subsequent deposition cycles of the cyclical deposition process. For example, in a first deposition cycle ( $C_1$ ), the time interval ( $T_1$ ) for the pulse of the refractory metal-containing precursor may be longer or shorter than the time interval ( $T_1$ ) for the pulse of the refractory metal-containing precursor in subsequent deposition cycles ( $C_2 \dots C_N$ ). Similarly, the duration of each pulse of the reducing gas and the periods of non-pulsing between the pulse of the refractory metal-containing precursor and the reducing gas in deposition cycle ( $C_1$ ) may be the same or different than the duration of corresponding pulses of the reducing gas and the periods of non-pulsing between the pulse of the refractory metal-containing precursor and the reducing gas in subsequent deposition cycles ( $C_2 \dots C_N$ ), respectively.

[0058] Referring to step 210, after each deposition cycle (steps 204 through 208) a total thickness of the second refractory metal will be formed on the substrate. Depending on specific device requirements, subsequent deposition cycles may be needed to achieve a desired thickness. As such, steps 204 through 208 are repeated until the desired thickness for the second refractory metal layer is achieved. Thereafter, when the desired thickness for the second refractory metal layer is achieved the process is stopped as indicated by step 212.

[0059] In an alternate process sequence described with respect to FIG. 6, the second refractory metal layer deposition cycle comprises separate pulses for each of the refractory metal-containing precursor, the reducing gas and a purge gas. For such an embodiment, a refractory metal layer deposition sequence 300 includes adjusting the process chamber conditions (step 302), providing a first pulse of a purge gas to the process chamber (step 304), providing a pulse of a refractory metal-containing precursor to the process chamber (step 306), providing a second pulse of a purge gas to the process chamber (step 308), providing a pulse of the reducing gas to the process chamber (step 310), and then repeating steps 304 through 308, or stopping the deposition process (step 314) depending on whether a desired thickness for the refractory metal layer has been achieved (step 312).

[0060] The time intervals for each of the pulses of the refractory metal-containing precursor, the reducing gas and the purge gas may have the same or different durations as discussed above with respect to FIG. 5. Alternatively, corresponding time intervals for one or more pulses of the refractory metal-containing precursor, the reducing gas and the purge gas in one or more of the deposition cycles of the refractory metal layer deposition process may have different durations.

[0061] In FIGS. 5-6, the refractory metal layer deposition cycle is depicted as beginning with a pulse of the refractory metal-containing precursor followed by a pulse of the reducing gas. Alternatively, the refractory metal layer deposition cycle may start with a pulse of the reducing gas followed by a pulse of the refractory metal-containing precursor.

[0062] One exemplary process of depositing a tungsten layer comprises sequentially providing pulses of tungsten hexafluoride ( $WF_6$ ) and pulses of diborane ( $B_2H_6$ ). The tungsten hexafluoride ( $WF_6$ ) may be provided to an appropriate flow control valve, for example, an electronic control valve, at a flow rate of between about 10 sccm (standard cubic centimeters per minute) and about 400 sccm, preferably between about 20 sccm and about 100 sccm, and thereafter pulsed for about 1 second or less, preferably about 0.2 seconds or less. A carrier gas comprising argon (Ar) is provided along with the tungsten hexafluoride ( $WF_6$ ) at a flow rate between about 250 sccm to about 1000 sccm, preferably between about 500 sccm to about 750 sccm. The diborane ( $B_2H_6$ ) may be provided to an appropriate flow control valve, for example, an electronic control valve, at a flow rate of between about 5 sccm and about 25 sccm, and thereafter pulsed for about 1 second or less, preferably about 0.2 seconds or less. A carrier gas comprising argon (Ar) is provided along with the diborane ( $B_2H_6$ ) at a flow rate between about 250 sccm to about 1000 sccm, preferably between about 500 sccm to about 750 sccm. The substrate may be maintained at a temperature between about

250° C. and about 350° C., preferably about 300° C. at a chamber pressure between about 1 torr to about 10 torr, preferably about 5 torr.

[0063] Another exemplary process of depositing a tungsten layer comprises sequentially providing pulses of tungsten hexafluoride ( $WF_6$ ) and pulses of silane ( $SiH_4$ ). The tungsten hexafluoride ( $WF_6$ ) may be provided to an appropriate flow control valve, for example, an electronic control valve, at a flow rate of between about 10 sccm (standard cubic centimeters per minute) and about 400 sccm, preferably between about 20 sccm and about 100 sccm, and thereafter pulsed for about 1 second or less, preferably about 0.2 seconds or less. A carrier gas comprising argon (Ar) is provided to along with the tungsten hexafluoride ( $WF_6$ ) at a flow rate between about 250 sccm to about 1000 sccm, preferably between about 300 sccm to about 500 sccm. The silane ( $SiH_4$ ) may be provided to an appropriate flow control valve, for example, an electronic control valve, at a flow rate between about 10 sccm to about 500 sccm, preferably between about 50 sccm to about 200 sccm, and thereafter pulsed for about 1 second or less, preferably about 0.2 seconds or less. A carrier gas comprising argon (Ar) is provided along with the silane ( $SiH_4$ ) at a flow rate between about 250 sccm to about 1000 sccm, preferably between about 300 sccm to about 500 sccm. A pulse of a purge gas comprising argon (Ar) at a flow rate between about 300 sccm to about 1000 sccm, preferably between about 500 sccm to about 750 sccm, in pulses of about 1 second or less, preferably about 0.3 seconds or less is provided between the pulses of the tungsten hexafluoride ( $WF_6$ ) and the pulses of silane ( $SiH_4$ ). The substrate may be maintained at a temperature between about 300° C. to about 400° C., preferably about 350° C., at a chamber pressure between about 1 torr to about 10 torr.

[0064] Referring to FIG. 4, the dual-mode deposition process is depicted as forming the first refractory metal layer using a chemical vapor deposition (CVD) process followed by formation of the second refractory metal layer using a cyclical deposition process. Alternatively, the dual-mode deposition process may start with a first refractory metal layer deposited using a cyclical deposition process followed by a second refractory metal layer deposited using a chemical vapor deposition (CVD) process.

## Integrated Circuit Fabrication Processes

### 1. Copper Interconnects

[0065] FIGS. 7A-7C illustrate cross-sectional views of a substrate at different stages of a copper interconnect fabrication sequence incorporating the integrated barrier layer of the present invention. FIG. 7A, for example, illustrates a cross-sectional view of a substrate 400 having metal contacts 404 and a dielectric layer 402 formed thereon. The substrate 400 may comprise a semiconductor material such as, for example, silicon (Si), germanium (Ge), or gallium arsenide (GaAs). The dielectric layer 402 may comprise an insulating material such as, for example, silicon oxide or silicon nitride. The metal contacts 404 may comprise for example, copper (Cu). Apertures 404H may be defined in the dielectric layer 402 to provide openings over the metal contacts 404. The apertures 404H may be defined in the dielectric layer 402 using conventional lithography and etching techniques.

[0066] Referring to FIG. 7B, an integrated barrier layer 406 is formed in the apertures 404H defined in the dielectric layer 402. The integrated barrier layer 406 comprises a titanium

nitride (TiN) layer formed with a chemical vapor deposition (CVD) process and a tungsten (W) layer formed with a cyclical deposition process. The integrated barrier layer **406** is formed using the deposition techniques described above with respect to FIGS. 4-6. The thickness of the integrated barrier layer **406** is typically about 20 Å to about 500 Å.

[0067] Thereafter, the apertures **404H** are filled with copper (Cu) metallization **408** using a suitable deposition process as shown in FIG. 7C. For example, copper (Cu) may be deposited with a chemical vapor deposition (CVD) process using copper-containing precursors such as  $\text{Cu}^{+2}(\text{hfac})_2$  (copper hexafluoro acetylacetonate),  $\text{Cu}^{+2}(\text{fod})_2$  (copper heptafluoro dimethyl octanediene),  $\text{Cu}^{+1}\text{hfac TMVS}$  (copper hexafluoro acetylacetonate trimethylvinylsilane), among others.

## 2. Gate Electrodes

[0068] FIGS. 8A-8C illustrate cross-sectional views of a substrate at different stages of a gate electrode fabrication sequence incorporating the integrated barrier layer of the present invention. FIG. 8A, for example, illustrates a cross-sectional view of a substrate **500** having gate regions **504** formed on the surface thereof. The gate regions **504** are surrounded by a dielectric material **502**. The substrate **500** may comprise a semiconductor material such as, for example, silicon (Si), germanium (Ge), or gallium arsenide (GaAs). The dielectric material **502** may comprise an insulating material such as, for example, silicon oxide or silicon nitride.

[0069] Referring to FIG. 8B, an integrated barrier layer **506** is formed on the gate regions **504**. The integrated barrier layer **506** comprises a titanium nitride (TiN) layer formed with a chemical vapor deposition (CVD) process and a tungsten (W) layer formed with a cyclical deposition process. The integrated barrier layer **506** is formed using the deposition techniques described above with respect to FIGS. 4-6. The thickness of the integrated barrier layer **506** is typically about 20 Å to about 500 Å.

[0070] Thereafter, the gate electrodes are completed by depositing gate metallization **508** on the integrated barrier layer **506** as shown in FIG. 8C. The gate metallization may comprise tungsten (W), aluminum (Al) or copper (Cu), among others. For example, tungsten (W) may be deposited with a chemical vapor deposition (CVD) process from the thermal decomposition of tungsten hexafluoride ( $\text{WF}_6$ ) or tungsten carbonyl ( $\text{W}(\text{CO})_6$ ); aluminum may be deposited with a chemical vapor deposition (CVD) process using dimethyl aluminum hydride (DMAH); or copper (Cu) may be deposited with a chemical vapor deposition (CVD) process using copper-containing precursors such as  $\text{Cu}^{+2}(\text{hfac})_2$  (copper hexafluoro acetylacetonate),  $\text{Cu}^{+2}(\text{fod})_2$  (copper heptafluoro dimethyl octanediene), or  $\text{Cu}^{+1}\text{hfac TMVS}$  (copper hexafluoro acetylacetonate trimethylvinylsilane), among others.

## 3. Trench Capacitors

[0071] FIGS. 9A-9D are illustrative of a metal-insulator-metal (MIM) trench capacitor fabrication sequence incorporating the integrated barrier layer of the present invention. FIG. 9A, for example, illustrates a cross-sectional view of a substrate **655** having a dielectric material layer **657** formed thereon. The substrate **655** may comprise a semiconductor material such as, for example, silicon (Si), germanium (Ge), or gallium arsenide (GaAs). The dielectric material layer **657** may comprise an insulator such as, for example, silicon oxide

or silicon nitride. At least one trench **659** is defined in the dielectric material layer **657**. The trench may be formed using conventional lithography and etching techniques.

[0072] Referring to FIG. 9B, a first integrated barrier layer **660** is formed on the trench **659**. The first integrated barrier layer **660** comprises a titanium nitride (TiN) layer formed with a chemical vapor deposition (CVD) process and a tungsten (W) layer formed with a cyclical deposition process. The first integrated barrier layer **660** is formed using the deposition techniques described above with respect to FIGS. 4-6. The thickness of the integrated barrier layer **660** is typically about 20 Å to about 500 Å.

[0073] A first metal layer **661** is formed over the first integrated barrier layer **660**. The first metal layer **661** comprises the first electrode of the metal-insulator-metal (MIM) trench capacitor. A suitable metal for the first metal layer **661** includes, for example, tungsten (W). The thickness of the first metal layer **661** is typically about 100 Å to about 1000 Å.

[0074] The trench capacitor further includes an insulating layer **663** formed over the metal layer **661**, as shown in FIG. 9C. The insulating layer **663** preferably comprises a high dielectric constant material (dielectric constant greater than about 10). High dielectric constant materials advantageously permit higher charge storage capacities for the capacitor structures. Suitable dielectric materials may include for example, tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ), silicon oxide/silicon nitride/oxynitride (ONO), aluminum oxide ( $\text{Al}_2\text{O}_3$ ), barium strontium titanate (BST), barium titanate, lead zirconate titanate (PZT), lead lanthanum titanate, strontium titanate and strontium bismuth titanate, among others.

[0075] The thickness of the insulating layer **663** is variable depending on the dielectric constant of the material used and the geometry of the device being fabricated. Typically, the insulating layer **663** has a thickness of about 100 Å to about 1000 Å.

[0076] A second integrated barrier layer **664** is formed on the insulating layer **663**. The second integrated barrier layer **664** comprises a titanium nitride (TiN) layer formed with a chemical vapor deposition (CVD) process and a tungsten (W) layer formed with a cyclical deposition process. The second integrated barrier layer **664** is formed using the deposition techniques described above with respect to FIGS. 4-6. The thickness of the integrated barrier layer **664** is typically about 20 Å to about 500 Å.

[0077] A second metal layer **665** is formed over the second integrated barrier layer **664**. The second metal layer **665** comprises the second electrode of the metal-insulator-metal (MIM) trench capacitor. A suitable metal for the second metal layer **665** includes, for example, tungsten (W). The thickness of the second metal layer **665** is typically about 100 Å to about 1000 Å.

[0078] After the second metal layer **665** is formed, the metal-insulator-metal (MIM) trench capacitor is completed by filling the trench **659** with, for example, a polysilicon layer **667**, as shown in FIG. 9D. The polysilicon layer **667** may be formed using conventional deposition techniques. For example, the polysilicon layer **667** may be deposited using a chemical vapor deposition (CVD) process in which silane ( $\text{SiH}_4$ ) is thermally decomposed to form polysilicon at a temperature between about 550° C. and 700° C.

## 4. Crown Capacitors

[0079] FIGS. 10A-10B illustrate cross-sectional views of a substrate at different stages of a crown capacitor fabrication

sequence incorporating the integrated barrier layer of the present invention. The term crown capacitor as used herein refers to a capacitor structure having a three-dimensional shape formed above the surface of the substrate. The three-dimensional shape increases the capacitance of the device by increasing the surface area thereof.

[0080] FIG. 10A, for example, illustrates a cross-sectional view of a substrate 712 having a dielectric layer 714 formed thereon. The substrate 712 may comprise a semiconductor material such as, for example, silicon (Si), germanium (Ge), or gallium arsenide (GaAs). The dielectric 714 may comprise an oxide such as, for example, a silicon oxide. The dielectric layer 714 has at least one aperture 716 formed therein.

[0081] A first polysilicon layer 718 is formed over the dielectric layer 714 and the at least one aperture 716. The first polysilicon layer 718 may be doped with a suitable dopant such as, for example, arsenic (As), antimony (Sb), phosphorous (P) and boron (B), among others.

[0082] A hemispherical silicon grain layer (HSG) 720 or a rough polysilicon layer may optionally be formed over the first polysilicon layer 718 to increase the surface area thereof. The hemispherical silicon grain layer 720 may be formed, for example, by depositing an amorphous silicon layer and then annealing it to form a rough surface thereon. The hemispherical silicon grain layer 720 may optionally be doped.

[0083] The first polysilicon layer 718 and the hemispherical silicon grain layer (HSG) 720 are patterned and etched to form a crown structure 730. Both the first polysilicon layer 718 and the hemispherical silicon grain layer (HSG) act as a first electrode for the crown capacitor.

[0084] The crown capacitor further includes an insulating layer 732 formed over the hemispherical silicon grain layer 718 of the crown structure 730. The insulating layer 732 preferably comprises a high dielectric constant material (dielectric constant greater than about 10). High dielectric constant materials advantageously permit higher charge storage capacities for the capacitor structures. Suitable dielectric materials may include for example, tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ), silicon oxide/silicon nitride/oxy-nitride (ONO), aluminum oxide ( $\text{Al}_2\text{O}_3$ ), barium strontium titanate (BST), barium titanate, lead zirconate titanate (PZT), lead lanthanum titanate, strontium titanate and strontium bismuth titanate, among others.

[0085] Referring to FIG. 10B, an integrated barrier layer 734 is formed on the insulating layer 732. The integrated barrier layer 734 comprises a titanium nitride (TiN) layer formed with a chemical vapor deposition (CVD) process and a tungsten (W) layer formed with a cyclical deposition process. The integrated barrier layer 734 is formed using the deposition techniques described above with respect to FIGS. 4-6. The thickness of the integrated barrier layer 734 is typically about 20 Å to about 500 Å.

[0086] A metal layer 742 is formed over the integrated barrier layer 734. The metal layer 742 comprises the second electrode of the crown capacitor. A suitable metal for the metal layer 742 includes, for example, tungsten (W). The thickness of the metal layer 742 is typically about 100 Å to about 1000 Å.

[0087] After the metal layer 742 is formed, the crown capacitor is completed by depositing, for example, a second polysilicon layer 752 thereover, as shown in FIG. 10B. The second polysilicon layer 752 may be formed using conventional deposition techniques. For example, the second polysilicon layer 752 may be deposited using a chemical vapor

deposition (CVD) process in which silane ( $\text{SiH}_4$ ) is thermally decomposed to form polysilicon at a temperature between about 550° C. and 700° C.

[0088] While the foregoing is directed to the preferred embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. An apparatus for processing a substrate, comprising:
  - a process chamber; and
  - a dual-mode gas distribution plate disposed within the process chamber, the dual-mode gas distribution plate having:
    - a first gas distribution zone disposed in a center of the gas distribution plate; and
    - a second gas distribution zone surrounding the first gas distribution zone, the second gas distribution zone being fluidly isolated from the first gas distribution zone, wherein:
      - the first gas distribution zone is coupled to a valve system to deliver sequential pulses of a first gas to the first gas distribution zone to perform a cyclical deposition process; and
      - the second gas distribution zone is in communication with a flow controller to deliver a second gas to perform a chemical vapor deposition process.
2. The apparatus of claim 1, wherein the valve system comprises one or more electronic control valves.
3. The apparatus of claim 2, wherein each of the one or more electronic control valves deliver pulses of the first gas in intervals of less than about 1 second to about 2 seconds.
4. The apparatus of claim 1, wherein the first gas distribution zone has a center opening and the second distribution zone has a plurality of openings radially dispersed around the center opening.
5. The apparatus of claim 1, further comprising:
  - a seal disposed between the first gas distribution zone and the second gas distribution zone.
6. The apparatus of claim 1, wherein the second gas distribution zone is in fluid communication with at least two gas sources.
7. The apparatus of claim 6, wherein the at least two gas sources are coupled to a mixing chamber disposed between the flow controller and the second gas distribution zone.
8. The apparatus of claim 6, wherein one of the at least two gas sources comprises a titanium containing precursor.
9. The apparatus of claim 6, wherein the valve system is coupled to a tungsten containing gas source and a reducing gas source.
10. An apparatus for processing a substrate, comprising:
  - a process chamber; and
  - a dual-mode gas distribution plate disposed within the process chamber, the dual-mode gas distribution plate comprising:
    - a first gas distribution zone having an opening in a center of the gas distribution plate; and
    - a second gas distribution zone having a plurality of openings surrounding the opening in the center of the gas distribution plate, the second gas distribution zone being fluidly isolated from the first gas distribution zone, wherein:

the first gas distribution zone is coupled to an electronic valve to deliver sequential pulses of a first gas to the first gas distribution zone to perform a cyclical deposition process; and

the second gas distribution zone is in communication with a flow controller to deliver a second gas to perform a chemical vapor deposition process.

**11.** The apparatus of claim **10**, wherein the electronic valve delivers pulses of the first gas in intervals of less than about 1 second to about 2 seconds.

**12.** The apparatus of claim **10**, further comprising:

a seal disposed between the first gas distribution zone and the second gas distribution zone.

**13.** The apparatus of claim **10**, wherein the second gas distribution zone is in fluid communication with at least two gas sources.

**14.** The apparatus of claim **13**, wherein the at least two gas sources are coupled to a mixing chamber disposed between the flow controller and the second gas distribution zone.

**15.** The apparatus of claim **13**, wherein one of the at least two gas sources comprises a titanium containing precursor.

**16.** The apparatus of claim **13**, wherein the electronic valve is coupled to a tungsten containing gas source and a reducing gas source.

**17.** An apparatus for processing a substrate, comprising:

a process chamber; and

a dual-mode gas distribution plate disposed within the process chamber, the dual-mode gas distribution plate comprising:

a first gas distribution zone having an opening in a center of the gas distribution plate; and

a second gas distribution zone having a plurality of openings radially dispersed around the opening in the center of the gas distribution plate, the second gas distribution zone being fluidly isolated from the first gas distribution zone, wherein:

the first gas distribution zone is coupled to an electronic valve to deliver sequential pulses of a tungsten containing gas and a reducing gas to the first gas distribution zone to perform a cyclical deposition process; and

the second gas distribution zone is in communication with a flow controller to deliver a second gas comprising a titanium containing precursor gas to perform a chemical vapor deposition process.

**18.** The apparatus of claim **17**, wherein the electronic valve delivers pulses of the tungsten containing gas and the reducing gas in intervals of less than about 1 second to about 2 seconds.

**19.** The apparatus of claim **17**, further comprising:

a seal disposed between the first gas distribution zone and the second gas distribution zone.

**20.** The apparatus of claim **17**, further comprising:

a mixing chamber disposed between the flow controller and the second gas distribution zone.

\* \* \* \* \*