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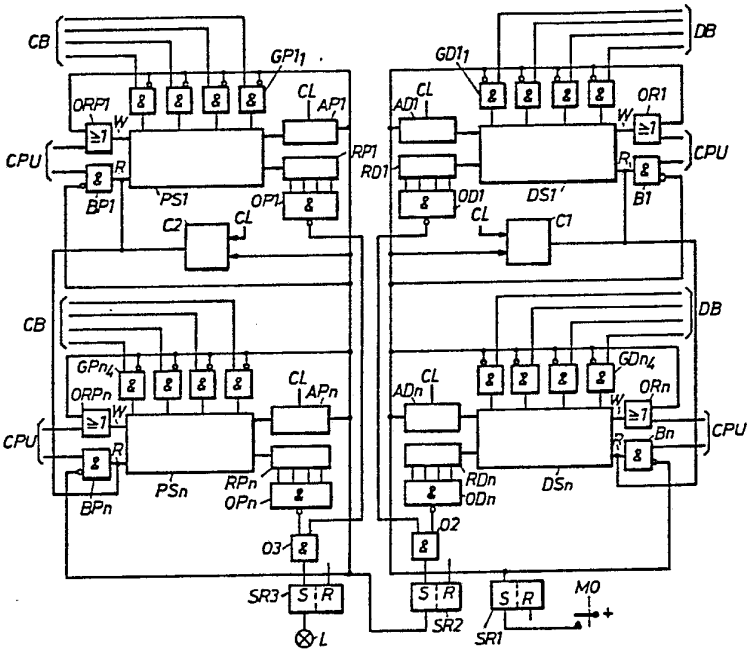
(54) Title: ARRANGEMENT FOR AUTOMATIC ERASING OF THE INFORMATION CONTENTS IN DATA BASES

(57) Abstract

Arrangement to destroy by erasing the information contents in data memories and program memories included in a data base installation, without destroying the equipment. An operation device (MO) is brought to activate a first group of parallelly working address generators (AD1-ADn), these generators successively generating and selecting all addresses in a memory (DS1-DSn) which is separately connected to each of the generators and which is part of a first memory group. Gate circuits ($GD1_1$-GDn_4) are connected to the data inputs on each memory unit in this first memory group through which binary digits of the same logical level is written into the selected addresses of the memories irrespective of what is already written there. The operation device (MO) also activates a second group of parallelly working address generators (AP1-APn), these generators successively generating and selecting all addresses in a memory (PS1-PSn) which is separately connected to each of the generators, said memory being part of a second memory group. Gate circuits (GP_1-GPn_4) are connected to the data inputs of each memory unit in this second memory group through which circuits binary digits of the same logical level are written into the selected addresses of the memories. After completed erasing in said first and second memory group an activation signal is transmitted to a control device (L) which then indicates that the erasing is finished.



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ARRANGEMENT FOR AUTOMATIC ERASING OF THE INFORMATION CONTENTS IN DATA BASES.

FIELD OF THE INVENTION

The invention relates to an arrangement in data bases to prevent someone from unduly access to, or misuse of, the information contents in the data base.

DESCRIPTION OF PRIOR ART

In such data bases where the information contents are confidential or secret, there is always risk of sabotage or undue access to the information. Access to data in such plants is normally limited in different ways for example by classifying terminals, ciphering of data at data transmission or using some kind of system with pass words. The plants are also guarded and located in protected premises. In spite of this there is a risk that groups might occupy a plant. Then it can be difficult to protect data and the functions of the installation. In such extreme cases blasting of the whole installation is in certain cases prescribed.

SUMMARY OF THE INVENTION

The problem in known technics is of course that in manned plants there is a great risk that the staff is hurt at possible blasting, furthermore perhaps a quantity of valuable equipment is destroyed unnecessarily. Furthermore it has proved to be very difficult to destroy data stored on tape or tape casettes in a sufficiently effective way.

The invention, which is characterized in the claim, solves said problem by providing the data base with a special button a so called emergency button which when activated provides electrical impulses to an electronic circuit which in a first step erases all data information in the data base and then in a second step erases all program information in the data base.

The advantage with the arrangement according to the invention compared with known arrangements is that the whole installation can be made

unusable without material destruction and without exposing the staff for any risk of danger. As the data information has been erased the contents on tapes, casettes or disk memories cannot be read in other computers. As all programs have been erased the data base cannot be used for spreading false information either. Furthermore with the arrangement according to the invention a technically simpler and economically more advantageous solution than in known arrangements is obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

The arrangement according to the invention is closer described below by means of an embodiment with reference to the accompanying drawing which is a block diagram of an arrangement according to the invention.

PREFERRED EMBODIMENT

As appears from the figure the arrangement according to the invention is part of a data base installation comprising a data system of a known kind which for example is described in AXE 10 System Survey, LME 118708 where a computer controls writing and reading in connected data memories and program memories. Such writing and reading is known technics and is not included in the inventive idea but is mentioned to facilitate the judgement of the arrangement. In a data base installation such data- and program memories can be for example tape memories, casette memories, disk memories, semiconductor memories etc.

In the installation according to the figure there is a number of data memories DS1-DSn for storing the information with which the data base works. The memories can be of different types and can also contain different kind of information, i.e. they can be considered as function units completely separated from each other. A number of additional memories are also included in the data base, that is the program memories PS1-PSn. Also these memories can provide function units separated from each other. In the memories PS1-PSn those programs are stored which control the processes in the data base. All the memories, data memories as well as program memories receive write- and read

orders from a computer CPU which is connected but not shown in the figure. By dividing the memories in function units a very short access time is obtained. As both data- and program information in a data base can be of a very great value to a saboteur or an attacker there must be in the plant, beside the purely physical protection, a possibility to prevent undue access to the important information which is stored in the memories. As previously mentioned the blasting of the plant is a method which is both dangerous and unsafe. The arrangement according to the invention admits effective elimination of data and program through erasing so that neither staff nor equipment will be damaged.

Furthermore it appears from the figure that the arrangement according to the invention contains address generators AD1-ADn and AP1-APn, respectively, separately connected to the address inputs of each data store DS1-DSn and program store PS1-PSn, respectively, for pointing out each memory position appearing in the connected memory. Gate circuits $GD1_1$- GDn_4 and GP1-GPn_4, respectively, are connected to the data inputs of the memories, from which gates logical zeros are written into each position on a pointed out address in the memory when the memory receives a writing pulse on a writing input W. Thus the idea of the erasing is that for each pointed out address in the memory only zeros are written into the pointed out positions irrespective of what is written there before until the whole memory is filled with zeros.

As appears from the figure the output from an operation point MO is connected to the set-input on a bistable flip-flop SR1, the task of which is, when activated, to provide a signal of a determined logical level as long as no activation signal is fed to the reset-input of the flip-flop. The output of the flip-flop is connected to the inputs of a number of address generators AD1-ADn made by TEXAS INSTRUMENTS type 74 LS 191. Each of the address generators is separately connected on the outputs to the address inputs on a corresponding data memory DS1-DSn made by INTEL type 2114 L. The task of the address generators, when activated and when controlled by a clock CL being common to the system, is to generate all addresses which can appear in the connected data memory and in turn point out each address in the

memory. In the embodiment it has been assumed that each word which is stored in the memory consists of 4 bits, of course the memories can also be designed for other word lengths, for example 8 bits. This, however, does not effect the principle for erasing. The output from a gate circuit $GD1_1$-GDn_4 is connected to each of the data inputs on each data memory DS1-DSn. The gate circuits are logical AND-circuits made by NATIONAL type 74 LS 02 provided with two inputs one of which is inverting. The output from said flip-flop SR1 is connected to all the mentioned inverting inputs of the AND-circuits. The second input on each of the AND-circuits is connected to a data bus DB which is common to the memories through which data bus the communication is maintained between the computer CPU and the memories DS1-DSn. According to the embodiment the computer can be a microprocessor made by MOTOROLA type MC 68000. The output from the flip-flop SR1 is also connected to one of the inputs of an OR-circuit OR1-ORn, the second input of which is fed from the computer CPU. The output of said OR-circuits is connected to the write input of respective associated data memory. A register RD1-RDn made by TEXAS INSTRUMENTS type 74LS174 is connected to the data outputs on each of the data memories. The registers contain as many positions as the data word, i.e. in the chosen case 4. The outputs from the registers are connected to corresponding inputs of AND-circuits OD1-ODn, the outputs of which are inverting and connected to inputs of a further AND-circuit O2. The circuit O2 has as many inputs as the number of AND-circuits OD1-ODn, which in its turn depends on the number of data memories. In the chosen embodiment the number of memories is two DS1-DSn, which implies two AND-circuits OD1-ODn and consequently two inputs on the circuit O2. As appears from the labelling of the memories of course there can be more than two memories.

A counter C1 common to all data memories is also connected to the output of the flip-flop SR1, which counter controlled by the system clock CL, transmits a read pulse to the data memory when the last position in the data memory has been pointed out, so that the word in the last position of the data memory is read out to respective register RD1-RDn. In order to prevent data from being read from the memory from any other address than the last selected when erasing, blocking circuits B1-Bn are connected to the read inputs of the data memories, said

blocking circuits consisting of AND-circuits the one input of which is inverting and connected to the output on the flip-flop SR1. The second input of the circuits B1-Bn is fed from the computer CPU, which in normal circumstances provides a reading pulse on this input. The output from the AND-circuit 02 is connected to the set-input on a second bistable flip-flop SR2 of the same type as the flip-flop SR1 and the output of which, in exactly the same manner as the output from the flip-flop SR1, feeds an exactly identical electronic circuit which controls the work towards the data memories but this circuit is now intended for the program memories PS1-PSn, which memories are of the same type as the data memories. Thus the output of the flip-flop SR2 is connected to the inputs of the address generators AP1-APn, which address generators are of the same type as the generators AD1-ADn. Each of the address generators is connected to the address inputs of a corresponding program memory PS1-PSn. The task of the generators, as previously mentioned, is to generate all addresses which can appear in the connected program memory controlled by the common system clock, and in turn point out each address in the memory. The word length in the program memories is the same as in the data memories i.e. 4 bits. Gate circuits $GP1_1$-GPn_4 of the same type as the gate circuits $GD1_1$-GDn_4 are connected to the data inputs of the program memories. The output of the flip-flop SR2 is connected to the inverting input of all AND-circuits $GP1_1$-GPn_4. A second input on each of the AND-circuits is connected to a control bus CB being common to the program memories through which bus the computer CPU in the normal case exchange data with the memories PS1-PSn. The output from an OR-circuit ORP1-ORPn is connected to the writing input on each of the program memories. One input on each OR-circuit is fed from the computer CPU providing a writing pulse at normal operation. The second input of the OR-circuits is connected to the output of the flip-flop SR2, from which write pulses are obtained when erasing. A register RP1-RPn of the same type as the registers RD1-RDn is connected to the data outputs on each of the memories PS1-PSn. The outputs from the registers are connected to corresponding inputs on AND-circuits OP1-OPn the outputs of which are inverting and connected to inputs of a further AND-circuit 03.

The output of the circuit 03 is connected to the set-input on a third bistable flip-flop SR3, of the same type as the flip-flops SR1-SR2, and

the output of which is connected to a supervisory lamp L. To the output of the flip-flop SR2 is also in this case connected a counter C2 common for all program memories and of the same type as the counter C1, which counter C2 when the last position in the program memory has been pointed out, reads the selected word into respective register RP1-RPn. AND-circuits BP1-BPn are connected to the read inputs of the program memories to block reading in the memory during erasing. One of the inputs of each of the circuits BP1-BPn is inverting and fed from the output of the flip-flop SR2. Under normal conditions the computer CPU providing read pulses to the memories by connection to the second input of the circuits BP1-BPn. As mentioned the counter C2 cancels the read blocking each time the last address in the memory has been selected. In normal cases a computer CPU works in a known manner towards connected memories DS1-DSn and PS1-PSn, respectively. If, however, such a situation should occur that the information in all memories has to be erased, this is done according to the process described below.

The operator activates a non-locking push-button a so called "emergency button" at an operation point MO. Then a positive voltage pulse is transmitted to the set-input of the bistable flip-flop SR1 which then is set to ONE, i.e. providing a logical one-signal on the output and remaining in this position if not a zero-setting-signal is fed to the reset input of the flip-flop. The output signal from the flip-flop SR1 activates the address generators AD1-ADn, which controlled by signals from the common system clock CL starts generating all addresses which can appear in the connected data memories DS1-DSn. The address generators work in parallel but each towards its own data memory. In turn all addresses in the data memories are pointed out. The output signal from the flip-flop SR1 also activates the inverting inputs of the AND-circuits $GD1_1$-GDn_4, the outputs from the mentioned AND-circuits being seized by a logical ZERO-signal. The ONE-signal from the flip-flop SR1 is fed to one of the inputs of each of the OR-circuits OR1-ORn the outputs of which then transmitting write pulses to the write input W on respective data memory DS1-DSn. When a data memory receives a writing pulse the zeros from the outputs of the AND-circuits $GD1_1$-GDn_4 are written into each memory position on the address pointed out by the address generators. In this manner the pointing out and writing

into each memory continues until the whole memory is filled with zeros irrespective of what has been written previously. To obtain acknowledgement signal that the memories are completely erased, i.e. filled with zeros and to start the erasing process for the program memories PS1-PSn, information from the last address position of respective data memory is read to the registers RD1-RDn. As previously mentioned the reading from the data memories is locked in all address positions but the last. The counter C1 which contains as many steps as the number of words in the data memory is activated by the signal from the flip-flop SR1 and is stepped, controlled by the common system clock, one step for each selected address in the data memory. When the counter has reached the position corresponding to the last address position of the data memory it provides on the output a signal which directly activates the read input R of all data memories DS1-DSn, the contents in the last address position of each data memory being fed to respective register RD1-RDn. In the rest of the address positions the reading is locked by the ONE-signal from the output of the flip-flop SR1, which signal is fed to the inverting inputs of the AND-circuits B1-Bn, the outputs from these circuits transmitting zero-signal to the read input of respective data memory. On these addresses no activation signal from the counter C1 is transmitted. The output signals from the registers RD1-RDn are fed to corresponding inputs on the AND-circuits OD1-ODn. As the outputs of said AND-circuits are inverting each circuit provides a logical ONE-signal which is fed to a corresponding input of an AND-circuit O2. Thus the inputs of the circuit O2 are activated in parallel when the last address position of respective data memory is read. The signal from the output on the circuit O2 is fed to the input of the flip-flop SR2 which then is activated and transmits an ONE-signal on the output. This signal constitutes activation signal for erasing in the program memories PS1-PSn. The process is exactly the same as has been described when erasing in the data memories DS1-DSn. The signals from the flip-flop SR2 activate the address generators AP1-APn, which controlled by the system clock CL generates all addresses which can appear in the connected program memories PS1-PSn. In turn all addresses are pointed out. The signal from the flip-flop SR2 activates the inverting inputs of the AND-circuits $GP1_1$-GPn_4, and furthermore it provides writing pulse to the writing input W of

the program memories by activating one input of each of the OR-circuits ORP1-ORPn. The logical zeros appearing on the data inputs of the memories when erasing, are written into the addresses pointed out by the address generators so that finally also all program memories are filled with zeros. The erasing is then finished and the information in the last selected address position in each program memory is read to respective register RP1-RPn, when reading pulse is obtained from the counter C2 which is stepped syncronously with the address generators and common to the memories. Blocking of reading in the rest of the memory positions is obtained by the fact that the output signal from the flip-flop SR2 activates the inverting inputs of the AND-circuits BP1-BPn, zero signal being obtained on the reading inputs R of the memories as also the counter C2 in these address positions transmits zero signal. The signals from the registers RP1-RPn are fed to corresponding inputs of the AND-circuits OP1-OPn, the inverting outputs of which transmit signals to corresponding inputs of an AND-circuit 03. When all memories have been erased and the inputs to the circuit 03 consequently has been activated this circuit transmits an output signal to the third bistable flip-flop SR3, which then is set to ONE and transmits activation signal to the lamp L which then is turned on and shows that the whole erasing process is ended.

Under normal conditions where all flip-flops SR are set to zero, i.e. there is no erasing going on, the computer CPU, not shown in the drawing, controls the writing and reading in the memories. The writing is carried out by connection to the OR-circuits OR1-ORn and ORP1-ORPn, respectively. The reading is carried out by connecting the computer to the AND-circuits B1-Bn and BP1-BPn, respectively. When zero-signal is transmitted from the outputs of the flip-flops SR1 and SR2 to the inverting inputs of the AND-circuits $GD1_1$-GDn_4 and $GP1_1$-GPn_4, respectively, the feeding of information to the memories from the data bus DB and the control bus CB is completely controlled by the computer CPU.

Further advantages with the arrangement according to the invention are:

As several physical memories are utilized it would take a long time to erase all information if the computer itself should perform this with normal access methods, one word at a time. By parallel erasing

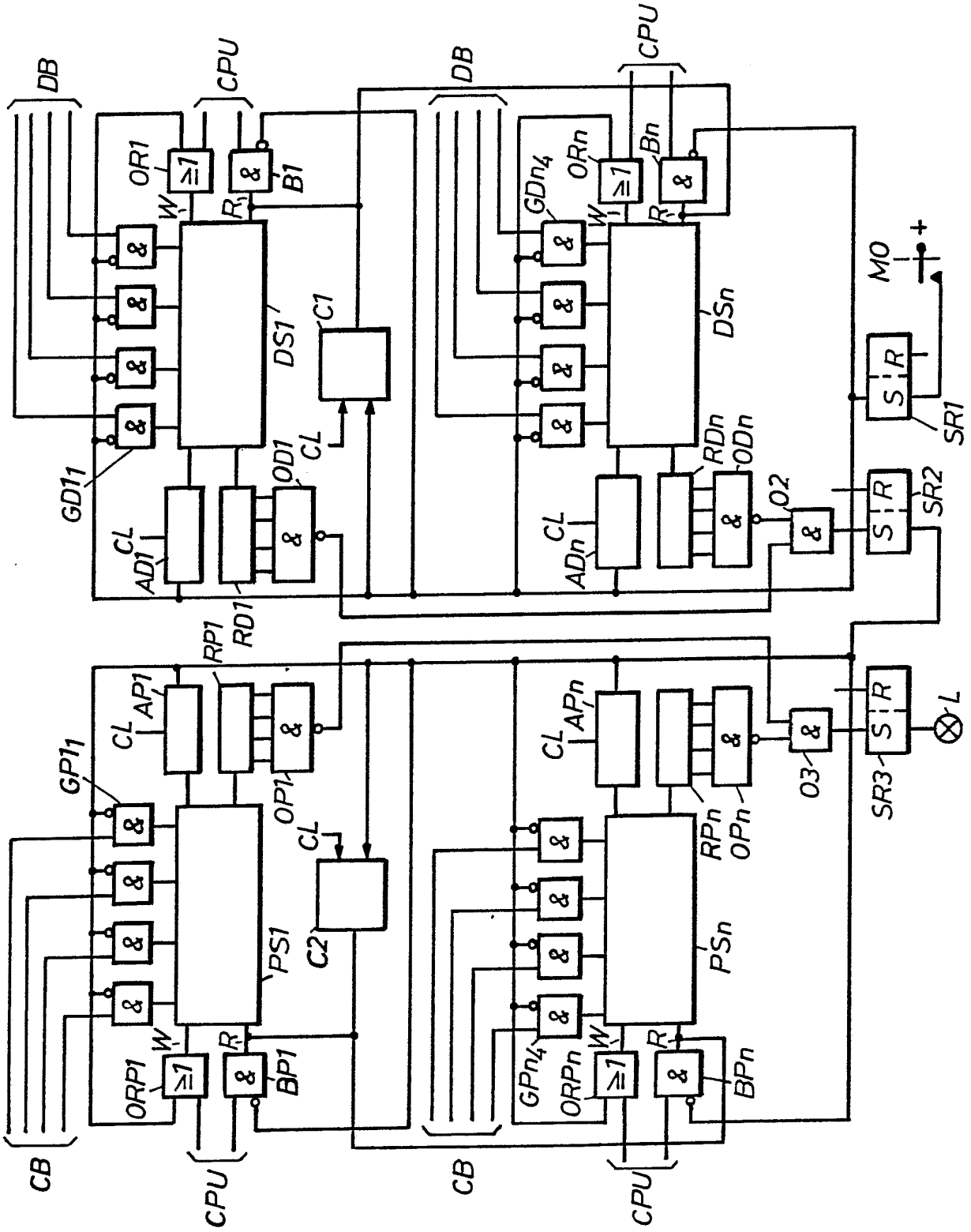
in the memories a considerable gain of time is obtained.

By the arrangement according to the invention a capacity demanding work is unloaded from the computer.

A short access time by dividing into serveral memories which also implies modularity at a possible expansion.

WHAT WE CLAIM IS:

An arrangement for automatic destroying by erasing the information contents in data memories and program memories in a data base installation without destroying the equipment, characterized in that an operation device (MO), when activated transmits a control signal to a first group of parallelly working address generators (AD1-ADn) for successive generation and selection of all addresses in a memory (DS1-DSn) being separately connected to each of the generators and which memory being included in a first memory group, said control signal also being connected to a second group of parallelly working address generators (AP1-APn) for successive generation and selection of all addresses in a memory (PS1-PSn) being separately connected to each of the address generators, which memory is included in a second memory group, and that gate circuits ($GD1_1$-GDn_4) are connected to the data inputs on each memory unit of said first memory group through which circuits binary digits of the same logical level in a first step are written into the successively selected addresses of said memories of said first memory group, and that gate circuits ($GP1_1$- GP_n4) are connected to the data inputs on each memory unit of said second memory group through which circuits binary digits of the same logical level in a second step are written into the successively selected addresses of said memories of said second memory group.



INTERNATIONAL SEARCH REPORT

International Application No PCT/SE81/00385

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC 3

G 11 C 7/00, 8/00, G 11 B 5/02

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC 3	G 11 B 5/02-/09, G 11 C 8/00, 7/00
US Cl	365:189, 218, 230; 360:57, 66

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

SE, NO, DK, FI classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [15] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 4 172 291 (FAIRCHILD CAMERA AND INSTRUMENT CORP) 23 October 1979	
A	GB, A, 1 486 386 (INTERNATIONAL BUSINESS MACHINES CORP) 21 September 1977	

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]

1982-01-11

Date of Mailing of this International Search Report [2]

1982 -01- 20

International Searching Authority [1]

Swedish Patent Office

Signature of Authorized Officer [20]

Carl-Göran Forsberg