(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 July 2014 (24.07.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/110653 A1

(51) International Patent Classification:
H04N 5/228 (2006.01) *H04N 7/18* (2006.01)

(21) International Application Number:
PCT/CA2013/050059

(22) International Filing Date:
28 January 2013 (28.01.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/752,896 15 January 2013 (15.01.2013) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

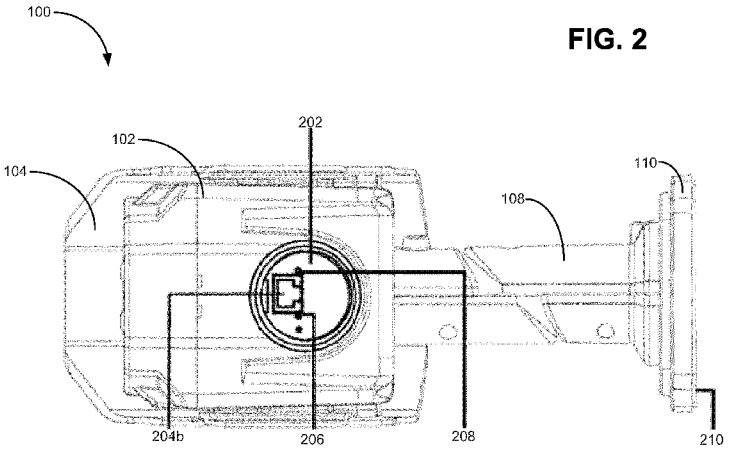
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: SECURITY CAMERA HAVING DUAL COMMUNICATION PORTS

FIG. 2



(57) Abstract: The present disclosure is directed at a security camera having dual communication ports. The camera includes a camera body mountable to a mounting surface and comprising an aperture, a lens, an imager, primary communication circuitry comprising a primary communication port accessible from outside the camera body, secondary communication circuitry comprising a secondary communication port accessible from outside the camera body, and control and processing circuitry communicatively coupled to the imager and to the primary and secondary communication circuitry. The primary communication port is on one side of the mounting when the camera body is mounted and the secondary communication port and the aperture are on an opposing side of the mounting surface when the camera body is mounted. A digital communication signal is sent to the secondary communication port when the secondary communication port is coupled to an active link.

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SECURITY CAMERA HAVING DUAL COMMUNICATION PORTS

TECHNICAL FIELD

[0001] The present disclosure is directed at a security camera having dual communication ports.

BACKGROUND

[0002] The security industry, and in particular the market for internet protocol (IP) security cameras, continues to grow. This is, at least in part, due to the advantages that IP security cameras enjoy over conventional, analog security cameras. For example, IP cameras permit two-way communication, allow for higher resolution than analog cameras, and can easily be relocated on an IP network. Given their increasing popularity, research and development continue into making IP security cameras easier to install and use.

SUMMARY

[0003] According to a first aspect, there is provided a security camera having dual communication ports. The camera comprises a camera body mountable to a mounting surface and comprising an aperture to permit light to enter the camera body; a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture; an imager located within the camera body and positioned to receive the light refracted by the lens; primary communication circuitry comprising a primary communication port accessible from outside the camera body, wherein the primary communication port is on one side of the mounting surface when the camera body is mounted; secondary communication circuitry comprising a secondary communication port accessible from outside the camera body, wherein the secondary communication port and one or both of the lens and the aperture are on an opposing side of the mounting surface when the camera body is mounted; and control and processing circuitry communicatively coupled to the imager and to the primary and secondary communication circuitry, the control and processing circuitry comprising a processor and a computer readable medium, communicatively coupled to the processor, having encoded thereon statements and instructions to cause the processor to send a digital communication signal derived

from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link.

[0004] According to another aspect, there is provided a security camera having dual communication ports. The camera comprises a camera body comprising an aperture to permit light to enter the camera body; a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture; an imager located within the camera body and positioned to receive the light refracted by the lens; an attachment assembly attached to the camera body and mountable to a mounting surface; primary communication circuitry comprising a primary communication port accessible through the attachment assembly; secondary communication circuitry comprising a secondary communication port accessible through the camera body; and control and processing circuitry communicatively coupled to the imager and to the primary and secondary communication circuitry, the control and processing circuitry comprising a processor and a computer readable medium, communicatively coupled to the processor, having encoded thereon statements and instructions to cause the processor to send a digital communication signal derived from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link. The attachment assembly may comprise a mounting arm affixed to an attachment plate, and the attachment plate may comprise an access port through which the primary communication port is accessible. The access port may be positioned on a surface of the attachment plate adjacent to the mounting surface when the camera is mounted.

[0005] According to another aspect, there is provided a security camera having dual communication ports that comprises a camera body mountable to a mounting surface and comprising an aperture to permit light to enter the camera body; a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture; an imager located within the camera body and positioned to receive the light refracted by the lens; primary communication circuitry comprising a primary communication port accessible from outside the camera body, wherein the primary communication port is behind the mounting surface when the camera body is mounted; secondary communication circuitry comprising a secondary communication port accessible from outside the camera body, wherein the secondary communication is in front of the mounting surface when the camera body is mounted; and

control and processing circuitry communicatively coupled to the imager and to the primary and secondary communication circuitry, the control and processing circuitry comprising a processor and a computer readable medium, communicatively coupled to the processor, having encoded thereon statements and instructions to cause the processor to send a digital communication signal derived from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link.

[0006] The following describes potential variations to all of the foregoing aspects.

[0007] The digital communication signal may be simultaneously sent to both the primary and secondary communication ports.

[0008] Alternatively, the digital communication signal may be separately sent to the primary communication port or to the secondary communication port.

[0009] The statements and instructions may further cause the processor to detect whether the secondary communication port is coupled to the active link, and to send the digital communication signal to the secondary communication port only when the secondary communication port is coupled to the active link.

[0010] Detecting whether the secondary communication port is coupled to the active link may comprise polling the secondary communication port.

[0011] The statements and instructions may further cause the processor, when the secondary communication port is not coupled to the active link, to send the digital communication signal to the primary communication port.

[0012] The secondary communication port may be located on an underside of the camera body.

[0013] The digital communication signal may be communicated using Ethernet.

[0014] The control and processing circuitry may further comprise a media access controller (MAC) and input/output control circuitry, each of which is communicatively coupled to the processor and to the primary and secondary communication circuitry.

[0015] The primary communication circuitry may comprise a primary PHY communicatively coupled to the primary communication port and to the MAC and the secondary communication circuitry may comprise a secondary PHY communicatively coupled to the secondary communication port and to the MAC.

[0016] The primary and secondary PHYs may be communicatively coupled to the MAC through a shared media-independent interface (MII bus) and a shared management data input/out interface (MDIO bus) of the MAC.

[0017] The primary and secondary PHYs may be pin strapped to commence operation by setting their outputs that are connected to the MII bus to a high impedance state.

[0018] The input/output circuitry may comprise a primary reset line communicatively coupled to a reset input of the first PHY, a secondary reset line communicatively coupled to a reset input of the second PHY, and an address line communicatively coupled to an MDIO address select input on the first and second PHYs.

[0019] The statements and instructions may further cause the processor, prior to detecting that the secondary communication port is coupled to the active link, to send the digital communication signal to the primary communication port via the primary PHY and to set outputs of the secondary PHY connected to the MII bus to a high impedance state, and following detecting that the secondary communication port is coupled to the active link: to stop the primary PHY; to notify the application layer that there is no active link prior to activating the secondary PHY; to set outputs of the primary PHY connected to the MII bus to a high impedance state; to take the outputs of the secondary PHY connected to the MII bus out of a high impedance state; to activate the secondary PHY; and to notify the application layer that the active link is present.

[0020] The camera may be a bullet camera.

[0021] According to another aspect, there is provided a method for switching between primary and secondary communication ports of a security camera comprising a camera body mountable to a mounting surface, an aperture in the camera body to permit light to enter the camera body, a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture, and an imager located within the camera body and positioned

to receive the light refracted by the lens, wherein the primary communication port is on one side of the mounting surface when the camera body is mounted and the secondary communication port and one or both of the lens and aperture are on an opposing side of the mounting surface when the camera body is mounted. The method comprising sending a digital communication signal comprising a video signal derived from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link.

[0022] The digital communication signal may be simultaneously sent to both the primary and secondary communication ports. Alternatively, the digital communication signal may be separately sent to the primary communication port or to the secondary communication port.

[0023] The method may further comprise detecting whether the secondary communication port is coupled to the active link, and sending the digital communication signal to the secondary communication port only when the secondary communication port is coupled to the active link.

[0024] Detecting whether the secondary communication port is coupled to the active link may comprise polling the secondary communication port.

[0025] The method may further comprise when the secondary communication port is not coupled to the active link, sending the digital communication signal to the primary communication port.

[0026] The secondary communication port may be located on an underside of the camera body.

[0027] The digital communication signal may be communicated using Ethernet.

[0028] The camera may further comprise a media-independent interface (MII) bus and a primary PHY and a secondary PHY, each of which has outputs connected to the MII bus and via which the digital communication signal is sent to the primary and secondary communication ports, and the method may further comprise: prior to detecting that the secondary communication port is coupled to the active link, sending the digital communication signal to the primary communication port via the primary PHY and setting the outputs of the secondary PHY

connected to the MII bus to a high impedance state; and following detecting that the secondary communication port is coupled to the active link: stopping the primary PHY; notifying the application layer that there is no active link prior to activating the secondary PHY; setting outputs of the primary PHY connected to the MII bus to a high impedance state; taking the outputs of the secondary PHY connected to the MII bus out of a high impedance state; activating the secondary PHY; and notifying the application layer that the active link is present.

[0029] The camera may be a bullet camera.

[0030] According to another aspect, there is provided a non-transitory computer readable medium having encoded thereon statements and instructions to cause a processor to perform any of the foregoing aspects of methods or combinations thereof.

[0031] This summary does not necessarily describe the entire scope of all aspects. Other aspects, features and advantages will be apparent to those of ordinary skill in the art upon review of the following description of specific embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] In the accompanying drawings, which illustrate one or more exemplary embodiments:

[0033] Figure 1 is a perspective view of a security camera having dual communication ports, according to one embodiment.

[0034] Figure 2 is a bottom plan view of the camera of Figure 1.

[0035] Figure 3 is a block diagram of an imager, control and processing circuitry, and communication circuitry used in the camera of Figure 1.

[0036] Figures 4(a) and (b) are a flowchart of a method for switching between the dual communication ports of the camera of Figure 1, according to another embodiment.

[0037] Figures 5(a) to (c) are block diagrams of alternative embodiments of the imager, control and processing circuitry, and communication circuitry of Figure 3.

DETAILED DESCRIPTION

[0038] Directional terms such as "top," "bottom," "upwards," "downwards," "vertically," and "laterally" are used in the following description for the purpose of providing relative reference only, and are not intended to suggest any limitations on how any article is to be positioned during use, or to be mounted in an assembly or relative to an environment.

[0039] During conventional installation of an IP security camera, an installation technician connects the camera to a network via which the camera will transmit a digital communication signal, which includes digital video information used to generate a video and control information. The connection between the camera and the network ("network connection") is behind the surface to which the camera is mounted ("mounting surface"); for example, if the mounting surface is a wall, the network connection is made behind the wall. The location of the network connection means that once the camera is in place and secured to the mounting surface the technician can no longer physically access the network connection.

[0040] Once the camera has been mounted, the installation process involves the technician viewing the video generated from the digital communication signal that the camera outputs to the network to properly focus and aim the camera. Because the network connection is inaccessible to the technician, however, the technician either directly views the video from a video terminal connected to the network and remote from the camera or works with a partner who is at the video terminal and relays information to the technician. Neither solution is optimal: in the former case, time is wasted as the technician travels between the camera and the video terminal while in the latter case labor costs are higher than if the technician works alone.

[0041] The embodiments disclosed herein are directed at a security camera that has dual communication ports, which are used to output the digital communication signal. One of the communication ports ("primary communication port") is positioned to be behind the mounting surface when the camera is installed, while the other ("secondary communication port") is positioned to be in front of the mounting surface and accessible to the technician even after the camera has been mounted. When the technician connects a video terminal to the secondary communication port, the camera outputs the digital communication signal to the technician's video terminal to allow the technician to view the video and to focus and aim the camera while

working alone and without having to leave the camera, thereby facilitating installation of the camera.

[0042] Referring now to Figures 1 and 2, there are respectively shown a perspective view and a bottom plan view of a security camera 100 having dual communications ports, a mounting arm 108, and an attachment plate 110, according to one embodiment. The mounting arm 108 and attachment plate 110 are collectively the "attachment assembly" of the camera. The camera 100 includes and is housed within a camera body 102 that has an aperture 106 to permit light to enter the camera body 102. A lens (not shown) is mounted to the camera body 102 and is positioned to refract the light entering the camera body 102 through the aperture 106. In the depicted embodiment, the lens is contained within the camera body 102; however, in alternative embodiments (not depicted), the lens may be mounted to the exterior of the camera body 102. Attached to the left and right sides of the camera body 102 and extending along the top of the camera body 102 is a hood 104 that overhangs the front of the camera body 102. The rear of the camera body 102 is attached to the mounting arm 108, which connects the camera body 102 to the attachment plate 110 that is affixed to the mounting surface.

[0043] On the underside of the camera body 102 is a configuration panel 202 that has on it a secondary communication port in the form of a configuration Ethernet port 204b, a connection status LED 206, and a link LED 208, which are discussed in more detail below. On the attachment plate 110 are a serial number tag 210 that identifies the camera 100 and an access port (not shown) on the surface of the attachment plate 110 that is adjacent the mounting surface when the camera 100 is mounted. A primary communication port in the form of a primary Ethernet port 204a (shown in Figure 3) is accessible through the access port and is connected to the network during camera installation. The Ethernet port 204a is on one side of the mounting surface when the camera body 102 is mounted (*e.g.*: behind a wall) whereas the configuration Ethernet port 204b and the lens are on an opposing side of the mounting surface when the camera body 102 is mounted (*e.g.*: in front of the wall). The configuration Ethernet port 204b is consequently easily accessible by the technician even after the camera 100 has been mounted to the mounting surface, whereas the access port is not.

[0044] Referring now to Figure 3, there is shown a block diagram 300 of an imager 318, control and processing circuitry 302, and communication circuitry 304a,304b housed within the camera body 102. The imager 318 is positioned to receive the light refracted by the lens and to output a signal to the control and processing circuitry 302, which in Figure 3 is a system on chip (SoC) 308 and a computer readable medium 320 such as non-volatile memory storing statements and instructions for the SoC 308 to perform. Exemplary statements and instructions include a method 400 for switching between the ports 204a,b of the camera 100 as shown in Figure 4 and discussed in more detail below. The SoC 308 includes a processor 310 that is communicatively coupled to each of the other components of the SoC 308: an image signal processor (ISP) 316, a media access controller (MAC) 314, and input/output control circuitry in the form of general purpose input/output (GPIO) lines 312. The processor 310 is also communicatively coupled to the computer readable medium 320.

[0045] Two buses are connected to the MAC 314: a media independent interface (MII) bus and a management data input/output (MDIO) bus. These two buses are used by the MAC 314 to communicate with, and are shared by, the primary and secondary communication circuitry 304a,304b. The primary communication circuitry 304a includes a primary Ethernet physical layer IC (an Ethernet physical layer IC is hereinafter referred to as a "PHY") 324a that is communicatively coupled using transmit and receive lines to the primary Ethernet port 204a via Ethernet magnetics 326a. Electrically coupled to the Ethernet magnetics 326a is a DC to DC converter 322 that receives power from the network when the camera is connected to the network via the primary Ethernet port 204a; this power is used to power the camera 100 using power over Ethernet (PoE) technology. The primary PHY 324a is connected to the MAC 314 via the MDIO and MII buses. Similarly, the secondary communication circuitry 304b includes a secondary PHY 324b that is communicatively coupled using transmit and receive lines to the configuration Ethernet port 204b via Ethernet magnetics 326b. The secondary PHY 324b is also connected to the MAC 314 via the MDIO and MII buses. In the depicted embodiment, each of the Ethernet ports 204a,b is an RJ-45 connector and each of the PHYs 324a,b is a Broadcom™ BCM5421 10/100BaseT (Fast) Ethernet physical layer IC.

[0046] One of the GPIO lines 312, labeled RESET_PHY1 in Figure 3, is connected to a reset pin on the primary PHY 324a while another of the GPIO lines 312, labeled RESET_PHY2

in Figure 3, is connected to a reset pin on the secondary PHY 324b. The SoC 308 is accordingly able to independently reset each of the PHYs 324a,b. Another of the GPIO lines 312, labeled PHY_ADDRESS in Figure 3, is connected to an MDIO address select pin on each of the PHYs 324a,b. By controlling the PHY_ADDRESS line while de-asserting the reset signal for a particular one of the PHYs 324a,b the SoC 308 can assign a separate MDIO address to each of the PHYs 324a,b, which is done to allow both of the PHYs 324a,b to communicate on the shared MDIO bus. This procedure is performed during system initialization.

[0047] Each of the PHYs 324a,b also has an isolate pin that is pin strapped high. The PHYs 324a,b consequently boot up in "super isolated" mode in which each of the PHYs 324a,b ignores any input it receives from the Ethernet ports 204a,b and their outputs that are connected to the MII bus are set to a high impedance state. The SoC 308 can use the MDIO bus to configure the PHYs 324a,b to transition to "isolated" mode in which the PHYs 324a,b are able to detect whether the ports 204a,b are coupled to an active link but its outputs that are connected to the MII bus are still set to a high impedance state, and to exit isolated mode and enter an active mode in which the PHYs 324a,b are able to transmit data over the MII bus. In the depicted embodiment in which Ethernet is used to communicate, being coupled to an active link refers to the PHYs 324a,b being coupled to an active Ethernet connection via the ports 204a,b. More generally, being coupled to an active link refers to the primary and secondary communication circuitry being coupled, via the primary and secondary communication ports, respectively, to an active connection that communicates using a protocol that the primary and secondary communication circuitry is designed to use.

[0048] Each of the PHYs 324a,b has a "link" pin that is low when the PHYs 324a,b do not detect an active link and high when they do. The link pins from the PHYs 324a,b are logically ORed together with the result output to the link LED 208; the link LED 208 accordingly indicates whether either of the PHYs 324a,b is coupled to an active link. The primary PHY 324a also has a "status" pin that the SoC 308 controls via the MDIO bus. The status pin is connected to the status LED 206, which accordingly shows the status as determined by the SoC 308.

[0049] Referring now to Figures 4(a) and (b), there is shown a flowchart of the method 400 for switching between the dual communication ports 204a,b of the camera 100. The SoC 308 monitors the configuration Ethernet port 204b to detect when it is coupled to an active link. When it is coupled to an active link, such as when the technician connects a video terminal to it to focus and aim the camera 100 during installation, the SoC 308 then sends the digital communication signal, which includes the digital video information derived from the light incident on the imager 318, to the configuration Ethernet port 204b. If the SoC 308 was previously sending the digital communication signal to the primary Ethernet port 204a, in the depicted embodiment the SoC 308 ceases sending the digital communication signal to the primary Ethernet port 204a before sending the signal to the configuration Ethernet port 204b. In Figures 4(a) and (b), the primary PHY 324a is referred to as PHY1 and the secondary PHY 324b is referred to as PHY2.

[0050] At block 402, the camera 100 boots up. As discussed above, the PHYs 324a,b are pin strapped to boot up in super isolated mode. At block 404, the SoC 308 sets both of the PHYs 324a,b to isolated mode by issuing a command over the MDIO bus. At block 406, the SoC 308 takes both of the PHYs 324a,b out of super isolated mode. While in the depicted embodiment the PHYs 324a,b boot up in super isolated mode, in alternative embodiments (not depicted) the PHYs 324a,b may boot up in isolated mode. The SoC 308 then takes the primary PHY 324a out of isolated mode at block 408, which is tantamount to setting the primary PHY 324a to active mode. The SoC 308 then initializes drivers and sets the variable ActivePHY, which the SoC 308 uses to store which of the PHYs 324a,b is currently in active mode, to the primary PHY 324a at block 410. The SoC 308 also initializes a variable, timeout, to invalid. As discussed in more detail below the timeout variable is used to determine when to send messages from the physical layer to the application layer. Blocks 404 to 410 represent the initialization phase of the method 400.

[0051] At block 412 the SoC 308 sleeps for N ms, which in the depicted embodiment is 500 ms. At block 414 the SoC 308 determines whether timeout is valid. The first time the SoC 308 performs the method 400 timeout is invalid, and the SoC 308 proceeds to block 416 where it determines whether the configuration Ethernet port 204b is coupled to an active link, which the SoC 308 can monitor via the MDIO bus. If no, then the SoC 308 determines that the technician

has not connected a video terminal to the configuration Ethernet port 204b, and the SoC 308 proceeds to block 418 where it sets a variable OldPHY to represent the secondary PHY 324b and sets a variable NewPHY to represent the primary PHY 324a. The SoC 308 then proceeds to block 420 where it determines whether the PHY 324a,b represented by NewPHY is the ActivePHY. In this case, as NewPHY and ActivePHY are both the primary PHY 324a, the answer is yes and the SoC 308 returns to block 412 where it loops through blocks 412 to 420 until the technician couples the configuration Ethernet port 204b to an active link.

[0052] Once the technician couples the configuration Ethernet port 204b to an active link, such as by connecting the configuration Ethernet port 204b to a laptop with software used to interface with the camera 100 via an Ethernet cable, the secondary PHY 324b detects the active link and reports this to the SoC 308 via the MDIO bus. The next time the SoC 308 arrives at block 416 it detects the active link and proceeds to block 422 where OldPHY is set to the primary PHY 324a and NewPHY is set to the secondary PHY 324b. At block 420, the SoC 308 determines that ActivePHY is not NewPHY, and consequently proceeds to block 424 where it stops OldPHY (the primary PHY 324a) and sets it to isolated mode via the MDIO bus (block 426). The SoC 308 notifies the application layer that the Ethernet link is down at block 428. The application software running on the camera 100 accordingly believes that the Ethernet connection has been lost and can react accordingly as the physical layer transitions from the primary PHY 324a to the secondary PHY 324b. At block 430 the SoC 308 takes NewPHY (the secondary PHY 324b) out of isolated mode, then sets ActivePHY to represent the secondary PHY 324b (block 432), and then starts using the secondary PHY 324b (block 434). The SoC 308 then proceeds to block 436 where it sets timeout to a valid value of the current time + M, where in the depicted embodiment M is 2,000 ms. After setting timeout the SoC 308 returns to block 412.

[0053] In the depicted embodiment where N = 500 ms and M = 2,000 ms, the SoC 308 then loops through blocks 412, 414, and 438 three times until on the fourth time, the SoC 308 at block 438 determines that the current time equals timeout and proceeds to block 440 where it resets timeout to invalid instead of proceeding directly back to block 412. After block 440 the SoC 308 proceeds to block 442 where it notifies the application layer that the active link has returned, and then proceeds back to block 412. This effectively causes the physical layer to

simulate to the application layer that the active link returns after having been lost for 2,000 ms, thereby allowing the application layer to handle the transition from the primary PHY 324a to the secondary PHY 324b with legacy programming designed for use only with the primary PHY 324a. The application layer is able to function without knowledge of the dual ports 204a,b and without knowledge that what it perceives as a loss and return of the active link on one port is actually a transition from the primary PHY 324a to the secondary PHY 324b. In alternative embodiments (not shown), however, the application layer may be programmed with knowledge that the camera 100 has two ports 204a,b, and may be able to handle the transition between the two ports 204a,b without the physical layer simulating a lost link as described above.

[0054] After returning to block 412, the SoC 308 loops between blocks 412 and 420 until the technician removes the active link from the configuration Ethernet port 204b by, for example, unplugging the Ethernet cable from the configuration Ethernet port 324b.

[0055] After the active link is removed, the secondary PHY 324b detects the termination of the active link and reports this to the SoC 308 via the MDIO bus. The next time the SoC 308 arrives at block 416 it detects the lack of an active link and proceeds to block 418 where OldPHY is set to the secondary PHY 324b and NewPHY is set to the primary PHY 324a. At block 420, the SoC 308 determines that ActivePHY is not NewPHY, and consequently proceeds to block 424 where it stops OldPHY (the secondary PHY 324b) and sets it to isolated mode (block 426). The SoC 308 notifies the application layer that the Ethernet link is down at block 428. The application software running on the camera 100 accordingly believes that the Ethernet connection has been lost again and can react accordingly as the physical layer transitions from the secondary PHY 324b to the primary PHY 324a. At block 430 the SoC 308 takes NewPHY (the primary PHY 324a) out of isolated mode, then sets ActivePHY to represent the primary PHY 324a (block 432), and then starts using the primary PHY 324a (block 434). The SoC 308 then proceeds to block 436 where it sets timeout to a valid value of the current time + M, where in the depicted embodiment M is 2,000 ms. After setting timeout the SoC 308 returns to block 412 where the SoC 308 will wait for 2,000 ms before it notifies the application layer that the active link has returned. The SoC 308 then returns to block 412 where it loops between blocks 412 and 420 until the configuration Ethernet port 204b is used again.

[0056] While in the foregoing embodiments the primary Ethernet port 204a is coupled to an active link before, during, and after the configuration Ethernet port 204b is coupled to an active link, in alternative embodiments this need not be the case. For example, the technician may use the configuration Ethernet port 204b prior to connecting the primary Ethernet port 204a to the network, or the network may be offline while the configuration Ethernet port 204b is being used.

[0057] Additionally, in the foregoing embodiments the PHYs 324a,b share the MII and MDIO buses and are thereby coupled to the same MAC 314. However, in alternative embodiments this need not be the case. For example, in one of these alternative embodiments depicted in Figure 5(a), the control and processing circuitry 302 is as shown in Figure 3 except it also includes an additional processor 310', an additional MAC 314' communicatively coupled to the processor 310', and an additional computer readable medium 320'communicatively coupled to the processor 310'. The additional processor 310' is connected to the processor 310 shown in Figure 3. Instead of the communication circuitry 304a,b sharing the same MAC 314, the primary PHY 324a (not expressly shown in Figure 5(a), but part of the primary communication circuitry 304a) is coupled to the MII and MDIO buses of one of the MACs 314 while the secondary PHY 324b (not expressly shown in Figure 5(a), but part of the secondary communication circuitry 304b) is coupled to the MII and MDIO buses of the other MAC 314'. The PHYs 324a,b are reset in conjunction with a system-wide reset as opposed to individually by the processors 310,310'. Because the PHYs 324a,b do not share MDIO or MII buses the address pins of the PHYs 324a,b are unused. As in Figure 3, the imager 318 is connected to the ISP 316, which communicates with one of the processors 310 and the DC to DC converter 322 is connected to the primary communication circuitry 304a to power the camera 100. The two processors 310,310' communicate with each other to send the digital communication signal to one or both of the ports 204a,b at any given time.

[0058] In another of these alternative embodiments, the control and processing circuitry 302 has two MACs 314,314' but these are either incorporated into the SoC 308 or, if not part of the SoC 308 are nonetheless controlled by the same processor 310. Figure 5(b) shows an embodiment in which the two MACs 314,314' are integrated into the SoC 308; the control and processing circuitry 302 is otherwise the same as that shown in Figure 3. As in the embodiment

of Figure 5(a), each of the PHYs 324a is connected to one of the MACs 314,314' via the MDIO bus and MII bus of that MAC 314,314'. The PHYs 324a,b are reset in conjunction with a system-wide reset as opposed to individually by the GPIO lines 312. Also as in Figure 5(a), because each of the PHYs 324a,b is connected to its own MAC 314,314', the address pins of the PHYs 324a,b are left unused. As in Figures 3 and 5(a) the DC to DC converter 322 is connected to the primary communication circuitry 304a to power the camera 100.

[0059] In another of these alternative embodiments depicted in Figure 5(c), the control and processing circuitry 302 includes a hub 502 or switch 503 interposed between the MAC 314 and the PHYs 324a,b. Additionally, the PHYs 324a,b are reset in conjunction with a system-wide reset as opposed to individually by the GIPO lines 312. The control and processing circuitry 302 is otherwise identical to that shown in Figure 3, and the PHYs 324a,b are connected to the same MAC 314 via the hub 502 or switch 503. When the hub 502 is used, the hub 502 duplicates all packets sent from the MAC 314 to the PHYs 324a,b so each of the PHYs 324a,b receives the same digital communication signal from the SoC 308. The hub 502 analogously serializes all packets sent from either of the PHYs 324a,b to the MAC 314. The hub 502 may be implemented using, for example, an FPGA or as an integrated circuit. Instead of duplicating all packets sent from the MAC 314 to the PHYs 324a,b, when the switch 503 is used the packets from the MAC 314 destined for the primary Ethernet port 204a are transmitted only to the primary PHY 324a while packets destined for the secondary Ethernet port 204b are transmitted only to the secondary PHY 324b. In the alternative embodiments that incorporate the switch 503 or hub 502, the SoC 308 does not notify the application layer that the link is up or down (blocks 442 and 428) as the SoC 308 is in continuous communication with the switch or hub. As in Figures 3, 5(a), and 5(b) the DC to DC converter 322 is connected to the primary communication circuitry 304a to power the camera 100.

[0060] Also, in the foregoing embodiments the SoC 308 detects whether the configuration Ethernet port 204b is coupled to the active link, and sends the digital communication signal only to the configuration Ethernet port 204b and only when the configuration Ethernet port 204b is coupled to the active link. In alternative embodiments (not shown) this need not be the case. For example, the SoC 308 may simultaneously send the digital communication signal to both ports 204a,b at all times, as described in the embodiment above

using the hub, or only when the configuration Ethernet port 204b is coupled to the active link. Alternatively, the SoC 308 may always send the digital communication signal to the configuration Ethernet port 204b regardless of whether the configuration Ethernet port 204b is coupled to the active link. Alternatively, in the depicted embodiments and in the alternative embodiment described above incorporating the switch, the digital communication signal may be separately sent to the primary Ethernet port 204a or to the configuration Ethernet port 204b.

[0061] Furthermore, while in the foregoing embodiments the camera 100 is shown as a bullet camera, in alternative embodiments (not depicted) different types of cameras, such as dome cameras, may be used.

[0062] While an SoC is used in the foregoing embodiments, in alternative embodiments (not depicted) the SoC may instead be, for example, a microprocessor, microcontroller, programmable logic controller, field programmable gate array, or an application-specific integrated circuit. Examples of computer readable media are non-transitory and include disc-based media such as CD-ROMs and DVDs, magnetic media such as hard drives and other forms of magnetic disk storage, and semiconductor based media such as flash media, random access memory, and read only memory.

[0063] It is contemplated that any part of any aspect or embodiment discussed in this specification can be implemented or combined with any part of any other aspect or embodiment discussed in this specification.

[0064] For the sake of convenience, the exemplary embodiments above are described as various interconnected functional blocks. This is not necessary, however, and there may be cases where these functional blocks are equivalently aggregated into a single logic device, program or operation with unclear boundaries. In any event, the functional blocks can be implemented by themselves, or in combination with other pieces of hardware or software.

[0065] Figures 4(a) and (b) depict a flowchart of an exemplary embodiment of a method. Some of the blocks illustrated in the flowchart may be performed in an order other than that which is described. Also, it should be appreciated that not all of the blocks described in the

flowchart are required to be performed, that additional blocks may be added, and that some of the illustrated blocks may be substituted with other blocks.

[0066] While particular embodiments have been described in the foregoing, it is to be understood that other embodiments are possible and are intended to be included herein. It will be clear to any person skilled in the art that modifications of and adjustments to the foregoing embodiments, not shown, are possible.

CLAIMS

1. A security camera having dual communication ports, the camera comprising:

(a) a camera body mountable to a mounting surface and comprising an aperture to permit light to enter the camera body;

(b) a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture;

(c) an imager located within the camera body and positioned to receive the light refracted by the lens;

(d) primary communication circuitry comprising a primary communication port accessible from outside the camera body, wherein the primary communication port is on one side of the mounting surface when the camera body is mounted;

(e) secondary communication circuitry comprising a secondary communication port accessible from outside the camera body, wherein the secondary communication port and the aperture are on an opposing side of the mounting surface when the camera body is mounted; and

(f) control and processing circuitry communicatively coupled to the imager and to the primary and secondary communication circuitry, the control and processing circuitry comprising a processor and a computer readable medium, communicatively coupled to the processor, having encoded thereon statements and instructions to cause the processor to send a digital communication signal derived from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link.

2. The camera of claim 1 wherein the digital communication signal is simultaneously sent to both the primary and secondary communication ports.

3. The camera of claim 1 wherein the digital communication signal is separately sent to the primary communication port or to the secondary communication port.

4. The camera of claim 1 wherein the statements and instructions further cause the processor to detect whether the secondary communication port is coupled to the active link, and to send the digital communication signal to the secondary communication port only when the secondary communication port is coupled to the active link.

5. The camera of claim 4 wherein detecting whether the secondary communication port is coupled to the active link comprises polling the secondary communication port.

6. The camera of claims 4 or 5 wherein the statements and instructions further cause the processor, when the secondary communication port is not coupled to the active link, to send the digital communication signal to the primary communication port.

7. The camera of any one of claims 4 to 6 wherein the secondary communication port is located on an underside of the camera body.

8. The camera of any one of claims 4 to 7 wherein the digital communication signal is communicated using Ethernet.

9. The camera of any one of claims 4 to 8 wherein the control and processing circuitry further comprises a media access controller (MAC) and input/output control circuitry, each of which is communicatively coupled to the processor and to the primary and secondary communication circuitry.

10. The camera of claim 9 wherein the primary communication circuitry comprises a primary PHY communicatively coupled to the primary communication port and to the MAC and the secondary communication circuitry comprises a secondary PHY communicatively coupled to the secondary communication port and to the MAC.

11. The camera of claim 9 wherein the primary and secondary PHYs are communicatively coupled to the MAC through a shared media-independent interface (MII bus) and a shared management data input/out interface (MDIO bus) of the MAC.

12. The camera of claim 11 wherein the primary and secondary PHYs are pin strapped to commence operation by setting their outputs that are connected to the MII bus to a high impedance state.

13. The camera of claims 11 or 12 wherein the input/output circuitry comprises a primary reset line communicatively coupled to a reset input of the first PHY, a secondary reset line communicatively coupled to a reset input of the second PHY, and an address line communicatively coupled to an MDIO address select input on the first and second PHYs.

14. The camera of any one of claims 11 to 13 wherein the statements and instructions further cause the processor, prior to detecting that the secondary communication port is coupled to the active link, to send the digital communication signal to the primary communication port via the primary PHY and to set outputs of the secondary PHY connected to the MII bus to a high impedance state, and following detecting that the secondary communication port is coupled to the active link:

(a) to stop the primary PHY;

(b) to notify the application layer that there is no active link prior to activating the secondary PHY;

(c) to set outputs of the primary PHY connected to the MII bus to a high impedance state;

(d) to take the outputs of the secondary PHY connected to the MII bus out of a high impedance state;

(e) to activate the secondary PHY; and

(f) to notify the application layer that the active link is present.

15. The camera of any one of claims 1 to 14 wherein the camera is a bullet camera.

16. A method for switching between primary and secondary communication ports of a security camera comprising a camera body mountable to a mounting surface, an aperture in the camera body to permit light to enter the camera body, a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture, and an imager located within the camera body and positioned to receive the light refracted by the lens, wherein the primary communication port is on one side of the

mounting surface when the camera body is mounted and the secondary communication port and the aperture are on an opposing side of the mounting surface when the camera body is mounted, the method comprising sending a digital communication signal comprising a video signal derived from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link.

17. The method of claim 16 wherein the digital communication signal is simultaneously sent to both the primary and secondary communication ports.

18. The method of claim 16 wherein the digital communication signal is separately sent to the primary communication port or to the secondary communication port.

19. The method of claim 16 wherein the method further comprises detecting whether the secondary communication port is coupled to the active link, and sending the digital communication signal to the secondary communication port only when the secondary communication port is coupled to the active link.

20. The method of claim 19 wherein detecting whether the secondary communication port is coupled to the active link comprises polling the secondary communication port.

21. The method of claims 19 or 20 wherein the method further comprises when the secondary communication port is not coupled to the active link, sending the digital communication signal to the primary communication port.

22. The method of any one of claims 19 to 21 wherein the secondary communication port is located on an underside of the camera body.

23. The method of any one of claims 19 to 22 wherein the digital communication signal is communicated using Ethernet.

24. The method of any one of claims 19 to 23 wherein the camera further comprises a media-independent interface (MII) bus and a primary PHY and a secondary PHY, each of which has outputs connected to the MII bus and via which the digital communication signal is sent to the primary and secondary communication ports, and further comprising:

(a) prior to detecting that the secondary communication port is coupled to the active link, sending the digital communication signal to the primary communication port via the primary PHY and setting the outputs of the secondary PHY connected to the MII bus to a high impedance state; and

(b) following detecting that the secondary communication port is coupled to the active link:

(i) stopping the primary PHY;

(ii) notifying the application layer that there is no active link prior to activating the secondary PHY;

(iii) setting outputs of the primary PHY connected to the MII bus to a high impedance state;

(iv) taking the outputs of the secondary PHY connected to the MII bus out of a high impedance state;

(v) activating the secondary PHY; and

(vi) notifying the application layer that the active link is present.

25. The method of any one of claims 1 to 14 wherein the camera is a bullet camera.

26. A non-transitory computer readable medium having encoded thereon statements and instructions to cause a processor to perform a method as claimed in any one of claims 16 to 25.

27. A security camera having dual communication ports, the camera comprising:

(a) a camera body comprising an aperture to permit light to enter the camera body;

(b) a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture;

(c) an imager located within the camera body and positioned to receive the light refracted by the lens;

(d) an attachment assembly attached to the camera body and mountable to a mounting surface;

(e) primary communication circuitry comprising a primary communication port accessible through the attachment assembly;

(f) secondary communication circuitry comprising a secondary communication port accessible through the camera body; and

(g) control and processing circuitry communicatively coupled to the imager and to the primary and secondary communication circuitry, the control and processing circuitry comprising a processor and a computer readable medium, communicatively coupled to the processor, having encoded thereon statements and instructions to cause the processor to send a digital communication signal derived from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link.

28. The camera of claim 27 wherein the attachment assembly comprises a mounting arm affixed to an attachment plate, and wherein the attachment plate comprises an access port through which the primary communication port is accessible.

29. The camera of claim 28 wherein the access port is positioned on a surface of the attachment plate adjacent to the mounting surface when the camera is mounted.

30. A security camera having dual communication ports, the camera comprising:

(a) a camera body mountable to a mounting surface and comprising an aperture to permit light to enter the camera body;

(b) a lens mounted to the camera body and positioned to refract the light entering the camera body through the aperture;

(c) an imager located within the camera body and positioned to receive the light refracted by the lens;

(d) primary communication circuitry comprising a primary communication port accessible from outside the camera body, wherein the primary communication port is behind the mounting surface when the camera body is mounted;

(e) secondary communication circuitry comprising a secondary communication port accessible from outside the camera body, wherein the secondary communication is in front of the mounting surface when the camera body is mounted; and

(f) control and processing circuitry communicatively coupled to the imager and to the primary and secondary communication circuitry, the control and processing circuitry comprising a processor and a computer readable medium, communicatively coupled to the processor, having encoded thereon statements and instructions to cause the processor to send a digital communication signal derived from the light incident on the imager to the secondary communication port when the secondary communication port is coupled to an active link.

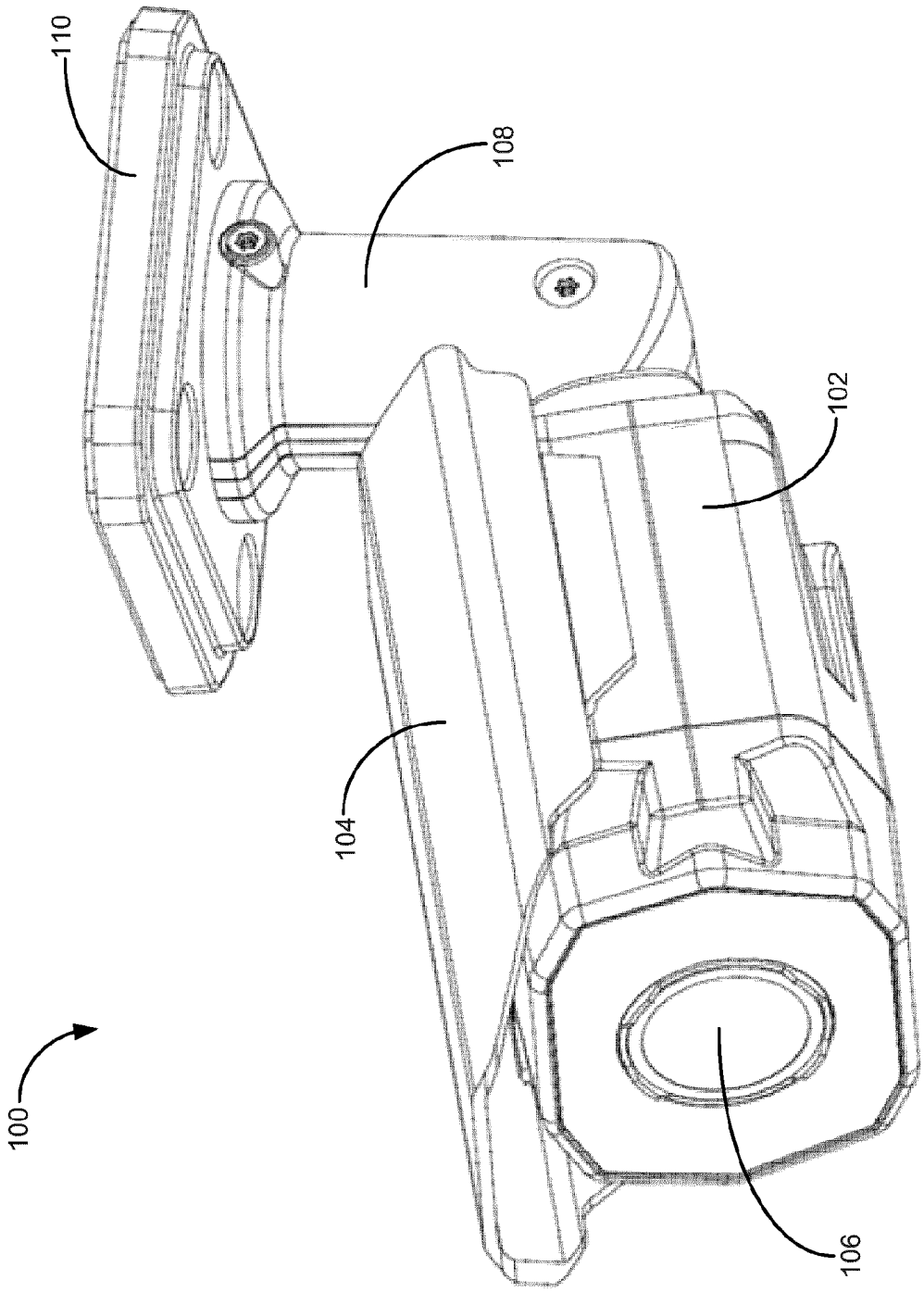

FIG. 1

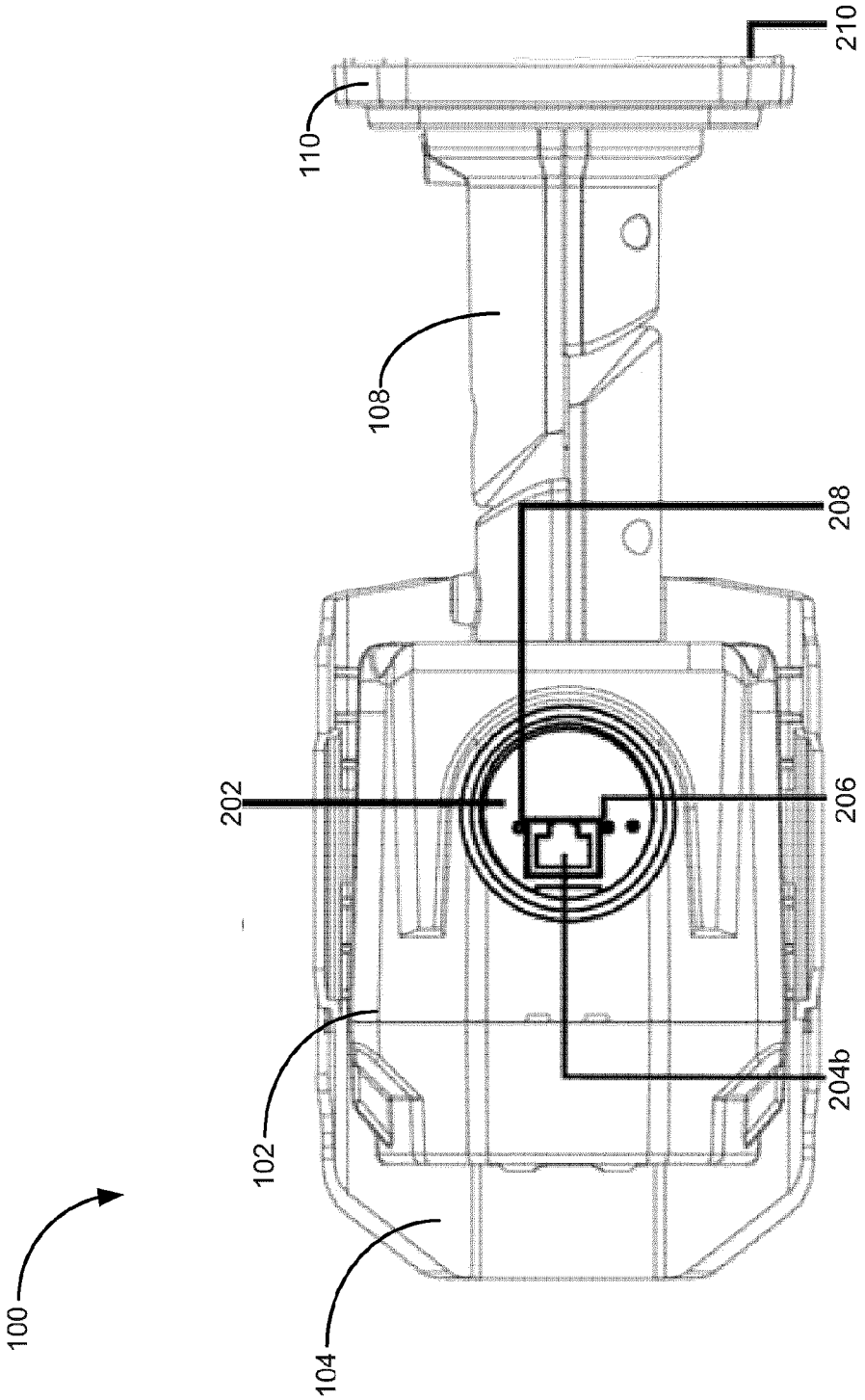

FIG. 2

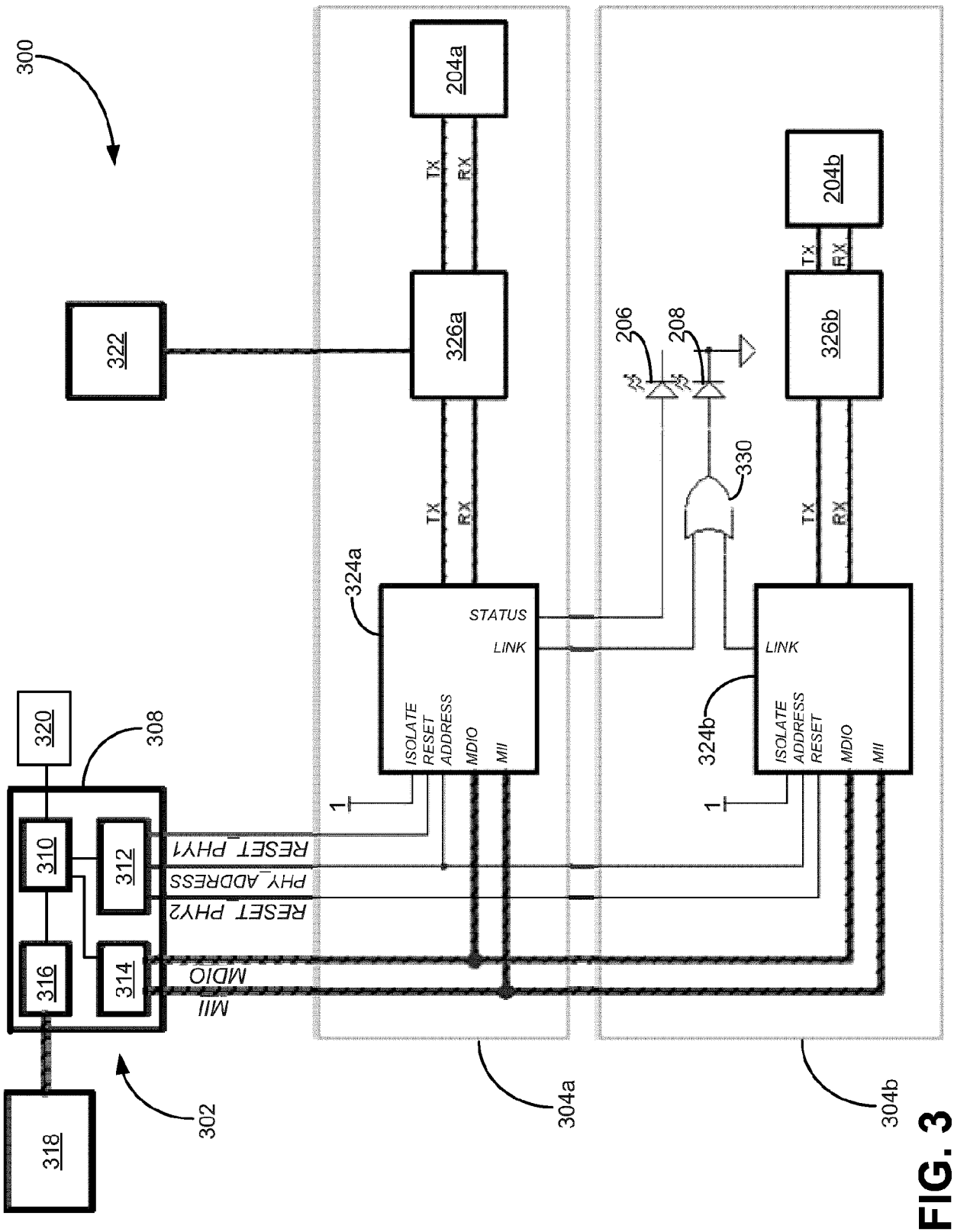
300
204a
TX
RX
322
326a
206
208
204b
326b
330
324a
STATUS
LINK
ISOLATE
RESET
ADDRESS
MDIO
MII
324b
320
308
310
312
316
314
318
302
304a
304b
RESET_PHY1
PHY_ADDRESS
RESET_PHY2
MDIO
MII

FIG. 3

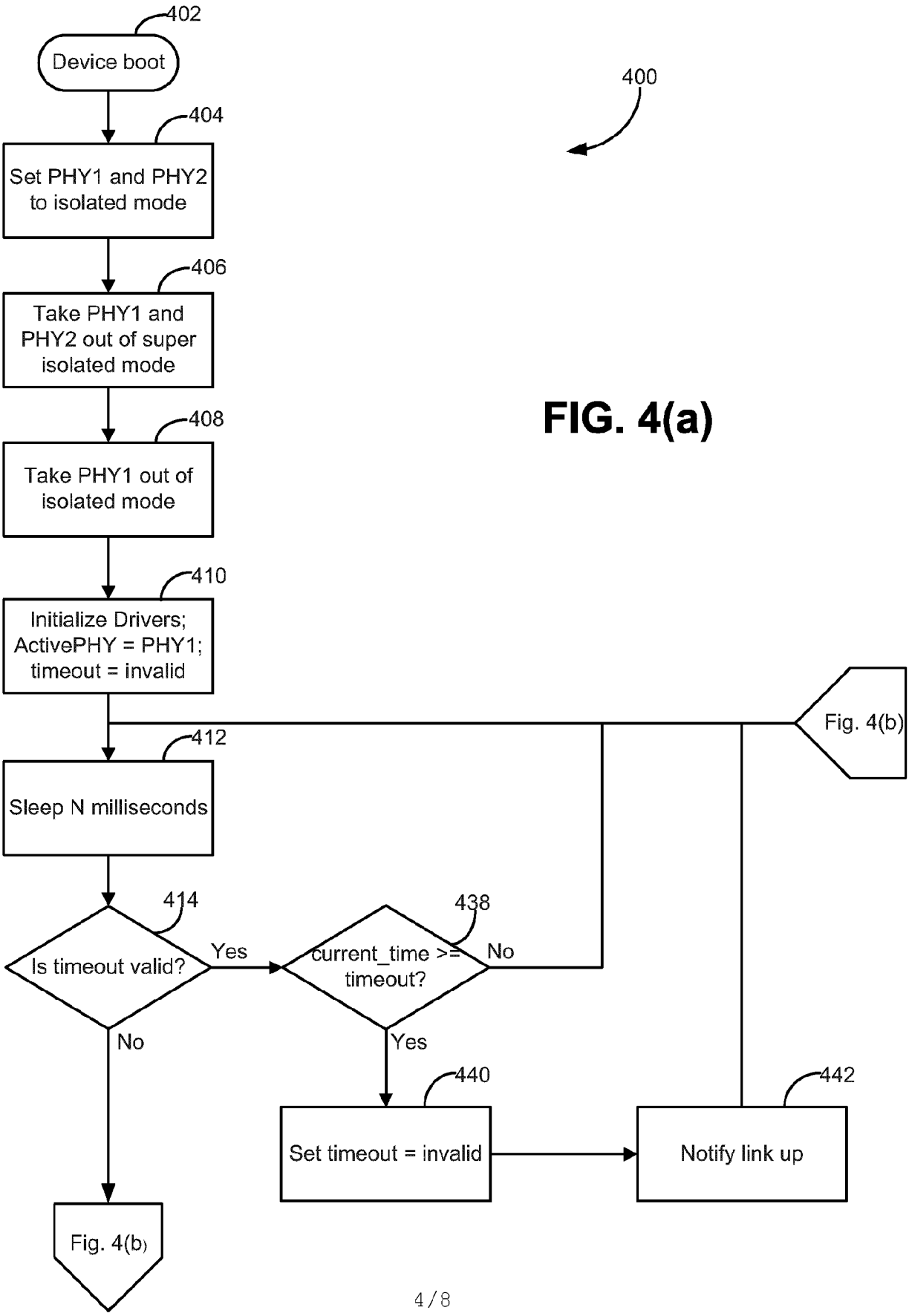
402
Device boot
400
404
Set PHY1 and PHY2 to isolated mode
406
Take PHY1 and PHY2 out of super isolated mode
408
Take PHY1 out of isolated mode
410
Initialize Drivers; ActivePHY = PHY1; timeout = invalid
Fig. 4(b)
412
Sleep N milliseconds
414
Is timeout valid?
Yes
438
current_time >= timeout?
No
No
Yes
440
Set timeout = invalid
442
Notify link up
Fig. 4(b)

FIG. 4(a)

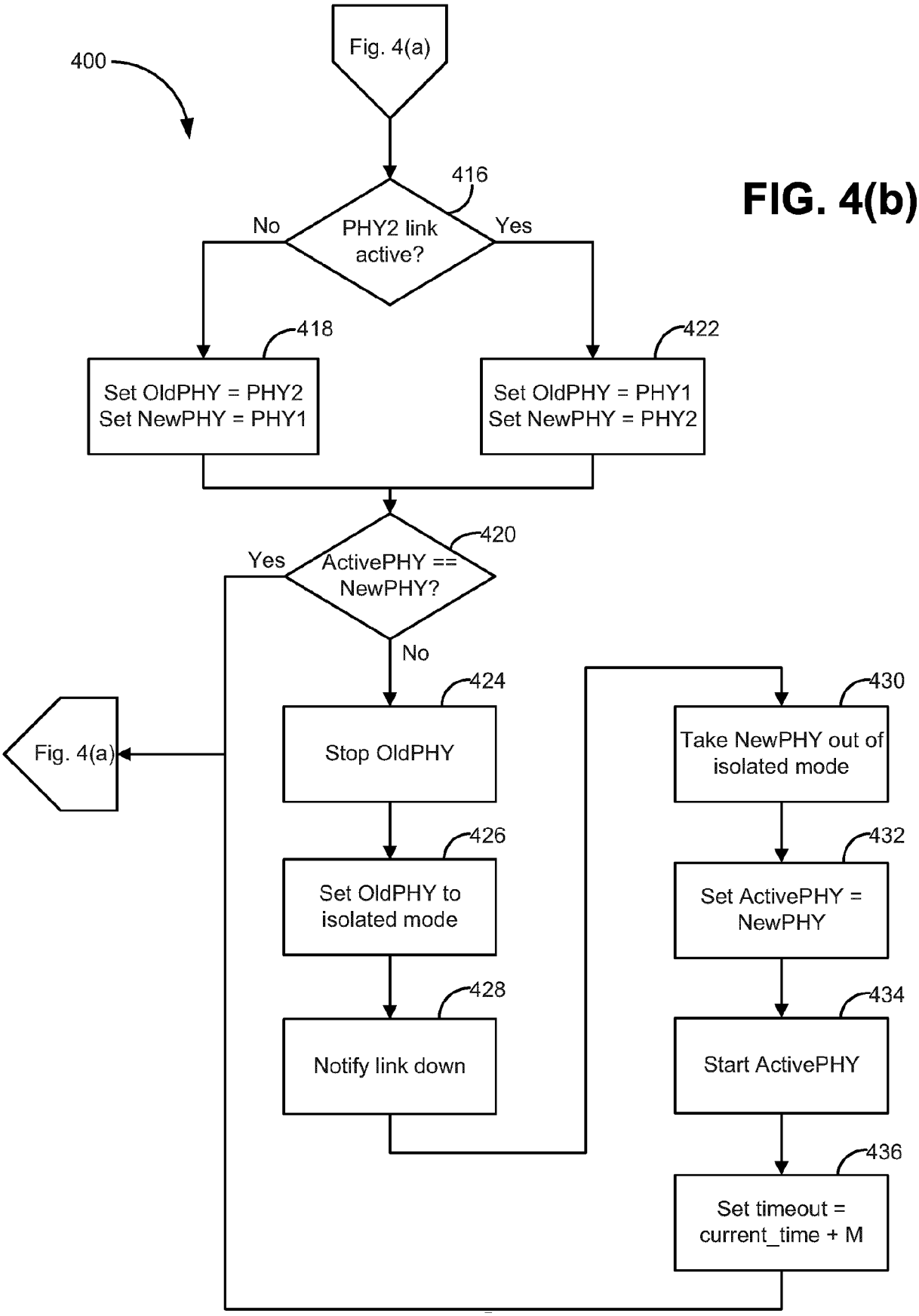
400
Fig. 4(a)
416
PHY2 link active?
No
Yes
418
Set OldPHY = PHY2
Set NewPHY = PHY1
422
Set OldPHY = PHY1
Set NewPHY = PHY2
420
ActivePHY == NewPHY?
Yes
No
Fig. 4(a)
424
Stop OldPHY
426
Set OldPHY to isolated mode
428
Notify link down
430
Take NewPHY out of isolated mode
432
Set ActivePHY = NewPHY
434
Start ActivePHY
436
Set timeout = current_time + M

FIG. 4(b)

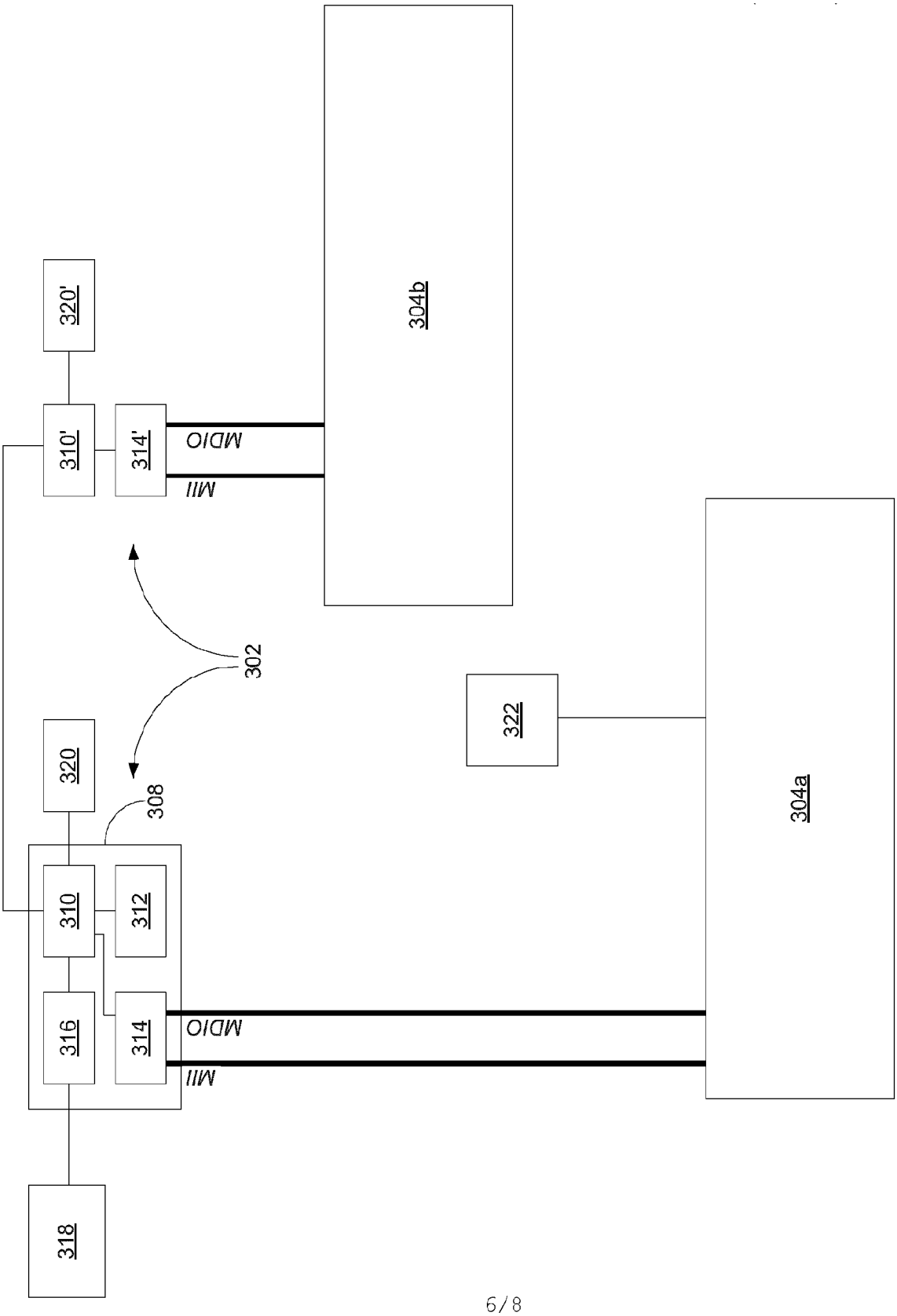
320'
310'
314'
MDIO
MII
304b
302
322
304a
320
308
310
312
316
314
MDIO
MII
318

FIG. 5(a)

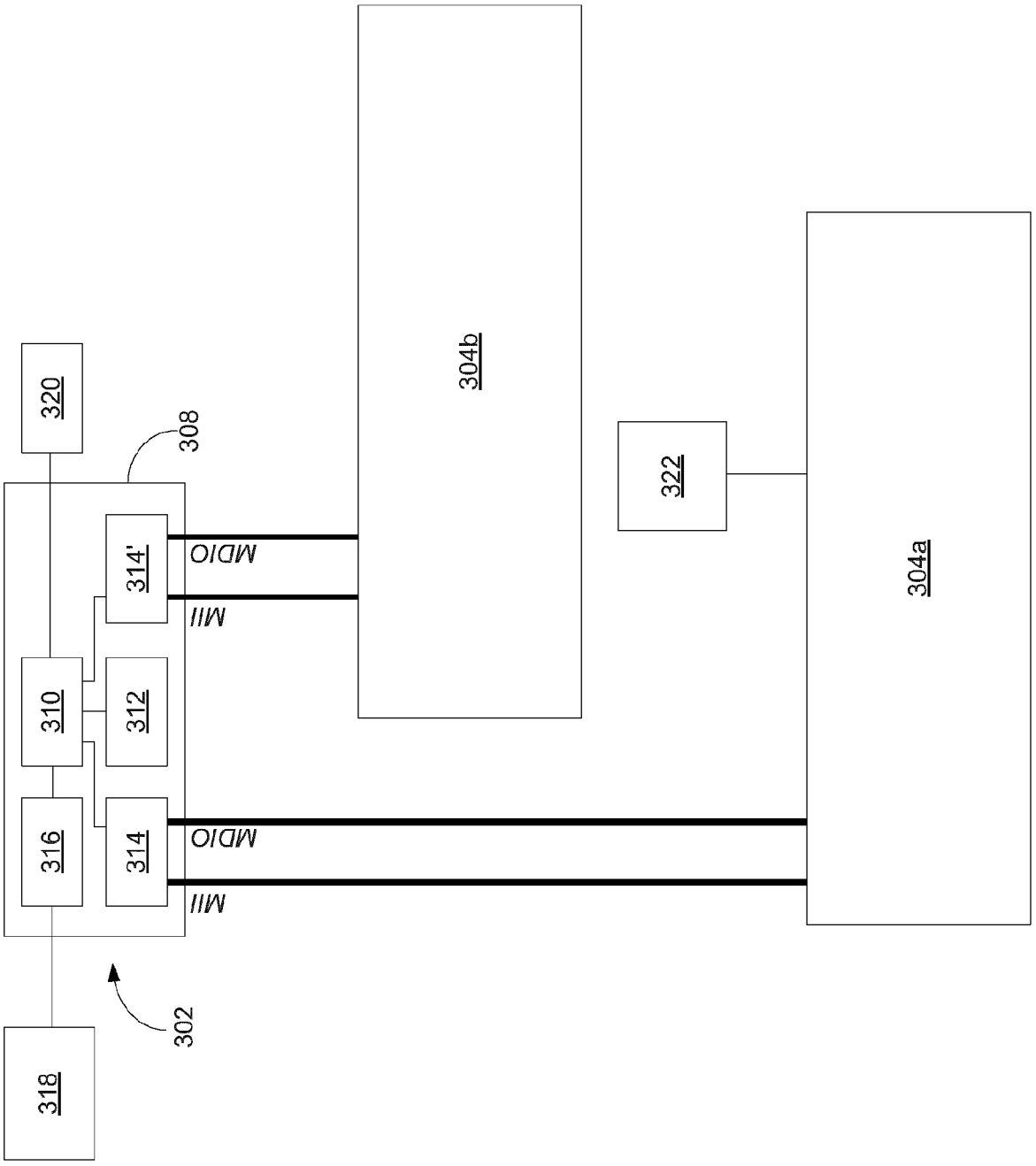
320
308
304b
322
304a
314'
MDIO
MII
310
312
316
314
MDIO
MII
302
318

FIG. 5(b)

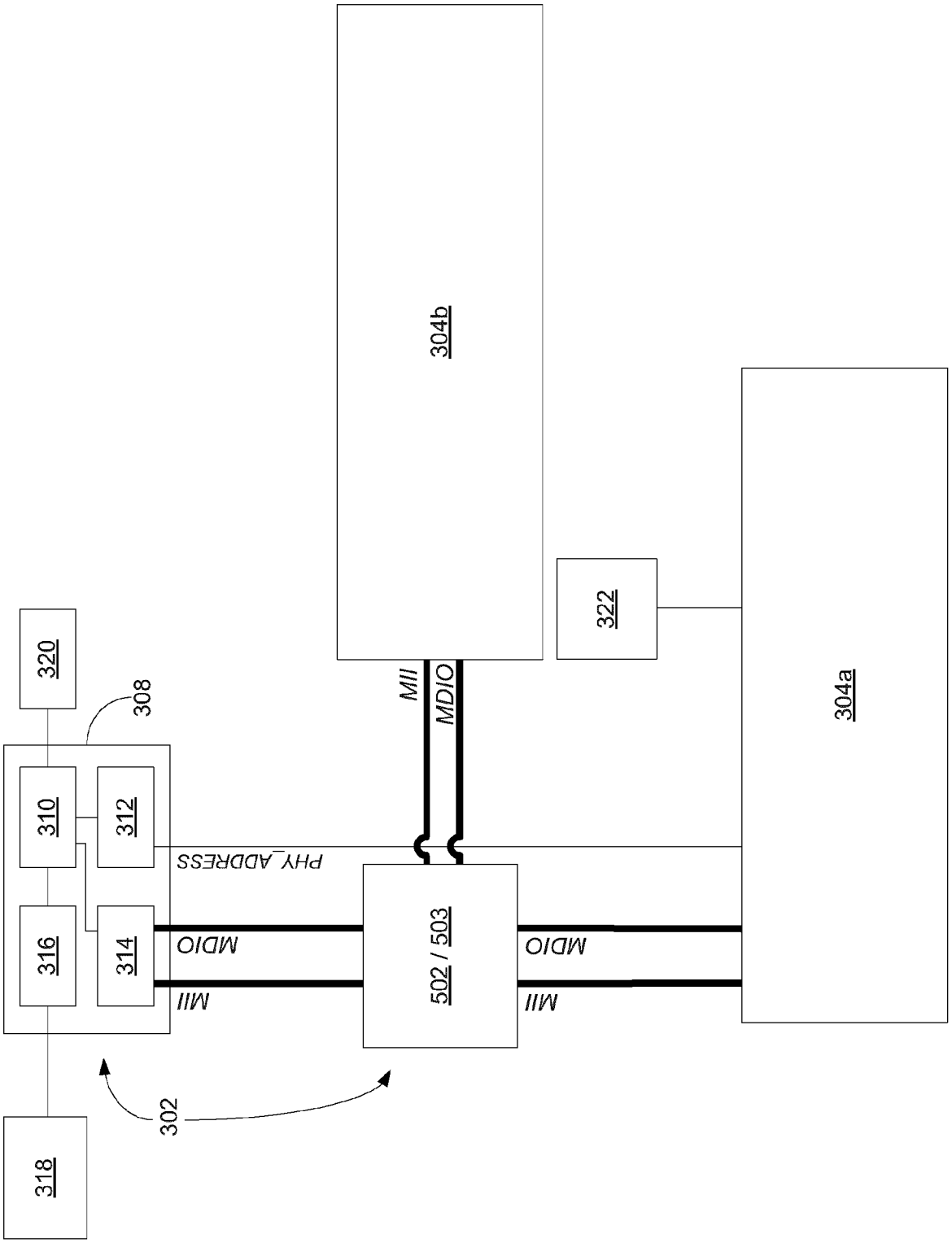
304b
322
304a
320
308
MII
MDIO
310
312
PHY_ADDRESS
316
314
MDIO
MII
502 / 503
MDIO
MII
302
318

FIG. 5(c)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2013/050059

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***H04N 5/228*** (2006.01) , ***H04N 7/18*** (2006.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: **ALL** (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
TotalPatent and keywords: security; "IP"; surveillance; bullet; camera/cameras; "port"; connector/connectors; digital; active; live; feed; connection; link; imager; sensor; lens; aperture; ethernet; mount/mounting/mounted; multiple; many; cables; dual; two; signal; bullet; maintenance; support plate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/0111489 A1 (*Presler*) - 6 May 2010 (06-05-2010) * [0039]; [0053]; [0088]-[0093]; [0098]; Figs. 1-4, 6, 8 *	1-4, 8, 9, 16-19, 23, 26
A	US 2013/0002883 A1 (*Creamer et al.*) - 3 January 2013 (03-01-2013) * the whole document *	ALL
A	US 2011/0195789 A1 (*Wells*) - 11 August 2011 (11-08-2011) * the whole document *	ALL
A	US 2010/0289904 A1 (*Zhang et al.*) - 18 November 2010 (18-11-2010) * the whole document *	ALL

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 September 2013 (10-09-2013)	17 September 2013 (17-09-2013)

Name and mailing address of the ISA/CA
Canadian Intellectual Property Office
Place du Portage I, C114 - 1st Floor, Box PCT
50 Victoria Street
Gatineau, Quebec K1A 0C9
Facsimile No.: 001-819-953-2476

Authorized officer

Reginald Linco (819) 994-1683

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2013/050059

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
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		US2006031902A1	09 February 2006 (09-02-2006)
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		US7640568B2	29 December 2009 (29-12-2009)
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		US8282480B2	09 October 2012 (09-10-2012)
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		US8479908B2	09 July 2013 (09-07-2013)
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		US2013130790A1	23 May 2013 (23-05-2013)
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