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VOLTAGE REGULATOR

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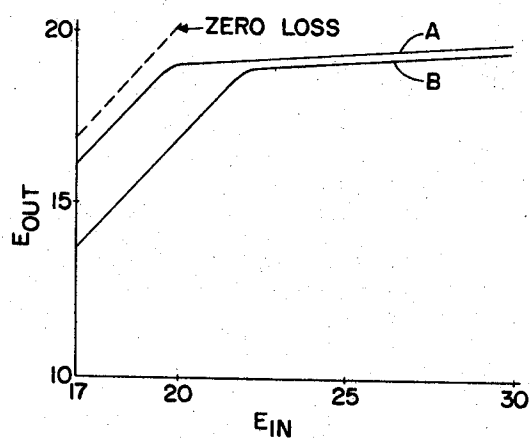
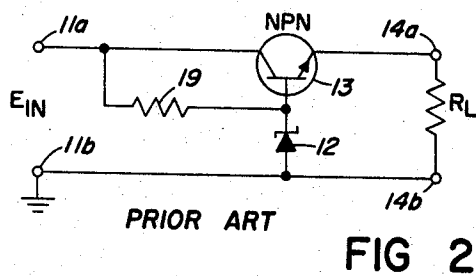
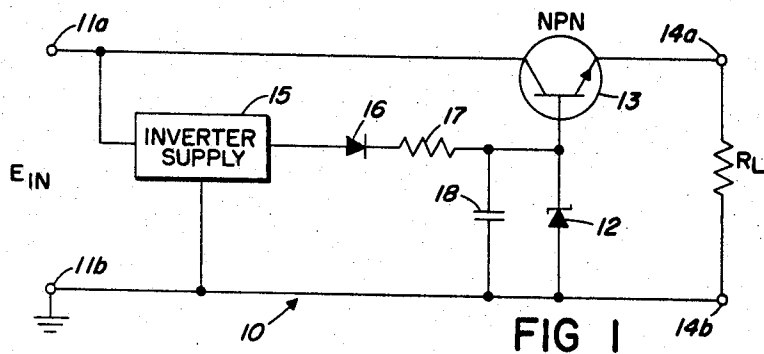


FIG 3

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VOLTAGE REGULATOR

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ABSTRACT OF THE DISCLOSURE

A voltage regulator circuit with a Zener diode voltage level control for an NPN transistor having a collector connection to a main DC voltage supply, a base connection through the Zener diode to the other side of the main DC voltage supply, an emitter load connection, and an additional base current supply capable of maintaining the transistor in a fully saturated state when the main DC voltage supply falls to relatively low levels such that the Zener diode is no longer voltage biased to conduction. Sufficient impedance is included in the additional base current supply, that impresses a higher potential at the base of the transistor than is impressed with the main voltage source alone, to insure that transistor base current never exceeds safe values.

This invention relates in general to transistor equipped voltage regulators, and in particular to a voltage regulator circuit having Zener diode voltage level control and a transistor base current supply source for insuring full current saturation of the transistor even though a main voltage supply may undergo a voltage level fall below the normal operational range of voltage output of the voltage regulator.

Various Zener diode and transistor equipped voltage regulators of the art are generally susceptible to considerable voltage drop across the transistor whenever voltage input levels are so reduced that voltage impressed on the Zener diode falls below its conduction level. Under such conditions of operation with these existing circuits, the transistor generally becomes a relatively inefficient collector-to-emitter conductor since it is not maintained in the fully saturated state. Obviously, with operation under such conditions of lowered supply voltage levels, voltage output of a voltage regulator would be optimized were impedance through the transistor minimized. While the solutions in some cases might be to bypass the transistor with a relay switching system, such a solution is operationally impractical with many installations. Under such conditions of operation where it is important that impedance be minimized through the collector-to-emitter path this may be accomplished by maintaining the transistor in a fully saturated state throughout operation of the voltage regulator when the Zener diode is voltage biased below conduction levels.

It is, therefore, a principal object of this invention to provide voltage source means in a voltage regulator, in addition to a main voltage source, capable of maintaining the transistor in a saturated state whenever the Zener diode of the voltage regulator is not biased to conduction.

Another object is to provide voltage circuit means for impressing a higher potential at the base of the transistor than impressed by the main voltage source on the collector and with sufficient impedance to insure adequate limitation of transistor base current to within safe values.

Features of this invention useful in accomplishing the above objects include, in a voltage regulator, a transistor and a Zener diode with the transistor having a collector connected to one terminal of the main input voltage supply, the emitter connected to the output load, and the base connected through the Zener diode to the other terminal of the main voltage supply. A particularly im-

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portant feature is an additional voltage supply system connected for impressing a positive voltage bias on the base relative to the collector whenever the Zener diode is not voltage biased to conduction.

A specific embodiment representing what is presently regarded as the best mode of carrying out the invention is illustrated in the accompanying drawing.

In the drawing:

FIGURE 1 represents a schematic of a voltage regulator having a transistor and a Zener diode and including an auxiliary voltage source circuit;

FIGURE 2, a schematic of a prior art transistor and Zener diode equipped voltage regulator circuit; and

FIGURE 3, a graph having curves illustrating the performance of the prior art voltage regulator illustrated in FIGURE 2 and a curve illustrating the improved performance of applicant's voltage regulator as illustrated in FIGURE 1, both as related to a zero loss line, particularly in the range of operation where, in the respective voltage regulators, the Zener diode is not biased to conduction.

Referring to the drawing:

In the voltage regulator 10 of FIGURE 1, the input terminals 11a and 11b are interconnected by a Zener diode 12 and an NPN transistor 13 with the collector of transistor 13 connected to terminal 11a, the anode of the Zener diode 12 connected to terminal 11b, and with the cathode and the base of transistor 13 interconnected by a common junction. The emitter of transistor 13 is connected to an output terminal 14a, and a load may be connected, as indicated by resistance R_L , between output terminals 14a and 14b. The connection of the anode of the Zener diode 12 with input terminal 11b and with output terminal 14b could be through a common ground or a common ground line connected to output terminal 14b.

An inverter voltage supply 15 is provided with opposite voltage input connections to input terminals 11a and 11b, respectively, and with an output connection through, serially, diode 16, with its anode connected to supply 15, and resistor 17 to the common junction between Zener diode 12 and transistor 13. The common junction between Zener diode 12, transistor 13, and resistor 17 is also connected through capacitor 18 to the common ground or line interconnecting input terminal 11b and output terminal 14b.

Please refer also to FIGURE 2 for a prior art circuit quite similar to a voltage regulator circuit disclosed in T. G. Marshall, Jr.'s U.S. Patent No. 3,099,790, with, as a matter of convenience, like components numbered the same as in applicant's voltage regulator of FIGURE 1. Input terminals 11a and 11b are connected to Zener diode 12 and NPN transistor 13 and to output terminals 14a and 14b in substantially the same manner as with the embodiment of FIGURE 1. The prior art circuit also includes a resistor 19 between input terminal 11a and the common junction of Zener diode 12 and NPN transistor 13. Both applicant's voltage regulator circuit of FIGURE 1 and the prior art voltage regulator as shown in FIGURE 2 provide substantially the same operational results under conditions of operation where voltage input levels insure biasing of the Zener diode to conduction in the respective circuits. This similarity of operation becomes readily apparent when observing the more horizontal over the knee portions of the respective voltage output to voltage input graph curves, curve A of FIGURE 1 embodiment and curve B, obtained with the prior art voltage regulator shown in FIGURE 2.

However, where applicant's voltage regulator circuit is particularly useful is when operational conditions are encountered where the voltage input (E_{in}) for the respective circuits falls to such a point that the respective Zener

diodes 12 are no longer biased to conduction. When this occurs, it is desirable that the impedance through the respective NPN transistors 13 be as low as possible for optimized voltage output (E_{out}) results. This is accomplished in applicant's voltage regulator by developing via applicant's inverter supply voltage source diode 16, resistor 17, and capacitor 18 circuit, a base voltage bias higher than the collector potential applied to the transistor 13 by the input voltage E_{in} . This effectively insures full saturation of the transistor under such conditions of operation, bringing the collector-to-emitter resistance through transistor 13 down to a very low minimum level, advantageously close to a zero loss line indicated in FIGURE 3. The advantageous improvement in E_{out} with operational conditions below the Zener diode firing points is particularly apparent in comparing the relative locations of both curves A and B to the zero loss line in portions of the curves before the sharp turns occurring with firing of the Zener diodes in the voltage regulators.

With the prior art circuit of FIGURE 2, the base of the transistor is always held at a slightly lower potential than the collector and, therefore, it is not possible to draw sufficient current in the base circuit to fully saturate the transistor 13 of that circuit. Thus, the collector-to-emitter resistance through the transistor in the prior art circuit is found to be approximately three times greater than with applicant's circuit throughout the range of operational conditions of low voltage input from the primary voltage supply insufficient to result in firing of the respective Zener diode 12.

The inverter supply 15 used in a working embodiment of the invention was an approximately 55 volt output square wave inverter supply, of a conventional nature, providing a square wave output half wave rectified by the diode 16 and with the time constant of the resistor 17 and capacitor 18, along with additional impedance in the circuit providing adequate filtering for the pulsation of the rectified direct current out of diode 16. An adequate square wave output is provided by inverter supply 15 throughout a variation of the voltage input E_{in} in the approximate range of 17 to 30 volts DC. It should be noted that other alternating signal inverter supplies may be provided in place of the inverter supply 15 used in the working embodiment so long as the voltage output excursion is of sufficient amplitude to provide the required output giving the desired performance in the circuit. Furthermore, a direct current supply could be substituted for the inverter supply 15 and the diode 16 shown, and connected between the resistor 17 and the ground line interconnecting the terminals 11b and 14b, and through the resistor 17 to the common junction of transistor 13, Zener diode 12, and capacitor 18.

The collector-to-emitter resistance through the transistor 13 is minimized by saturation of the transistor with it turned on as hard as possible in the voltage regulator of FIGURE 1, particularly and primarily when input voltages are so low as to not result in firing of the Zener diode 12. In both applicant's circuit and the prior art circuit when voltage input levels are adequate to insure the firing of the Zener diode, operation is, practically speaking, substantially the same. Performance in the region above Zener diode conduction is with the base of the transistor in both circuits being held at a more or less constant voltage with the voltage across the load being, relatively speaking, substantially constant except for a relatively small rise as the input voltage E_{in} is increased. The base current in the transistor 13 of applicant's circuit is prevented from increasing above a safe level by the internal impedance of the voltage supply 15 in series with the resistances of diode 16 and resistor 17. This same combination of resistance when the Zener diode 12 is fired prevents, by increased current flow through the Zener diode with higher voltage input levels, the voltage at the common junction of the Zener diode and transistor 13 from significant increase other than a slight increase consistent with the rela-

tively horizontal portions of the curve A. Capacitor 18 may be of such size, and is of adequate value in the working embodiment, to minimize difficulty with excessive collector current through the transistor when filaments of supply circuits are first turned on.

Component values used in a working embodiment of applicant's circuit as shown in FIGURE 1 using an approximately 55 volt square wave output inverter supply, of a conventional nature, and a main voltage supply input with an approximate range of from 17 to 30 volts DC and providing the results as indicated by curve A in FIGURE 3, are as follow:

Zener diode 12	-----	1N1358.
NPN transistor 13	-----	2N1486.
Diode 16	-----	1N1095.
Resistor 17	-----	150 ohms at 6.5 watts.
Capacitor 18	-----	47 microfarads.

Whereas this invention is here illustrated and described with respect to a specific embodiment thereof, it should be realized that various changes may be made without departing from the essential contribution to the art made by the teachings hereof.

I claim:

1. A voltage regulator having input connective means for connection to a main DC voltage supply; output connective means; a multielement solid state device and a Zener diode connected across said input connective means; said solid state device and said Zener diode also being connected across said output connective means; a first element of said solid state device connected to one side of said input connective means; a second element of said solid state device connected to said Zener diode and through said Zener diode to the other side of said input connective means and to an interconnection between said input connective means and a side of said output connective means and also in common with this connection to said side of said output connective means; a third element of said solid state device connected to the other side of said output connective means; an additional voltage supply having a connection to the side of said input connective means having a common connection with a side of said output means; said additional voltage supply also having a connection with the junction between said Zener diode and the second element of said solid state device; and resistive means in said additional voltage supply circuit.

2. The voltage regulator of claim 1, wherein said multielement solid state device is a transistor with said first element being a collector, said second element a base, and said third element an emitter.

3. The voltage regulator of claim 1, wherein said additional voltage supply is an inverter voltage supply and a diode is included in the connection between the additional voltage supply and the common junction between the Zener diode and the second element of said solid state device.

4. The voltage regulator of claim 3, wherein said multielement solid state device is a transistor.

5. The voltage regulator of claim 3, wherein said additional voltage supply also has a connection to the side of said input connective means connected to said first element of said solid state device; and wherein said resistive means in said additional voltage supply circuit includes a resistor in the connection between said inverter supply and the junction between said Zener diode and the second element of said solid state device.

6. The voltage regulator of claim 5, wherein a capacitor is connected in parallel across said Zener diode from the common junction between the second element of said solid state device and the Zener diode to the common connection between a side of said input connective means and a side of said output means.

7. The voltage regulator of claim 5, wherein the Zener diode is connected in the circuit with cathode to the second element of said solid state device and anode to the

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common connection between a side of said input connective means and a side of said output means; and the diode in the connection between the inverter supply and the connection between the Zener diode and the second element of said solid state device is connected anode toward the inverter supply and cathode toward the junction between the Zener diode and the second element of said solid state device.

8. The voltage regulator of claim 7, wherein said multielement solid state device is an NPN transistor with said first element being a collector, said second element a base, and said third element an emitter.

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