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New Method for Detecting Fast Time Constant Targets Using a Time Domain Metal Detector

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ABSTRACT

A metal detector comprising: a transmit waveform generation circuit; a transmit winding and its damping circuit; a receive winding and its damping circuit; and a circuit capable of reducing the minimum delay between the end of a high-to-low voltage transition of a transmit signal and the beginning of demodulation of a receive signal, comprising: means for beginning demodulation while an underdamped response in the receive winding occurs; means for connecting a DC current source to at least one input of the op amp of the analogue demodulation circuit to offset the demodulation output; means for adjusting the DC current source, damping circuit, demodulation timing waveform, or a combination of these factors when switching to a different coil to offset the demodulation output such that the demodulation output is closer to zero when no metal is detected than it would be without the adjustment.

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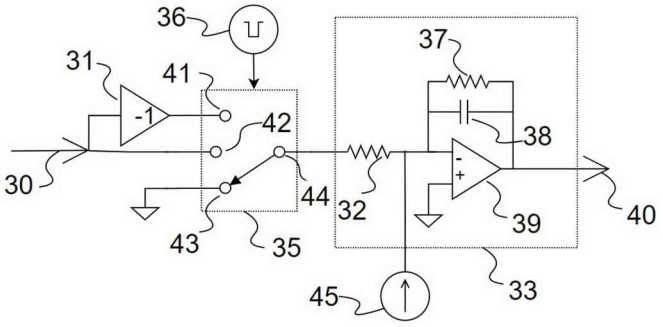

Figure 4

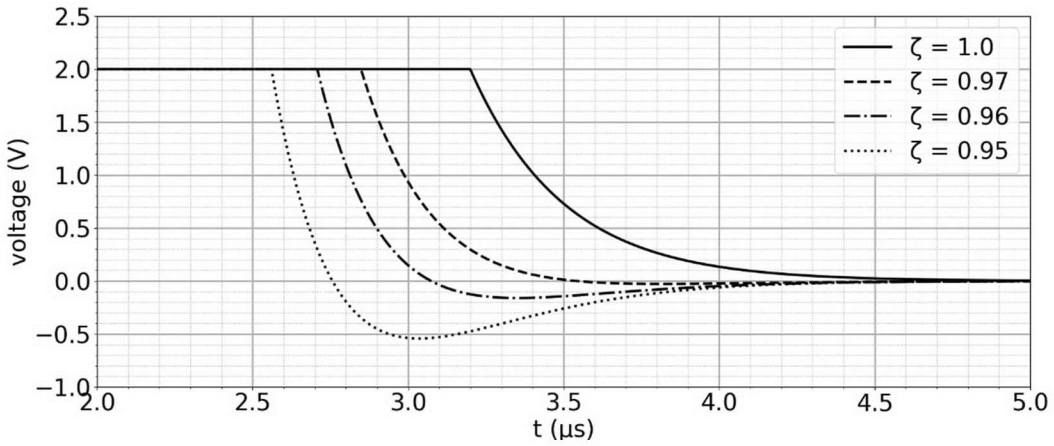

Figure 5

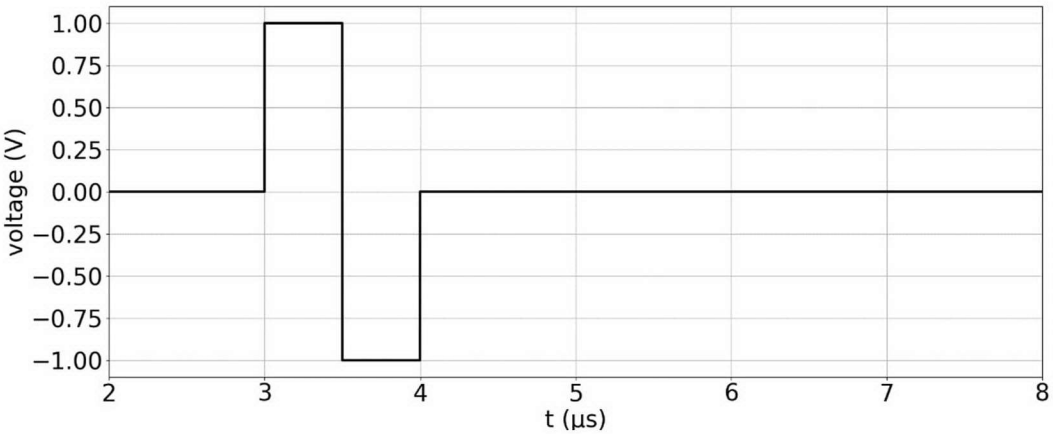

Figure 6

NEW METHOD FOR DETECTING FAST TIME CONSTANT TARGETS USING A TIME DOMAIN METAL DETECTOR

TECHNICAL FIELD

This invention relates to a method for detecting fast time constant targets using a time domain metal detector.

BACKGROUND OF THE INVENTION

The invention described relates to the field of metal detection and particularly to the detection of fast time constant targets using a time domain metal detector. Fast time constant targets include objects such as landmines that have minimal metal components, and small gold nuggets.

Metal detection is a widely used technique for locating buried objects, such as coins, relics, or even unexploded ordnance. However, the ability to detect targets with fast time constants has been a challenge for metal detectors.

The new method described involves using a specialised detection circuit to detect fast time constant targets with greater accuracy and sensitivity than conventional metal detectors. This approach could significantly improve the detection of a wide range of targets that were previously difficult to detect, thereby expanding the capabilities of time domain metal detectors.

Overall, this new method presents a promising solution for improving the performance of time domain metal detectors, particularly in detecting challenging targets. The technology has potential applications in various industries, including security, archaeology, and geology, where the ability to detect fast time constant targets could prove invaluable.

Time domain metal detectors usually synchronously demodulate (or sample) a receive signal from a receive winding commencing after a short delay following a voltage transition of a transmit signal. In most detectors, the minimum of the practical delay is usually limited by

the time constant of the critically damped receive winding. The delay required before demodulation or sampling is not ideal for detecting fast time constant metal targets because a significant portion of the decaying signal from fast time constant targets occurs during the delay, resulting in reduced sensitivity. To improve the sensitivity to fast time constant targets, the delay before demodulation must be reduced.

US patent publication US 9,547,065 B2 describes a technique to reduce the delay before demodulation by implementing a negative capacitance generator, which increases the natural resonance of the receive winding while taking into account the distributed capacitance and inductance. This approach provides several advantages for the demodulation process.

US patent publication US 10,969,511 B2 describes another technique to reduce the delay before demodulation. A damping resistor and a circuit with a variable parameter are connected in series, and the series connection is connected to one end of the receive winding. A signal is induced in the receive winding during a period of rapid change of the transmit magnetic field, and the variable parameter is controlled to change when the signal induced in the receive winding is decaying, resulting in a more rapid decay rate. The control circuit for the variable parameter circuit needs to operate not only precisely but at very high speed because the decay duration of the signal induced in the receive winding is typically only a few microseconds.

In addition to US patent publication US 10,969,511 B2, US patent application publications US 2012/0146647 A1 and US 2015/0168584 A1 also describe techniques involving high-speed actively controlled switches to reduce the delay before demodulation.

The aim of the present invention is to provide an alternative approach to the methods described above, which does not require high-speed actively controlled switches or circuits, resulting in a simpler and more cost-effective solution.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a metal detector comprising: a transmit waveform generation circuit for transmitting a repeating sequence of transmit waveform; a transmit winding and its damping circuit; a receive winding and its

damping circuit; and a circuit capable of reducing the minimum delay between the end of a transition from a high voltage to a low voltage of a transmit signal of the metal detector and the beginning of demodulation of a receive signal received by a receive winding of the metal detector, comprising: means for beginning demodulation while an underdamped response in the receive winding occurs; means for connecting a DC current source to at least one input of the op amp of the analogue demodulation circuit to offset the output of the analogue demodulation circuit; means for adjusting the DC current source, damping circuit, demodulation timing waveform, or a combination of these factors when switching to a different coil to offset the output of the analogue demodulation circuit such that the output of the analogue demodulation circuit is closer to zero when no metal is detected than it would be without the adjustment.

In one form, the parameters required for adjusting the DC current source, damping circuit, demodulation timing waveform, or a combination of these factors are stored in the metal detector.

In one form, the DC current source comprises a DC voltage source in series with a resistor.

In one form, the magnitude of the DC voltage source is controllable.

In one form, the value of the resistor in series with the DC voltage source is controllable.

In one form, the damping circuit of the transmit winding includes at least a diode, and when the diode is in an off state, an underdamped response is present in the receive winding.

In one form, the damping circuit of the receive winding includes at least a diode, and when the diode is in an off state, an underdamped response is present in the receive winding.

In one form, at least a resistor in the damping circuit of the transmit winding is adjustable.

In one form, at least a resistor in the damping circuit of the receive winding is adjustable.

According to a second aspect of the present invention, there is provided a method for reducing the minimum delay between the end of a transition from a high voltage to a low voltage of a transmit signal of a metal detector and the beginning of demodulation of a

receive signal received by a receive winding of the metal detector, the method comprising: beginning demodulation of the receive signal while an underdamped response is present in the receive winding; connecting a DC current source to at least one input of the op amp of the analogue demodulation circuit; and adjusting the DC current source, damping circuit, demodulation timing waveform, or a combination of these factors when switching to a different coil to offset the output of the analogue demodulation circuit such that the output of the analogue demodulation circuit is closer to zero when no metal is detected than it would be without the adjustment.

According to a third aspect of the present invention, there is provided a non-transitory computer readable medium including instructions, when executed, to perform the method of the second aspect.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 depicts a simple prior art circuit of a metal detector to describe the problem addressed by the present invention.

Figure 2 depicts an example transmit waveform.

Figure 3 shows the overdamped, underdamped and critically damped responses of the transmit winding in Figure 1 to the transmit waveform in Figure 2.

Figure 4 shows an analogue demodulation circuit that implements a feature of the present invention.

Figure 5 illustrates the voltage decay of a receive winding that has been amplified by the pre-amplifier for various damping factors.

Figure 6 depicts an illustration of the output voltage generated by the timing generation circuit, which is also referred to as the demodulation timing waveform.

Figure 7 displays the DC components of the output that are generated by the analogue demodulation circuit in Figure 4, based on the underdamped voltage decay illustrated in Figure 5 and the demodulation timing waveform presented in Figure 6.

Figure 8 shows the DC components of the output that are generated by the analogue demodulation circuit in Figure 4 for different demodulation start times.

Figure 9 shows another analogue demodulation circuit that implements a feature of the present invention.

Figure 10 shows the circuit where the DC current source in Figure 4 has been replaced by a DC voltage source connected in series with a resistor.

Figure 11 shows the circuit where each of the DC current sources in Figure 9 has been replaced by a DC voltage source connected in series with a resistor.

Figure 12 depicts an alternative circuit of a metal detector with the addition of a resistor diode series circuit in parallel with the damping resistor in the transmit winding damping circuit, as well as a resistor diode series circuit in parallel with the damping resistor in the receive winding damping circuit.

Figure 13 shows the voltage decay of the transmit winding in Figure 12, in response to the transmit waveform shown in Figure 2 for various damping factors when the diodes are off.

DETAILED DESCRIPTION OF EMBODIMENTS

Figure 1 illustrates a basic prior art circuit for a metal detector, consisting of a transmit winding 7 and a receive winding 9, to describe the problem addressed by the present invention. This circuit is used to detect the presence of metal objects in the vicinity of the detector. The transmit winding 7, connected to a transmit waveform generation circuit 20, generates a magnetic field that induces a current in any nearby metal objects, which in turn generates a secondary magnetic field that is detected by the receive winding 9. The received signal is a pulse signal that is proportional to the rate of change of the secondary magnetic field caused by the metal object. The receive winding is connected 12, 13 to a pre-amplifier 14 to amplify the received signal. The output 15 of the pre-amplifier is connected to an analogue demodulation circuit 16 to extract the detected signal from the amplified received pulse signal. The resulting output 17 of the demodulation circuit is further processed to detect the presence of metal objects.

The transmit winding 7 and its stray capacitance 6 create a self-resonant element 5 that can oscillate at its natural frequency when sudden transitions are applied by the transmit waveform generation circuit 20. The stray capacitance 6 comprises the distributed capacitance of the transmit winding and the distributed capacitance of the cable connected to the transmit winding. A damping circuit consisting of only a damping resistor 4 in this case is added to dampen the oscillation.

Sudden transitions in the transmit winding 7 can be capacitively or magnetically coupled to the receive winding 9 through virtual capacitance or imperfect magnetic null. The receive winding 9, in parallel with its stray capacitance 10, forms a self-resonant element 8 as well. The stray capacitance 10 comprises the distributed capacitance of the receive winding and the distributed capacitance of the cable connected to the receive winding. When sudden transitions are coupled from the transmit winding 7, this self-resonant element 8 oscillates at its natural frequency. To prevent excessive oscillation, a damping circuit consisting of only a damping resistor 11 in this case is added to dampen the self-resonant element 8.

The transmit waveform generation circuit 20 contains three parts: a DC voltage source 1, a transmitter switch 2 and a transmitter waveform generator 3. The transmitter waveform generator controls the on/off state of the transmitter switch. Without loss of generality, assume that the transmit waveform is a square wave, as shown in Figure 2. Assume that the transmitter switch is turned on when the transmit waveform is at a high voltage level and turned off when the transmit waveform is at a low voltage level. The transmit waveform generation circuit connects the DC voltage source to the transmit winding for a duration of T_{on} (=50μs), followed by an abrupt disconnection from the transmit winding. Depending on the value of the damping factor ζ (=$\sqrt{LC}/(2RC)$), the self-resonant element exhibits different behaviours after the abrupt disconnection, including overdamped (ζ > 1), underdamped (ζ < 1), and critically damped (ζ = 1). R, L, and C represent the resistance of the damping resistor 4, the inductance of the transmit winding 7, and the distributed capacitance 6 of the transmit winding, respectively.

The overdamped (ζ > 1) response is a decay of the transient voltage without oscillation. In this case, the voltage of the transmit winding after the abrupt disconnection can be expressed using the following equation:

$$v(t) = A_1 e^{-\omega_0(\zeta-\sqrt{\zeta^2-1})t} + A_2 e^{-\omega_0(\zeta+\sqrt{\zeta^2-1})t}. \quad (1)$$

In the above equation, the constants A_1 and A_2 are dependent on the circuit parameters of the self-resonant element and the transmit waveform, while ω_0 ($=1/\sqrt{LC}$) represents the undamped natural frequency. Additionally, t denotes the time elapsed after abruptly disconnecting the DC voltage from the transmit winding.

In the underdamped ($\zeta < 1$) case, we can express the underdamped response as follows:

$$v(t) = B_1 e^{-\alpha t} \sin(\omega_d t + \varphi), \quad (2)$$

where the constants B_1 and φ depend on both the transmit waveform and the circuit parameters of the self-resonant element, while ω_d ($=\omega_0\sqrt{1-\zeta^2}$) and α ($=1/(2RC)$) represent the damped natural frequency and the attenuation factor, respectively. The underdamped response is a decaying oscillation at frequency ω_d, with its rate of decay determined by the attenuation factor α.

The critically damped ($\zeta = 1$) response can be expressed as:

$$v(t) = D_1 t e^{-\alpha t} + D_2 e^{-\alpha t}, \quad (3)$$

where the constants D_1 and D_2 are dependent on the circuit parameters of the self-resonant element and the transmit waveform. In the critically damped case, the circuit response decays in the fastest possible time without going into oscillation.

The overdamped, underdamped and critically damped responses of the transmit winding to the transmit waveform in Figure 2 are shown in Figure 3 for L=300μH and C=250pF. During the shaded period in Figure 3, an EHT (extra high tension) voltage is induced across the transmit winding for all the responses. The peak of the EHT voltage can exceed 200V. As observed in Figure 3, the underdamped response initially exhibits a faster voltage decay than the critically damped response after the EHT voltage peak. However, it eventually results in a significant oscillation, which is undesirable in traditional design as the oscillation of the transmit winding could be coupled to the receive winding through virtual capacitance or imperfect magnetic null and may cause the analogue demodulation circuit to saturate.

When the receive winding is separate from the transmit winding, in addition to the coupling of the oscillation of the transmit winding through virtual capacitance or imperfect magnetic null, the oscillation of the voltage decay of the receive winding may also occur when the receive winding is underdamped. This is because the abrupt voltage decay of the transmit winding is coupled to the receive winding and triggers the underdamped response. The above equations (1)-(3) can also be applied to the calculation of the voltage decay of the receive winding after the abrupt disconnection of the DC voltage source from the transmit winding. In this case, R, L and C should be replaced with the resistance of the damping resistor 11, the inductance of the receive winding 9, and the stray capacitance 10 of the receive winding, respectively. The constants A_1, A_2, B_1, φ, D_1 and D_2 are dependent on the circuit parameters of the self-resonant element 8 and the transmit waveform.

To decrease the demodulation delay of the receive winding in time domain metal detectors, both the damping resistor for the transmit winding and the damping resistor for the receive winding are traditionally selected so that both self-resonant elements are critically damped.

In contrast, the current invention takes advantage of the rapid voltage decay of the underdamped response to achieve early demodulation of the receive signal, while preventing the saturation of the analogue demodulation circuit. This technique enhances the system's sensitivity to fast time constant targets, surpassing that of traditional critically damped methods. The following paragraphs will explain how this is achieved.

Figure 4 shows a circuit that implements a feature of the present invention. A DC current source 45 is connected to the negative input of the op amp in a typical analogue demodulation circuit to offset its output. The analogue demodulation circuit functions as an integrator circuit 33 with selectable inputs. A timing generation circuit 36 controls a single pole triple throw switch 35, which is used to select the input to the integrator circuit 33. Depending on the switch's position, the input to the integrator circuit will be different.

When node 44 is connected to node 41, the output signal 30 of the pre-amplifier is inverted by an inverter 31 and used as the input to the integrator circuit. When node 44 is connected to node 42, the output signal 30 of the pre-amplifier is used directly as the input to the integrator circuit. When node 44 is connected to node 43, the input to the integrator circuit is zero, meaning that no signal is passed to the integrator circuit.

Taking the DC current source 45 into account, the output voltage 40 of the integrator circuit in the frequency domain, denoted as $V_{out}(f)$, can be expressed by the following equation:

$$V_{out}(f) = -V_{in}\frac{R_{fb}}{R_{in}}\frac{1}{(1+2\pi f C_{fb})} - I_s R_{fb}. \quad (4)$$

Here, the input resistors 32, the feedback resistor 37 and the feedback capacitor 38 are known as R_{in}, R_{fb} and C_{fb}, respectively. In the above equation, I_s represents the magnitude and direction (or sign) of the adjustable current of the DC current source. V_{in} is the voltage at node 44. The integrator circuit without the addition of the DC current source can be viewed as a low pass filter with a DC gain of $-R_{fb}/R_{in}$. With the addition of the DC current source, the output voltage of the integrator circuit will be offset by $-I_sR_{fb}$. This is due to the fact that the DC current source is effectively adding a constant current to the circuit, which causes a voltage drop across the feedback resistor R_{fb}. By adjusting the value of I_s, the output of the integrator circuit can be offset to different levels, either in the positive or negative direction. Increasing the value of I_s will cause the output voltage to shift in the negative direction, while decreasing the value of Is will cause the output voltage to shift in the positive direction.

It's important to note that the analogue demodulation circuit of a metal detector may have more or fewer selectable inputs than the three mentioned in this example. Additionally, each input path may include a separate resistor to allow for different DC gains for each input. Any combination of these inputs may be selected simultaneously, depending on the specific needs of the metal detector design.

Figure 5 illustrates the voltage decay of a receive winding that has been amplified by the pre-amplifier 14 for various damping factors ζ. There are no metallic target signals or soil signals included. In this specific example, we are assuming that the output of the pre-amplifier falls within the range of ±2V. However, it's important to note that the saturation voltage can vary based on the design of the pre-amplifier. The flattening of the beginning of the curves is caused by the pre-amplifier saturating. This amplified voltage decay is then utilized as the input 30 to the analogue demodulation circuit. In practice, due to the saturation of the pre-amplifier, there is a limit to how early the demodulation can occur. For the critically damped ($\zeta=1$) case, the earliest time to start demodulation is t=3.2μs. For the underdamped ($\zeta<1$) cases, the earliest time is less than 2.9μs.

Figure 6 depicts an illustration of the output voltage generated by the timing generation circuit 36, which is also referred to as the demodulation timing waveform. Without loss of generality, assume that whenever the demodulation timing waveform exhibits a positive value, node 44 becomes connected to node 42. Conversely, when the demodulation timing waveform demonstrates a negative value, node 44 is connected to node 41. Lastly, when the demodulation timing waveform assumes a zero value, node 44 gets linked to node 43. Demodulation for this waveform starts at 3µs. In a time domain metal detector, the demodulation timing waveform is crucial for accurately detecting metal objects. The waveform is chosen based on several factors, including the parameters of the transmit and receive coils, the associated damping resistors, and the type of material being detected. The waveform selection is typically determined through experimentation and optimization to achieve the best balance between sensitivity and noise rejection. It can be varied by adjusting parameters such as pulse width, pulse delay, and amplitude modulation to tailor the detector's performance to specific detection scenarios. For instance, a wider pulse width might be preferred for detecting larger metallic objects buried at greater depths, while a narrower pulse width could enhance sensitivity to smaller targets. Similarly, adjusting the pulse delay can help mitigate interference from ground minerals or other environmental factors. Ultimately, the flexibility to vary the demodulation timing waveform allows operators to optimize the detector's performance for different applications and detection conditions.

Figure 7 displays the DC components of the output 40 that are generated by the analogue demodulation circuit for various I_s 45, based on the underdamped ($\zeta<1$) voltage decay illustrated in Figure 5 and the demodulation timing waveform presented in Figure 6. It should be noted that Figure 7 assumes R_{in} = 1kΩ and R_{fb} = 100kΩ during its generation. It can be observed from Figure 7 that the output 40 of the analogue demodulation circuit can be offset by adjusting I_s. By setting I_s to 1.5µA, 0 µA, and -1.5µA for the cases of ζ=0.97, ζ=0.96, and ζ=0.95, respectively, the DC component of the output 40 can be brought very close to zero.

In practical applications, it is not necessary to precisely bring the DC component of the output 40 to zero. The main objective of offsetting the DC component is to prevent the analogue demodulation circuit from saturating, allowing for a wider dynamic range for metallic target detection. While the patent description uses zero DC component as an example, in some embodiments, the DC component may be intentionally offset to counteract soil effects. For instance, if the soil consistently generates a negative output, intentionally

offsetting the DC component towards the positive direction can help maintain a large dynamic range for detecting metallic targets.

The damping factor ζ affects the shape of the voltage decay. In some embodiments, the damping factor ζ may be adjusted to offset the output of the analogue demodulation circuit for a given demodulation timing waveform. Figure 7 shows that by reducing ζ from 0.97 to 0.96 or 0.95, a negative offset can be added to the DC component of the output 40 for any given value of I_s. Notably, when ζ is lowered from 0.97 to 0.96, the DC component of the output 40 is zero when I_s is set to 0.

In some embodiments, due to the oscillating nature of the underdamped voltage decay around zero and the integrator-like behaviour of the analogue demodulator, the demodulation timing waveform may be adjusted to offset the output of the integrator towards zero. One way to achieve this is by passing a certain period of the positive voltage decay to the integrator and then cancelling it with another certain period of the negative voltage decay. Another approach is to pass a certain period of the voltage decay and then cancel it with another certain period of the voltage decay with the same sign but through a different input path with an opposite DC gain sign.

For example, if the shape of the demodulation timing waveform in Figure 6 is kept unchanged but it is shifted left and right by changing the time when demodulation starts, the effect on the DC components of the output 40 can be observed. Figure 8 shows the DC components of the output 40 for different demodulation start times. It can be observed that when the demodulation starts at 3.45μs, 3.0μs, and 2.675μs for the cases of ζ=0.97, ζ=0.96, and ζ=0.95, respectively, the DC component of the output 40 is very close to zero. While the above example involves shifting the demodulation timing waveform in the time domain to offset the analogue demodulator output, it is also possible to achieve the same objective by altering the shape of the demodulation timing waveform and the individual DC gain of each input path.

There are various forms that analogue demodulation circuits can take. Figure 9 shows another circuit that implements a feature of the present invention, which includes an op amp integrator circuit 67 with selectable inputs, along with two DC current sources. One of the current sources is connected to the negative input of the op amp 59, while the other is

connected to the positive input. These sources are used to offset the output of the analogue demodulation circuit. The circuit shown in Figure 9 receives the output signal 50 of the pre-amplifier, which is then directed into two switches, 51 and 52. These switches are controlled by the timing generation circuits 61 and 62. The values of resistor 53, resistor 57, and capacitor 58 are typically the same as those of resistor 54, resistor 55, and capacitor 56, respectively. This configuration results in an analogue demodulation circuit with a differential input and a robust common-mode rejection capability. The output voltage 60 of the analogue demodulation circuit in the frequency domain can be written as:

$$V_{out}(f) = -V_{in}\frac{R_{fb}}{R_{in}}\frac{1}{(1+2\pi f C_{fb})} + (I_{pos} - I_{neg})R_{fb}. \quad (5)$$

In this context, the input resistors 53 and 54 are referred to as R_{in}, while the feedback resistors 57 and 55 are referred to as R_{fb}. The feedback capacitors 58 and 56 are known as C_{fb}. I_{pos} denotes the adjustable current of the DC current source 66 connected to the positive input of the op amp, including its magnitude and direction (or sign). Similarly, I_{neg} represents the adjustable current of the DC current source 65 connected to the negative input of the op amp, including its magnitude and direction (or sign). V_{in} denotes the voltage difference between node 63 and node 64. The op amp integrator circuit 67 without the DC current sources can be regarded as a low-pass filter with a DC gain of $-R_{fb}/R_{in}$. By adjusting I_{pos} and I_{neg}, the output of the integrator circuit will be shifted by $(I_{pos} - I_{neg})R_{fb}$ and can be shifted to different levels in the positive or negative direction.

In some embodiments, the DC current source depicted in Figure 4 and Figure 9 may comprise a DC voltage source connected in series with a resistor. In some embodiments, the DC voltage source and the resistor may be adjustable. Consider the circuit shown in Figure 4 with the DC current source 45 replaced by a DC voltage source 47 connected in series with a resistor 46, as shown in Figure 10. In this case, I_s in equation (3) should be replaced with V_s/R_s, where V_s and R_s are the voltage of the DC voltage source 47 and the resistance of the resistor 46, respectively. When each of the DC current sources 65 and 66 in Figure 9 are replaced with a DC voltage source in series with a resistor, as shown in Figure 11, I_{pos} and I_{neg} in equation (4) should be replaced with V_{sp}/R_{spn} and V_{sn}/R_{spn}, respectively, where V_{sp}, V_{sn}, and R_{spn} are the voltage of the DC voltage source 91, the voltage of the DC voltage source 92, and the resistance of the resistors 90 and 93, respectively. In this example, the

resistance of resistor 90 is set to be the same as that of resistor 93 in order to maintain the high common mode rejection capability of the analogue demodulation circuit.

Figure 12 depicts another circuit that incorporates an aspect of the present invention. This circuit is similar to the one shown in Figure 1, but with a modification to the damping circuit for both the transmit and receive windings. In the prior art example shown in Figure 1, the damping circuit for either the transmit winding or the receive windings comprises of only a damping resistor. In Figure 12, a resistor diode series circuit 72 is added in parallel with the damping resistor 70 in the transmit winding damping circuit 82, and a resistor diode series circuit 76 is added in parallel with the damping resistor 71 in the receive winding damping circuit 83. While Figure 12 illustrates the inclusion of the resistor diode series circuit in the damping circuits for both the transmit and receive windings, it is important to note that the resistor diode series circuit can be implemented in only one of the windings.

To illustrate the mechanics of the addition of a resistor diode series circuit, the transmit winding can be used as an example. During state one when any diode of the resistor diode series circuit is in the forward conducting mode, the equivalent damping resistor of the damping circuit 82 can be calculated as the parallel combination of resistor 70 and resistor 73. During state two when the voltage of the winding decays to a low enough value, all diodes in the damping circuit 82 turn off. Now the equivalent damping resistor of the damping circuit 82 equals the resistance of resistor 70 alone. The damping factor for state one can be designed to be either underdamped ($\zeta < 1$), overdamped ($\zeta > 1$), or critically damped ($\zeta = 1$). However, it is important to note that for the method described in this specification to be used for early demodulation, the damping factor for state two must be underdamped ($\zeta < 1$).

Figure 13 shows the voltage decay of the transmit winding in Figure 12, in response to the transmit waveform shown in Figure 2, with L = 300uH and C = 250pF, for various damping factors when the diodes are off (i.e., ζ_{OFF}). L and C are the inductance of the transmit winding 81 and the stray capacitance 80, respectively. In all instances, the damping factor when the diodes are on (i.e., ζ_{ON}) is 0.975. For comparison, the traditional critically damped (ζ=1.0) response is also plotted in the same figure. It is important to note that the threshold voltage of the diodes in this example is 0.7V. We can observe that by selecting resistor 73 (R_{73}) and resistor 70 (R_{70}) appropriately, the voltage decay occurs much more rapidly compared to the

traditional critically damped case, while still maintaining a very small overshoot. Typically, decreasing ζ_{OFF} results in a faster voltage decay; however, it can also lead to a larger overshoot. Once ζ_{ON} and ζ_{OFF} are determined, R_{73} and R_{70} can be calculated using the formulas $\zeta_{ON} = (R_{73}+R_{70})\sqrt{LC}/(2R_{73}R_{70}C)$ and $\zeta_{OFF} = \sqrt{LC}/(2R_{70}C)$.

In Figure 12, the resistor diode series circuit incorporates two diodes connected in parallel with opposite polarity. However, it is worth noting that in some embodiments, only a single diode may be required, depending on the polarity of the transient voltage applied to the winding.

In some embodiments, the diode symbol in Figure 12 may represent a series connection of multiple diodes of the same polarity. This configuration can be utilized to increase the overall threshold voltage. An increase in the overall threshold voltage would cause the diodes to turn off sooner, resulting in the early activation of the underdamped response. This would result in a faster voltage decay but with a greater overshoot for the same damping factor ζ_{OFF}.

It's worth noting that in some embodiments the diode symbol in Figure 12 may also represent a series connection of a resistor and a diode, or a parallel connection of a resistor or a diode.

A metal detector coil typically has a transmit winding and a receive winding, although a mono-loop coil can have a single winding for both. Other types of coils can have multiple transmit and/or receive windings. Coil size and shape vary depending on the detector's intended use. Larger coils are more sensitive and can detect objects at greater depths, but they may be more difficult to handle. Smaller coils are more manoeuvrable and better suited for searching in tight spaces. The coil connects to the detector's control box through a cable, and different coils may be used depending on the working environment and intended targets. Every coil has unique electrical characteristics, such as winding inductance and stray capacitance, which can impact the damping factor and voltage decay of both the transmit winding and the receive winding. In some embodiments, it may be necessary to adjust the DC current source, damping circuit, demodulation timing waveform, or a combination of these factors when switching to a different coil to maintain the DC component of the output of the analogue demodulation circuit. In some embodiments, these adjustment parameters can be stored in the metal detector so that when a different coil is connected to the control box of the metal detector, the proper adjustments can be applied for that specific coil. Within this

specification, the coil and the control box are both regarded as components of a metal detector.

This specification primarily focuses on metal detectors having separate receive windings from the transmit windings. However, it is worth noting that some of the techniques described herein can also be applied to mono-loop detectors where the transmit winding may also function as the receive winding. Therefore, the methods described in this patent can be adapted to a variety of metal detection systems, including both mono-loop and multi-coil systems.

The disclosed methods include one or more steps or actions for achieving the described method, which can be interchanged with each other without deviating from the claims' scope. In other words, unless a specific order of steps or actions is explicitly stated, the use and/or order of specific steps and/or actions may be altered without departing from the scope of the claims.

The system can be a computer-based system consisting of a display device, a processor, a memory, and an input device. The memory contains instructions that enable the processor to execute the method described herein. The processor, memory, and display device can be part of a standard computing device, such as a desktop computer, laptop computer, or tablet, or they can be integrated into a customized device or system. The computing device can be a unitary or programmable device, or a distributed device that includes several components connected through wired or wireless connections. An embodiment of a computing device can include a central processing unit (CPU), a memory, a display device, and an input device like a keyboard or a mouse. The CPU comprises an Input/Output Interface, an Arithmetic and Logic Unit (ALU), and a Control Unit and Program Counter element that communicates with input and output devices through the Input/Output Interface. The Input/Output Interface can contain a network interface and/or communication module that uses a predefined communication protocol like Bluetooth, Zigbee, IEEE 802.15, IEEE 802.11, TCP/IP, UDP, etc. The computing device may also include a graphical processing unit (GPU). The display device can be a flat screen display (e.g. LCD, LED, plasma, touch screen, etc.), a projector, CRT, etc. The computing device can have a single CPU (core) or multiple CPUs (multiple cores), or multiple processors. The computing device can use a parallel processor, a vector processor, or a distributed computing device. The memory is connected to the processor(s)

and can include RAM and ROM components, which can be internal or external to the device. The memory can store the operating system and additional software modules or instructions, and the processor(s) can load and execute these software modules or instructions from the memory.

Throughout the specification and the claims that follow, unless the context requires otherwise, the terms "comprise" and "include", as well as any variations like "comprising" and "including", should be understood to indicate the inclusion of the specified integer or group of integers, but not to exclude any other integer or group of integers.

Any reference to prior art in this specification is not intended to be, and should not be construed as, an acknowledgement that such prior art is part of the common general knowledge.

Skilled persons in the art will recognize that the invention is not limited to the specific application described herein. Furthermore, the preferred embodiment of the invention described or illustrated herein is not necessarily restrictive with respect to particular features or elements. The invention is capable of various modifications, substitutions, and rearrangements without departing from the scope of the claims defining the invention.

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CLAIMS

The invention claimed is:

1. A metal detector comprising:

a transmit waveform generation circuit for transmitting a repeating sequence of a transmit waveform; a transmit winding and a transmit damping circuit; a receive winding and a receive damping circuit; and a circuit capable of reducing the minimum delay between the end of a transition from a high voltage to a low voltage of the transmit signal of the metal detector and the beginning of demodulation of a receive signal received by the receive winding of the metal detector, the circuit comprising:

means for generating a demodulation timing waveform;

means for beginning demodulation while an underdamped response in the receive winding occurs;

means for connecting a DC current source to at least one input of an op amp of an analogue demodulation circuit to offset an output of the analogue demodulation circuit;

means for adjusting the DC current source, the receive damping circuit, the transmit damping circuit, demodulation timing waveform, or a combination of these factors when switching to a different coil to offset the output of the analogue demodulation circuit such that the output of the analogue demodulation circuit is closer to zero when no metal is detected than it would be without the adjustment.

2. A metal detector according to claim 1, wherein parameters required for adjusting the DC current source, the receive damping circuit, the transmit damping circuit, demodulation timing waveform, or a combination of these factors are stored in the metal detector.

3. A metal detector according to claim 1, wherein the DC current source comprises a DC voltage source of a voltage in series with a resistor.

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4. A metal detector according to claim 3, wherein the voltage of the DC voltage source is controllable.

5. A metal detector according to claim 3, wherein the value of the resistor in series with the DC voltage source is controllable.

6. A metal detector according to claim 1, wherein the transmit damping circuit of the transmit winding includes at least a diode, and when the diode is in an off state, an underdamped response is present in the receive winding.

7. A metal detector according to claim 1, wherein the receive damping circuit of the receive winding includes at least a diode, and when the diode is in an off state, an underdamped response is present in the receive winding.

8. A metal detector according to claim 1, wherein at least a resistor in the transmit damping circuit of the transmit winding is adjustable.

9. A metal detector according to claim 1, wherein at least a resistor in the receive damping circuit of the receive winding is adjustable.

10. A method for reducing the minimum delay between the end of a transition from a high voltage to a low voltage of a transmit signal of a metal detector and the beginning of demodulation of a receive signal received by a receive winding of the metal detector to produce an output of an analogue demodulation circuit, the method comprising:

beginning demodulation of the receive signal while an underdamped response is present in the receive winding;

connecting a DC current source to at least one input of an op amp of the analogue demodulation circuit; and

adjusting the DC current source, a receive damping circuit, a transmit damping circuit, the demodulation timing waveform, or a combination of these factors when switching to a different coil to offset the output of the analogue demodulation circuit such that the

output of the analogue demodulation circuit is closer to zero when no metal is detected than it would be without the adjustment.

11. A non-transitory computer readable medium including instructions, when executed, to perform the method of claim 10.

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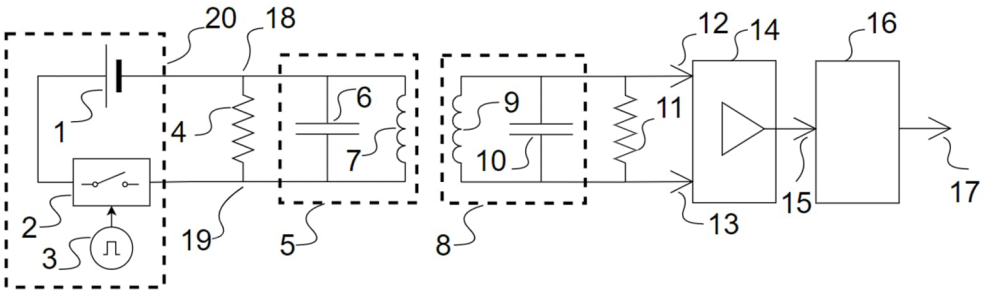


PRIOR ART

Figure 1

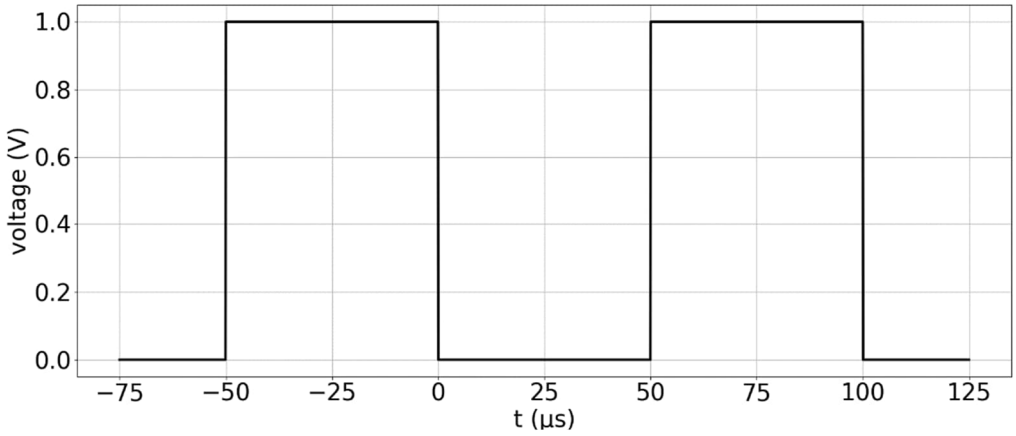


Figure 2

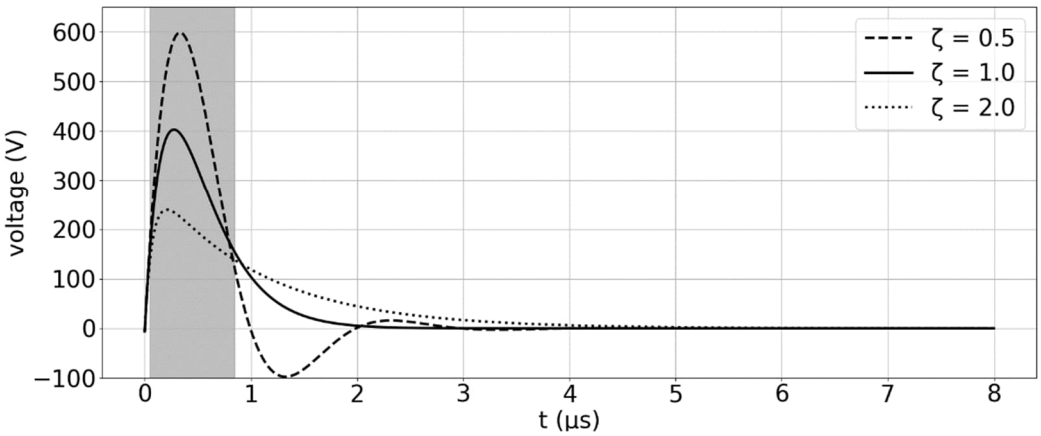


Figure 3

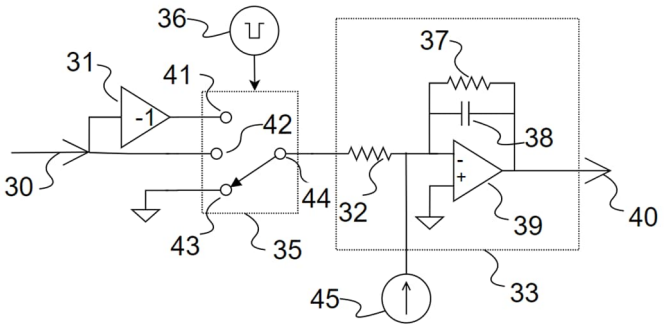
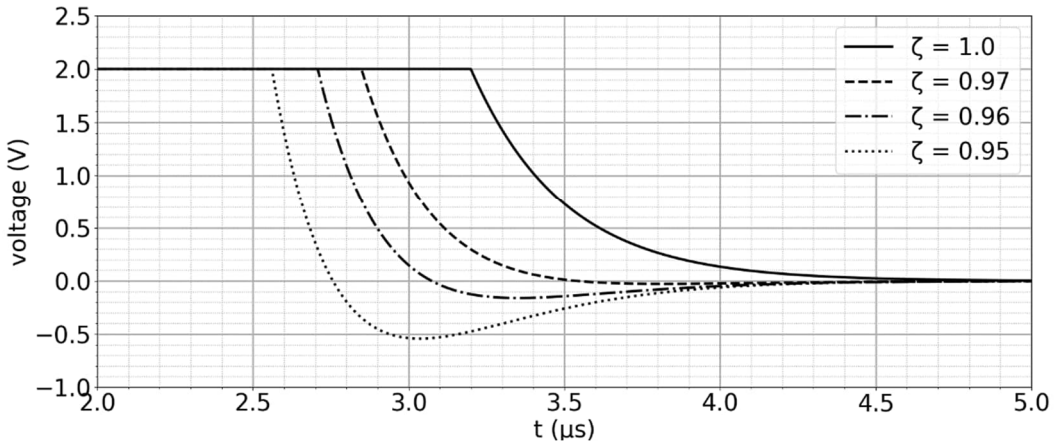


Figure 4



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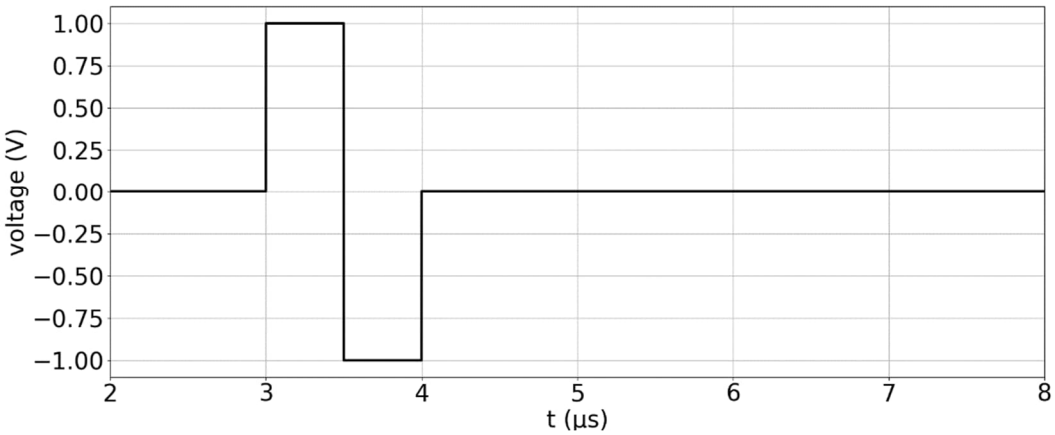
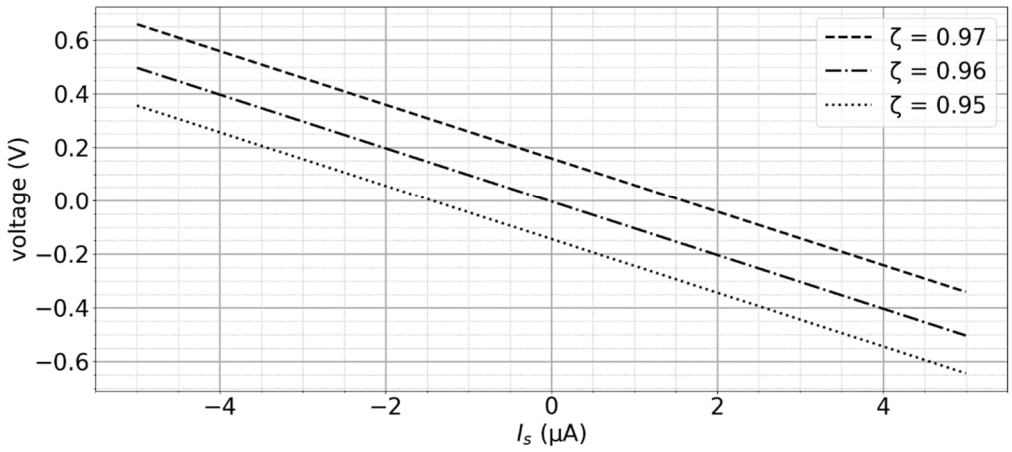


Figure 6



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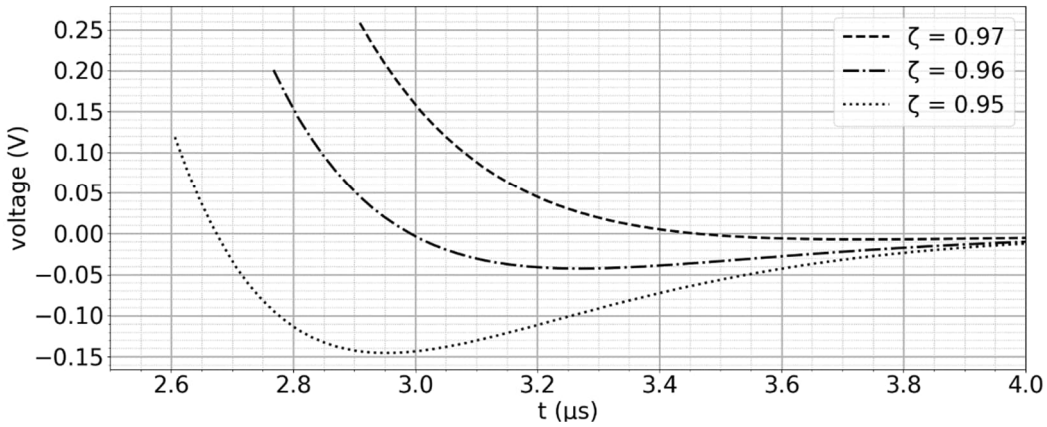

Figure 8

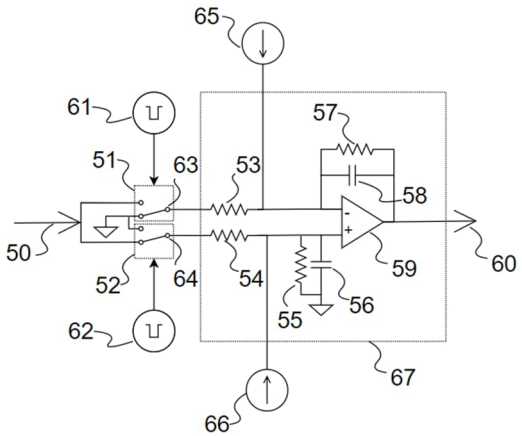

Figure 9

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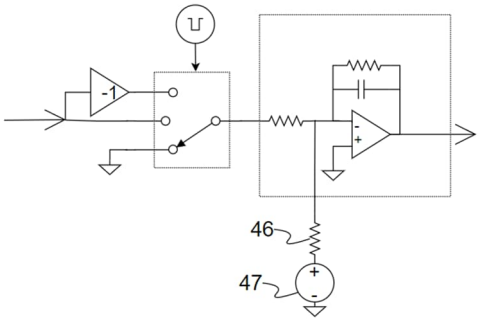

Figure 10

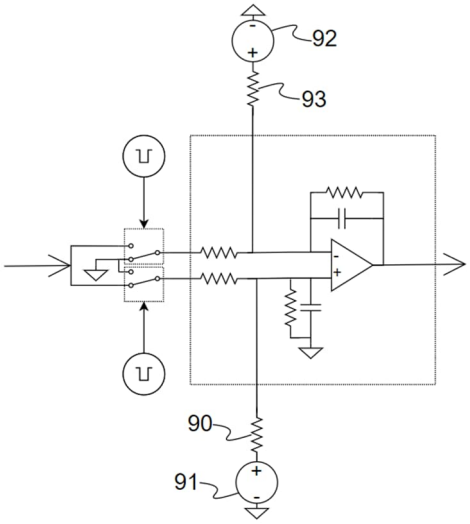

Figure 11

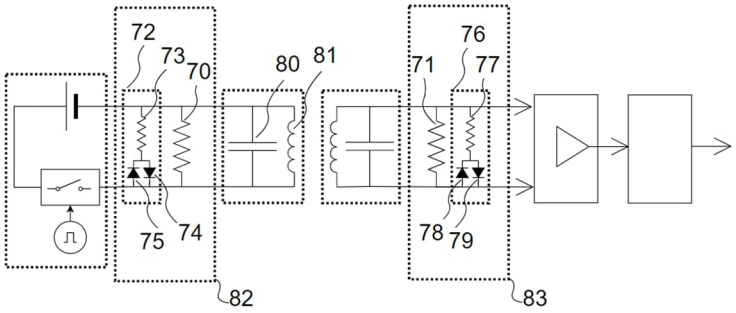

Figure 12

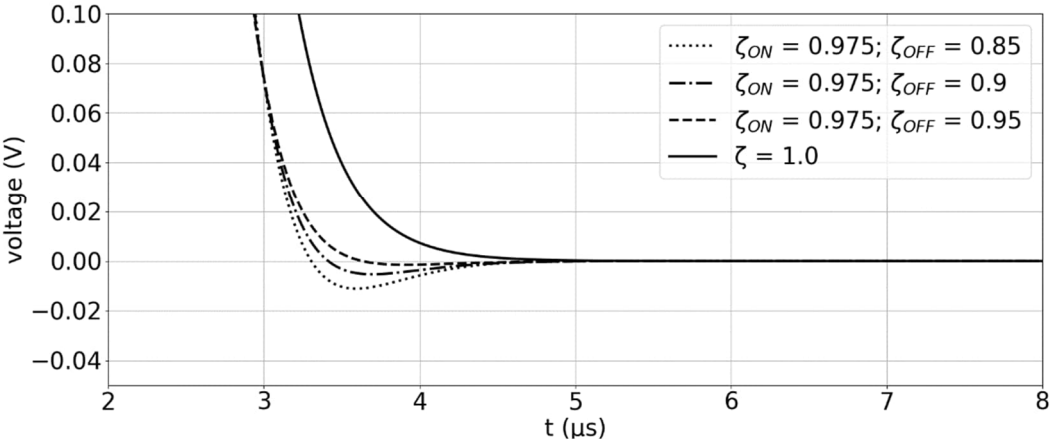

Figure 13